METHOD AND APPARATUS FOR DIGITAL SCAN CONVERSION


Filed: Dec. 29, 1972

Appl. No.: 319,217

U.S. Cl. 340/172.5; 340/324 AD
Int. Cl. G06f 3/14; G06f 13/06
Field of Search 340/172.5, 324 AD

ABSTRACT

A hardware system for converting digital graphical line information into a form suitable for display on a raster-scan output device is provided. Each graphical line is encoded and stored in a memory device. Each encoded graphical line is read prior to each scan of the raster-scan output device. The intersections of each graphical line with each scan line are determined on a line-by-line basis and the raster-scan output device is activated and de-activated accordingly in order to reconstruct all of the vectors.

49 Claims, 24 Drawing Figures

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FIG. 1A

FIG. 1B

FIG. 1C

FIG. 1D
FIG. 2

DATA FROM COMPUTER 16

1. CONVERT INPUT TO VSW

2. CALCULATE NEXT SCAN LINE

3. UPDATE/RESET VSW

4. ADD/DELETE VSW TO/FROM MEMORY

5. VECTOR MEMORY

6. SCAN LINE BUFFER SET 1

7. SCAN LINE BUFFER SET 2

8. SWITCH 1

9. SWITCH 2

10. CONVERT BUFFER TO VIDEO SIGNAL

11. TO TELEVISION MONITOR 12

FIG. 3
FIG. 4

FIG. 5A

FIG. 5B
CLOCK PULSE EVERY 200 NSEC.

MULTIPLEXER

DEMULTIPLEXER

FIG. 5C
RECEIVE INPUT: TWO COMMANDS

DECODE COMMAND BITS:
ADD/DELETE
ABSOLUTE/HEAD-TO-TAIL/RELATIVE

ABSOLUTE  HEAD-TO-TAIL  RELATIVE

RECEIVE INPUT: TWO ENDPOINTS  RECEIVE INPUT: ONE ENDPOINT  RECEIVE INPUT: TWO DISPLACEMENTS

GET FIRST ENDPOINT FROM SAVED ENDPOINT  GET FIRST ENDPOINT FROM SAVED ENDPOINT

SAVE SECOND ENDPOINT

DETERMINE:
SIGN XT YT YB XCUR

CALCULATE:
XINC

ADD  DELETE

SORT NEW VSW INTO VECTOR MEMORY  SEARCH VECTOR MEMORY FOR MATCH AND REMOVE VSW

FIG. 9
THIS FIELD EVEN?

YES

NO

YSCAN\leftarrow 514

YSCAN\leftarrow 513

DECREMENT YSCAN BY 2

YES

YSCAN\leq 0?

NO

RESET XCUR FOR ALL VECTORS IN VECTOR MEMORY 22

READ A VSW FROM VECTOR MEMORY 22

YES

VECTOR MEMORY 22 COMPLETELY CYCLED?

NO

YB\leq YSCAN\leq YT?

YES

CALCULATE NEW XCUR

WRITE XCUR INTO VSW IN VECTOR MEMORY 22

DETERMINE FROM, TO VALUES

IS DPYON\textsubscript{142}(FROM)=1?

NO

YES

IS DPYOFF\textsubscript{144}(TO)=1?

NO

WRITE 1 AT DPYON\textsubscript{142}(FROM);

DPYOFF\textsubscript{144}(TO)

FIG. 14
TO SWITCH 158 (FIGURE 13)

190

XSCAN
RESET

186

COUNTER
XSCAN

190

DPYON

192

DPYOFF

SLBS 38

142

144

SLBS 40

142

144

186

READ ZERO
DPYON(XSCAN)

192

READ ZERO
DPYOFF(XSCAN)

194

AND

180

ADD 1
SUB 1
COUNTER

181

AND

198

SINGLE SHOT
MULTIVIBRATOR

184

DISPLAY SIGNAL
(ELECTRON BEAM)

182

CRT
OUTPUT
DISPLAY

188

SYNCHRONIZING
BLANKING GENERATOR
CLOCK

OFF

ON

194

196

198

AND

CRT
OUTPUT
DISPLAY

TO YSCAN COUNTER 122 (FIG. 13)

FIG. 15
\begin{figure}
\centering
\includegraphics[width=\textwidth]{figure16.png}
\caption{Flowchart for the operation of the single shot multivibrator.}
\end{figure}
FIG. 17
METHOD AND APPARATUS FOR DIGITAL SCAN CONVERSION

BACKGROUND OF THE INVENTION

The present invention relates to a system for scan conversion and, in particular, to a hardware system for converting coded graphical information, typically coded in the form of Cartesian or other suitable coordinates, into a format suitable for driving a raster-scan output device such as a conventional television monitor.

Scan conversion is the transformation necessary to change data in Cartesian coordinates, for example, into raster-scan line data. In television, for example, this is the conversion from digital data to a video signal.

One application for scan conversion is a part of a graphical output terminal in a computer system. Remote graphical terminals are one form of output devices used to communicate with a computer. One example of a non-graphical remote output terminal is the teletype. The teletype is a convenient and cheap input/output device and is the most widely used terminal today. The major disadvantage of the teletype is that they are slow and cannot produce graphic output.

Two major types of display units utilize a cathode ray tube (CRT). The first type includes units which display only alphabetic, numeric (alphanumeric) and special characters at pre-defined positions of the face of the CRT.

Their main advantage over the teletype is their operating speed of 120 to 300 characters per second. Typically, they display 16 lines of 64 characters each, on a 9 inch by 7 inch viewing area. The number of characters is limited by the beam writing speed during a refresh cycle. Refresh memory is typically magnetic core or delay line. The characters are generated by one of three methods: dot matrix, stroke or extruded beam. The first method, and the simplest method, is to construct the characters from a matrix of 5 × 7 dots. In the second method, the beam actually traces out a series of line segments which form the matrix letters. In the third method, extruded beam character generation, the beam is shaped by deflecting it through the appropriate letter on a mask. It is then further deflected to the proper display position on the face of the CRT. Perfect font letters are generated by this method. The alphanumeric CRT displays usually have some form of line editing and deleting capability, tab and margin sets, and a cursor to indicate position.

The second major type of cathode ray tube includes devices which display graphical line drawings and alphanumeric data at random positions on the CRT face. These devices can be grouped into two further categories, the first, including those devices using a standard CRT and the second, those using a television or raster-scan CRT. The former type of CRT is used in such applications as oscilloscopes, etc., and the second is used in conventional television sets. In the case of the former, the beam from the CRT is deflected to draw each of the individual lines making up the graphical display on the CRT screen. That is, the beam is scanned laterally or horizontally across the screen beginning from the top of the screen and moving downward.

There are two main forms of CRT’s. Those using conventional fast decay phosphors, hereinafter called refresh CRT’s and those using very slowly decaying phos-
stepped from top to bottom in discrete steps, for a total of 512 lines. Higher performance CRT's are available with 800 and 1200 lines.

To produce one field, then, the beam scans the even lines from top to bottom, then goes back up to the top of the screen and fills in the odd lines, all in 1/30 second. It is, therefore, necessary to supply a video or modulation signal, which varies the CRT grid voltage, Vs, to produce the varying intensities that make up the picture on the screen.

Although the Vs signal is analog, there are only about 512 distinguishable points on a scan line for a good television monitor. Therefore, the electron beam modulation signal, Vs, can be made to have 512 discrete values along the scan line, one value for each scan line point.

For commercial television broadcasts, the video signal is created by a television camera which is basically the inverse of the monitor. It scans the image on an internal "retina" 30 times a second and transmits an analog intensity reading along each scan line to the monitor.

The fact about the television system that makes it difficult from an engineering standpoint is the time constraints imposed by the scanning deflection circuitry. A frame is scanned in 1/30 second (30 milliseconds). One line is scanned in 65 microseconds. This means the electron beam moves from one point to the next adjacent point of the same scan line in about 130 nanoseconds. So, after telling the beam whether or not to intensify a point, and with how many electrons, there is only 130 nsec to tell it whether or not and by how much to intensify the next point.

Retrace is the term for the time needed to re-position the beam. For instance, horizontal retrace occurs at the end of a scan line to position the beam at the beginning of the next scan line. Vertical retrace occurs at the end of the last line of a field to position the beam at the beginning of the first scan line of the next field. During the retrace time, no signal is displayed. Horizontal retrace takes 13 usec; vertical retrace takes 1.5 msec. To establish a time reference, today's medium-high speed logic requires 10 nsec to do a logical AND very high speed requires 5 nsec, and the fastest logic is 3 nsec. These speeds are due to production processes and are not theoretical limits.

Presently, there are two types of systems for using a television monitor, i.e., a raster-scan CRT, as a computer display. A very straightforward method is to point a television camera at the graphics to be displayed. The desired video signal is the output of the camera. There are several ways of producing the picture that the camera is pointed at. A standard CRT can be used to draw the graphics since the deflection voltages are not constrained as in a television monitor. It must be refreshed, however, for the same reasons as a television CRT. Some designs of storage CRT's allow random writing and raster-scan readout. Another design couples the CRT and camera in one electron tube, face to face.

There are several drawbacks to this technique. First, there is the need for a random scan writing device, essentially a double display console. A second drawback is the comparably poor resolution: typically one-half of the capabilities of the television CRT. Third, this system has very slow writing speed since the storage CRT shares the electron beam between writing and reading.

The reading speed is fixed at 30 frames per second so the writing speed must be significantly less than that. Finally, to delete a portion of the picture on the storage CRT requires the picture be erased from the screen (0.2 seconds, typically) and then redrawn without the deleted element (0.2 to 0.5 seconds).

The second kind of system, digital television, is a technique which has been receiving increasing attention as a means for attaining some of the advantages associated with television systems, while avoiding most of the disadvantages resulting from use of the analog scan converters or television cameras to convert from digital inputs to television format. Although there must be a digital to analog conversion before the signals are applied to the television CRT, all data processing, conversion to television format, and display generation are done with digital signals.

A digital television system typically includes three units, the data process unit, the picture assembly unit, and the picture refresh unit. Since computer output data is delivered too rapidly to be converted to display format instantly, the data is input through a buffer memory. The computer generated data is in the form of digital words which contain the X, Y coordinate addresses as well as the coded designation of symbols, alpha-numeric lines, or other conics to be displayed. The software conversion logic and the character-vector generators then decode the input data and transfer it to the picture assembly unit. There it is stored in magnetic core memory as a geometric pattern which duplicates, point for point, the desired display pattern. That is, there is one bit of core memory for every possible point on the television display. Typical digital displays are 1000 by 1000 points. After the total pattern is formed, it is transferred by destructive readout from the core memory to the refresh memory, which is a drum or magnetic disc memory. This transfer is necessary to relieve the storage burden on the core memory of the computer.

If a bit is a ONE, the corresponding screen location is intensified. If ZERO, it is not intensified. The drum or disc rotates at a speed sufficiently fast such that the value of each bit is available to the electron beam as needed. The video signal is therefore supplied, by conversion of vectors to raster-scan coordinates, not a part of the device. A computer and software program are needed to turn on the appropriate bits of the bulk storage. To write all the bits for a full screen requires the transfer of up to 8k, 36-bit words from the computer to bulk storage.

Digital type television systems have several advantages over CRT display devices and analog scan conversion television systems. On refreshed CRT displays, the maximum number of characters is limited by the number of random deflections during a refresh cycle which can occur without flicker. This is usually 2000-3000 characters. Television systems aren't limited by this factor, but by the resolution of the picture. For a 12 inch X 12 inch television display, a maximum of approximately 10,000 characters is possible, though this is well beyond the limit imposed by human considerations.

Both television camera and analog scan conversion have the disadvantages of loss of resolution due to the Kell factor, the smearing of moving points because of scan conversion storage time, and difficulty in achieving selective updating. The Kell factor results from the
possibility that data points may not be covered by a scanning line. It has been established empirically that resolution is 0.7 times the resolution before scan conversion. Digital TV eliminates this since each generated display point is associated with a scan line point. Magnetic memory eliminates smear since there is no retention of data after it has been updated.

There are a couple of important disadvantages using this form of the latter type of digital TV scheme. Since the picture assembly unit needs one bit of memory for each point on the display, this is typically one megabit of core storage required. This isn't economical for driving one or several displays.

Another disadvantage is that a vector is "lost" once it is stored in core storage. Thus, individual vectors cannot be added or deleted without completely rewriting the entire picture into the computer core memory. Since the latter operation utilizes expensive computer time, a graphical display with rapidly changing vectors becomes very expensive in operation.

Third, such systems require expensive bulk storage equipment such as a magnetic disc or drum. Besides being expensive, this equipment is subject to frequent maintenance and repair.

**SUMMARY OF THE INVENTION**

It is therefore an object of the invention to provide a hardware system for converting digital graphical data into a form suitable for display on a raster-scan output device.

Another object of the invention is to provide a hardware system for providing digital scan conversion with television time and speed constraints.

Another object of the invention is to provide an improved vector display system using a television monitor.

Another object of the invention is to provide an improved line drawing system for display on a raster-scan device.

Another object of the invention is to provide a computer graphical display device using a conventional television monitor.

Another object of the invention is to provide a raster-scan conversion system applicable in television transmission systems.

Another object of the invention is to provide a conversion system for use in a conventional digital television system which eliminates the need for core memory storage.

Another object of the invention is to provide a self-refreshing or regenerating raster output vector device.

Another object of the invention is to provide an unbuffered system for digital scan conversion.

In accordance with the invention, graphical line information is first received from a computer. Based on this information boundary data for each line or vector in the graphical display is stored, for example, in a memory device such as a shift register. From the graphical line information the incremental or intersection scan lengths or segments required to be provided by each scan of the raster-scan output device, such as a television CRT, in order to synthesize or reconstruct each of the lines or vectors, is determined. In the case of straight line vectors, the incremental scan lengths for each of the vectors is most conveniently stored with the boundary data for each vector.

Based upon the boundary data for each vector and the incremental scan lengths, means are provided for determining, for each sweep or scan of the raster-scan output device, the location of any and all vectors or lines which might be displayed as an incremental scan segment, during that sweep. That is, the intersection of all vectors or lines with each individual scan line is determined.

Based upon this determination, means are provided for energizing and de-energizing the raster-scan output so that the incremental scan lengths are properly displayed or projected. In this manner, after a complete cycle of the output raster-scan device, the net effect of all of the incremental scan lengths is that the pattern of vectors and lines is synthesized or recreated.

One application where the invention is particularly useful is for vector display using a conventional television monitor. Thus, in one particular application of the invention graphics data is input from the computer in the form of binary coded boundary data for each vector to be drawn. The data passes through an arithmetic unit which calculates the value XINC, the length of the line segment of each horizontal raster-scan line which must be displayed to generate the desired vector.

Where only straight line vectors are being displayed, XINC is a constant for each vector and hence need only be determined once. Where curved lines are displayed, XINC must be determined for each horizontal raster-scan line. From there the binary-coded words representing the boundary data for each line is loaded into a vector memory. If straight line segments only are displayed, then a coded value for XINC is also loaded with the boundary data for that word into the vector memory.

Where straight lines only are displayed, the memory, desirably, is a rotating type storage device. For example, shift registers, each N-bits long can be used, where N is equal to the maximum number of vectors to be displayed. The shift register must be at least M-bits wide, where M is equal to the number of bits necessary to code the boundary data and XINC for each vector. Each word appearing at the output represents all the required data about one vector to be displayed. A salient feature of storing vector boundary data in the circulating memory as contrasted with core storage in a conventional digital television system is that the individuality of the input vectors is not lost. Since the boundary data and XINC for each vector are kept in memory, any vector can be identified when its word appears at the output of the shift registers, and it can be deleted if desired. New vector words are easily inserted into the circulating vector memory stream. The memory is circulated such that each of the vectors appears at the output during one raster-scan line period.

An arithmetic unit calculates the intersection of each of the vectors to be displayed with the next television scan line. Such intersections are in the form of scan line segments. The coordinates of the beam turn-on and turn-off points are calculated which will display the line segment in the proper position on the scan line. These coordinates are loaded into display turn-on and display turn-off buffers respectively. This is done for each vector as it appears at the output of circulating memory.

Thus, by the end of one scan line period, the buffers for beam turn-on and turn-off are loaded with the proper coordinates to display the intersections of all of the vectors with the next raster line to be scanned. By alter-
nating between two display buffers, one buffer is being loaded while the other is being read and displayed. The display buffers also drive the raster-scan output device, such as a television monitor. For each horizontal scan line about to be scanned, the appropriate buffer dictates the state of the video output as the beam moves across the display. In one embodiment each buffer comprises a pair of buffers, a turn-on and a turn-off buffer; the pair is read in parallel such that the output bit being read corresponds to the X-coordinate of the display beam’s present position. A common sync generator keeps the beam and each pair of buffers synchronized. An output 1 in the turn-on buffer increments an up-down counter, and a 1 in the turn-off buffer decrements the counter. Whenever the counter shows a 1 or greater, the display beam is turned on and it remains on until the counter is returned to zero by the turn-off buffer. This procedure is repeated for all of the scan lines, and the end result is that all of the vectors are displayed on the television. Since a frame is produced every 1/30 of a second, any new vector can be added or deleted in 1/30 sec. The selective insertion or deletion of vectors occurs, desirably, during horizontal retrace and can add or delete one vector every scan line. Therefore, up to 502 vectors may be changed per frame.

The present invention, as applied to graphical displays on a television monitor, has several important advantages over the conventional digital television systems. Since the present system uses its vector storage memory for picture refreshing and input storage and conversion, it needs only one memory, needing only a fraction of the storage of conventional digital television. Further, it does not require a disc or drum refresh memory.

This is because the present invention does not require a full-frame buffer or storage memory. Rather than storing all of the bits necessary to display an entire frame of television, one horizontal scan line is developed at a time, based upon the vector boundary information and on XINC.

The conventional digital TV system stores the composite picture in its refresh memory and thus loses the data regarding individual input vectors which made up the geometrical pattern. Therefore, if a single vector is to be deleted, the system must ask the computer for all the input data so it can reconstruct the picture. This can be avoided if the input buffer is a complete memory, storing all the input data, but this requires another large memory for each display. Again, since the system according to the present invention stores the vector input data, any vector can be deleted without the necessity of requesting all input vectors from the computer.

The following detailed description of the invention is illustrative of only one, albeit attractive, embodiment of the invention, namely to a system for displaying graphical data, in the form of straight line vectors, on a conventional television monitor. However, with only minor modifications and additions, the basic features of the invention are equally applicable to other applications and modifications.

Thus, the present scan conversion system is suitable for use with raster-scan output devices other than television. For example, one very desirable application of the invention is as the interface with electrostatic or photo-printers which use a scan line output format.

In computer centers where terminals can be connected to the computer via high bandwidth cables, the present system is particularly applicable for making special purpose computations which lend themselves to television displays.

Also, the present invention can be incorporated into a conventional digital display system. It can be used as the data processing unit and picture assembly unit for a digital television system. When used in conjunction with a disc storage unit, it can be time-shared among many displays at once, making a digital television system which doesn’t require the enormous picture assembly memory now required. In a digital television system such as the one manufactured by Data Disc Corp., the present invention, in this manner, with one disc drive could serve approximately 30 users simultaneously.

As cable television develops from its present function as a distribution system for entertainment television into a multifunctional, two-way communications system, digital television will be a necessity. Scan conversion will be done at the computer end of the network, and video signals will be sent directly to the terminals. Thus, in future CATV system, the present system can be used to convert computer data concerning prices, inventories, current movies, and almost anything imaginable into alphanumeric and graphical displays for the home viewers.

With minor modifications and additions, the present system is capable of providing alphanumeric displays, as well as graphical displays. Other modifications which can be made to the basic digital scan conversion system of the present invention include color display, halftone display, windowing and image expansion, and threedimensional rotation. When incorporated into a remote terminal, input devices such as a keyboard and light pen, and line editing subsystems can be added.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a graphical illustration of a vector represented on a raster-scan device; FIG. 1B is a geometric representation of a graphical line; FIG. 1C is a representation of the line of FIG. 1B suitable for raster-scan output; and FIG. 1D is a graphical representation of a video signal for a typical scan line in accordance with the present invention.

FIG. 2 is a generalized block diagram of a system for displaying graphical information on a conventional television monitor in accordance with the present invention.

FIG. 3 is a detailed block schematic diagram of the scan conversion system of FIG. 2 in accordance with the present invention.

FIG. 4 graphically illustrates XCUR and XINC utilized in the present invention.

FIG. 5A is a block illustration of a rotary storage device for storing vector storage words defining the vectors to be displayed; and FIGS. 5B and 5C illustrate another embodiment of the rotary storage device of FIG. 5A.

FIG. 6A graphically illustrates the intersection of typical lines to be displayed and the scan lines of a raster-scan device; FIGS. 6B and 6C are detailed illustrations of the intersections of FIG. 6A.

FIG. 7 illustrates graphically the calculation of XCUR to compensate for alternate odd and even fields in video applications.
FIG. 8 is a detailed diagram of blocks 30 and 32 of FIG. 3.

FIG. 9 is a flow chart of the logical sequence of operation of the circuit of FIG. 8.

FIG. 10 is a detailed schematic diagram of block 73 of FIG. 8.

FIG. 11 is a detailed diagram of block 84 of FIG. 8.

FIG. 12 is a schematic diagram of a 20-bit compare circuit.

FIG. 13 is a detailed block schematic diagram of blocks 34 and 36 of FIG. 3.

FIG. 14 is a flow chart of the logical sequence of operation of the circuit of FIG. 13.

FIG. 15 is a schematic diagram of converter 12 of FIG. 3.

FIG. 16 is a flow chart of the logical sequence of operation of the circuit of FIG. 15.

FIG. 17 is a detailed schematic diagram of block 127 of FIG. 13.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Graphics as used here, refers to points and lines or vectors. Graphics are most conveniently dealt with in a computer as geometric quantities, with respect to a Cartesian coordinate x, y axis, in the case of straight lines or vectors. A point is represented by a single x, y pair, i.e., two numbers. A line is represented by its endpoints, each endpoint represented by an x, y pair, for a total of 4 numbers.

A line can be specified by only two numbers, if one endpoint is assumed to be known; for example, the last endpoint of the previous line or the previously specified point. These two numbers may be interpreted in one of two ways; as an endpoint (called head-to-tail mode) or as a displacement in the x and y directions from the previous endpoint (called relative mode). The motivation behind this representation is to save computer memory space. Since much graphical data involves connected lines, this method prevents the repetitious specification of an endpoint that is common to two lines. This consideration is most important when this data must be transmitted to a display since only half the data need be transmitted. These endpoints are beam positions, and for simplicity, the video signal can be assumed to be an on-off signal.

Since the path of the beam of a raster-scan device does not necessarily follow along the vectors and, in fact, will only trace out vectors lying on a scan line, it is necessary to determine all the scan lines that the vectors intersect, and how much of those scan lines are covered by a vector. See FIG. 1A.

Referring now to FIGS. 1B and 1C, scan conversion is the term applied to the process of converting a line, geometrically represented in FIG. 1B, into a form suitable for raster-scan output as shown in FIG. 1C. As illustrated therein, e1 are endpoints.

The conversion should be such that e1 = e2 and e3 = e4. Each of the line segments of the converted form occupies exactly one scan line. For each scan line, all these segments, as well as points, are determined and, where the raster-scan output device is a television monitor, are the video signal for the television monitor. For any given scan line, the video signal as a function of time might look like that shown in FIG. 1D.

FIG. 2 is a general block diagram, in accordance with the invention, of a system 10 for displaying graphical information on a conventional television monitor 12 by the use of the present scan conversion system 14. The detailed description which follows is intended to be illustrative of only one embodiment of the invention. Thus, as explained previously, the system is equally applicable for use with other raster-scan devices other than television. Also, the invention is not limited to displaying straight line vectors. Graphical data to be displayed is sent in the form of binary coded numbers from a computer 16, via path 18 to a controller 20 of the digital scan conversion system 14. A controller as used herein is the generic term for a device that drives a display; in this case the television monitor.

The graphical data sent over the path 18, in the case of a system for displaying straight line graphics, is in the form of binary-coded Cartesian coordinates. A point encoded in this manner is thus provided with x and y position numbers, where x is given by a 9-bit number and y is given by a 9-bit number. Nine-bit numbers are required since, as previously explained, a television picture may be considered to be a matrix of points 512 long by 512 wide.

As explained previously, a vector can be expressed in one of three ways; namely, in the absolute mode, the head-to-tail mode, and the relative mode.

In the absolute mode, the coordinates of the two endpoints of a vector are given. Thus, two 9-bit numbers for each of the endpoints is provided. In the head-to-tail mode only the second endpoint of the vector is given, i.e., only two 9-bit numbers are required. In the relative mode, where the displacements, dx and dy are given, two signed 9-bit numbers are given.

The representation of each vector called a vector storage word (VSW) is stored in the memory 22, which, for example, can comprise a rotating storage device such as a shift register. The vector storage words are sent along path 24 between the memory 22 and the controller 20. The controller 20 also provides update information for each of the VSWs stored in memory 22 via path 26, in a manner to be explained subsequently. Finally, the controller 20 provides signals representative of the analog video signal along the path 28. This signal dictates the intensity of each of the points along the scan beam, i.e., whether the beam is "on" or "off."

Referring now to FIG. 3, a block diagram of the present scan conversion system 14 for graphical displays of straight line vectors on a television monitor is shown. Graphical data, in either the absolute, head-to-tail, or relative mode is converted at 30 into the internally used vector storage words (VSW). The VSW for each vector contains the following data fields:

<table>
<thead>
<tr>
<th>sign</th>
<th>XT</th>
<th>YT</th>
<th>YB</th>
<th>XINC</th>
<th>XCUR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>9</td>
<td>9</td>
<td>18</td>
<td>18</td>
<td></td>
</tr>
</tbody>
</table>

These data fields contain the following number of bits:

Here XT=Xtop, YT=Ytop, YB=Ybottom (See FIG. 1A), and sign = 1 if the vector has negative slope, and sign = 0 if the vector has a positive slope. As will be explained, XINC and XCUR are used to construct the characteristic "stepped" representation of the vector on the television monitor.

An input from the computer contains the following information:
The first command determines whether the vector is to be added to the numerical data. The second command indicates the format of the numerical data. When in the absolute mode the VSW converter expects to receive four 9-bit positive numbers as the numerical data, the first two are the (x,y) value for the first vector endpoint and the second two are the second vector endpoint. The first endpoint value that will be assumed in the other two input modes is this second endpoint. The second endpoint for a vector specified by a head-to-tail or relative vector is determined from the input numerical data for that vector. This simulates a random scan CRT display by "remembering" the last point the drawing beam was sent to.

A head-to-tail mode command indicates that only two 9-bit positive numbers are to be expected as the numerical data. The input, then, is the second endpoint for the vector. The first endpoint is taken to be the saved endpoint; the second endpoint of the previous vector. The input mode becomes the saved endpoint. When a relative mode command is given, the saved endpoint is used twice. This vector's first endpoint is the saved endpoint and the vector's second endpoint is calculated from the saved endpoint and the input data. For this mode, the numerical data input is the two signed 9-bit displacements which, when added to the saved endpoint, yield the second endpoint for the vector. The resultant endpoint value becomes the new saved endpoint.

Referring to FIG. 4, XINC is basically the length of the segment that represents a vector on a particular scan line. This length is constant where only straight lines are being displayed. For vectors that are more vertical than horizontal (|dx| < |dy|, where dx = XT - XB, dy = YT - YB), then XINC is always less than 1. XINC can be calculated as follows:

\[ dx \geq 0 \text{ then set XINC to } \frac{|dx|}{|dy|} + 1, \]
\[ dx < 0 \text{ then set XINC to } \frac{|dx| + 1}{|dy|}, \]

where XINC becomes a positive 18-bit number, 9 bits of integer and 9 bits of fraction.

While it might at first glance appear the XINC should be equal to the absolute value of the inverse of the slope of each vector, i.e., \( \frac{1}{|dx/dy|} \), this produces an unfavorable result for very steep lines. For example, for a line where \( dx = 1 \) and \( dy = 512 \), with this latter approximation the line drawn on the screen would be absolutely vertical until the 512th scan of the monitor at which time a point would be displayed a distance of \( dx = 1 \) to the left or right, depending upon the sign of the slope. The calculation for XINC used yields ILS's for each vector that are approximately equal in length, within the resolution used to represent XINC and XCUR, in the embodiment therein described.

Referring again to FIG. 4, XCUR is the x value of the beginning of the vector intersection line segment on a scan line. It is also a positive 18-bit number, whose 9-bit integer part is initially set to XT, and whose 9 bits of fraction are set to zero.

The VSW is a unique description of each vector, i.e., the same two endpoints always produce the same VSW. In one embodiment, the vector memory 22 is sorted according to XINC from greatest to least. This sort that is performed for each VSW added to the memory 22 allows an important geometric assumption to be made later in the system as will be explained.

The first command of the input from the computer in each VSW tells the add/delete block 32 what is to be done with the vector specified by the remainder of the input. But in either case, add or delete, the VSW must be calculated, since that is the internal (and only) identification for a vector. As explained, the vector memory 22 is sorted as each VSW is added, by the value of XINC such that as memory 22 is read sequentially, the VSWs read from greatest XINC to least XINC. The new VSW is sorted into memory 22 by comparing the new XINC with all XINCs in the memory, in sequence. When a XINC is found in memory 22 that is less than the new XINC, then the new VSW goes into the memory 22 just before this VSW. This sort is done dynamically, and memory 22 is expanded by one location and the new VSW slipped in.

To delete a vector, the VSW values (sign, XT, YT, YB, XINC) are compared with those same values of each VSW in memory 22, in sequence, and when a match is found, the VSW is removed from memory 22. The latter is compacted, so there are no empty locations. Notice that vector memory 22 starts sorted and always stays sorted.

Because each of the vectors stored in memory 22 must be accessed and read at least once each scan line period, the access time of the memory must be such that all of the vectors can be read during this period of time. Where it is desired to have the capability of displaying up to 1000 vectors on a television monitor, for example, it is necessary to read or access the next VSW every 50 nsec.

The memory 22 can most conveniently be thought of as having a storage capability of at least MXN, where M is the maximum number of vectors to be displayed, and N is the number of bits for a VSW. In the present example, M=1000 and N=64, so memory 22 must have the capability of storing 1000 words of 64 bits each. If the requirement that it is necessary to access a VSW every 50 nsec, it has been found desirable to use a rotating storage device for the memory 22. Thus, FIG. 5A shows memory 22 comprised of a shift register 50. At each clock pulse, every 50 nsec, each 64-bit VSW shifts left by one location. The VSW at location marked VSW1 travels along the lines marked "data path" to the location marked VSW1000. Of course, such a memory is special purpose and is not manufactured exactly as described above. Available shift registers are limited in both size and speed. The shift register 50 is thus shifted such that each of the 1000 vectors appears at the output during one television raster-scan line period.

With presently existing shift registers on the market, shift register 50 can be made from a plurality of smaller shift registers linked together. Thus, in FIG. 5B each of the 64 lines of the shift register 50 is made up of four, 256 and by 1-bit shift registers 52. Sixty-four of these 4-register combinations are required to provide the single 1000 x 64-bit shift register 50 of FIG. 5A.

It is possible to form the shift register 50 from a plurality of smaller shift registers having a slower access time than 50 nsec. This is accomplished by providing a number of slower operating registers in parallel and then multiplexing the inputs and outputs of each. Thus, in FIG. 5C one 200 nsec, 256 x 64-bit shift registers
Thus, the points stored in each SLBS define the "envelope" of each ILS.

The reason for the two SLBS for a television display monitor is the following. The converter 46, which drives the television monitor 12 must be able to scan the SLBS in a sequential order, left to right, from the bit representing \( x=0 \) to the bit representing \( x=512 \). The buffer set is actually 1024 bits long to allow half values for \( x \), thus putting the resolution much beyond the resolution of even good television monitors (about 2 to 4 times better).

Arithmetic unit 34, however, cannot prepare a SLBS in a sequential order, so it is not possible to drive converter 46 directly by unit 34. Therefore, one SLBS is loaded while the other SLBS is emptied. The latter refers to setting the bits of the buffer to zero after reading the bits. Just as the emptied SLBS is being loaded again, the other SLBS is read.

When switch 1 points to SLBS 1, i.e., block 38, then switch 2 points to SLBS 2, and vice versa. These switches change after each scan line is displayed, i.e., every 65 uses. Arithmetic units 34 and 46 never have access to the same SLBS at the same time.

The SLBS that arithmetic unit 34 reads and writes is the next scan line for the current field, i.e., the one which will next be displayed on the monitor. Thus, one scan line is being calculated in advance while another is being displayed. This "buffering ahead" is an interface between two very different types of calculations, which couldn't otherwise be accomplished within the time constraints of the television data rate requirements. This has the very minor disadvantage that the data being displayed is 65 uses old.

As stated before, memory 22 holds a VSW for each vector. Two values in a VSW, XCUR and XINC, are all that is needed to display the ILS, the portion of the vector that is visible on each scan line. As explained earlier, XINC is a static value. It is calculated for each vector and remains unchanged as long as the vector is retained in memory 22. XCUR is a dynamic value; it is changed, updated, after each scan line for which the vector is visible. It is also reset after each field. To specify an ILS for a vector on a given scan line, it is sufficient to specify the endpoints of the ILS, e.g., two \( x \) values. The scan line allows \( x \) values from 0 to 512. A vector's XCUR is always one endpoint for that vector's ILS and the other endpoint is XCUR+XINC.

As the electron scans the line, the two endpoints represent the positions where the beam must turn-on and turn-off, respectively. Since one scan line is calculated ahead of the physical displaying of the scan line, these values are temporarily stored in one of the two SLB's, say SLBS 40, one RAM of the SLBS for the turn-on endpoints and the other RAM (i.e., the other of the two 1024-bit RAM's comprising the SLBS) for the turn-off endpoints. Hence, after all VSW's have been considered for a scan line, the SLBS contains the envelope of the actual points to be intensified for the scan line.

While the electron beam deflection circuitry in the television monitor 12 sweeps the beam from left to right on a scan line, video converter 46 sequentially reads the two RAM's of the SLBS, SLBS 40 in this example, that contains the envelope. Converter 46 converts the envelope of the displayable line segments into an intensified image on the television monitor 12, i.e., as the electron beam is deflected to trace out the scan line, the CRT beam is turned on to intensify the points.

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54, 56, 58 and 60 are connected in parallel. Each of these shift registers in turn being comprised of sixty-four 256 x 1 shift register. Each of these shift registers holds every 4th VSW. Thus, register 54 holds VSW’s 1, 5, 9 etc.; register 56 holds VSW’s 2, 6, 10, etc.; register 58 holds VSW’s 3, 7, 11, etc.; and register 60 holds VSW’s 4, 8, 12, etc.

VSW’s are alternately read into the shift registers 54, 56, 58 and 60 by means of a demultiplexer 62 and in a similar manner the VSW’s are sequentially read out of the registers by a multiplexer 64. The multiplexer 64 and demultiplexer 62 are constructed of a plurality of single-pole, four-throw solid state switches, such as Texas Instruments TTL/MSI IC numbers SN74S153 and SN74S139, respectively, which can step positions in 50 nsec. The two switches are synchronized such that a VSW, or part of a VSW, can be changed and written back into the shift register 50 at the proper VSW location.

With the foregoing arrangement it can be seen that the output from the multiplexer 64 and the input to the demultiplexer 62 will be one VSW every 50 nsec, even though the shift rate of each of the individual shift registers 54, 56, 58 and 60 is 200 nsec.

Thus, the add/delete arithmetic unit 40 adds and deletes entire vector memory words. The 1000 words of memory 22 circulate in a closed path through the shift registers forming the memory 22. A word makes a complete cycle in 50 uses. VSW’s to be added or deleted are slipped into, or switched out of, the internal flow of the memory 22 in a manner which will be explained in greater detail subsequently.

An incremental scan segment, hereinafter also referred to as an intersection line segment (ILS) is the term used to describe the part of a vector that is visible on a scan line; it is the intersection of a vector with a scan line. Of course, not all vectors will likely be visible on every scan line. It may have a length of from one point, e.g., a vector with slope greater than or equal to 45°, up to 512 points, e.g., a horizontal vector with slope 0 degrees. This length, for each vector, is the XINC field of the VSW for the vector.

Blocks 34 and 36 of FIG. 3 form an arithmetic unit which performs operations for each scan line in a field. Each VSW is examined to see if it is visible, i.e., if it intersects the current scan line. A vector is visible if and only if \( Y \geq YS \geq YB \), where \( YS \) is the vertical position of the current scan and \( YT \) and \( YB \) are picked up from the vector's VSW in memory 22. If it is not visible, it is considered no further. If it is visible, the ILS is calculated, and the endpoints are stored into one of two scan line-buffer or storage units, 38 and 40. And one field contained in the VSW, i.e., XCUR, is updated to be the new endpoint for the next scan line.

In the embodiment which will be described, each of the scan line buffer sets (SLBS) 38 and 40 consists of two 1024-bit random access memories (RAM). There are two SLBS required for the present scan conversion system. At any given time, the video signal converter block 46 is displaying a scan line from one SLBS while the other SLBS is being used for the next scan line to be displayed.

The SLBS that is read by converter 46 contains the endpoints of the ILS's of the vectors that are visible on the scan line. In particular, binary ONES are written at locations corresponding to the endpoints of the ILS's.
at the locations corresponding to the bits between the turn-on and turn-off bits in the SLBS.

Converter 46 is implemented as an up/down counter 130, as explained with reference to FIG. 15. That means, if the “count-up” input gets a pulse, then one is added to the value held in the counter. If a pulse is applied to the “count-down” input line, then one is subtracted from the value held in the counter. The value held in the counter is the number that appears on the output lines of the counter. In addition, converter 46 is designed such that:

1. The counter output is never allowed to be negative.
2. The count-up and count-down input lines never receive a pulse at the same time.

Actually, it should never be the case that the counter “wants” to go negative, so this constraint guards against hardware malfunctions. XCUR is accurate to \(1/512\) of an \(x\) unit, i.e., 9 bits of integer and 9 bits of fraction, but the SLBS is only accurate to \(1/2\) of an \(x\) unit. Therefore, if a vector is nearly vertical it will often be the case that the bits written into the turn-on and turn-off buffers of the SLBS will correspond to the same point, i.e. the same \(x\) location. This would imply that the counter would receive count-up and count-down inputs at the same time. Instead, as explained in more detail subsequently, the count is not changed, but a single-shot multivibrator 198 (FIG. 15) is fired which turns on the electron beam to intensify just the one point.

There are several advantageous reasons for sorting, by XINC, the vectors in memory 22. However, it should be understood that other techniques can be employed which do not require sorting.

Both reasons are due to all the IL’s that are produced by the many vectors that may cross an individual scan line. For example, consider, in FIG. 6A, the three vectors crossing scan lines 1 and 2. FIG. 6B shows in more detail the intersection of vectors 1 and 3 with raster-scan line 1. Also shown is how the ILS data for intersection of these two vectors is stored in one of the SLBS’s. Note again that each SLBS comprises two 1024 (RAM) buffers, one for storing ILS-turn-on points and the other for storing ILS-turn-off points.

If only one 1024-bit buffer was used to represent the on-off values, then the on endpoint for the ILS of vector 1 would be mistakenly taken to be the off endpoint for the ILS of vector 3. One bit is not enough information to distinguish on and off bits. It is not necessary to distinguish between an individual vector’s on-off bits, only the distinction between any on and any off bit. Therefore, two bits are sufficient, hence two 1024-bit buffers make up each SLBS.

FIG. 6C is a detail of the intersection of vectors 1 and 2 with raster-scan line 2. It is this difficult situation that lends itself to the ordering or sorting of the vectors in the memory 22. Because both ILSs have beginning points at the same \(x\) coordinate, only one turn-on bit, but two turn-off bits are loaded in the respective buffers forming one of the SLBSs.

Were this allowed to happen, the SLBS would describe an ambiguous situation. Decoding of the envelope by converter 46 would be quite confused. Therefore, before either endpoint value of an ILS is recorded in the SLBS, the appropriate RAM of the buffer is read to see if it already contains a 1 at that location. If a 1 is found, no bits are written in the SLBS and the ILS is known to be obscured completely by another ILS. This is guaranteed to be true since the length of the ILS is the value of XINC. Memory 22 is sorted according to XINC from greatest to least. Therefore, the obscuring ILS, handled first, is longer than the obscured ILS in every case. Hence, the obscured ILS can be neglected.

During each scan line of each field, all VSWs are read once, and if the vector represented by the VSW actually crosses the scan line, e.g., \(Y \geq YS \geq YB\), then XCUR in the VSW will be updated. This update finds the next endpoint for the ILS and also compensates for the fact that the very next scan line is skipped over until the next field.

As previously explained, a CRT in a television monitor first displays a field of video picture on the odd numbered scan lines and then a second field on the even numbered scan lines. Thus, during any given field every other line is scanned. Thus, to update XCUR (XCUR’), a value of twice XINC must be added to the present XCUR to compensate for the skipped lines. This is best illustrated by reference to FIG. 7, showing a field being scanned on even lines only. The update, XCUR' (the new XCUR), is calculated as follows:

If the sign is 1 (negative slope), then XCUR’ becomes XCUR + (2.XINC)
If the sign is 0 (positive slope), then XCUR’ becomes XCUR - (2.XINC).

At the end of each field XCUR must be reset. Were it not for the existence of two fields of video per frame, XCUR would be reset to XT at the end of each picture.

To compensate for the two fields, XCUR is reset according to the following rules:

1. If the next field is composed of the ODD scan lines, then:
   a. if YT is odd and sign = 0 (positive slope) then XCUR’ becomes XT – XINC
   b. if YT is even and sign = 0, then XCUR’ becomes XT - (2.XINC)
   c. if YT is even and sign = 1, then XCUR’ becomes XT + XINC

2. If the next field is composed of the even scan lines, then:
   a. if YT is even and sign = 0, then XCUR’ becomes XT – XINC
   b. if YT is even and sign = 1, then XCUR’ becomes XT - (2.XINC)
   c. if YT is odd and sign = 0, then XCUR’ becomes XT + XINC
   d. if YT is odd and sign = 1, then XCUR’ becomes XT + XINC.

This algorithm makes sure the interleaved fields are properly registered. Since this algorithm is not applied to a vector when it is first entered into vector memory, and since a vector might be added to vector memory during any scan line, there is a 99% probability that XCUR will be incorrect until it is reset. So the new vector will be displayed incorrectly for 1/60 second, it is reset to the correct starting value. The incorrect vector is clearly invisible to the human eye.

FIG. 8 is a detailed drawing of blocks 30 and 32 of FIG. 3. FIG. 9, giving the logical sequence of operational steps carried out by the hardware of FIG. 8 should be read in conjunction with the following description of FIG. 8. In order to simplify the schematic diagram only single lines are used to indicate data flow paths. The number in brackets indicates the width, in
bits, of a data line when the path is greater than 1 bit wide. Dotted lines indicate a decision path or line of influence.

The circuit of FIG. 8 accomplishes three major computations:
1. The receiving and decoding of graphical input data from the computer and determination of the two vector endpoints;
2. The deriving of the internal vector representation, VSW, which is to be stored in memory 22; and
3. The storing into, or deletion from, memory 22 of the VSW for each vector.

Input is received by input register 70 from the computer 16 and may contain as much data as is indicated in the input register 70; i.e.,
1. Two commands—action (add/delete) and the vector mode (absolute, relative, or head-to-tail); and
2. Up to two endpoints, or data for determining the endpoints, termed X₀, Y₀, and X₁, Y₁.

The input is decoded in a straightforward manner. The command bits are held as values in the command word register 72. The value is either 1 or 0, i.e., logic states true or false. The command bits determine the switching of gates later in the computations. The numerical data, the endpoints, are decoded or determined at 73 as specified by the mode command bits. For relative and head-to-tail mode, the endpoint value in the saved endpoint register 74 is used in this calculation.

As a result of the input decoding and endpoint calculation, two absolute Cartesian coordinate endpoints are derived which exactly define the endpoints of the vector received as input. These endpoints are the X₀, Y₀ and X₁, Y₁ values in the endpoint register 76. These are nine-bit quantities, i.e., capable of representing any point on the 512 by 512 screen. The X₁, Y₁ endpoint corresponds to the second endpoint received in absolute mode, or calculated in relative or head-to-tail mode.

Note that in the absolute mode, X₀, Y₀, X₁ and Y₁ stored in register 70, define the two ends of a vector. In head-to-tail mode, X₀ and Y₀ define the second endpoint of the vector and nothing is inputted to register 70 in the X₁ and Y₁ positions. In the relative mode, X₀ and Y₀ define incremental values to be added to the second endpoint of the last vector. Again, nothing is provided at X₁ and Y₁.

The schematic diagram in FIG. 10 shows the endpoint calculation block 73 in greater detail. The data lines contain the saved endpoint, X₅, Y₅, as well as all the input data, including the vector mode command. The endpoint data lines carry 9-bits of data each (in parallel) and the command data lines are 1-bit data lines. When any one of the command lines is true, the other two command lines are false and the correct values for the endpoints are gated to the endpoint register 76.

In the case of relative mode, an addition or subtraction is performed to add the received values to the saved endpoint to determine the second endpoint for the new vector. For the x-coordinates, this is performed at 79 and for y-coordinates at 81.

The second endpoint is saved in the saved endpoint register 74, and is equivalent to updating the "drawing" position of the display, i.e., this endpoint represents the place where the drawing on the display stopped, i.e., where the artist "lifted the pencil."

The second major function of this part of the system is now started, namely the conversion of a vector expressed as Cartesian coordinate endpoints into a form suitable for storage in the vector memory 22. This internal form allows the scan conversion to be easily accomplished, by having available all the information needed for determining the raster-scan lines that the vector intersects.

Two calculations are performed simultaneously to derive the vector storage word. To determine the values of XT, YT, YB, and XCUR to be loaded into the VSW register 82, a simple compare on the values of Y₀ and Y₁ is done at 78. The maximum of Y₀ and Y₁ becomes YT, and the remaining y-value becomes YB. In the initial VSW, XT is equivalent to the integer portion (the left-most 9 bits) of XCUR, and is the x-value of the endpoint whose y-value becomes YT. Switches 80 show a simple scheme for insuring that the correct values arrive in the correct portion of the VSW register 82, depending on the results of the Y₀, Y₁ comparison operation.

The second operation for determining the remaining fields of the VSW is to calculate the values of XINC and SIGN, which is performed at block 84. A more detailed diagram of this calculation is given in FIG. 11. The two x-values of the endpoints in the endpoint register are subtracted at 85 to yield at 87 a delta-x (dx) value that is, the distance in the horizontal direction that the vector spans on the display area. Delta-x is a signed value, where the sign indicates whether the X₀, Y₀ vector endpoint is left or right of the X₁, Y₁ vector endpoint. Simultaneously, exactly the same operation is performed at 89 on the Y₀ and Y₁ values of the endpoint register, to yield a delta-y (dy) value at 91. The dy sign indicates whether the X₀, Y₀ endpoint is above or below the X₁, Y₁ endpoint. A logical exclusive-OR operation is performed at 93 on the sign bits of dx and dy to yield the SIGN field for the VSW. An operation 83 of the dx and dy values (un-signed) determines the XINC field. This operation is to either add one to dx and divide by dy or to divide dx by dy plus one. The division is a 9-bit integer division operation.

The third stage of operation indicates whether adding or deleting the vector received as input to or from the memory 22. The addition and deletion of vectors can proceed simultaneously if desired. Also the present system is not restricted to adding only one vector at a time, but for simplicity the diagram only shows the logic for one vector addition. A deletion or addition requires one cycle of vector memory 22. This constraint is so that every vector contained in the memory may be examined and compared to the vector (actually the VSW) to be added.

Referring again to FIG. 11, in the operation of the exclusive-OR gate 93, if after subtracting the respective x and y coordinate values, the signs of both are the same, whether true or false, then a logical false or 0 signal is provided by the Exclusive-OR gate 93. But if after subtracting, the signs are different, the gate 93 provides a true or 1 output.

In the vector deletion process, the VSW to be deleted is compared with all those contained in memory 22, and the first VSW in vector memory 22 that is identical is deleted. The VSW fields that are compared are XT, YT, YB, XINC and SIGN. Thus, in FIG. 8, the 46 bits making up these fields passes from the VSW register 82 over line 86 to equality compare circuit 88. The same
fields from each of the circulating VSW's from memory 22 are fed via line 90 to the compare circuit. Vectors which are not deleted circulate directly back to vector memory 22 via 64-bit line 92, after being read-out for further processing at 94. When compare circuit 88 finds the VSW from memory 22 to be deleted, i.e., when the input from 86 and 90 are identical, the 64-bit VSW passing along line 92 is stored in data register 96. Ganged switches 98, route the flow of subsequent VSW's for that field through path 100, around register 96. At the completion of the line the register 96 is cleared and switches 98 are reset. Essentially, switches 98 act like AND gates. Thus, to by-pass register 96 a delete command is required both from command word register 72 as well as from compare circuit 88.

The schematic diagram of FIG. 12 details a scheme for accomplishing a 20-bit compare in 50 nanoseconds. Four, 5-bit compare circuits, compare two, 20-bit numbers, A and B. The bits comprising each number are grouped in sets of five bits from the least to the most significant bits. When A=B for each of the five comparators 102, a true signal is given from AND-gate 104. The 5-bit comparators 102 are standard Fairchild TTL/MSI integrated circuits and the gates are high-speed logic gates of the indicated type.

A similar circuit can be made for comparing 10 bits in 50 nanoseconds. The operation of the circuit is essentially the same as the comparator circuit of FIG. 12 except that only two, 5-bit comparators are used.

To form the 46-bit comparator 88 three of the 20-bit compare circuits of FIG. 13 and one 10-bit compare circuit are combined. To combine these circuits, the outputs from all of the equality AND-gates are gated to another AND-gate (not shown). Also sent to this AND-gate is the output from still another AND-gate (also not shown). This latter AND-gate verifies the SIGN.

When a VSW is deleted from memory 22, the memory 22 is compacted so that no "hole" exists for that location. The data flow chart indicates data register 96 containing the deleted VSW is bypassed and the deleted VSW is just no longer in the memory 22 data flow circuit.

Vector memory 22 is sorted at all times, so the addition of a VSW requires that the new VSW be inserted into the memory 22 data flow at the correct location. As explained previously, memory 22 is sorted by XINC from greatest to least. Each VSW of memory 22 shown figuratively at 112 is examined at comparator 110 and is compared with XINC of the new VSW in VSW register 82, the new XINC being stored temporarily in another register 114. The data flow is normally along data line 95, so as to bypass register 114, holding the new VSW. If the XINC of VSW from memory 22 is less than the XINC of the new VSW, then the data flow is switched by ganged switches 116 to include the register 114 holding the new VSW, i.e. along data path 97, through the register 114. Thus, the new VSW is inserted at the correct time, and memory 22 is always sorted.

The add/delete command from register 72 determines which of these operations will be done for the new VSW. At the same time, as indicated on the diagram, the VSWs from memory 22 are read out and are displayed. It is possible and quite probable that all phases are operating at the same time. To add more than one vector per scan line, additional comparators 110 and registers 114 are required, i.e., one set of each is required per additional vector to be added.

Operation of blocks 34 and 36 of FIG. 3 is illustrated in greater detail in FIG. 13. FIG. 13 should be read in conjunction with FIG. 14. The later is a logical sequence of the functional operation of the circuit of FIG. 13. For the purposes of these figures the following definitions are used.

"From" and "to" are the endpoints of an ILS. "DPYON" (short for "display on") is the name for the "turn-on" buffer in each of the SLBSS 38 and 40. "DPYOFF" (short for "display off") is the name for the "turn-off" buffer in each of the SLBSS 38 and 40. And finally, "DPYON (x-position)" and "DPYOFF (x-position)" are functions which indicate (address) a bit in the SLBS.

The circuit of FIG. 13 performs two important functions. First, it determines the endpoints or envelope of points for all of the ILSs intersecting each scan line; and secondly, it updates XCUR for each vector in memory 22.

Compare circuit 120 compares Y1 and Y1B for each vector circulating out of memory 22 with Y SCAN, the current scan line, to determine if the vector intersects that scan line. The current scan line number is given from counter 122 which is driven by a signal from video converter 46.

If a vector does not intersect the current scan line, i.e., if the condition YB ≤ YSCAN ≤ YT is false and not met, the comparator 120 causes ganged switches 124 to return the 64-bit VSW directly back to memory 22 via line 126 without further processing. If the condition is true then the VSW is stored in register 128.

The new value of XCUR, XCUR', is calculated by an add/subtract circuit 130. Since XCUR' = XCUR + XINC, circuit 130 reads the values of XCUR and XINC of the current VSW from the register 128, and outputs this computed value to the TO register 140 along data path 135. And then, depending upon the sign of the VSW from register 112, either adds or subtracts twice XINC to determine the update value XCUR'.

At register 132, the 64-bit VSW from register 128, which arrives at the register 132 via line 134, is updated with XCUR' which is sent from add/subtract circuit 130. From the register 132, the updated VSW (with XCUR') returns to memory 22 via line 136.

As previously explained, because of geometric considerations, DPYON 142 and DPYOFF are read at 146 and 148 respectively to determine whether or not a ONE has previously been entered at that position. Gate 150 provides a true output only if there are no ONEs in either DPYON 142 or DPYOFF 144. If there are none, ganged data latches 152 allow write circuits 154 and 156 to write bits into the appropriate DYRON 142 or DYPOFF 144. Data latches 158, operated by video converter 46, switch the outputs from writers 154 and 156 to between SLBS 38 and 40.

Converter 46 converts the vector envelope or endpoints stored in the two SLB's 38 and 40 into a video signal for driving the television monitor 12. Details of the converter 46 are shown in FIG. 15. The logical decisions carried out by the circuit of FIG. 15 are described in the flow chart of FIG. 16 and should be read in conjunction with the following description of FIG. 15.

A key part of the converter circuit 46 is an up-down counter 180. The output from counter 180 activates
and deactivates the television monitor 12 by means of a digital to analog switch 182 which controls the grid voltage of the CRT of the television monitor 12. A binary ZERO from counter 180 prevents the electron beam from 184 from striking the CRT display screen while a binary value of ONE or higher allows the beam to strike the screen.

An x-scan converter 186 keeps track of the x-position of the electron beam of the CRT. The counter 186 is driven by a clock 188 driven by the synchronizing and blanking generator of the television monitor 12. This same clock drives the x-scan counter 122. (FIG. 13).

Counter 186 must have enough capacity for each discrete x-position along a scan line. In the present embodiment, there are 1024 possible x-positions and so the counter must have at least 10 bits to represent any x-position in this range of 1 to 1024. The counter is incremented by one for each x-position swept by the electron beam. When the counter overflows 1024 and becomes zero again, x-scan reset 190 switches the SLBS's 38 and 40, depending upon which is to be read next. This is accomplished through a pair of data flow switches 192.

The appropriate DPHYON 142 or DPOFF 144 is read by circuit 194 or 196, depending upon which SLBS is currently being read. The outputs from these two circuits are gated through AND-gates in order to turn-on or turn-off the electron beam and in order to update the counter 180. There are four possible cases which can occur, depending upon the status of the DPHYON and DPOFF. Case I: DPHYON (x) = 1; DPOFF (x) = 0. This is the situation that can occur when there is a steep line or when there is a point to be displayed on the screen, and hence the ILS is only one x-position in width. A single shot multivibrator 198 turns on switch 182 so that the electron beam is provided for only one burst of electrons.

Case II: DPHYON (x) = 1; DPOFF = 0. This is the case for the beginning or turn-on point of an ILS. The counter 180 is incremented by one. Of course, the electron beam is turned on (or maintained on) since the state of the counter 180, a fortiori, is greater than zero. As explained previously, so long as counter 180 is greater than zero, the electron beam will always be provided to the CRT screen.

Case III: DPHYON (x) = 0, DPOFF (x) = 0. This case occurs at the end of an ILS. First, the counter 180 is decremented by one. If the counter still is at a value greater than 0, then the electron beam is turned on (or maintained on). If the counter 180 is at zero, then the beam is turned off (or maintained off). Since this procedure shortens the display of an ILS by one x-position, the single shot multivibrator 198 is triggered via data path 181 to display the last point of the ILS.

Case IV: DPHYON (x) = 0; DPOFF = 0. The count in counter 180 remains the same, and the beam is on or off depending upon the existing count in the counter 180.

It was explained that because of the existence of interlacing odd and even fields, each time a complete field is displayed on the CRT screen, XCUR for each vector cannot automatically be reset to XT at the beginning of each new field. A set of rules was given previously for setting XCUR for each vector at the beginning of each new field. The circuitry for carrying out these rules is shown in FIGS. 13 and 17. Reference is also made to the logic diagram of FIG. 14.

FIG. 17 is a circuit to implement the rules given for resetting XCUR to the correct value before each field is scanned. This process requires only one cycle of vector memory 22 to reset all VSW's. Since there are several scan lines which are not displayed both before and after each field, there is ample time for this operation to be accomplished. Exclusive-OR gate 129 determines if, when the field is even, whether YT is also even, and when the field is odd, whether YT is odd. The VSW with XCUR reset to its initial value is returned to vector memory 22 via data path 131.

We claim:

1. A digital scan conversion system for displaying on a raster scan output device an arbitrary graphical pattern, wherein said pattern comprises one or more vectors and wherein each vector is defined by a graphical line data, comprising:

   a. means for receiving digitally-coded graphical line information for each vector forming said arbitrary graphical pattern;

   b. processing means responsive to said receiving means for determining at least graphical line boundary data for each vector and determining a vector storage word which uniquely defines each vector of said arbitrary graphical pattern, said processing means additionally including

   c. means for storing said vector storage word for each vector;

   d. means for accessing said vector storage words from said storing means so that the vector storage word for each vector is accessed at least once during each scan of said raster-scan output device;

   e. first means responsive to said accessing means for determining for each vector forming the pattern, the intersection scan-line segments for each scan of said output device intersected by each of said vectors required to synthesize each vector of the pattern;

   f. second means responsive to said vector storage words provided by said accessing means and to said intersection scan-line segments provided by said first means for determining for each scan of the raster scan output device the composite of all of the intersection scan-line segments which must be displayed during that scan and storing said composite; and

   g. means responsive to said second determining means for activating and de-activating said raster-scan output device according to the stored composite of all of the intersection scan lines during each scan thereof.

2. A digital scan conversion system as in claim 1 wherein said digitally-coded graphical line information is sent from a computer.

3. A digital scan conversion system as in claim 1 wherein said digitally-coded graphical line information is received over a high-bandwidth data transmission line.

4. A digital scan conversion system as in claim 1 wherein said raster-scan output device is a conventionally scanned television monitor.

5. A digital scan conversion system as in claim 1 wherein said raster-scan output device is an electrostatic printer.
6. A digital scan conversion system as in claim 1 wherein said storage and accessing means comprising a recirculating storage device.

7. A digital scan conversion system as in claim 1 wherein said vectors are all straight line vectors arbitrary as to both length, position and orientation, and said intersection scan-line segments are the same for each straight-line vector for each intersected scan of said raster-scan output device.

8. A digital scan conversion system as in claim 7 wherein for each straight-line vector said intersection scan-line segment data is stored with the vector storage word in said storage means.

9. A digital scan conversion system as in claim 8 wherein said vector storage word for each straight-line vector is stored in an order from the straight-line vector having the longest intersection scan-line segment to the straight-line vector having the shortest intersection scan-line segment.

10. A digital scan conversion system as in claim 8 wherein said second means comprises at least a pair of random access memory devices, and wherein each of said random access memory devices receives and stores intersection scan-line data for all straight-line vectors intersecting one scan line of said output device, the order of said scan-line data being arranged to coincide with the scan sequence, and wherein each one of said pair alternately and sequentially stores said intersection scan-line data.

11. A digital scan conversion system as in claim 10 wherein each of said random access memory devices comprises first and second display registers, said first display register storing the beginning points of each intersection scan-line segment for a scan-line and said second display register storing the end points for each intersection scan-line segment for a scan line.

12. A digital scan conversion system as in claim 11 wherein said activating and deactivating means comprises means responsive to said first display register for activating said output device and means responsive to said second register for deactivating said output device.

13. A digital scan conversion system as in claim 10 wherein said activating and deactivating means comprises means for alternately reading each of said random access memory devices and activating and deactivating said output device in accordance with the intersection scan-line data stored in each.

14. A digital scan conversion system as in claim 1 wherein said first means is operable to determine said intersection scan-line segments while the preceding scan-line composite is being provided as input to said raster-scan output device.

15. A digital scan line conversion system as in claim 10 wherein one of said pair of said random access memory devices stores said intersection scan-line segments while the other of said pair is being read by said activating and deactivating means.

16. A digital scan conversion system as in claim 1 including means for adding to and deleting from said storage means the vector storage words for selected individual vectors concurrent with the operation of the digital scan conversion system.

17. A system for displaying graphical information in the form of patterns of straight line vectors on a conventional raster-scan cathode ray tube television monitor, said graphical information being provided from a computer to said display system in the form of binary-coded Cartesian coordinates identifying each vector comprising:
   a. first means for determining for each vector comprising the pattern the incremental length that the beam of said cathode ray tube must be provided during those horizontal sweeps of said cathode ray tube beam necessary to reconstruct the vector;
   b. first storage means responsive to said first means for storing vector identification information for each vector comprising the pattern; said information comprising at least said incremental lengths;
   c. said first storage means including accessing means being capable of referencing each vector identification information at least once during each horizontal scan period;
   d. second means responsive to said vector identification information provided by said accessing means for determining for each horizontal scan of said cathode ray tube horizontal scan information comprising the location of said incremental lengths for all vectors which intersect that horizontal scan line and including second storage means for storing said horizontal scan information; and
   e. means for accessing said second storage means for activating and deactivating said cathode ray tube beam according to said stored horizontal scan information during each horizontal sweep thereof.

18. A system as in claim 17 wherein said storing means comprises a rotating storage device.

19. A system as in claim 17 wherein said storing means comprises a shift register.

20. A system as in claim 19 wherein said shift register has at least M by N storage capacity, where M corresponds to the maximum number of vectors which can be displayed, and N corresponds to minimum number of bits necessary to store said vector identification information.

21. A system as in claim 19 wherein the cycle rate of said shift register is at least as great as the horizontal scan rate of said cathode ray tube.

22. A system as in claim 17 wherein said second storage means includes first and second storage devices, said storage devices first storing horizontal scan information for the next succeeding horizontal scan and secondly providing horizontal scan information to said activating and deactivating means for the current horizontal scan being displayed on said cathode ray tube, and wherein said first storage device is storing said horizontal scan information while said second provides said information, and at the completion thereof, said first storage device provides said information while said second storage device is storing said scan information.

23. A system as in claim 22 wherein the access speed of said first and second storage devices is sufficiently great to enable all of said horizontal scan information to be stored and read during one horizontal scan period.

24. A system as in claim 22 wherein each of said first and second storage devices comprises a turn-on and turn-off storage device, said turn-on storage device storing information corresponding to the beginning points of said incremental lengths in a horizontal scan line and said turn-off storage device storing information corresponding to the endpoints of said incremental lengths, said activating and deactivating means being responsive to the information stored in said turn-on storage device to activate said cathode ray tube beam.
and being responsive to the information in said turn-off storage device to deactivate said cathode ray tube beam.

25. A system as in claim 24 wherein said turn-on and turn-off storage devices each comprise a random access memory device.

26. A system as in claim 17 wherein said second means is operable to determine said horizontal scan information for a scan line while the preceding scan-line is being outputted on said television monitor.

27. A system as in claim 17 including means for insuring registration of vectors displayed on said television monitor at the beginning of each new video field.

28. A system as in claim 1 wherein said activating and de-activating means includes an up-down counter, said counter being counted up by bits located in said turn-on storage device and counted down by bits located in said turn-off storage device; and wherein said cathode ray tube beam is provided whenever the output of said counter is greater than zero.

29. A system as in claim 28 wherein said beginning and said end points of said incremental lengths are stored in said turn-on and turn-off storage devices, respectively, only if no bits have previously been stored in either of those locations in said turn-on and turn-off storage devices.

30. A system as in claim 17 wherein said vector identification information is stored in an order from the vector having the largest incremental length to the vector having the smallest incremental length.

31. A system as in claim 29 wherein said activating and de-activating means includes a single pulse-providing circuit, and wherein said circuit is activated to provide a single point display on said television monitor whenever said turn-on and turn-off storage devices have bits stored at the same relative locations.

32. A system as in claim 17 including means for adding to and deleting from said first storage means vector identification information for selected individual vectors concurrent with the display of graphical information.

33. A scan conversion system for displaying graphical information in the form of patterns of straight line vectors on a raster-scan output device, said graphical information being provided from a computer to said scan conversion system in the form of binary coded Cartesian coordinates identifying each vector comprising:

a. first means for determining for each vector comprising the pattern the incremental length for each scan of said output device for those scans necessary to synthesize the vector;
b. first storage means responsive to said first means for storing vector identification information for each vector comprising the pattern, said information comprising at least said incremental length;
c. said first storage means including accessing means for referencing each vector identification information at least once during each scan of said output device;
d. second means responsive to said vector identification information provided by said accessing means for determining for each scan of said output device scan information comprising the location of said incremental lengths for all vectors which intersect that scan line and including second storage means for storing said information; and

e. means for accessing said second storage means for altering the intensity of the output device scan according to said stored scan information.

34. A system as in claim 33 wherein said first storage means comprises a rotating storage device.

35. A system as in claim 33 wherein said first storage means comprises a shift register.

36. A system as in claim 35 wherein said shift register has at least M by N storage capacity, where M corresponds to the maximum number of vectors which can be displayed, and N corresponds to the minimum number of bits necessary to store said vector identification information.

37. A system as in claim 35 wherein the cycle rate of said shift register is at least as great as the scan rate of said raster-scan output device.

38. A system as in claim 33 wherein said second storage means includes first and second storage devices, said storage devices first storing scan information for the next succeeding scan and secondly providing scan information to said activating and deactivating means for the current scan being displayed on said raster-scan output device wherein said first storage device is storing said scan information while said second provides said information, and at the completion thereof, said first storage device provides said information while said second storage device is storing said scan information.

39. A system as in claim 38 wherein each of said first and second storage devices comprises a turn-on and a turn-off storage device, said turn-on storage device storing information corresponding to the beginning points of said incremental lengths in a scan line and said turn-off storage device storing information corresponding to the endpoints of said incremental lengths, said activating and de-activating means being responsive to the information stored in said turn-on storage device to activate said raster-scan output device and being responsive to the information in said turn-off storage device to deactivate said raster-scan output device.

40. A system as in claim 39 wherein said turn-on and turn-off storage devices each comprise a random access memory device.

41. A system as in claim 33 wherein said second means is operable to determine said scan information for a scan line while the preceding scan line is being displayed by said raster-scan output device.

42. A system as in claim 41 wherein said vector identification information is stored in an order from the vector having the largest incremental length to the vector having the smallest incremental length.

43. A system as in claim 42 wherein said activating and de-activating means includes an up-down counter, said counter being counted up by bits located in said turn-on storage device and counted down by bits located in said turn-off storage device; and wherein intensity input to said raster-scan output device is provided whenever the output of said counter is greater than zero.

44. A system as in claim 43 wherein said beginning and said endpoints of said incremental lengths are stored in said turn-on and turn-off storage devices, respectively, only if no bits have previously been stored at either of those locations in said turn-on and turn-off storage devices.
45. A system as in claim 44 wherein said activating and de-activating means includes a single pulse-providing circuit, and wherein said circuit is activated to provide a single point display on said raster-Scan output device whenever said turn-on and turn-off storage devices have bits stored at the same relative locations.

46. A system as in claim 33 including means for adding to and deleting from said first storage means vector identification information for selected individual vectors concurrently with the display of graphical information.

47. A conversion system for converting digitally encoded graphical data comprising a plurality of arbitrary graphical lines for display on a raster-Scan output device, comprising:
   a. means for storing information for each graphical line forming the graphical display;
   b. means for accessing said information at least once during each scan period;
   c. means for determining from said information for each graphical line, the incremental length of each intersection of the graphical line with each scan which it intersects;
   d. means for determining for each scan line of said raster-Scan output device, on a scan line to scan line basis, the location of the intersection lengths of all of the graphical lines which cross the scan line;
   e. means, responsive to said accessing means, for generating activating and deactivating signals for said output device for each scan line according the location and incremental length of each graphical line determined by said determining means.

48. A method of digitally converting graphical information comprising a plurality of arbitrary graphical lines into a form suitable for displaying on a raster-Scan output device, comprising the steps of:
   a. receiving digitally encoded information for each graphical line to be displayed;
   b. determining from said information for each graphical line, the length of each intersection of the graphical line with each scan line which it intersects;
   c. determining for each scan line of said raster-Scan output device, on a scan line to scan line basis, the location of the intersection lengths of all of the graphical lines which cross the scan line; and
   d. providing to said raster-Scan output device, activating and deactivating signals in accordance with said determinations.

49. A method of digitally converting digitally encoded straight line vectors for display on a raster-Scan output device comprising the steps of:
   a. determining for each vector the incremental line segments of each scan of said output device for each of those scans intersected by the vector;
   b. storing vector identification information for each vector, said information comprising at least said incremental line segments;
   c. accessing each vector identification information for each vector at least once during each scan of said output device;
   d. determining for each scan of said output device, scan information comprising the location of said incremental line segments for all vectors which intersect that scan line; and
   e. providing to said raster-Scan output device, activating and deactivating signals in accordance with said determinations.

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