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- (54) Title: A POWER FIELD EFFECT TRANSISTOR, A POWER FIELD EFFECT TRANSISTOR DEVICE AND A METHOD OF MANUFACTURING A POWER FIELD EFFECT TRANSISTOR

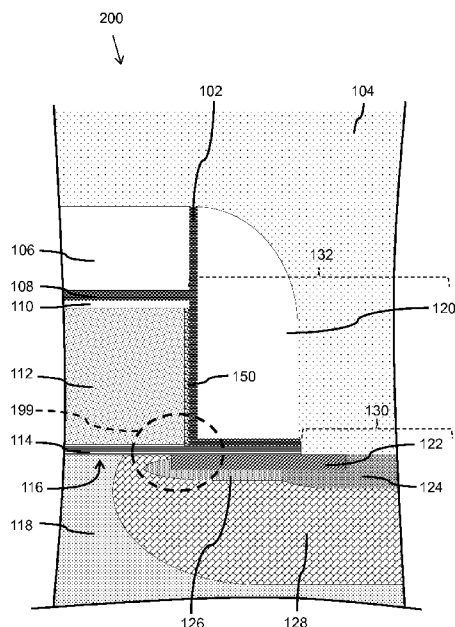


Fig. 2

- (57) Abstract: A power field effect transistor (200), a power field effect transistor device and a method of manufacturing a power field effect transistor are provided. During the manufacturing of the power field effect transistor (200), a body drive stage to manufacture the body region (128) of the power field effect transistor (200) is shortened to obtain a relatively low on resistance for the power field effect transistor (200). Before the implanting stage of the dopants of the body region (128), a pre body drive stage is introduced. During the pre body drive stage and the body drive stage sidewalls of a polysilicon layer (112) of the power field effect transistor (200) are oxidized to obtain a power field effect transistor (200) which has at the sidewalls an oxidized polysilicon layer (150) that is thick enough to prevent a premature current injection from the gate (112) to the source regions (122) of the power field effect transistor (200).



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Title : A power field effect transistor, a power field effect transistor device and a method of manufacturing a power field effect transistor.

Description

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Field of the invention

This invention relates to power field effect transistors, power field effect transistor devices and a method of manufacturing a power field effect transistor. Power field effect transistors are configured to operate under relatively large voltages, for example, voltages larger than 500 volts, or even larger than 1 kVolt. Thus, power field effect transistors have a relatively large breakdown voltage. When a plurality of power field effect transistors are combined in one device, the device is capable of conducting relatively large currents, for example, current larger than 250 ampere, or even larger than 500 ampere.

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Background of the invention

Semiconductor devices such as Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are commonly used as power devices in applications, such as automotive electronics, power supplies, telecommunications, which applications require devices to operate at currents in the range of tenths up to hundreds of amperes (A).

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Conventionally, by applying a voltage to the gate electrode of a MOSFET device, a channel will be formed connecting the source and the drain regions allowing a current to flow. Once the MOSFET device is turned on, the relation between the current and the voltage is nearly linear which means that the device behaves like a resistance. The resistance is referred to as the on-state resistance R_{dson} .

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Typically, power MOSFET devices with low on-state resistance R_{dson} are preferred as they have higher current capability. In the power MOSFET devices typically a plurality of transistor base cells are arranged in parallel for reducing the R_{dson} and the on-state resistance R_{dson} may be decreased by increasing the packing density of a power MOSFET device i.e. the number of base cells per cm^2 . The plurality of parallel arranged transistor base cells may be different shapes, such as hexagonal cells, fingers, strips or waves. US2006/0145252A1 discloses a power semiconductor device comprising a plurality of transistor base cells having a four branch shape.

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Document US6365931B1 presents a gate isolation structure which is suitable for isolating the gates of the above discussed power devices. Fig. 1 presents a cross-section view of the structure of the gate insulating structure. The N substrate 1 comprises an P-region 2 in which N material source regions 3 are provided. Partly above the source regions 3, the P-region 2 and the N substrate 1 a gate oxide layer 4 is provided and on a sub area of the gate oxide layer is provided an insulated gate 5 of polysilicon. On top of the gate 5 is an oxide layer deposited and at the lateral wall of the gate 5 is provided an oxide layer 9 separating the gate 5 from other layers. Around the gate 5, oxide layer 9 is provided a nitride layer 10. Adjacent to the lateral walls of the nitride layer 10 and on top of a portion of the nitride layer which is on top of the gate oxide layer 4, a oxide

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spacer 8 is provided and a metal layer 7 is deposited on top of the above discussed structure for forming the source contact. A backside surface (not shown) of the N substrate 1, which is a surface that is opposite the surface on which the gate oxide layer 4 is provided, is provided with a drain contact. According to the cited patent in a specific processing step, the oxide layer 9 is placed, thus, an additional process handling is used to manufacture the oxide layer 9. Additionally, the cited document proposes a thickness for the oxide layer 9 that is about equal to the thickness of the gate oxide layer 4. Depositing the oxide layer 9 is a relatively complex process step. According to the cited document, the oxide layer 9 is made during second dopant ion implantation and consequent diffusion for obtaining the source regions 3 by comprising oxidation for the oxide layers 9 formation on the sidewalls of the polysilicon layer 5.

Summary of the invention

The present invention provides a power field effect transistor, a power field effect transistor device and a method of manufacturing a power field effect transistor as described in the accompanying claims.

Specific embodiments of the invention are set forth in the dependent claims.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

Brief description of the drawings

Further details, aspects and embodiments of the invention will be described, by way of example only, with reference to the drawings. Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale.

Figure 1 schematically shows a prior art example of a gate isolation structure,

Figure 2 schematically shows an embodiment of a power field effect transistor according to this document,

Figure 3 schematically shows a detail of an embodiment of a power field effect transistor,

Figures 4 to 19 schematically show cross-sectional views of a wafer on which a power field effect transistor is manufactured, the cross-sectional views represent different stages of the manufacturing process - it is to be noted that after Figure 7 the scale changes towards a more zoomed-in view of the wafer.

Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. In the Figures, elements which correspond to elements already described may have the same reference numerals.

Detailed description of the preferred embodiments

Figure 2 schematically shows an embodiment of a portion of a power field effect transistor 200 according to the claims of this document. As indicated at the left side, the right side and the bottom end of the Figure, the power field effect transistor 200 extends further into these directions.

It is to be noted that the portion that is shown in Fig. 2 relates to the encircled portion 99 of the prior art device of Fig. 1. Thus, the structure shown in Fig. 2 continues at the right end with a mirrored configuration that is similar to the presented structure of Fig. 2. The presented embodiment of Fig. 2 is a cross-sectional view of the power field effect transistor 200 - the cross-sectional view is made in a direction that is perpendicular to an epitaxial layer 118. As discussed previously, power field effect transistors may have different shapes, and in an embodiment, the basis shape of the power field effect transistor 200 seen in a top view (which is when one looks towards the power field effect transistor 200 from the top side of the power field effect transistor 200 being the side where the conducting material 104 is provided) is the shape that is disclosed in the patent application US2006/0145252. The cross sectional view of Fig. 2 corresponds to a cross sectional view along a portion of line C-C of Figs. 4 and 5 of US2006/0145252A1.

The basis of the power field effect transistor 200 is a substrate (not shown) of a first conductivity type on which an epitaxy layer 118 of a first conductivity type is provided. Within this layer, a body region 128 of a second conductivity type is present. The body region 128 extends from a first side 116 of the epitaxy layer 118 into the epitaxy layer 118. Optionally, within the body region 128 is provided a region 124 which has a higher doping concentration of the second conductivity doping than the doping concentration of the second conductivity doping of the body region 128. The region 124 extends from the first side 116 into the body region 128. Optionally, within the body region 128 is also provided a protection region 126 which is defined in, and has characteristics according to document US8188539. A source region 122 with a majority of dopants of the first conductivity type, which may have an annular shape, is provided within the body region 128, and more in particular, in the optional protection region 126 and the optional region 124. In an embodiment, the first conductivity type is based on N dopants and the second conductivity type is based on P dopants. In another embodiment, the first conductivity type is based on P dopants and the second conductivity type is based on N dopants.

On top of the epitaxy layer 118 and at least partially on top of the respective body region 128, region 124, protection region 126 and the source region 122 a (patterned) gate oxide layer 114 is provided which has a first opening 130 adjacent to the body region 128 with the region 124, with the protection region 126 and with the source region 122. A portion of the source region 122 extends below the (patterned) gate oxide layer 114 and another portion of the source region 122 is adjacent to the first opening 130 of the gate oxide layer 114. On top of the gate oxide layer 114 is provided a (patterned) stack of a (patterned) polysilicon layer 112, a (patterned) first oxidized polysilicon layer 110 and a (patterned) first silicon nitride layer 108. The stack has a second opening 132 which is larger than the first opening 130 and which fully overlaps with the first opening 130. On top of the stack may be provided an inter layer dielectric layer 106. A sidewall of the polysilicon layer 112, which is the sidewall that faces towards the second opening 132 (and, thus, also to the first opening 130) is provided with a second oxidized polysilicon layer 150. A second silicon nitride layer 102 is provided to the complete sidewall of the stack, and, thus to the second oxidized polysilicon layer 150. The second silicon nitride layer 102 also extends over a surface of the gate oxide layer 114 that is not covered by the stack. In a corner defined by the

second silicon nitride layer 102 is provide a spacer 120 of a dielectric material, for example, a TEOS oxide layer. TEOS is an abbreviation for Tetraethyl orthosilicate. Within the space defined by the spacer(s) 120 an electrically conductive material 104, for example, aluminium silicon, is provided for providing a source contact. A first side of the substrate (not shown) which is opposite a second side of the substrate on which the epitaxy layer 118 is provided, an electrically conductive layer (not shown) may be provided for forming a drain contact.

The electrical operation of the power field effect transistor 200 is earlier described in several patent applications which disclose similar power field effect transistors. When an adequate voltage is applied to the gate, which is formed by polysilicon layer 112, a channel is formed between the source region 122 and the drain (not shown) through which a current may flow.

In an embodiment, a power field effect transistor device (not shown) is provided which comprises a plurality of power field effect transistors 200. In line with for example, the disclosure of US2006/0145252, the plurality of power field effect transistors 200 may be combined in a specific pattern to obtain a relatively low on-state resistance R_{dson} for the power field effect transistor device. It is to be noted that the plurality of power field effect transistors 200 are combined on a single substrate.

It is to be noted that, in a further embodiment, the power field effect transistor 200 may be manufactured with a manufacturing technology in which a body drive time is relatively short to obtain a relatively low on-state resistance for the power field effect transistor 200. In the body drive stage, which shortly follows after a stage of implanting dopants of the second conductivity type, the actual body region 128 is formed. The body drive stage comprises a thermal step in which the power field effect transistor under production (and ready in so far as possible at this stage) is given a thermal treatment of at least 850 degrees Celsius. In an embodiment, the body drive stage (after implanting the dopants of the second conductivity type) comprises a thermal treatment that is shorter than 45 minutes to obtain a relatively low on-state resistance for the power field effect transistor 200. By reducing the body drive time from 80 minutes to 40 minutes, the on-state resistance R_{dson} is reduced by 15%. If, for example, half a million power field effect transistor base cells (as power field effect transistor 200) are combined on a power field effect transistor device, and when power field effect transistors are used with a breakdown voltage of 25 volts and the on-state resistance R_{dson} of the power field effect transistor device was measured at a moment in time that the gate source voltage V_{gs} was 10 volts, the on-state resistance R_{dson} was reduced from 0.7mOhms down to 0.55mOhms as the result of significantly reducing the body drive time. In another example, if 1 million power field effect transistor base cells as discussed above (breakdown voltage 25 volts) are combined on a power field effect transistor device, and the R_{dson} of the power field effect transistor device was measured at a moment in time that the gate source voltage V_{gs} was 10 volts, the on-state resistance R_{dson} was reduced from 0.35mOhms down to 0.275mOhms as the result of significantly reducing the body drive time. In another example, with power field effect transistors with a breakdown voltage of 45 Volts, a reduction of 10% was obtained.

Fig. 3 presents a section 199 of Fig. 2. A first portion of the gate oxide layer 114, which is a portion that is sandwiched between the poly silicon layer 112 and the epitaxy layer 118 (with body region 128), has a first layer thickness that is indicated with t_{gox1} . A second portion of the gate oxide layer 114, which is a portion that is sandwiched between the source region 122 and the second silicon nitride layer 102, has a second layer thickness that is indicated with t_{gox2} . In practical situations, the second portion of the gate oxide layer 114 has a smaller second layer thickness t_{gox2} than the first layer thickness t_{gox1} of the first portion of the gate oxide layer 114. This is the result of an etching step that has been performed to create the second opening 132 (of Fig. 2). Typically, the etching step removes 70 Ångström at the second portion of the gate oxide layer 114, however, after a later performed oxidation steps the typical difference between the first layer thickness t_{gox1} and the second layer thickness t_{gox2} is reduced because the second portion partially re-oxidizes in the subsequently performed oxidation steps. The inventors have found that, in such a situation, a premature current injection may occur from the polysilicon layer 112 to the body region 128 / source region 122 via the surface of the silicon nitride layer 102. The current injection is a tunnelling through the gate oxide layer 114 and the oxidized polysilicon layer 150. The arrows 180, 182 indicate a trajectory of the current (which means that electrons travel in a direction reverse to the direction of the arrows 180, 182). It is a complex mechanism in which the second silicon nitride layer 102 is also involved, however, it is believed that the electrons do not travel through the second silicon nitride layer 102, but follow an interface between the second silicon nitride layer 102 and the gate oxide layer 114 and/or an interface between the second silicon nitride layer 102 and the second oxidized polysilicon layer 150.

The second oxidized polysilicon layer 150 has a lateral thickness indicated in Fig. 3 by $t_{\text{p_ox}}$. The lateral thickness $t_{\text{p_ox}}$ is measured in a direction from the polysilicon layer 112 towards the second opening 132 (see Figure 2). The premature current injection does not occur when the first layer thickness t_{gox1} is smaller than the sum of the second layer thickness t_{gox2} and the lateral thickness $t_{\text{p_ox}}$. If this condition is true, the "normal current injection" from the polysilicon layer 112 to the epitaxy layer 118 occurs instead of the premature current injection when a voltage difference between the gate (polysilicon layer 112) and the epitaxy layer 118 becomes too large. As such, according to this embodiment, the oxidized polysilicon layer 150 has a thickness which prevents the premature current injection from the second gate (polysilicon 112) to the epitaxial layer 118 (including the body region 128, etc.). In other words, the second oxidized polysilicon layer 150 is present in the power field effect transistor 200 of Fig. 2 to prevent that a premature current injection takes place. It is to be noted that the second oxidized polysilicon 150 of the power field effect transistor 200 of Fig. 2 is not manufactured by means of depositing additional material, but is an oxidized sidewall of the polysilicon layer 112. A processing step to oxidize the sidewall is less complex than a processing step in which material must be deposited to such a side-wall. Thereby costs are saved. Oxidizing the sidewalls may, for example, be done with a thermal treatment of the power field effect transistor at a specific moment of time in the production process of the power field effect transistor when the sidewall is not yet covered with the silicon nitride layer 102. As discussed above and will be discussed later in this description, the oxidation may be achieved by

applying a pre body drive stage and a body drive stage. Compared to known manufacturing technologies, the sum of the time of the pre body drive stage and the body drive stage does not increase when being compared to the time of a single body drive stage as is known in the prior art. Thus, the oxidizing the sidewalls does not directly increase the manufacturing costs.

5 In an embodiment, the lateral thickness of the oxidized polysilicon layer 150 is in a range from 50 Ångström to 200 Ångström. In another embodiment, the thickness of the oxidized polysilicon layer 150 is in the range from 70 Ångström to 160 Ångström. In a typical embodiment, the first layer thickness t_{gox1} is in between 300 Ångström and 900 Ångström. In a further typical embodiment, the first layer thickness t_{gox1} is in between 350 Ångström and 700 Ångström.

10 As discussed above, the actual formation of the body region 128 during the manufacturing of the power field effect transistor comprises a body drive stage. In an embodiment, the power field effect transistor 200 of Fig. 2 was also subject to a pre body drive stage which is applied shortly before the implantation of the dopants of the second conductivity type. The pre body drive stage comprises a thermal treatment of the power field effect transistor under production (in so far as
15 ready at this state of the manufacturing process) with a relatively high temperature (for example, larger than 850 degrees Celsius) during a period of time that is shorter than 45 minutes. It is to be noted that the oxidized polysilicon layer 150 is formed during the pre body drive stage and the body drive stage of the manufacturing process. The total length of these stages must be long enough to obtain a sufficient large lateral thickness $t_{\text{p,ox}}$ which fulfils the above discussed condition.

20 More will be elucidated about the manufacturing process hereinafter.

Referring to Figure 4, a wafer 200 of starting material is either grown or procured for fabricating a plurality of N-type power MOSFET devices. The wafer comprises a highly N-doped substrate 202, upon which an N-type epitaxial layer 204 is grown. The substrate 202 is a <100> substrate doped with Arsenic to yield a resistivity of about a few mΩ.cm. A backseal 206 is formed
25 on a backside of the substrate 202, the backseal 206 comprising an about 1μm polysilicon (PolySi) backseal layer 208 disposed adjacent an about 1μm Low Temperature Oxide (LTO) layer 210. An initial oxide layer 212 of silicon dioxide (SiO₂) is then grown on top of the epitaxial layer 104 to a depth, in this example, of more than 6000Å, for example 6750 Å.

Thereafter (Figure 5), using a known masking technique, an active area 214 is defined using
30 photoresist (not shown) and a part of the initial oxide layer 212 is removed in the active area 214 using a two-step etching technique comprising a dry, plasma, etch step and a wet etch step. Both these etching techniques are known to those skilled in the art and so will not be described further. Once the active area 214 has been etched, the photoresist is subsequently removed.

Referring to Figure 6, in this example 400Å, a gate oxide layer 216 formed from Silicon
35 Dioxide is then grown in the active area 214, followed by a deposition of another PolySi layer 218 over the wafer 200. In this example, the another PolySi layer 218 is more than 6000Å thick, for example, 6500 Å. The PolySi layer 218 is then subjected to an N-blanket implantation 220 of Phosphorous ions.

Turning to Figure 7, an Oxide-Nitride-Oxide (ONO) stack is then formed adjacent the another
40 PolySi layer 218 by growing a polyoxide layer 222 adjacent the PolySi layer 218, followed by

deposition of a 450Å thick Silicon Nitride (Si₃N₄) layer 224 using a Low Pressure Chemical Vapour Deposition (LPCVD) technique. In this example, the polyoxide layer is about 300Å thick. An Inter-Layer Dielectric (ILD) layer 226, in this example a 6000Å Tetra Ethyl OrthoSilicate (TEOS) layer, is then deposited on the Silicon Nitride layer 224.

5 It is to be noted that in the subsequent figures only a portion of the active area 214 is shown. In other words, the scaling in the y-dimension changes.

Although not shown in Figure 8, a photoresist gate mask is deposited to define a gate stack 228. Thereafter, a two-stage anisotropic etching process is carried out. Firstly, an exposed part of the ONO stack is removed in an oxide reactive ion plasma etcher. The photoresist layer is then
10 stripped away and the wafer 200 subjected to a cleaning stage. A now-exposed part of PolySi layer 218 is then etched away in a PolySi reactive ion plasma etcher in order to obtain a vertical stack profile comprising a part of the ONO stack in addition to the PolySi layer 218, and constituting the gate stack 228. Etching of the exposed part of the PolySi layer 218 is stopping at the gate oxide layer 216, and once again, the wafer 200 is then subjected to another cleaning stage.

15 The etched areas in combination with the gate stack 228 constitute an active region 230. The etching carried out in relation to Figure 8 yields an edge cell 232 and a central cell 234. As is known in the art, a MOSFET device comprises many edge and central cells (not shown), but for the purpose of simplicity of description and hence clarity, only one of each is shown.

According to this embodiment, after the above discussed etching stage, a pre PHV drive
20 stage is provided to the wafer 200. The pre PHV drive stage comprises the stage of exposing the wafer 200 to a thermal cycle, in this example, of more than 20 minutes at a temperature of 1080°C. The pre PHV drive stage may, for example, has a duration of 30 minute, or an even longer duration of, for example, 40 minutes. It is to be noted that in the discussion of Fig. 2 the pre PHV drive stage was termed "pre body drive stage". The pre PHV drive stage has a duration of a maximum time
25 period of 60 minutes, or, in another embodiment, a duration that is shorter than 45 minutes.

Referring to Figure 9, the active region 230 is subjected to an ion implantation processing stage 236, so that the epitaxial layer 204 beneath the edge cell 232 and the central cell 234 are implanted with positive boron ions 238 as a first stage to a formation of a first P-type High Voltage (PHV) region and a second PHV region (not shown in Figure 9). During the implantation of the
30 boron ions 238, the gate oxide layer 216 serves as a screen oxide for the PHV ionic implantation .

Turning to Figure 10a, as a second stage to the formation of the first and second PHV "body" regions 240, 242, a PHV drive stage follows the implantation stage 236, consisting of exposing the wafer 200 to a thermal cycle, in this example, of less than 45 minutes at a temperature of 1080°C. Such a relatively short PHV drive stage results in a relatively low on-state resistance R_{dson} of the
35 manufactured MOSFETs. The duration of the thermal cycle of the PHV drive stage is, for example, 30 minutes, or even shorter, for example, 20 minutes. It is to be noted that in the discussion of Fig. 2 the PHV drive stage was termed "body drive stage". The PHV drive stage has a duration of a minimum time period of 10 minutes, or, in another embodiment, a duration that is longer than 15 minutes.

Although now shown in Figure 10a, and not shown in the subsequent figures, during the above discussed pre PHV drive stage and the above discussed PHV drive stage sidewalls of the PolySi layer 218 (that face toward the previously mentioned central cell 234 and edge cell 232) are oxidized and an oxidized PolySi layer 243 is formed. This is shown in Figure 10b. Thus, at all figures 10a and 11 to 19, the oxidized PolySi layer 243 is also present at the locations that are indicated in Figures 10a and 10b. Specific advantages of the oxidized PolySi layer 243 are discussed in the context of Figures 2 and 3. In particular, it is to be noted that the PHV drive stage is shortened to obtain a relatively low on-state resistance R_{dson} and such a relatively short PHV drive stage results in a too thin oxidized PolySi layer 243 such that, as discussed in the context of Figure 3, a premature current may be injected from the gate to the source regions of the MOSFET. The pre PHV drive stage is introduced to create a thick enough oxidized PolySi layer 243 such that this premature current injection does not occur. At that stage, within the body region is also provided a protection region 126 (as discussed in the context of Fig. 2) which is defined in, and has characteristics according to document US8188539.

Another masking technique is then employed (see Figure 11), whereby a layer of photoresist 244 is patterned to expose a peripheral region 246 of the central cell 234. The layer of photoresist 244 is then subjected to an N⁺ implantation stage 245, the exposed peripheral region 246 of the central cell 234 permitting the implantation of Arsenic (As) ions 248 into the second PHV region 242. Thereafter, the layer of photoresist 244 is stripped away.

Referring to Figure 12, a thin nitride layer 250 is then deposited on the wafer 200 using a LPCVD technique. In this example, the nitride layer 250 is formed from Silicon Nitride and is 300Å thick. Although, in this example, the nitride layer 250 is 300Å thick, the nitride layer 250 can be between 150Å thick and 1000Å thick. In other embodiments, the nitride layer 250 can be between 300Å and 600Å thick. Further, the use of silicon nitride to form the nitride layer is only one type of protective layer and it should be appreciated that the function of the nitride layer 250 is to block at least one contaminant, for example hydrogen, and so any suitable material can be used that can block the passage of the at least one contaminant, for example hydrogen, therethrough. In this example in relation to silicon nitride, silane (SiH₄) is used by the LPCVD technique at a temperature of between about 700°C and 750°C. However, whilst the silane, of course, contains hydrogen, the silicon-hydrogen bonds created by use of the LPCVD technique are strong and do not result in the presence of free hydrogen. A TEOS oxide layer 252 is then deposited adjacent the nitride layer 250 using a Low Temperature Oxide (LTO) deposition technique. In this example, the TEOS oxide layer 252 is 6000Å thick.

Once formed, the nitride layer 250 and the TEOS oxide layer 252 are anisotropically etched (see Figure 13) in an oxide reactive ion etcher to yield composite spacers 254. Consequently, in the present example, the thickness of the nitride layer 150 is sufficiently thin to avoid any protuberances or cavities being formed that can affect the curved profile of the spacer 254.

A horizontal portion 256 of the nitride layer 250 serves as a protective layer against at least one type of contaminant as will be described in more detail later herein. In this example, the nitride layer 250 has a vertical portion 258 that also protects the gate stack 228.

Referring to Figure 14, a blanket implantation stage 260 is then carried out to implant boron ions 262 into the first and second PHV regions 240, 242 via the edge cell 232 and the central cell 234, respectively. This implantation stage 260 is carried out in order to fix the potential of the PHV body regions 240, 242 and improve the so-called unclamped inductive switching behaviour of the device. Turning to Figure 15, the implanted arsenic ions 248 and the implanted boron ions 262 are subjected to a thermal cycle of 30 minutes at more than 850°C, for example, 900 °C, and constituting an anneal stage. This stage is known in the art and so, for conciseness, will not be described further. As a result of the above anneal stage, the first PHV region 240 of the edge cell 232 only comprises a p+ region 264. With respect to the central cell 234, the second PHV region 242 comprises a p+ region 264 therein and an annular n-type Source/Drain (n s/d) region 266 bridging the p+ region beneath the central cell 234. It should be understood that the n s/d region 266 constitutes a source of one central cell of the device.

A region adjacent the surface of and in the second PHV region 242 between the peripheries of the second PHV region 242 and the n s/d region 266 constitutes a channel region 267. Due to the nature of the formation of the second PHV region 242, the level of doping of the channel region 267 at a first end thereof adjacent the source 266 is higher than at a second end thereof adjacent the periphery of the second PHV region 242. In this respect, the level of doping from the first end of the channel region 267 to the second end of the channel region 267 decreases gradually, i.e. is graduated. In the present example, the first end of the channel region 267 is very close to the edge of the gate stack 228, such as 0.13µm therefrom. However, the horizontal part 256 of the nitride layer 250 overlaps a substantial part of the source 266, thereby providing protection to the channel region, especially the first end of the channel region 267 from the at least one contaminant mentioned above, for example, hydrogen.

A further photoresist layer 270 (Figure 16) is then deposited over an uppermost surface of the wafer 200 using a known masking technique. Although not shown in Figure 16 due to the gate contact (also not shown) being at the periphery of the active region 230, the photoresist layer 270 comprises apertures that, when the device thus far is subjected to a reactive ion etching stage, result in openings (not shown) being formed for the deposition of metal therein so as permit the connection of a source pad (not shown) and a gate stack pad (not shown) to pads of a device package frame (not shown) by aluminium wires. Once etched, the photoresist layer 270 is stripped away and an aluminium-silicon layer 272 is deposited (Figure 17) using a sputtering technique known in the art. The aluminium-silicon layer 272 is deposited to a thickness of about 10 µm. Thereafter, the aluminium-silicon layer 272 is covered with another photoresist layer (not shown) using a known masking technique, and then etched in a spray etcher. In order to obtain a good metal-silicon alloy, the wafer undergoes a sinter step in a low temperature furnace, in this example, at a temperature of 390°C for 30 minutes.

Referring to Figure 18, a passivation nitride-above-oxide stack 274 comprising a layer of Silicon Nitride on Undoped Silicon Glass (USG) is deposited using a Plasma Enhanced Chemical Vapour Deposition (PECVD) system and, after a photomasking technique, etched in a oxide reactive ion etcher. However, in another embodiment, the passivation stack 274 can be replaced

with one or more layers of material suitable for performing the role of passivation that do not introduce, or alternatively, minimise the introduction of free hydrogen into the device. In this respect, the passivation stack comprises a predetermined amount of free hydrogen, free hydrogen being hydrogen atoms or ions that are weakly bonded within the passivation stack 274 and are freed or released from their respective bonds by energy imparted to break the bonds through mechanical stresses. In this example, the hydrogen is weakly bonded to silicon to form silicon-hydrogen bonds. The predetermined amount of free hydrogen should not be sufficient to cause drift of a threshold voltage of the power MOSFET device when the device is in use.

After provision of the passivation stack 274 (Figure 19), the PolySi backseal layer 208 and LTO backseal layer 210 are removed using a backgrinding technique known in the art until the wafer 200 is about 250µm thick, and a Titanium-Nickel-Vanadium-Silver alloy layer 276 is deposited on the back-side of the substrate 202 using a known metallisation technique to form a drain.

The above example is of an N-type epitaxial power MOSFET. It should therefore be appreciated that the above example can be modified to create a P-type epitaxial MOSFET device. Moreover, whilst the above example has been described in the context of a power MOSFET device, the provision of the protective layer described above can be applied to other Field Effect Transistor (FET) devices requiring protection of the channel region from contaminants, for example MOSFETs, i.e. non-power MOSFETs.

In summary, in this application a power field effect transistor, a power field effect transistor device and a method of manufacturing a power field effect transistor are provided. During the manufacturing of the power field effect transistor, a body drive stage to manufacture the body region of the power field effect transistor is shortened to obtain a relatively low on resistance for the power field effect transistor. Before the implanting stage of the dopants of the body region, a pre body drive stage is introduced. During the pre body drive stage and the body drive stage sidewalls of a polysilicon layer of the power field effect transistor are oxidized to obtain a power field effect transistor which has at the sidewalls an oxidized polysilicon layer that is thick enough to prevent a premature current injection from the gate to the source regions of the power field effect transistor.

In the foregoing specification, the invention has been described with reference to specific examples of embodiments of the invention. It will, however, be evident that various modifications and changes may be made therein without departing from the broader spirit and scope of the invention as set forth in the appended claims. For example, the connections may be any type of connection suitable to transfer signals from or to the respective nodes, units or devices, for example via intermediate devices. Accordingly, unless implied or stated otherwise the connections may for example be direct connections or indirect connections.

The semiconductor substrate described herein can be any semiconductor material or combinations of materials, such as gallium arsenide, silicon germanium, silicon-on-insulator (SOI), silicon, monocrystalline silicon, the like, and combinations of the above.

Although the invention has been described with respect to specific conductivity types or polarity of potentials, skilled artisans appreciated that conductivity types and polarities of potentials may be reversed.

Moreover, the terms "front," "back," "top," "bottom," "over," "under" and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions. It is understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation in other orientations than those illustrated or otherwise described herein.

Thus, it is to be understood that the architectures depicted herein are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. In an abstract, but still definite sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. \

Furthermore, those skilled in the art will recognize that boundaries between the functionality of the above described operations merely illustrative. The functionality of multiple operations may be combined into a single operation, and/or the functionality of a single operation may be distributed in additional operations. Moreover, alternative embodiments may include multiple instances of a particular operation, and the order of operations may be altered in various other embodiments.

However, other modifications, variations and alternatives are also possible. The specifications and drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive sense.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word 'comprising' does not exclude the presence of other elements or stages than those listed in a claim. Furthermore, the terms "a" or "an," as used herein, are defined as one or more than one. Also, the use of introductory phrases such as "at least one" and "one or more" in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles. Unless stated otherwise, terms such as "first" and "second" are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements. The mere fact that certain measures are recited in mutually different claims does not indicate that a combination of these measures cannot be used to advantage.

Claims

1. A method of manufacturing a power field effect transistor (200), the manufacturing method comprises the stages of:

- 5 - obtaining a substrate (118) of a first conductive type, the substrate having a first side (116),
 - forming a patterned gate oxide layer (114) on the first side (116) of the substrate (118), the
 patterned gate oxide layer (114) comprises a first opening (130),
 - forming a patterned polysilicon layer (112), the patterned polysilicon layer (112) is at least
 formed on a portion of the patterned gate oxide layer (114), the patterned polysilicon layer (112)
10 having a side wall facing towards the first opening (130) of the patterned gate oxide layer (114),
 - providing a pre body drive stage during a first period of time longer than 20 minutes,
 - forming a body region (128) of a second conductivity type in the substrate (118), wherein the
 forming of the region of the second conductivity type comprises the stage of blanket implanting
 dopants of a second conductivity type into the substrate (118) via the first opening (130) in the
15 patterned gate oxide layer (114) and the stage of providing a body drive stage during a second
 period of time shorter than 45 minutes to obtain the body region (128) that extends from the first
 side (116) into the substrate (118) below the first opening (130) and partially below the patterned
 gate oxide layer (114),
 wherein in the pre body drive stage and the body drive stage a lateral oxidized polysilicon layer
20 (150) is formed at the side walls of the patterned polysilicon layer (112).

2. A method according to claim 1, wherein a length of a sum of the first period of time and the
second period of time is long enough to obtain the lateral oxidized polysilicon layer (150) with a
sufficient lateral thickness (tp_ox) measured in a lateral direction to prevent a premature current
25 injection in the manufactured power field effect transistor (200) from the patterned polysilicon layer
 (112) to a source region (122) of the manufactured power field effect transistor (200), the source
 region extending from the first side (116) into the body region (128) and being provide partially
 below the patterned gate oxide layer (114).

- 30 3. A method according to any one of the preceding claims, wherein the pre body drive stage and
 the body drive stage comprise a thermal cycle of at least 850 degrees Celsius.

4. A method according to any one of the preceding claims, wherein the first period of time is
longer than 30 minutes, and/or the second period of time is shorter than 30 minutes.

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5. A method according to any one of the preceding claims, wherein the forming of the patterned
polysilicon layer (112) comprises a stage of etching a second opening (132) in the patterned
polysilicon layer (112) by means of an etching stage, wherein the second opening (132) is larger
than the first opening (130) and fully overlaps the first opening (130) thereby creating a first area of

the patterned gate oxide layer (114) adjacent to the first opening (130) that is not covered by the patterned polysilicon layer (112).

6. A method according to claim 5, when directly or indirectly referring to claim 2, wherein the patterned gate oxide layer (114) has a first thickness (t_{gox2}) at the first area measured in a direction perpendicular to the substrate, the patterned gate oxide layer (114) has a second thickness (t_{gox1}) at a second area of the patterned gate oxide layer (114) which is in between the patterned polysilicon layer (112) and the substrate (118), wherein the lengths of the sum of the first period of time and the second period of time is long enough to obtain the lateral thickness (t_{p_ox}) which fulfils the condition that the sum of the first thickness (t_{gox2}) and the lateral thickness (t_{p_ox}) is larger than the second thickness (t_{gox1}).

7. A method according to any one of the preceding claims, when directly or indirectly referring to claim 2, the lateral thickness (t_{p_ox}) is smaller than 200 Ångström and, optionally, the lateral thickness (t_{p_ox}) is larger than 50 Ångström.

8. A method according to any one of the preceding claims, wherein in the stage of forming a patterned polysilicon layer (112) includes forming a patterned stack of the patterned polysilicon layer (112), a patterned oxidized polysilicon layer (110) and a patterned silicon nitride layer (108), wherein the patterned oxidized polysilicon layer (112) is adjacent to the patterned polysilicon layer (114) and the patterned silicon nitride layer (108) is provided on a surface of the patterned oxidized polysilicon layer (110) that faces away from the patterned polysilicon layer (112).

9. A method according to any one of the preceding claims, wherein the stage of obtaining a substrate (118) of a first conductivity type comprises the stage of growing an epitaxial layer doped with dopants of the first conductivity type on a layer of a base material that is doped with dopants of the first conductivity type, the first side of the substrate being a surface of the epitaxial layer that is facing away from the layer of the base material.

10. A power field effect transistor (200) comprising

- a semiconductor layer (118) of a first conductivity type, the first semiconductor layer (118) having a first side (116),
- a body region (118) of a second conductivity type formed at the first side (116) inside the semiconductor layer (118),
- source regions (122) of the first conductivity type formed at the first side (116) within the body region (118),
- a patterned gate oxide layer (114) superimposed at the first side (116) on the semiconductor layer (118) with a first opening (130) over the body region (128),
- a patterned polysilicon layer (112) superimposed to at least a portion of the patterned gate oxide layer (114),

- a lateral oxidized polysilicon layer (150) at a sidewall of the patterned polysilicon layer (112), the sidewall facing towards a the first opening (130) in the patterned gate oxide layer (114), wherein a lateral thickness (tp_ox) of the lateral oxidized polysilicon layer (150) measured in the lateral direction is thick enough for preventing a premature current injection in the manufactured power field effect transistor (200) from the patterned polysilicon layer (112) source regions (122) of the manufactured power field effect transistor (200)..

11. A power field effect transistor (200) according to claim 10, wherein the patterned polysilicon layer (112) comprises a second opening (132), the second opening (132) is larger than the first opening (130) and fully overlaps the first opening (130), the patterned gate oxide layer (114) comprises a first area adjacent to the first opening (130) that is not covered by the patterned polysilicon layer (112).

12. A power field effect transistor (200) according to claim 11, wherein the patterned gate oxide layer (114) has a first thickness (tgox2) at the first area measured in a direction perpendicular to the semiconductor layer (118), the patterned gate oxide layer (114) has a second thickness (tgox2) at a second area of the patterned gate oxide (114) which is in between the patterned polysilicon layer (112) and the semiconductor layer (118), wherein the sum of the first thickness (tgox2) and the lateral thickness (tp_ox) is larger than the second thickness (tgox1).

13. A power field effect transistor (200) according to claim 12, wherein the first thickness (tgox2) is smaller than the second thickness (tgox1).

14. A power field effect transistor (200) according to any one of the claims 10 to 13, the lateral thickness (tp_ox) is smaller than 200 Ångström, and, optionally, the lateral thickness (tp_ox) is larger than 50 Ångström.

15. A power field effect transistor (200) according to any one of the claims 10 to 14, further comprising a patterned stack of an oxidized polysilicon layer (110) and a silicon nitride layer (108) superimposed to the patterned polysilicon layer (112), the oxidized polysilicon layer (110) being adjacent to the patterned polysilicon layer (112).

16. A power field effect transistor (200) according to claim 11 or any one of the claims 12 to 15 in so far claim 11 is included, further comprising

- a further silicon nitride layer (102) provided on i) a first surface of the of the lateral oxidized polysilicon layer (150), the first surface facing away from the patterned polysilicon layer (150) towards the first opening (130), ii) a second surface of the first area of the patterned gate oxide layer (114), the second surface facing away from the semiconductor layer (118).

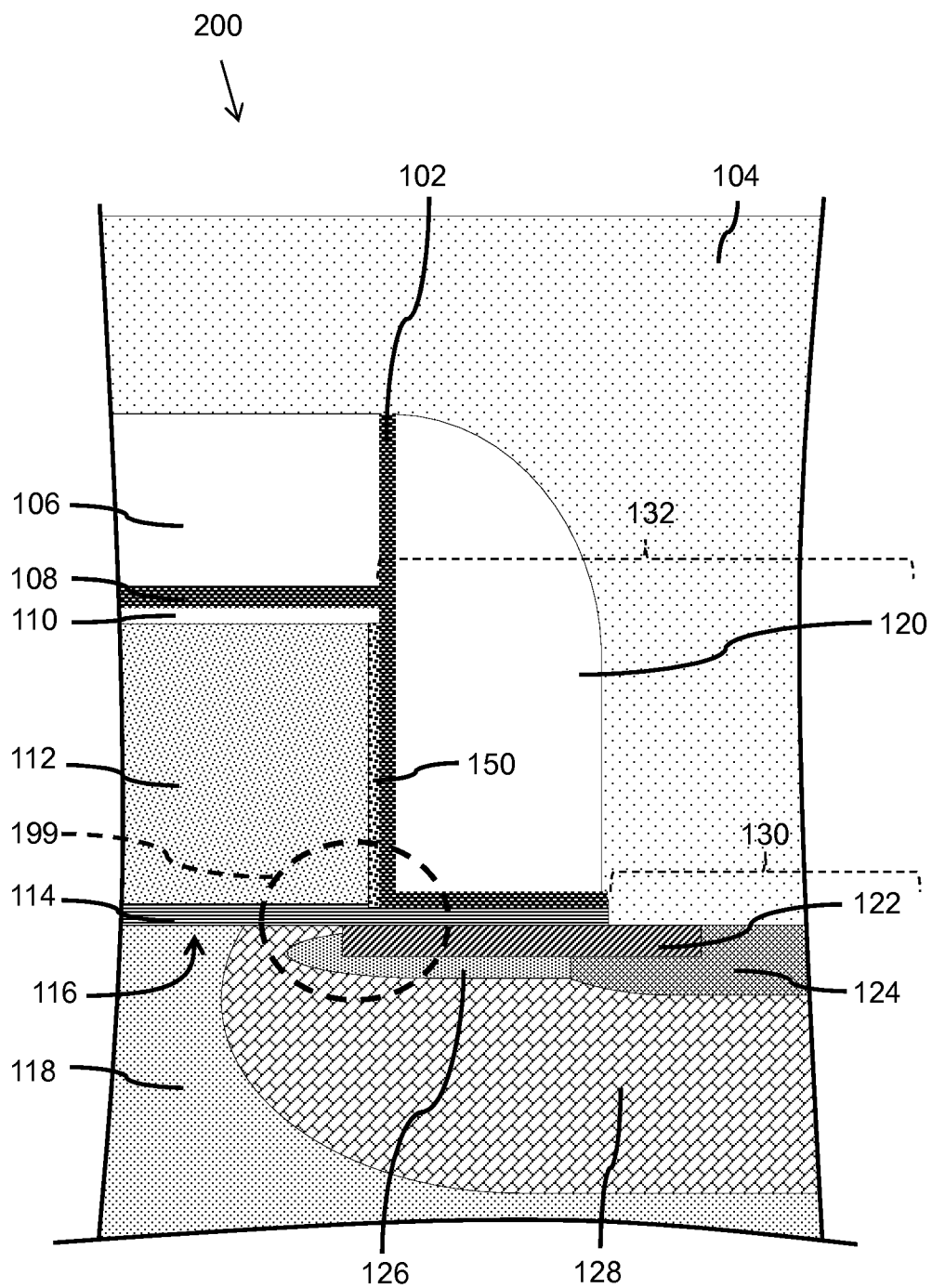


Fig. 2

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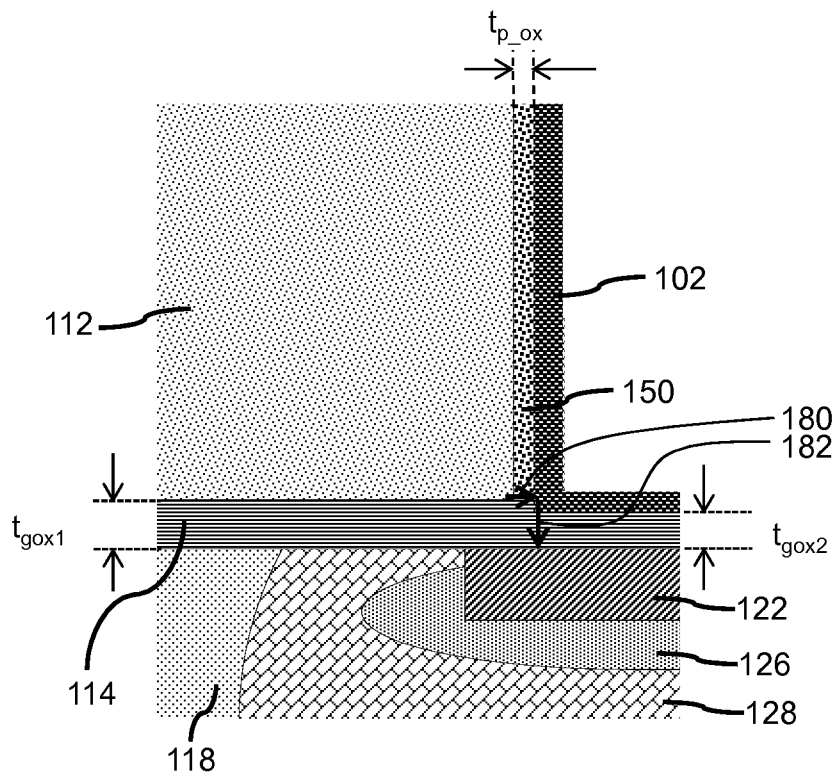


Fig. 3

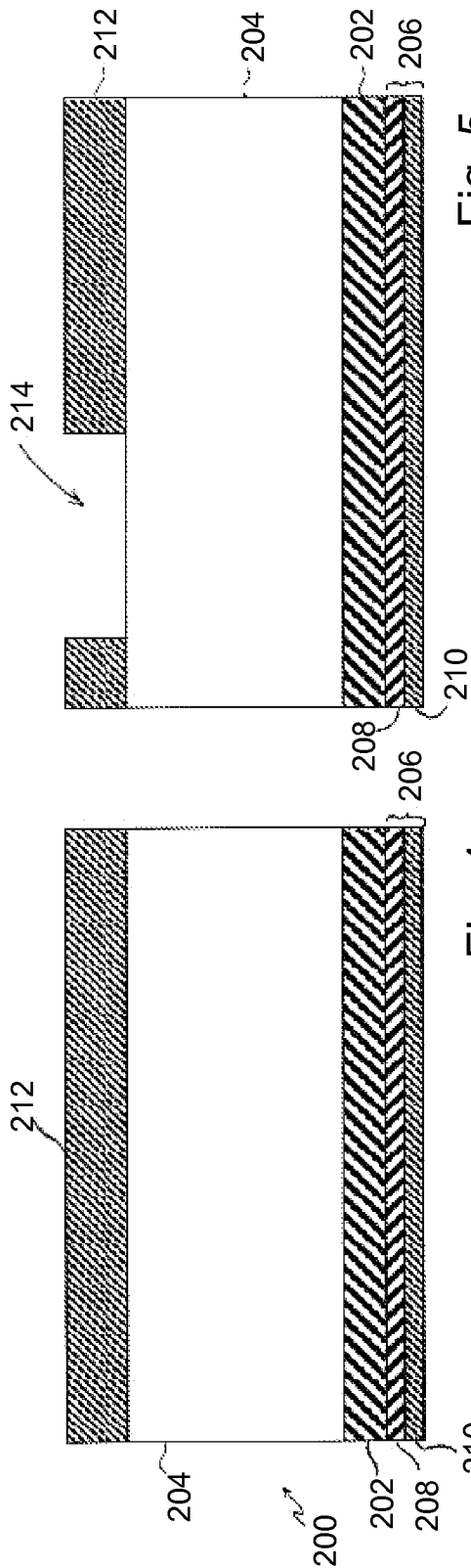


Fig. 5

Fig. 4

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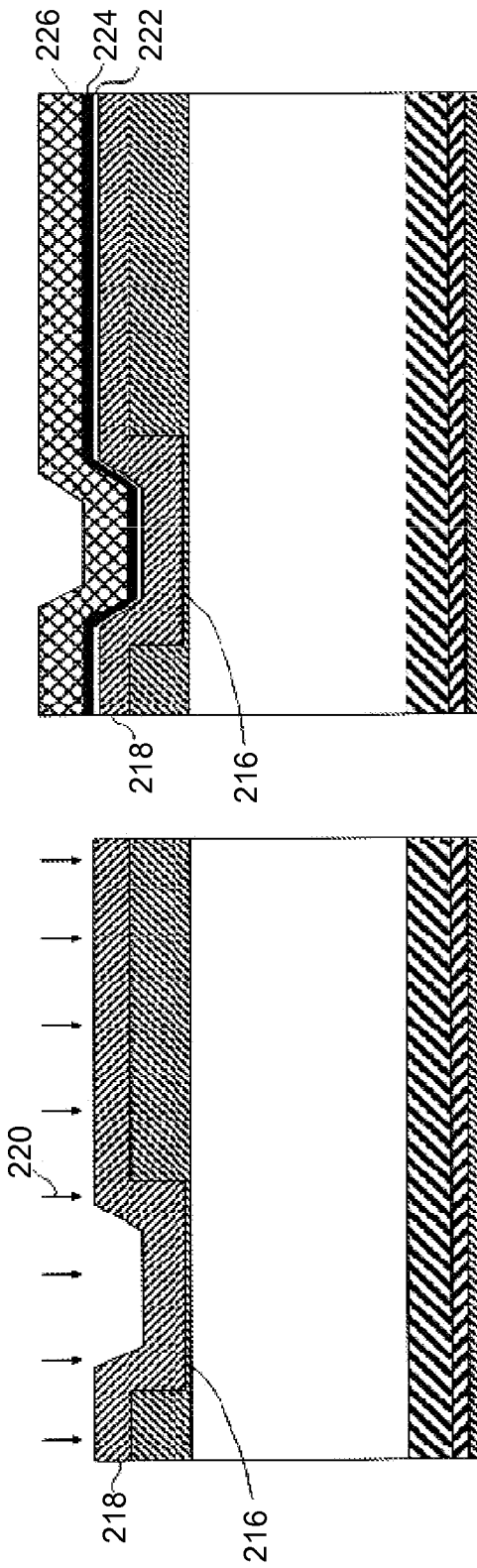


Fig. 7

Fig. 6

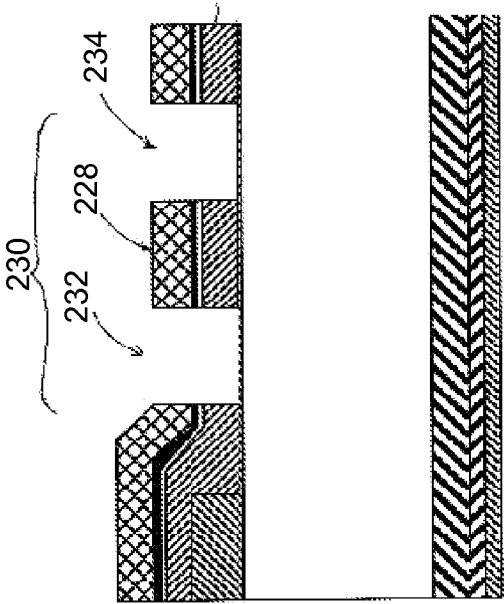


Fig. 8

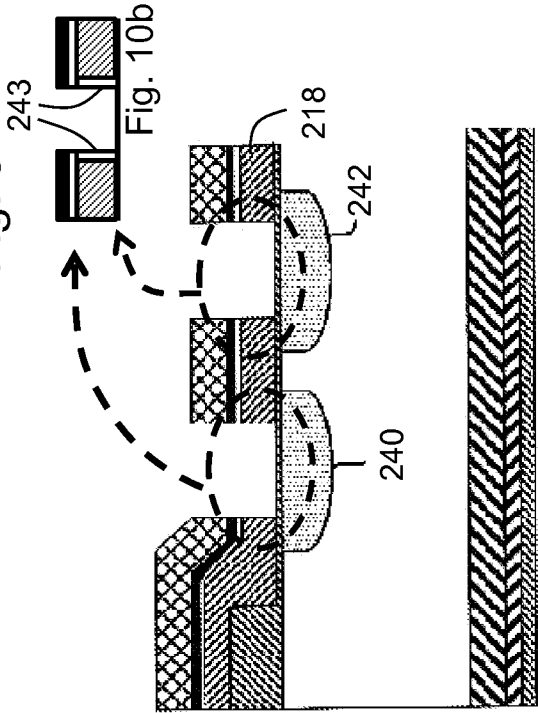


Fig. 10a

Fig. 10b

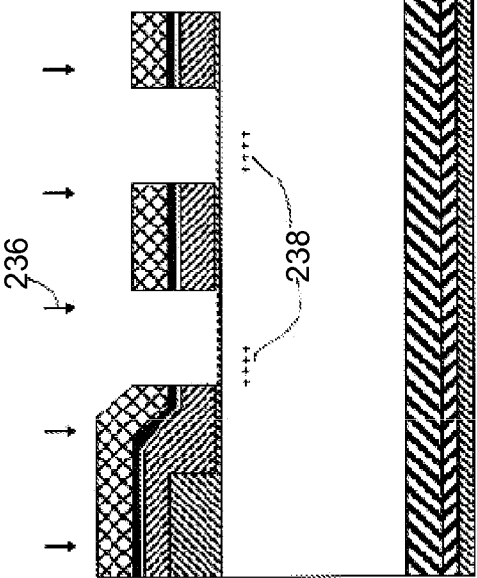


Fig. 9

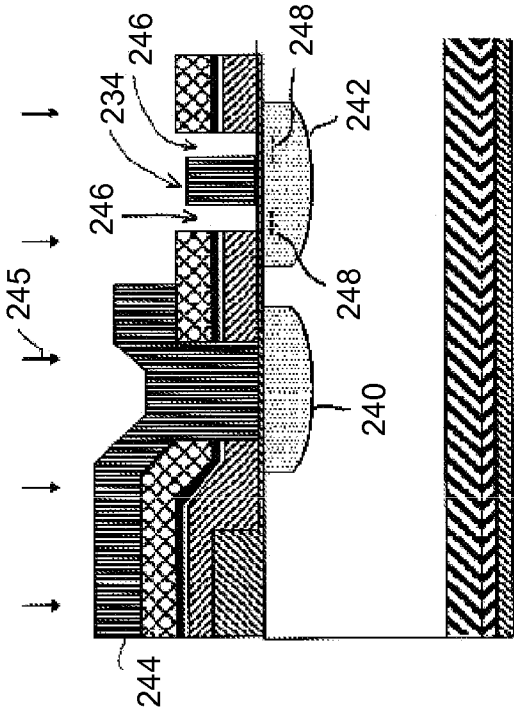


Fig. 11

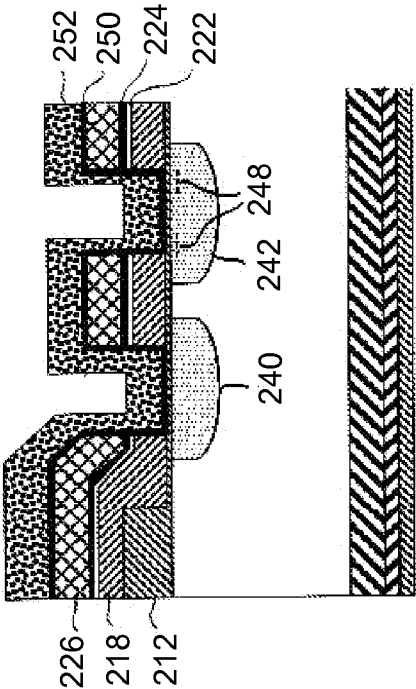


Fig. 12

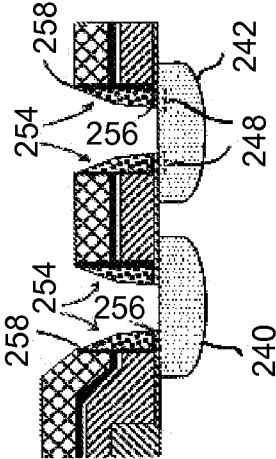


Fig. 13

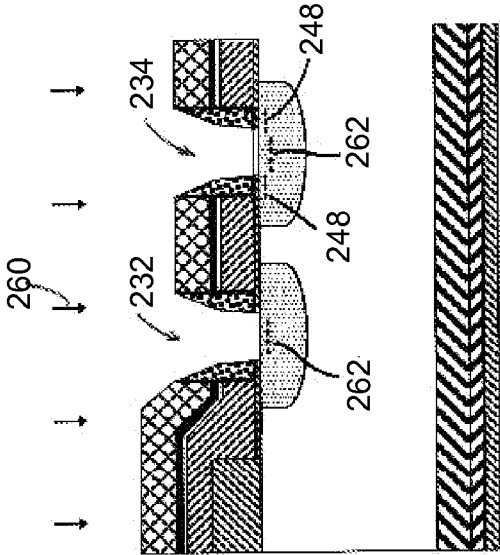


Fig. 14

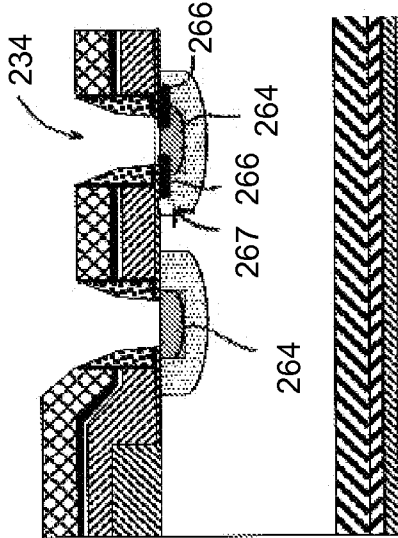


Fig. 15

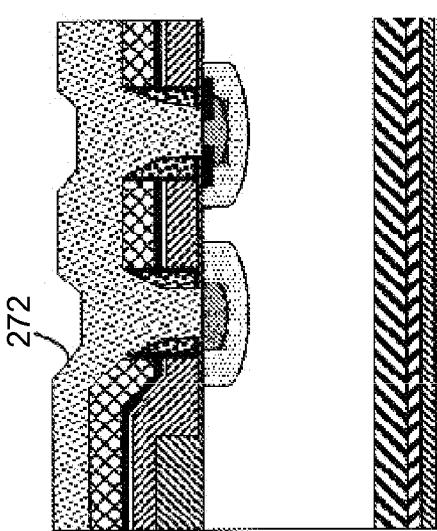


Fig. 17

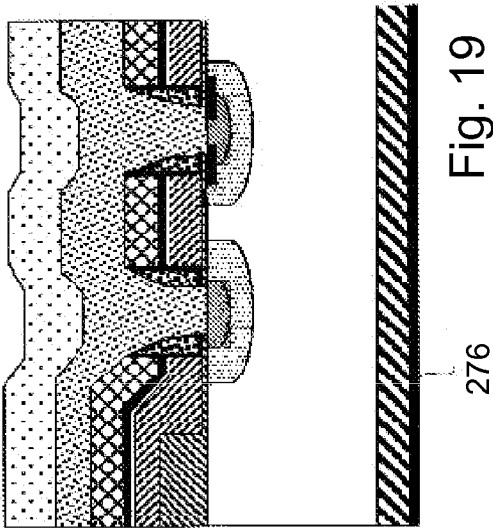


Fig. 19

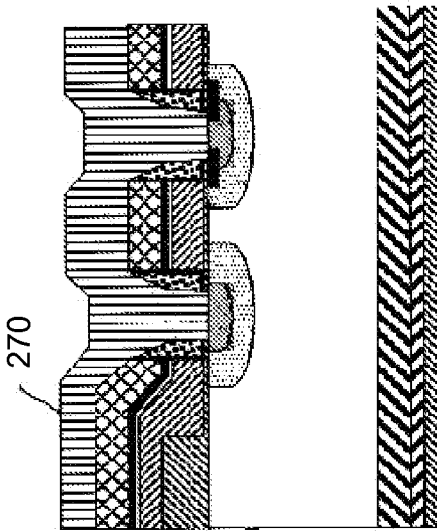


Fig. 16

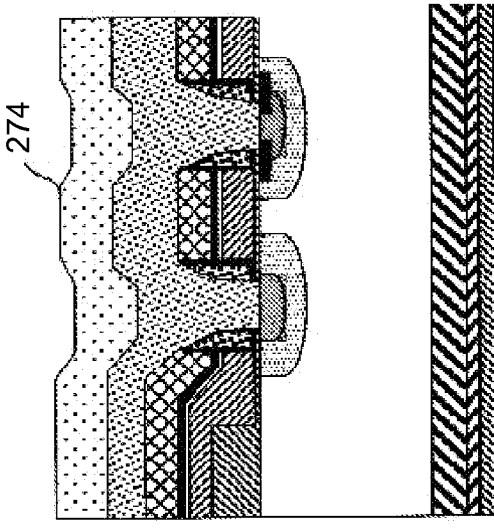


Fig. 18

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2013/002406**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/336(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/336; H01L 21/28; H01L 29/94; H01L 21/332; H01L 31/119; H01L 21/8234; H01L 21/3205; H01L 29/788; H01L 21/8239; H01L 21/44

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: power, FET, lateral, oxidized, polysilicon, layer and thickness

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012-0292682 A1 (SHANJEN PAN et al.) 22 November 2012 See abstract, paragraphs [0023]–[0040], claims 1–20 and figures 3A–5.	1–3, 10–14
A	US 2002-0100936 A1 (FERRUCCIO FRISINA et al.) 01 August 2002 See abstract, paragraphs [0027]–[0042] and figures 3–10.	1–3, 10–14
A	US 2006-0240625 A1 (GARY H. LOECHELT et al.) 26 October 2006 See abstract, paragraphs [0033]–[0045] and figures 5–9.	1–3, 10–14
A	US 2002-0006716 A1 (SE AUG JANG et al.) 17 January 2002 See abstract, paragraphs [0021]–[0025] and figures 3A–3E.	1–3, 10–14
A	JP 2005-228868 A (SONY CORP.) 25 August 2005 See paragraphs [0059]–[0082], claims 1–11 and figures 14–23.	1–3, 10–14

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 May 2014 (30.05.2014)

Date of mailing of the international search report

30 May 2014 (30.05.2014)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB2013/002406**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: 6, 17-18
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claims 6 and 17-18 are unclear, because they refer to multiple dependent claims 5 and 16, respectively, which do not comply with PCT Rule 6.4(a).
3. ☒ Claims Nos.: 4-5, 7-9, 15-16, 19-20
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/IB2013/002406

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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