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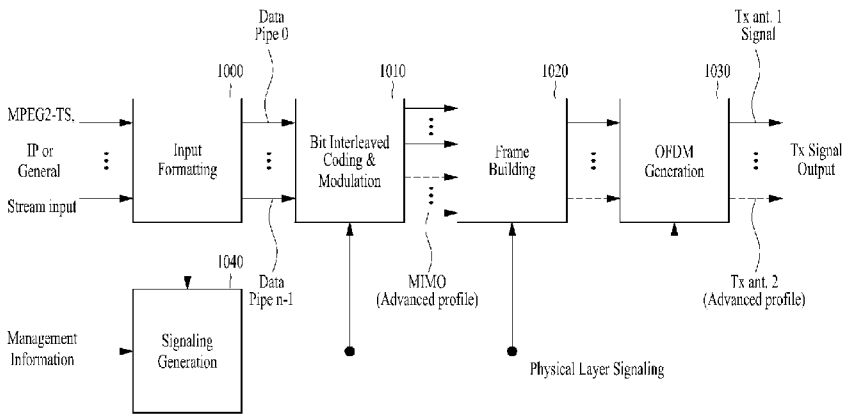
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(54) Title: APPARATUS FOR TRANSMITTING BROADCAST SIGNALS, APPARATUS FOR RECEIVING BROADCAST SIGNALS, METHOD FOR TRANSMITTING BROADCAST SIGNALS AND METHOD FOR RECEIVING BROADCAST SIGNALS



(57) Abstract: The present invention provides a method of transmitting broadcast signals, the method including encoding service data, building at least one signal frame by mapping the encoded service data, modulating data in the built at least one signal frame by an Orthogonal Frequency Division Multiplexing, OFDM, scheme and transmitting the broadcast signals having the modulated data.

Description

Title of Invention: APPARATUS FOR TRANSMITTING BROADCAST SIGNALS, APPARATUS FOR RECEIVING BROADCAST SIGNALS, METHOD FOR TRANSMITTING BROADCAST SIGNALS AND METHOD FOR RECEIVING BROADCAST SIGNALS

Technical Field

[1] The present invention relates to an apparatus for transmitting broadcast signals, an apparatus for receiving broadcast signals and methods for transmitting and receiving broadcast signals.

Background Art

[2] As analog broadcast signal transmission comes to an end, various technologies for transmitting/receiving digital broadcast signals are being developed. A digital broadcast signal may include a larger amount of video/audio data than an analog broadcast signal and further include various types of additional data in addition to the video/audio data.

[3] That is, a digital broadcast system can provide HD (high definition) images, multi-channel audio and various additional services. However, data transmission efficiency for transmission of large amounts of data, robustness of transmission/reception networks and network flexibility in consideration of mobile reception equipment need to be improved for digital broadcast.

Disclosure of Invention

Technical Problem

[4] An object of the present invention is to provide an apparatus and method for transmitting broadcast signals to multiplex data of a broadcast transmission/reception system providing two or more different broadcast services in a time domain and transmit the multiplexed data through the same RF signal bandwidth and an apparatus and method for receiving broadcast signals corresponding thereto.

[5] Another object of the present invention is to provide an apparatus for transmitting broadcast signals, an apparatus for receiving broadcast signals and methods for transmitting and receiving broadcast signals to classify data corresponding to services by components, transmit data corresponding to each component as a data pipe, receive and process the data

[6] Still another object of the present invention is to provide an apparatus for transmitting broadcast signals, an apparatus for receiving broadcast signals and

methods for transmitting and receiving broadcast signals to signal signaling information necessary to provide broadcast signals.

Solution to Problem

[7] To achieve the object and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the present invention provides The present invention provides a method of transmitting broadcast signals, the method including encoding service data, building at least one signal frame by mapping the encoded service data, modulating data in the built at least one signal frame by an Orthogonal Frequency Division Multiplexing, OFDM, scheme and transmitting the broadcast signals having the modulated data.

Advantageous Effects of Invention

[8] The present invention can process data according to service characteristics to control QoS (Quality of Services) for each service or service component, thereby providing various broadcast services.

[9] The present invention can achieve transmission flexibility by transmitting various broadcast services through the same RF signal bandwidth.

[10] The present invention can improve data transmission efficiency and increase robustness of transmission/reception of broadcast signals using a MIMO system.

[11] According to the present invention, it is possible to provide broadcast signal transmission and reception methods and apparatus capable of receiving digital broadcast signals without error even with mobile reception equipment or in an indoor environment.

Brief Description of Drawings

[12] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[13] FIG. 1 illustrates a structure of an apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention.

[14] FIG. 2 illustrates an input formatting block according to one embodiment of the present invention.

[15] FIG. 3 illustrates an input formatting block according to another embodiment of the present invention.

[16] FIG. 4 illustrates an input formatting block according to another embodiment of the present invention.

[17] FIG. 5 illustrates a BICM block according to an embodiment of the present invention.

[18] FIG. 6 illustrates a BICM block according to another embodiment of the present invention.

[19] FIG. 7 illustrates a frame building block according to one embodiment of the present invention.

[20] FIG. 8 illustrates an OFMD generation block according to an embodiment of the present invention.

[21] FIG. 9 illustrates a structure of an apparatus for receiving broadcast signals for future broadcast services according to an embodiment of the present invention.

[22] FIG. 10 illustrates a frame structure according to an embodiment of the present invention.

[23] FIG. 11 illustrates a signaling hierarchy structure of the frame according to an embodiment of the present invention.

[24] FIG. 12 illustrates preamble signaling data according to an embodiment of the present invention.

[25] FIG. 13 illustrates PLS1 data according to an embodiment of the present invention.

[26] FIG. 14 illustrates PLS2 data according to an embodiment of the present invention.

[27] FIG. 15 illustrates PLS2 data according to another embodiment of the present invention.

[28] FIG. 16 illustrates a logical structure of a frame according to an embodiment of the present invention.

[29] FIG. 17 illustrates PLS mapping according to an embodiment of the present invention.

[30] FIG. 18 illustrates EAC mapping according to an embodiment of the present invention.

[31] FIG. 19 illustrates FIC mapping according to an embodiment of the present invention.

[32] FIG. 20 illustrates a type of DP according to an embodiment of the present invention.

[33] FIG. 21 illustrates DP mapping according to an embodiment of the present invention.

[34] FIG. 22 illustrates an FEC structure according to an embodiment of the present invention.

[35] FIG. 23 illustrates a bit interleaving according to an embodiment of the present invention.

[36] FIG. 24 illustrates a cell-word demultiplexing according to an embodiment of the present invention.

[37] FIG. 25 illustrates a time interleaving according to an embodiment of the present invention.

[38] FIG. 26 shows a parity check matrix of a QC-IRA (quasi-cyclic irregular repeat accumulate) LDPC code.

[39] FIG. 27 shows a process of encoding the QC-IRA LDPC code according to an embodiment of the present invention.

[40] FIG. 28 illustrates a parity check matrix permutation process according to an embodiment of the present invention.

[41] FIG. 29 is a table showing addresses of parity check matrix according to an embodiment of the present invention.

[42] FIG. 30 is a table showing addresses of parity check matrix according to another embodiment of the present invention.

[43] FIG. 31 illustrates a method for sequentially encoding the QC-IRA LDPC code according to an embodiment of the present invention.

[44] FIG. 32 illustrates an LDPC decoder according to an embodiment of the present invention.

[45] FIG. 33 is a flowchart illustrating a method for transmitting broadcast signals according to an embodiment of the present invention.

[46] FIG. 34 is a flowchart illustrating a method for receiving broadcast signals according to an embodiment of the present invention.

[47] FIG. 35 illustrates the basic operation of a twisted row-column block interleaver according to an embodiment of the present invention.

[48] FIG. 36 illustrates an operation of a twisted row-column block interleaver according to another embodiment of the present invention.

[49] FIG. 37 illustrates a diagonal-wise reading pattern of a twisted row-column block interleaver according to an embodiment of the present invention.

[50] FIG. 38 illustrates interlaved XFECBLOCKs from each interleaving array according to an embodiment of the present invention.

[51] FIG. 39 is a table showing addresses of parity check matrix according to another embodiment of the present invention.

[52] FIG. 40 is a table showing addresses of parity check matrix according to another embodiment of the present invention.

Best Mode for Carrying out the Invention

[53] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. The detailed description, which will be given below with reference to the accompanying drawings, is intended to explain exemplary embodiments of the present invention, rather than to show the only embodiments that can be implemented according to the present invention. The following detailed description includes specific details in order to provide a thorough understanding of the present invention. However, it will be apparent to those skilled in the art that the present invention may be practiced without

such specific details.

[54] Although most terms used in the present invention have been selected from general ones widely used in the art, some terms have been arbitrarily selected by the applicant and their meanings are explained in detail in the following description as needed. Thus, the present invention should be understood based upon the intended meanings of the terms rather than their simple names or meanings.

[55] The present invention provides apparatuses and methods for transmitting and receiving broadcast signals for future broadcast services. Future broadcast services according to an embodiment of the present invention include a terrestrial broadcast service, a mobile broadcast service, a UHDTV service, etc. The present invention may process broadcast signals for the future broadcast services through non-MIMO (Multiple Input Multiple Output) or MIMO according to one embodiment. A non-MIMO scheme according to an embodiment of the present invention may include a MISO (Multiple Input Single Output) scheme, a SISO (Single Input Single Output) scheme, etc.

[56] While MISO or MIMO uses two antennas in the following for convenience of description, the present invention is applicable to systems using two or more antennas.

[57] The present invention may defines three physical layer (PL) profiles (base, handheld and advanced profiles) each optimized to minimize receiver complexity while attaining the performance required for a particular use case. The physical layer (PHY) profiles are subsets of all configurations that a corresponding receiver should implement.

[58] The three PHY profiles share most of the functional blocks but differ slightly in specific blocks and/or parameters. Additional PHY profiles can be defined in the future. For the system evolution, future profiles can also be multiplexed with the existing profiles in a single RF channel through a future extension frame (FEF). The details of each PHY profile are described below.

[59] 1. Base profile

[60] The base profile represents a main use case for fixed receiving devices that are usually connected to a roof-top antenna. The base profile also includes portable devices that could be transported to a place but belong to a relatively stationary reception category. Use of the base profile could be extended to handheld devices or even vehicular by some improved implementations, but those use cases are not expected for the base profile receiver operation.

[61] Target SNR range of reception is from approximately 10 to 20dB, which includes the 15dB SNR reception capability of the existing broadcast system (e.g. ATSC A/53). The receiver complexity and power consumption is not as critical as in the battery-operated handheld devices, which will use the handheld profile. Key system parameters for the base profile are listed in below table 1.

[62] Table 1

[Table 1]

LDPC codeword length	16K, 64K bits
Constellation size	4~10 bpcu (bits per channel use)
Time de-interleaving memory size	≤ 2^{19} data cells
Pilot patterns	Pilot pattern for fixed reception
FFT size	16K, 32K points

[63] 2. Handheld profile

[64] The handheld profile is designed for use in handheld and vehicular devices that operate with battery power. The devices can be moving with pedestrian or vehicle speed. The power consumption as well as the receiver complexity is very important for the implementation of the devices of the handheld profile. The target SNR range of the handheld profile is approximately 0 to 10dB, but can be configured to reach below 0dB when intended for deeper indoor reception.

[65] In addition to low SNR capability, resilience to the Doppler Effect caused by receiver mobility is the most important performance attribute of the handheld profile. Key system parameters for the handheld profile are listed in the below table 2.

[66] Table 2

[Table 2]

LDPC codeword length	16K bits
Constellation size	2~8 bpcu
Time de-interleaving memory size	≤ 2^{18} data cells
Pilot patterns	Pilot patterns for mobile and indoor reception
FFT size	8K, 16K points

[67] 3. Advanced profile

[68] The advanced profile provides highest channel capacity at the cost of more implementation complexity. This profile requires using MIMO transmission and reception, and UHDTV service is a target use case for which this profile is specifically designed. The increased capacity can also be used to allow an increased number of services in a given bandwidth, e.g., multiple SDTV or HDTV services.

[69] The target SNR range of the advanced profile is approximately 20 to 30dB. MIMO transmission may initially use existing elliptically-polarized transmission equipment, with extension to full-power cross-polarized transmission in the future. Key system parameters for the advanced profile are listed in below table 3.

[70] Table 3

[Table 3]

LDPC codeword length	16K, 64K bits
Constellation size	8~12 bpcu
Time de-interleaving memory size	≤ 2^{19} data cells
Pilot patterns	Pilot pattern for fixed reception
FFT size	16K, 32K points

[71] In this case, the base profile can be used as a profile for both the terrestrial broadcast service and the mobile broadcast service. That is, the base profile can be used to define a concept of a profile which includes the mobile profile. Also, the advanced profile can be divided advanced profile for a base profile with MIMO and advanced profile for a handheld profile with MIMO. Moreover, the three profiles can be changed according to intention of the designer.

[72] The following terms and definitions may apply to the present invention. The following terms and definitions can be changed according to design.

[73] auxiliary stream: sequence of cells carrying data of as yet undefined modulation and coding, which may be used for future extensions or as required by broadcasters or network operators

[74] base data pipe: data pipe that carries service signaling data

[75] baseband frame (or BBFRAME): set of Kbch bits which form the input to one FEC encoding process (BCH and LDPC encoding)

[76] cell: modulation value that is carried by one carrier of the OFDM transmission

[77] coded block: LDPC-encoded block of PLS1 data or one of the LDPC-encoded blocks of PLS2 data

[78] data pipe: logical channel in the physical layer that carries service data or related metadata, which may carry one or multiple service(s) or service component(s).

[79] data pipe unit: a basic unit for allocating data cells to a DP in a frame.

[80] data symbol: OFDM symbol in a frame which is not a preamble symbol (the frame signaling symbol and frame edge symbol is included in the data symbol)

[81] DP_ID: this 8 bit field identifies uniquely a DP within the system identified by the SYSTEM_ID

[82] dummy cell: cell carrying a pseudo random value used to fill the remaining capacity not used for PLS signaling, DPs or auxiliary streams

[83] emergency alert channel: part of a frame that carries EAS information data

[84] frame: physical layer time slot that starts with a preamble and ends with a frame edge symbol

[85] frame repetition unit: a set of frames belonging to same or different physical layer profile including a FEF, which is repeated eight times in a super-frame

[86] fast information channel: a logical channel in a frame that carries the mapping in-

formation between a service and the corresponding base DP

[87] FECBLOCK: set of LDPC-encoded bits of a DP data

[88] FFT size: nominal FFT size used for a particular mode, equal to the active symbol period Ts expressed in cycles of the elementary period T

[89] frame signaling symbol: OFDM symbol with higher pilot density used at the start of a frame in certain combinations of FFT size, guard interval and scattered pilot pattern, which carries a part of the PLS data

[90] frame edge symbol: OFDM symbol with higher pilot density used at the end of a frame in certain combinations of FFT size, guard interval and scattered pilot pattern

[91] frame-group: the set of all the frames having the same PHY profile type in a super-frame.

[92] future extension frame: physical layer time slot within the super-frame that could be used for future extension, which starts with a preamble

[93] Futurecast UTB system: proposed physical layer broadcasting system, of which the input is one or more MPEG2-TS or IP or general stream(s) and of which the output is an RF signal

[94] input stream: A stream of data for an ensemble of services delivered to the end users by the system.

[95] normal data symbol: data symbol excluding the frame signaling symbol and the frame edge symbol

[96] PHY profile: subset of all configurations that a corresponding receiver should implement

[97] PLS: physical layer signaling data consisting of PLS1 and PLS2

[98] PLS1: a first set of PLS data carried in the FSS symbols having a fixed size, coding and modulation, which carries basic information about the system as well as the parameters needed to decode the PLS2

[99] NOTE: PLS1 data remains constant for the duration of a frame-group.

[100] PLS2: a second set of PLS data transmitted in the FSS symbol, which carries more detailed PLS data about the system and the DPs

[101] PLS2 dynamic data: PLS2 data that may dynamically change frame-by-frame

[102] PLS2 static data: PLS2 data that remains static for the duration of a frame-group

[103] preamble signaling data: signaling data carried by the preamble symbol and used to identify the basic mode of the system

[104] preamble symbol: fixed-length pilot symbol that carries basic PLS data and is located in the beginning of a frame

[105] NOTE: The preamble symbol is mainly used for fast initial band scan to detect the system signal, its timing, frequency offset, and FFT size.

[106] reserved for future use: not defined by the present document but may be defined in

future

[107] super frame: set of eight frame repetition units

[108] time interleaving block (TI block): set of cells within which time interleaving is carried out, corresponding to one use of the time interleaver memory

[109] TI group: unit over which dynamic capacity allocation for a particular DP is carried out, made up of an integer, dynamically varying number of XFECBLOCKs

[110] NOTE: The TI group may be mapped directly to one frame or may be mapped to multiple frames. It may contain one or more TI blocks.

[111] Type 1 DP: DP of a frame where all DPs are mapped into the frame in TDM fashion

[112] Type 2 DP: DP of a frame where all DPs are mapped into the frame in FDM fashion

[113] XFECBLOCK: set of Ncells cells carrying all the bits of one LDPC FECBLOCK

[114] FIG. 1 illustrates a structure of an apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention.

[115] The apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention can include an input formatting block 1000, a BICM (Bit interleaved coding & modulation) block 1010, a frame structure block 1020, an OFDM (Orthogonal Frequency Division Multiplexing) generation block 1030 and a signaling generation block 1040. A description will be given of the operation of each module of the apparatus for transmitting broadcast signals.

[116] IP stream/packets and MPEG2-TS are the main input formats, other stream types are handled as General Streams. In addition to these data inputs, Management Information is input to control the scheduling and allocation of the corresponding bandwidth for each input stream. One or multiple TS stream(s), IP stream(s) and/or General Stream(s) inputs are simultaneously allowed.

[117] The input formatting block 1000 can demultiplex each input stream into one or multiple data pipe(s), to each of which an independent coding and modulation is applied. The data pipe (DP) is the basic unit for robustness control, thereby affecting quality-of-service (QoS). One or multiple service(s) or service component(s) can be carried by a single DP. Details of operations of the input formatting block 1000 will be described later.

[118] The data pipe is a logical channel in the physical layer that carries service data or related metadata, which may carry one or multiple service(s) or service component(s).

[119] Also, the data pipe unit: a basic unit for allocating data cells to a DP in a frame.

[120] In the BICM block 1010, parity data is added for error correction and the encoded bit streams are mapped to complex-value constellation symbols. The symbols are interleaved across a specific interleaving depth that is used for the corresponding DP. For the advanced profile, MIMO encoding is performed in the BICM block 1010 and the

additional data path is added at the output for MIMO transmission. Details of operations of the BICM block 1010 will be described later.

[121] The Frame Building block 1020 can map the data cells of the input DPs into the OFDM symbols within a frame. After mapping, the frequency interleaving is used for frequency-domain diversity, especially to combat frequency-selective fading channels. Details of operations of the Frame Building block 1020 will be described later.

[122] After inserting a preamble at the beginning of each frame, the OFDM Generation block 1030 can apply conventional OFDM modulation having a cyclic prefix as guard interval. For antenna space diversity, a distributed MISO scheme is applied across the transmitters. In addition, a Peak-to-Average Power Reduction (PAPR) scheme is performed in the time domain. For flexible network planning, this proposal provides a set of various FFT sizes, guard interval lengths and corresponding pilot patterns. Details of operations of the OFDM Generation block 1030 will be described later.

[123] The Signaling Generation block 1040 can create physical layer signaling information used for the operation of each functional block. This signaling information is also transmitted so that the services of interest are properly recovered at the receiver side. Details of operations of the Signaling Generation block 1040 will be described later.

[124] FIGS. 2, 3 and 4 illustrate the input formatting block 1000 according to embodiments of the present invention. A description will be given of each figure.

[125] FIG. 2 illustrates an input formatting block according to one embodiment of the present invention. FIG. 2 shows an input formatting module when the input signal is a single input stream.

[126] The input formatting block illustrated in FIG. 2 corresponds to an embodiment of the input formatting block 1000 described with reference to FIG. 1.

[127] The input to the physical layer may be composed of one or multiple data streams. Each data stream is carried by one DP. The mode adaptation modules slice the incoming data stream into data fields of the baseband frame (BBF). The system supports three types of input data streams: MPEG2-TS, Internet protocol (IP) and Generic stream (GS). MPEG2-TS is characterized by fixed length (188 byte) packets with the first byte being a sync-byte (0x47). An IP stream is composed of variable length IP datagram packets, as signaled within IP packet headers. The system supports both IPv4 and IPv6 for the IP stream. GS may be composed of variable length packets or constant length packets, signaled within encapsulation packet headers.

[128] (a) shows a mode adaptation block 2000 and a stream adaptation 2010 for signal DP and (b) shows a PLS generation block 2020 and a PLS scrambler 2030 for generating and processing PLS data. A description will be given of the operation of each block.

[129] The Input Stream Splitter splits the input TS, IP, GS streams into multiple service or service component (audio, video, etc.) streams. The mode adaptation module 2010 is

comprised of a CRC Encoder, BB (baseband) Frame Slicer, and BB Frame Header Insertion block.

[130] The CRC Encoder provides three kinds of CRC encoding for error detection at the user packet (UP) level, i.e., CRC-8, CRC-16, and CRC-32. The computed CRC bytes are appended after the UP. CRC-8 is used for TS stream and CRC-32 for IP stream. If the GS stream doesn't provide the CRC encoding, the proposed CRC encoding should be applied.

[131] BB Frame Slicer maps the input into an internal logical-bit format. The first received bit is defined to be the MSB. The BB Frame Slicer allocates a number of input bits equal to the available data field capacity. To allocate a number of input bits equal to the BBF payload, the UP packet stream is sliced to fit the data field of BBF.

[132] BB Frame Header Insertion block can insert fixed length BBF header of 2 bytes is inserted in front of the BB Frame. The BBF header is composed of STUFFI (1 bit), SYNCD (13 bits), and RFU (2 bits). In addition to the fixed 2-Byte BBF header, BBF can have an extension field (1 or 3 bytes) at the end of the 2-byte BBF header.

[133] The stream adaptation 2010 is comprised of stuffing insertion block and BB scrambler.

[134] The stuffing insertion block can insert stuffing field into a payload of a BB frame. If the input data to the stream adaptation is sufficient to fill a BB-Frame, STUFFI is set to '0' and the BBF has no stuffing field. Otherwise STUFFI is set to '1' and the stuffing field is inserted immediately after the BBF header. The stuffing field comprises two bytes of the stuffing field header and a variable size of stuffing data.

[135] The BB scrambler scrambles complete BBF for energy dispersal. The scrambling sequence is synchronous with the BBF. The scrambling sequence is generated by the feed-back shift register.

[136] The PLS generation block 2020 can generate physical layer signaling (PLS) data. The PLS provides the receiver with a means to access physical layer DPs. The PLS data consists of PLS1 data and PLS2 data.

[137] The PLS1 data is a first set of PLS data carried in the FSS symbols in the frame having a fixed size, coding and modulation, which carries basic information about the system as well as the parameters needed to decode the PLS2 data. The PLS1 data provides basic transmission parameters including parameters required to enable the reception and decoding of the PLS2 data. Also, the PLS1 data remains constant for the duration of a frame-group.

[138] The PLS2 data is a second set of PLS data transmitted in the FSS symbol, which carries more detailed PLS data about the system and the DPs. The PLS2 contains parameters that provide sufficient information for the receiver to decode the desired DP. The PLS2 signaling further consists of two types of parameters, PLS2 Static data

(PLS2-STAT data) and PLS2 dynamic data (PLS2-DYN data). The PLS2 Static data is PLS2 data that remains static for the duration of a frame-group and the PLS2 dynamic data is PLS2 data that may dynamically change frame-by-frame.

[139] Details of the PLS data will be described later.

[140] The PLS scrambler 2030 can scramble the generated PLS data for energy dispersal.

[141] The above-described blocks may be omitted or replaced by blocks having similar or identical functions.

[142] FIG. 3 illustrates an input formatting block according to another embodiment of the present invention.

[143] The input formatting block illustrated in FIG. 3 corresponds to an embodiment of the input formatting block 1000 described with reference to FIG. 1.

[144] FIG. 3 shows a mode adaptation block of the input formatting block when the input signal corresponds to multiple input streams.

[145] The mode adaptation block of the input formatting block for processing the multiple input streams can independently process the multiple input streams.

[146] Referring to FIG. 3, the mode adaptation block for respectively processing the multiple input streams can include an input stream splitter 3000, an input stream synchronizer 3010, a compensating delay block 3020, a null packet deletion block 3030, a head compression block 3040, a CRC encoder 3050, a BB frame slicer 3060 and a BB header insertion block 3070. Description will be given of each block of the mode adaptation block.

[147] Operations of the CRC encoder 3050, BB frame slicer 3060 and BB header insertion block 3070 correspond to those of the CRC encoder, BB frame slicer and BB header insertion block described with reference to FIG. 2 and thus description thereof is omitted.

[148] The input stream splitter 3000 can split the input TS, IP, GS streams into multiple service or service component (audio, video, etc.) streams.

[149] The input stream synchronizer 3010 may be referred as ISSY. The ISSY can provide suitable means to guarantee Constant Bit Rate (CBR) and constant end-to-end transmission delay for any input data format. The ISSY is always used for the case of multiple DPs carrying TS, and optionally used for multiple DPs carrying GS streams.

[150] The compensating delay block 3020 can delay the split TS packet stream following the insertion of ISSY information to allow a TS packet recombining mechanism without requiring additional memory in the receiver.

[151] The null packet deletion block 3030, is used only for the TS input stream case. Some TS input streams or split TS streams may have a large number of null-packets present in order to accommodate VBR (variable bit-rate) services in a CBR TS stream. In this case, in order to avoid unnecessary transmission overhead, null-packets can be

identified and not transmitted. In the receiver, removed null-packets can be re-inserted in the exact place where they were originally by reference to a deleted null-packet (DNP) counter that is inserted in the transmission, thus guaranteeing constant bit-rate and avoiding the need for time-stamp (PCR) updating.

[152] The head compression block 3040 can provide packet header compression to increase transmission efficiency for TS or IP input streams. Because the receiver can have a priori information on certain parts of the header, this known information can be deleted in the transmitter.

[153] For Transport Stream, the receiver has a-priori information about the sync-byte configuration (0x47) and the packet length (188 Byte). If the input TS stream carries content that has only one PID, i.e., for only one service component (video, audio, etc.) or service sub-component (SVC base layer, SVC enhancement layer, MVC base view or MVC dependent views), TS packet header compression can be applied (optionally) to the Transport Stream. IP packet header compression is used optionally if the input steam is an IP stream.

[154] The above-described blocks may be omitted or replaced by blocks having similar or identical functions.

[155] FIG. 4 illustrates an input formatting block according to another embodiment of the present invention.

[156] The input formatting block illustrated in FIG. 4 corresponds to an embodiment of the input formatting block 1000 described with reference to FIG. 1.

[157] FIG. 4 illustrates a stream adaptation block of the input formatting module when the input signal corresponds to multiple input streams.

[158] Referring to FIG. 4, the mode adaptation block for respectively processing the multiple input streams can include a scheduler 4000, an 1-Frame delay block 4010, a stuffing insertion block 4020, an in-band signaling 4030, a BB Frame scrambler 4040, a PLS generation block 4050 and a PLS scrambler 4060. Description will be given of each block of the stream adaptation block.

[159] Operations of the stuffing insertion block 4020, the BB Frame scrambler 4040, the PLS generation block 4050 and the PLS scrambler 4060 correspond to those of the stuffing insertion block, BB scrambler, PLS generation block and the PLS scrambler described with reference to FIG. 2 and thus description thereof is omitted.

[160] The scheduler 4000 can determine the overall cell allocation across the entire frame from the amount of FECBLOCKs of each DP. Including the allocation for PLS, EAC and FIC, the scheduler generate the values of PLS2-DYN data, which is transmitted as in-band signaling or PLS cell in FSS of the frame. Details of FECBLOCK, EAC and FIC will be described later.

[161] The 1-Frame delay block 4010 can delay the input data by one transmission frame

such that scheduling information about the next frame can be transmitted through the current frame for in-band signaling information to be inserted into the DPs.

[162] The in-band signaling 4030 can insert un-delayed part of the PLS2 data into a DP of a frame.

[163] The above-described blocks may be omitted or replaced by blocks having similar or identical functions.

[164] FIG. 5 illustrates a BICM block according to an embodiment of the present invention.

[165] The BICM block illustrated in FIG. 5 corresponds to an embodiment of the BICM block 1010 described with reference to FIG. 1.

[166] As described above, the apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention can provide a terrestrial broadcast service, mobile broadcast service, UHDTV service, etc.

[167] Since QoS (quality of service) depends on characteristics of a service provided by the apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention, data corresponding to respective services needs to be processed through different schemes. Accordingly, the a BICM block according to an embodiment of the present invention can independently process DPs input thereto by independently applying SISO, MISO and MIMO schemes to the data pipes respectively corresponding to data paths. Consequently, the apparatus for transmitting broadcast signals for future broadcast services according to an embodiment of the present invention can control QoS for each service or service component transmitted through each DP.

[168] (a) shows the BICM block shared by the base profile and the handheld profile and (b) shows the BICM block of the advanced profile.

[169] The BICM block shared by the base profile and the handheld profile and the BICM block of the advanced profile can include plural processing blocks for processing each DP.

[170] A description will be given of each processing block of the BICM block for the base profile and the handheld profile and the BICM block for the advanced profile.

[171] A processing block 5000 of the BICM block for the base profile and the handheld profile can include a Data FEC encoder 5010, a bit interleaver 5020, a constellation mapper 5030, an SSD (Signal Space Diversity) encoding block 5040 and a time interleaver 5050.

[172] The Data FEC encoder 5010 can perform the FEC encoding on the input BBF to generate FECBLOCK procedure using outer coding (BCH), and inner coding (LDPC). The outer coding (BCH) is optional coding method. Details of operations of the Data FEC encoder 5010 will be described later.

[173] The bit interleaver 5020 can interleave outputs of the Data FEC encoder 5010 to achieve optimized performance with combination of the LDPC codes and modulation scheme while providing an efficiently implementable structure. Details of operations of the bit interleaver 5020 will be described later.

[174] The constellation mapper 5030 can modulate each cell word from the bit interleaver 5020 in the base and the handheld profiles, or cell word from the Cell-word demultiplexer 5010-1 in the advanced profile using either QPSK, QAM-16, non-uniform QAM (NUQ-64, NUQ-256, NUQ-1024) or non-uniform constellation (NUC-16, NUC-64, NUC-256, NUC-1024) to give a power-normalized constellation point, el. This constellation mapping is applied only for DPs. Observe that QAM-16 and NUQs are square shaped, while NUCs have arbitrary shape. When each constellation is rotated by any multiple of 90 degrees, the rotated constellation exactly overlaps with its original one. This "rotation-sense" symmetric property makes the capacities and the average powers of the real and imaginary components equal to each other. Both NUQs and NUCs are defined specifically for each code rate and the particular one used is signaled by the parameter DP_MOD filed in PLS2 data.

[175] The SSD encoding block 5040 can precode cells in two (2D), three (3D), and four (4D) dimensions to increase the reception robustness under difficult fading conditions.

[176] The time interleaver 5050 can operates at the DP level. The parameters of time interleaving (TI) may be set differently for each DP. Details of operations of the time interleaver 5050 will be described later.

[177] A processing block 5000-1 of the BICM block for the advanced profile can include the Data FEC encoder, bit interleaver, constellation mapper, and time interleaver. However, the processing block 5000-1 is distinguished from the processing block 5000 further includes a cell-word demultiplexer 5010-1 and a MIMO encoding block 5020-1.

[178] Also, the operations of the Data FEC encoder, bit interleaver, constellation mapper, and time interleaver in the processing block 5000-1 correspond to those of the Data FEC encoder 5010, bit interleaver 5020, constellation mapper 5030, and time interleaver 5050 described and thus description thereof is omitted.

[179] The cell-word demultiplexer 5010-1 is used for the DP of the advanced profile to divide the single cell-word stream into dual cell-word streams for MIMO processing. Details of operations of the cell-word demultiplexer 5010-1 will be described later.

[180] The MIMO encoding block 5020-1 can processing the output of the cell-word demultiplexer 5010-1 using MIMO encoding scheme. The MIMO encoding scheme was optimized for broadcasting signal transmission. The MIMO technology is a promising way to get a capacity increase but it depends on channel characteristics. Especially for broadcasting, the strong LOS component of the channel or a difference in the received

signal power between two antennas caused by different signal propagation characteristics makes it difficult to get capacity gain from MIMO. The proposed MIMO encoding scheme overcomes this problem using a rotation-based pre-coding and phase randomization of one of the MIMO output signals.

[181] MIMO encoding is intended for a 2x2 MIMO system requiring at least two antennas at both the transmitter and the receiver. Two MIMO encoding modes are defined in this proposal; full-rate spatial multiplexing (FR-SM) and full-rate full-diversity spatial multiplexing (FRFD-SM). The FR-SM encoding provides capacity increase with relatively small complexity increase at the receiver side while the FRFD-SM encoding provides capacity increase and additional diversity gain with a great complexity increase at the receiver side. The proposed MIMO encoding scheme has no restriction on the antenna polarity configuration.

[182] MIMO processing is required for the advanced profile frame, which means all DPs in the advanced profile frame are processed by the MIMO encoder. MIMO processing is applied at DP level. Pairs of the Constellation Mapper outputs NUQ (e1,i and e2,i) are fed to the input of the MIMO Encoder. Paired MIMO Encoder output (g1,i and g2,i) is transmitted by the same carrier k and OFDM symbol l of their respective TX antennas.

[183] The above-described blocks may be omitted or replaced by blocks having similar or identical functions.

[184] FIG. 6 illustrates a BICM block according to another embodiment of the present invention.

[185] The BICM block illustrated in FIG. 6 corresponds to an embodiment of the BICM block 1010 described with reference to FIG. 1.

[186] FIG. 6 illustrates a BICM block for protection of physical layer signaling (PLS), emergency alert channel (EAC) and fast information channel (FIC). EAC is a part of a frame that carries EAS information data and FIC is a logical channel in a frame that carries the mapping information between a service and the corresponding base DP. Details of the EAC and FIC will be described later.

[187] Referring to FIG. 6, the BICM block for protection of PLS, EAC and FIC can include a PLS FEC encoder 6000, a bit interleaver 6010, a constellation mapper 6020 and time interleaver 6030.

[188] Also, the PLS FEC encoder 6000 can include a scrambler, BCH encoding/zero insertion block, LDPC encoding block and LDPC parity punturing block. Description will be given of each block of the BICM block.

[189] The PLS FEC encoder 6000 can encode the scrambled PLS 1/2 data, EAC and FIC section.

[190] The scrambler can scramble PLS1 data and PLS2 data before BCH encoding and shortened and punctured LDPC encoding.

[191] The BCH encoding/zero insertion block can perform outer encoding on the scrambled PLS 1/2 data using the shortened BCH code for PLS protection and insert zero bits after the BCH encoding. For PLS1 data only, the output bits of the zero insertion may be permutted before LDPC encoding.

[192] The LDPC encoding block can encode the output of the BCH encoding/zero insertion block using LDPC code. To generate a complete coded block, C_{ldpc}, parity bits, Pldpc are encoded systematically from each zero-inserted PLS information block, I_{ldpc} and appended after it.

[193] MathFigure 1

[Math.1]

$$\mathbf{C}_{ldpc} = [\mathbf{I}_{ldpc} \ \mathbf{P}_{ldpc}] = [i_0, i_1, \ldots, i_{K_{ldpc}-1}, \ p_0, p_1, \ldots, p_{N_{ldpc}-K_{ldpc}-1}]$$

[194] The LDPC code parameters for PLS1 and PLS2 are as following table 4.

[195] Table 4

[Table 4]

Signaling Type	K_{sig}	K_{bch}	N_{bch_parity}	K_{ldpc} (= N_{bch})	N_{ldpc}	N_{ldpc_parity}	code rate	Q_{ldpc}
PLS1	342	1020	60	1080	4320	3240	1/4	36
PLS2	<1021							
	>1020	2100		2160	7200	5040	3/10	56

[196] The LDPC parity punturing block can perform puncturing on the PLS1 data and PLS 2 data.

[197] When shortening is applied to the PLS1 data protection, some LDPC parity bits are punctured after LDPC encoding. Also, for the PLS2 data protection, the LDPC parity bits of PLS2 are punctured after LDPC encoding. These punctured bits are not transmitted.

[198] The bit interleaver 6010 can interleave the each shortened and punctured PLS1 data and PLS2 data.

[199] The constellation mapper 6020 can map the bit ineterlaeved PLS1 data and PLS2 data onto constellations.

[200] The time interleaver 6030 can interleave the mapped PLS1 data and PLS2 data.

[201] The above-described blocks may be omitted or replaced by blocks having similar or identical functions.

[202] FIG. 7 illustrates a frame building block according to one embodiment of the present invention.

[203] The frame building block illustrated in FIG. 7 corresponds to an embodiment of the frame building block 1020 described with reference to FIG. 1.

[204] Referring to FIG. 7, the frame building block can include a delay compensation

block 7000, a cell mapper 7010 and a frequency interleaver 7020. Description will be given of each block of the frame building block.

[205] The delay compensation block 7000 can adjust the timing between the data pipes and the corresponding PLS data to ensure that they are co-timed at the transmitter end. The PLS data is delayed by the same amount as data pipes are by addressing the delays of data pipes caused by the Input Formatting block and BICM block. The delay of the BICM block is mainly due to the time interleaver 5050. In-band signaling data carries information of the next TI group so that they are carried one frame ahead of the DPs to be signaled. The Delay Compensating block delays in-band signaling data accordingly.

[206] The cell mapper 7010 can map PLS, EAC, FIC, DPs, auxiliary streams and dummy cells into the active carriers of the OFDM symbols in the frame. The basic function of the cell mapper 7010 is to map data cells produced by the TIs for each of the DPs, PLS cells, and EAC/FIC cells, if any, into arrays of active OFDM cells corresponding to each of the OFDM symbols within a frame. Service signaling data (such as PSI(program specific information)/SI) can be separately gathered and sent by a data pipe. The Cell Mapper operates according to the dynamic information produced by the scheduler and the configuration of the frame structure. Details of the frame will be described later.

[207] The frequency interleaver 7020 can randomly interleave data cells received from the cell mapper 7010 to provide frequency diversity. Also, the frequency interleaver 7020 can operate on very OFDM symbol pair comprised of two sequential OFDM symbols using a different interleaving-seed order to get maximum interleaving gain in a single frame. Details of operations of the frequency interleaver 7020 will be described later.

[208] The above-described blocks may be omitted or replaced by blocks having similar or identical functions.

[209] FIG. 8 illustrates an OFMD generation block according to an embodiment of the present invention.

[210] The OFMD generation block illustrated in FIG. 8 corresponds to an embodiment of the OFMD generation block 1030 described with reference to FIG. 1.

[211] The OFDM generation block modulates the OFDM carriers by the cells produced by the Frame Building block, inserts the pilots, and produces the time domain signal for transmission. Also, this block subsequently inserts guard intervals, and applies PAPR (Peak-to-Average Power Radio) reduction processing to produce the final RF signal.

[212] Referring to FIG. 8, the frame building block can include a pilot and reserved tone insertion block 8000, a 2D-eSFN encoding block 8010, an IFFT (Inverse Fast Fourier Transform) block 8020, a PAPR reduction block 8030, a guard interval insertion block 8040, a preamble insertion block 8050, other system insertion block 8060 and a DAC block 8070. Description will be given of each block of the frame building block.

[213] The pilot and reserved tone insertion block 8000 can insert pilots and the reserved tone.

[214] Various cells within the OFDM symbol are modulated with reference information, known as pilots, which have transmitted values known a priori in the receiver. The information of pilot cells is made up of scattered pilots, continual pilots, edge pilots, FSS (frame signaling symbol) pilots and FES (frame edge symbol) pilots. Each pilot is transmitted at a particular boosted power level according to pilot type and pilot pattern. The value of the pilot information is derived from a reference sequence, which is a series of values, one for each transmitted carrier on any given symbol. The pilots can be used for frame synchronization, frequency synchronization, time synchronization, channel estimation, and transmission mode identification, and also can be used to follow the phase noise.

[215] Reference information, taken from the reference sequence, is transmitted in scattered pilot cells in every symbol except the preamble, FSS and FES of the frame. Continual pilots are inserted in every symbol of the frame. The number and location of continual pilots depends on both the FFT size and the scattered pilot pattern. The edge carriers are edge pilots in every symbol except for the preamble symbol. They are inserted in order to allow frequency interpolation up to the edge of the spectrum. FSS pilots are inserted in FSS(s) and FES pilots are inserted in FES. They are inserted in order to allow time interpolation up to the edge of the frame.

[216] The system according to an embodiment of the present invention supports the SFN network, where distributed MISO scheme is optionally used to support very robust transmission mode. The 2D-eSFN is a distributed MISO scheme that uses multiple TX antennas, each of which is located in the different transmitter site in the SFN network.

[217] The 2D-eSFN encoding block 8010 can process a 2D-eSFN processing to distorts the phase of the signals transmitted from multiple transmitters, in order to create both time and frequency diversity in the SFN configuration. Hence, burst errors due to low flat fading or deep-fading for a long time can be mitigated.

[218] The IFFT block 8020 can modulate the output from the 2D-eSFN encoding block 8010 using OFDM modulation scheme. Any cell in the data symbols which has not been designated as a pilot (or as a reserved tone) carries one of the data cells from the frequency interleaver. The cells are mapped to OFDM carriers.

[219] The PAPR reduction block 8030 can perform a PAPR reduction on input signal using various PAPR reduction algorithm in the time domain.

[220] The guard interval insertion block 8040 can insert guard intervals and the preamble insertion block 8050 can insert preamble in front of the signal. Details of a structure of the preamble will be described later. The other system insertion block 8060 can multiplex signals of a plurality of broadcast transmission/reception systems in the time

domain such that data of two or more different broadcast transmission/reception systems providing broadcast services can be simultaneously transmitted in the same RF signal bandwidth. In this case, the two or more different broadcast transmission/ reception systems refer to systems providing different broadcast services. The different broadcast services may refer to a terrestrial broadcast service, mobile broadcast service, etc. Data related to respective broadcast services can be transmitted through different frames.

[221] The DAC block 8070 can convert an input digital signal into an analog signal and output the analog signal. The signal output from the DAC block 7800 can be transmitted through multiple output antennas according to the physical layer profiles. A Tx antenna according to an embodiment of the present invention can have vertical or horizontal polarity.

[222] The above-described blocks may be omitted or replaced by blocks having similar or identical functions according to design.

[223] FIG. 9 illustrates a structure of an apparatus for receiving broadcast signals for future broadcast services according to an embodiment of the present invention.

[224] The apparatus for receiving broadcast signals for future broadcast services according to an embodiment of the present invention can correspond to the apparatus for transmitting broadcast signals for future broadcast services, described with reference to FIG. 1.

[225] The apparatus for receiving broadcast signals for future broadcast services according to an embodiment of the present invention can include a synchronization & demodulation module 9000, a frame parsing module 9010, a demapping & decoding module 9020, an output processor 9030 and a signaling decoding module 9040. A description will be given of operation of each module of the apparatus for receiving broadcast signals.

[226] The synchronization & demodulation module 9000 can receive input signals through m Rx antennas, perform signal detection and synchronization with respect to a system corresponding to the apparatus for receiving broadcast signals and carry out demodulation corresponding to a reverse procedure of the procedure performed by the apparatus for transmitting broadcast signals.

[227] The frame parsing module 9100 can parse input signal frames and extract data through which a service selected by a user is transmitted. If the apparatus for transmitting broadcast signals performs interleaving, the frame parsing module 9100 can carry out deinterleaving corresponding to a reverse procedure of interleaving. In this case, the positions of a signal and data that need to be extracted can be obtained by decoding data output from the signaling decoding module 9400 to restore scheduling information generated by the apparatus for transmitting broadcast signals.

[228] The demapping & decoding module 9200 can convert the input signals into bit domain data and then deinterleave the same as necessary. The demapping & decoding module 9200 can perform demapping for mapping applied for transmission efficiency and correct an error generated on a transmission channel through decoding. In this case, the demapping & decoding module 9200 can obtain transmission parameters necessary for demapping and decoding by decoding the data output from the signaling decoding module 9400.

[229] The output processor 9300 can perform reverse procedures of various compression/ signal processing procedures which are applied by the apparatus for transmitting broadcast signals to improve transmission efficiency. In this case, the output processor 9300 can acquire necessary control information from data output from the signaling decoding module 9400. The output of the output processor 8300 corresponds to a signal input to the apparatus for transmitting broadcast signals and may be MPEG-TSs, IP streams (v4 or v6) and generic streams.

[230] The signaling decoding module 9400 can obtain PLS information from the signal demodulated by the synchronization & demodulation module 9000. As described above, the frame parsing module 9100, demapping & decoding module 9200 and output processor 9300 can execute functions thereof using the data output from the signaling decoding module 9400.

[231] FIG. 10 illustrates a frame structure according to an embodiment of the present invention.

[232] FIG. 10 shows an example configuration of the frame types and FRUs in a super-frame. (a) shows a super frame according to an embodiment of the present invention, (b) shows FRU (Frame Repetition Unit) according to an embodiment of the present invention, (c) shows frames of variable PHY profiles in the FRU and (d) shows a structure of a frame.

[233] A super-frame may be composed of eight FRUs. The FRU is a basic multiplexing unit for TDM of the frames, and is repeated eight times in a super-frame.

[234] Each frame in the FRU belongs to one of the PHY profiles, (base, handheld, advanced) or FEF. The maximum allowed number of the frames in the FRU is four and a given PHY profile can appear any number of times from zero times to four times in the FRU (e.g., base, base, handheld, advanced). PHY profile definitions can be extended using reserved values of the PHY_PROFILE in the preamble, if required.

[235] The FEF part is inserted at the end of the FRU, if included. When the FEF is included in the FRU, the minimum number of FEFs is 8 in a super-frame. It is not recommended that FEF parts be adjacent to each other.

[236] One frame is further divided into a number of OFDM symbols and a preamble. As shown in (d), the frame comprises a preamble, one or more frame signaling symbols

(FSS), normal data symbols and a frame edge symbol (FES).

[237] The preamble is a special symbol that enables fast Futurecast UTB system signal detection and provides a set of basic transmission parameters for efficient transmission and reception of the signal. The detailed description of the preamble will be will be described later.

[238] The main purpose of the FSS(s) is to carry the PLS data. For fast synchronization and channel estimation, and hence fast decoding of PLS data, the FSS has more dense pilot pattern than the normal data symbol. The FES has exactly the same pilots as the FSS, which enables frequency-only interpolation within the FES and temporal interpolation, without extrapolation, for symbols immediately preceding the FES.

[239] FIG. 11 illustrates a signaling hierarchy structure of the frame according to an embodiment of the present invention.

[240] FIG. 11 illustrates the signaling hierarchy structure, which is split into three main parts: the preamble signaling data 11000, the PLS1 data 11010 and the PLS2 data 11020. The purpose of the preamble, which is carried by the preamble symbol in every frame, is to indicate the transmission type and basic transmission parameters of that frame. The PLS1 enables the receiver to access and decode the PLS2 data, which contains the parameters to access the DP of interest. The PLS2 is carried in every frame and split into two main parts: PLS2-STAT data and PLS2-DYN data. The static and dynamic portion of PLS2 data is followed by padding, if necessary.

[241] FIG. 12 illustrates preamble signaling data according to an embodiment of the present invention.

[242] Preamble signaling data carries 21 bits of information that are needed to enable the receiver to access PLS data and trace DPs within the frame structure. Details of the preamble signaling data are as follows:

[243] PHY_PROFILE: This 3-bit field indicates the PHY profile type of the current frame. The mapping of different PHY profile types is given in below table 5.

[244] Table 5

[Table 5]

Value	PHY profile
000	Base profile
001	Handheld profile
010	Advanced profiled
011~110	Reserved
111	FEF

[245] FFT_SIZE: This 2 bit field indicates the FFT size of the current frame within a frame-group, as described in below table 6.

[246] Table 6

[Table 6]

Value	FFT size
00	8K FFT
01	16K FFT
10	32K FFT
11	Reserved

[247] GI_FRACTION: This 3 bit field indicates the guard interval fraction value in the current super-frame, as described in below table 7.

[248] Table 7

[Table 7]

Value	GI_FRACTION
000	1/5
001	1/10
010	1/20
011	1/40
100	1/80
101	1/160
110~111	Reserved

[249] EAC_FLAG: This 1 bit field indicates whether the EAC is provided in the current frame. If this field is set to '1', emergency alert service (EAS) is provided in the current frame. If this field set to '0', EAS is not carried in the current frame. This field can be switched dynamically within a super-frame.

[250] PILOT_MODE: This 1-bit field indicates whether the pilot mode is mobile mode or fixed mode for the current frame in the current frame-group. If this field is set to '0', mobile pilot mode is used. If the field is set to '1', the fixed pilot mode is used.

[251] PAPR_FLAG: This 1-bit field indicates whether PAPR reduction is used for the current frame in the current frame-group. If this field is set to value '1', tone reservation is used for PAPR reduction. If this field is set to '0', PAPR reduction is not used.

[252] FRU_CONFIGURE: This 3-bit field indicates the PHY profile type configurations of the frame repetition units (FRU) that are present in the current super-frame. All profile types conveyed in the current super-frame are identified in this field in all preambles in the current super-frame. The 3-bit field has a different definition for each profile, as show in below table 8.

[253] Table 8

[Table 8]

	Current PHY_PROFILE = '000' (base)	Current PHY_PROFILE = '001' (handheld)	Current PHY_PROFILE = '010' (advanced)	Current PHY_PROFILE = '111' (FEF)
FRU_CONFIGURE = 000	Only base profile present	Only handheld profile present	Only advanced profile present	Only FEF present
FRU_CONFIGURE = 1XX	Handheld profile present	Base profile present	Base profile present	Base profile present
FRU_CONFIGURE = X1X	Advanced profile present	Advanced profile present	Handheld profile present	Handheld profile present
FRU_CONFIGURE = XX1	FEF present	FEF present	FEF present	Advanced profile present

[254] RESERVED: This 7-bit field is reserved for future use.

[255] FIG. 13 illustrates PLS1 data according to an embodiment of the present invention.

[256] PLS1 data provides basic transmission parameters including parameters required to enable the reception and decoding of the PLS2. As above mentioned, the PLS1 data remain unchanged for the entire duration of one frame-group. The detailed definition of the signaling fields of the PLS1 data are as follows:

[257] PREAMBLE_DATA: This 20-bit field is a copy of the preamble signaling data excluding the EAC_FLAG.

[258] NUM_FRAME_FRU: This 2-bit field indicates the number of the frames per FRU.

[259] PAYLOAD_TYPE: This 3-bit field indicates the format of the payload data carried in the frame-group. PAYLOAD_TYPE is signaled as shown in table 9.

[260] Table 9

[Table 9]

value	Payload type
1XX	TS stream is transmitted
X1X	IP stream is transmitted
XX1	GS stream is transmitted

[261] NUM_FSS: This 2-bit field indicates the number of FSS symbols in the current frame.

[262] SYSTEM_VERSION: This 8-bit field indicates the version of the transmitted signal format. The SYSTEM_VERSION is divided into two 4-bit fields, which are a major version and a minor version.

[263] Major version: The MSB four bits of SYSTEM_VERSION field indicate major version information. A change in the major version field indicates a non-backward-compatible change. The default value is '0000'. For the version described in this standard, the value is set to '0000'.

[264] Minor version: The LSB four bits of SYSTEM_VERSION field indicate minor version information. A change in the minor version field is backward-compatible.

[265] CELL_ID: This is a 16-bit field which uniquely identifies a geographic cell in an ATSC network. An ATSC cell coverage area may consist of one or more frequencies, depending on the number of frequencies used per Futurecast UTB system. If the value of the CELL_ID is not known or unspecified, this field is set to '0'.

[266] NETWORK_ID: This is a 16-bit field which uniquely identifies the current ATSC network.

[267] SYSTEM_ID: This 16-bit field uniquely identifies the Futurecast UTB system within the ATSC network. The Futurecast UTB system is the terrestrial broadcast system whose input is one or more input streams (TS, IP, GS) and whose output is an RF signal. The Futurecast UTB system carries one or more PHY profiles and FEF, if any. The same Futurecast UTB system may carry different input streams and use different RF frequencies in different geographical areas, allowing local service insertion. The frame structure and scheduling is controlled in one place and is identical for all transmissions within a Futurecast UTB system. One or more Futurecast UTB systems may have the same SYSTEM_ID meaning that they all have the same physical layer structure and configuration.

[268] The following loop consists of FRU_PHY_PROFILE, FRU_FRAME_LENGTH, FRU_GI_FRACTION, and RESERVED which are used to indicate the FRU configuration and the length of each frame type. The loop size is fixed so that four PHY profiles (including a FEF) are signaled within the FRU. If NUM_FRAME_FRU is less than 4, the unused fields are filled with zeros.

[269] FRU_PHY_PROFILE: This 3-bit field indicates the PHY profile type of the (i+1)th (i is the loop index) frame of the associated FRU. This field uses the same signaling format as shown in the table 8.

[270] FRU_FRAME_LENGTH: This 2-bit field indicates the length of the (i+1)th frame of the associated FRU. Using FRU_FRAME_LENGTH together with FRU_GI_FRACTION, the exact value of the frame duration can be obtained.

[271] FRU_GI_FRACTION: This 3-bit field indicates the guard interval fraction value of the (i+1)th frame of the associated FRU. FRU_GI_FRACTION is signaled according to the table 7.

[272] RESERVED: This 4-bit field is reserved for future use.

[273] The following fields provide parameters for decoding the PLS2 data.

[274] PLS2_FEC_TYPE: This 2-bit field indicates the FEC type used by the PLS2 protection. The FEC type is signaled according to table 10. The details of the LDPC codes will be described later.

[275] Table 10

[Table 10]

Content	PLS2 FEC type
00	4K-1/4 and 7K-3/10 LDPC codes
01 ~ 11	Reserved

[276] PLS2_MOD: This 3-bit field indicates the modulation type used by the PLS2. The modulation type is signaled according to table 11.

[277] Table 11

[Table 11]

Value	PLS2_MODE
000	BPSK
001	QPSK
010	QAM-16
011	NUQ-64
100~111	Reserved

[278] PLS2_SIZE_CELL: This 15-bit field indicates $C_{total_partial_block}$, the size (specified as the number of QAM cells) of the collection of full coded blocks for PLS2 that is carried in the current frame-group. This value is constant during the entire duration of the current frame-group.

[279] PLS2_STAT_SIZE_BIT: This 14-bit field indicates the size, in bits, of the PLS2-STAT for the current frame-group. This value is constant during the entire duration of the current frame-group.

[280] PLS2_DYN_SIZE_BIT: This 14-bit field indicates the size, in bits, of the PLS2-DYN for the current frame-group. This value is constant during the entire duration of the current frame-group.

[281] PLS2_REP_FLAG: This 1-bit flag indicates whether the PLS2 repetition mode is used in the current frame-group. When this field is set to value '1', the PLS2 repetition mode is activated. When this field is set to value '0', the PLS2 repetition mode is de-activated.

[282] PLS2_REP_SIZE_CELL: This 15-bit field indicates $C_{total_partial_block}$, the size (specified as the number of QAM cells) of the collection of partial coded blocks for PLS2 carried in every frame of the current frame-group, when PLS2 repetition is used. If repetition is not used, the value of this field is equal to 0. This value is constant during the entire

duration of the current frame-group.

[283] PLS2_NEXT_FEC_TYPE: This 2-bit field indicates the FEC type used for PLS2 that is carried in every frame of the next frame-group. The FEC type is signaled according to the table 10.

[284] PLS2_NEXT_MOD: This 3-bit field indicates the modulation type used for PLS2 that is carried in every frame of the next frame-group. The modulation type is signaled according to the table 11.

[285] PLS2_NEXT_REP_FLAG: This 1-bit flag indicates whether the PLS2 repetition mode is used in the next frame-group. When this field is set to value '1', the PLS2 repetition mode is activated. When this field is set to value '0', the PLS2 repetition mode is deactivated.

[286] PLS2_NEXT_REP_SIZE_CELL: This 15-bit field indicates $C_{total_full_block}$, The size (specified as the number of QAM cells) of the collection of full coded blocks for PLS2 that is carried in every frame of the next frame-group, when PLS2 repetition is used. If repetition is not used in the next frame-group, the value of this field is equal to 0. This value is constant during the entire duration of the current frame-group.

[287] PLS2_NEXT_REP_STAT_SIZE_BIT: This 14-bit field indicates the size, in bits, of the PLS2-STAT for the next frame-group. This value is constant in the current frame-group.

[288] PLS2_NEXT_REP_DYN_SIZE_BIT: This 14-bit field indicates the size, in bits, of the PLS2-DYN for the next frame-group. This value is constant in the current frame-group.

[289] PLS2_AP_MODE: This 2-bit field indicates whether additional parity is provided for PLS2 in the current frame-group. This value is constant during the entire duration of the current frame-group. The below table 12 gives the values of this field. When this field is set to '00', additional parity is not used for the PLS2 in the current frame-group.

[290] Table 12

[Table 12]

Value	PLS2-AP mode
00	AP is not provided
01	AP1 mode
10~11	Reserved

[291] PLS2_AP_SIZE_CELL: This 15-bit field indicates the size (specified as the number of QAM cells) of the additional parity bits of the PLS2. This value is constant during the entire duration of the current frame-group.

[292] PLS2_NEXT_AP_MODE: This 2-bit field indicates whether additional parity is provided for PLS2 signaling in every frame of next frame-group. This value is constant

during the entire duration of the current frame-group. The table 12 defines the values of this field

[293] PLS2_NEXT_AP_SIZE_CELL: This 15-bit field indicates the size (specified as the number of QAM cells) of the additional parity bits of the PLS2 in every frame of the next frame-group. This value is constant during the entire duration of the current frame-group.

[294] RESERVED: This 32-bit field is reserved for future use.

[295] CRC_32: A 32-bit error detection code, which is applied to the entire PLS1 signaling.

[296] FIG. 14 illustrates PLS2 data according to an embodiment of the present invention.

[297] FIG. 14 illustrates PLS2-STAT data of the PLS2 data. The PLS2-STAT data are the same within a frame-group, while the PLS2-DYN data provide information that is specific for the current frame.

[298] The details of fields of the PLS2-STAT data are as follows:

[299] FIC_FLAG: This 1-bit field indicates whether the FIC is used in the current frame-group. If this field is set to '1', the FIC is provided in the current frame. If this field set to '0', the FIC is not carried in the current frame. This value is constant during the entire duration of the current frame-group.

[300] AUX_FLAG: This 1-bit field indicates whether the auxiliary stream(s) is used in the current frame-group. If this field is set to '1', the auxiliary stream is provided in the current frame. If this field set to '0', the auxiliary stream is not carried in the current frame. This value is constant during the entire duration of current frame-group.

[301] NUM_DP: This 6-bit field indicates the number of DPs carried within the current frame. The value of this field ranges from 1 to 64, and the number of DPs is NUM_DP+1.

[302] DP_ID: This 6-bit field identifies uniquely a DP within a PHY profile.

[303] DP_TYPE: This 3-bit field indicates the type of the DP. This is signaled according to the below table 13.

[304] Table 13

[Table 13]

Value	DP Type
000	DP Type 1
001	DP Type 2
010~111	reserved

[305] DP_GROUP_ID: This 8-bit field identifies the DP group with which the current DP is associated. This can be used by a receiver to access the DPs of the service components associated with a particular service, which will have the same

DP_GROUP_ID.

[306] BASE_DP_ID: This 6-bit field indicates the DP carrying service signaling data (such as PSI/SI) used in the Management layer. The DP indicated by BASE_DP_ID may be either a normal DP carrying the service signaling data along with the service data or a dedicated DP carrying only the service signaling data

[307] DP_FEC_TYPE: This 2-bit field indicates the FEC type used by the associated DP. The FEC type is signaled according to the below table 14.

[308] Table 14

[Table 14]

Value	FEC_TYPE
00	16K LDPC
01	64K LDPC
10 ~ 11	Reserved

[309] DP_COD: This 4-bit field indicates the code rate used by the associated DP. The code rate is signaled according to the below table 15.

[310] Table 15

[Table 15]

Value	Code rate
0000	5/15
0001	6/15
0010	7/15
0011	8/15
0100	9/15
0101	10/15
0110	11/15
0111	12/15
1000	13/15
1001 ~ 1111	Reserved

[311] DP_MOD: This 4-bit field indicates the modulation used by the associated DP. The modulation is signaled according to the below table 16.

[312] Table 16

[Table 16]

Value	Modulation
0000	QPSK
0001	QAM-16
0010	NUQ-64
0011	NUQ-256
0100	NUQ-1024
0101	NUC-16
0110	NUC-64
0111	NUC-256
1000	NUC-1024
1001~1111	reserved

[313] DP_SSD_FLAG: This 1-bit field indicates whether the SSD mode is used in the associated DP. If this field is set to value '1', SSD is used. If this field is set to value '0', SSD is not used.

[314] The following field appears only if PHY_PROFILE is equal to '010', which indicates the advanced profile:

[315] DP_MIMO: This 3-bit field indicates which type of MIMO encoding process is applied to the associated DP. The type of MIMO encoding process is signaled according to the table 17.

[316] Table 17

[Table 17]

Value	MIMO encoding
000	FR-SM
001	FRFD-SM
010~111	reserved

[317] DP_TI_TYPE: This 1-bit field indicates the type of time-interleaving. A value of '0' indicates that one TI group corresponds to one frame and contains one or more TI-blocks. A value of '1' indicates that one TI group is carried in more than one frame and contains only one TI-block.

[318] DP_TI_LENGTH: The use of this 2-bit field (the allowed values are only 1, 2, 4, 8) is determined by the values set within the DP_TI_TYPE field as follows:

[319] If the DP_TI_TYPE is set to the value '1', this field indicates PI, the number of the frames to which each TI group is mapped, and there is one TI-block per TI group (NTI=1). The allowed PI values with 2-bit field are defined in the below table 18.

[320] If the DP_TI_TYPE is set to the value '0', this field indicates the number of TI-blocks NTI per TI group, and there is one TI group per frame (PI=1). The allowed PI values

with 2-bit field are defined in the below table 18.

[321] Table 18

[Table 18]

2-bit field	P_I	N_{TI}
00	1	1
01	2	2
10	4	3
11	8	4

[322] DP_FRAME_INTERVAL: This 2-bit field indicates the frame interval (I_{JUMP}) within the frame-group for the associated DP and the allowed values are 1, 2, 4, 8 (the corresponding 2-bit field is '00', '01', '10', or '11', respectively). For DPs that do not appear every frame of the frame-group, the value of this field is equal to the interval between successive frames. For example, if a DP appears on the frames 1, 5, 9, 13, etc., this field is set to '4'. For DPs that appear in every frame, this field is set to '1'.

[323] DP_TI_BYPASS: This 1-bit field determines the availability of time interleaver 5050. If time interleaving is not used for a DP, it is set to '1'. Whereas if time interleaving is used it is set to '0'.

[324] DP_FIRST_FRAME_IDX: This 5-bit field indicates the index of the first frame of the super-frame in which the current DP occurs. The value of DP_FIRST_FRAME_IDX ranges from 0 to 31

[325] DP_NUM_BLOCK_MAX: This 10-bit field indicates the maximum value of DP_NUM_BLOCKS for this DP. The value of this field has the same range as DP_NUM_BLOCKS.

[326] DP_PAYLOAD_TYPE: This 2-bit field indicates the type of the payload data carried by the given DP. DP_PAYLOAD_TYPE is signaled according to the below table 19.

[327] Table 19

[Table 19]

Value	Payload Type
00	TS.
01	IP
10	GS
11	reserved

[328] DP_INBAND_MODE: This 2-bit field indicates whether the current DP carries in-band signaling information. The in-band signaling type is signaled according to the below table 20.

[329] Table 20

[Table 20]

Value	In-band mode
00	In-band signaling is not carried.
01	INBAND-PLS is carried only
10	INBAND-ISSY is carried only
11	INBAND-PLS and INBAND-ISSY are carried

[330] DP_PROTOCOL_TYPE: This 2-bit field indicates the protocol type of the payload carried by the given DP. It is signaled according to the below table 21 when input payload types are selected.

[331] Table 21

[Table 21]

Value	If DP_PAYLOAD_TYPE Is TS	If DP_PAYLOAD_TYPE Is IP	If DP_PAYLOAD_TYPE Is GS
00	MPEG2-TS	IPv4	(Note)
01	Reserved	IPv6	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved

[332] DP_CRC_MODE: This 2-bit field indicates whether CRC encoding is used in the Input Formatting block. The CRC mode is signaled according to the below table 22.

[333] Table 22

[Table 22]

Value	CRC mode
00	Not used
01	CRC-8
10	CRC-16
11	CRC-32

[334] DNP_MODE: This 2-bit field indicates the null-packet deletion mode used by the associated DP when DP_PAYLOAD_TYPE is set to TS (‘00’). DNP_MODE is signaled according to the below table 23. If DP_PAYLOAD_TYPE is not TS (‘00’), DNP_MODE is set to the value ‘00’.

[335] Table 23

[Table 23]

Value	Null-packet deletion mode
00	Not used
01	DNP-NORMAL
10	DNP-OFFSET
11	reserved

[336] ISSY_MODE: This 2-bit field indicates the ISSY mode used by the associated DP when DP_PAYLOAD_TYPE is set to TS (‘00’). The ISSY_MODE is signaled according to the below table 24 If DP_PAYLOAD_TYPE is not TS (‘00’), ISSY_MODE is set to the value ‘00’.

[337] Table 24

[Table 24]

Value	ISSY mode
00	Not used
01	ISSY-UP
10	ISSY-BBF
11	reserved

[338] HC_MODE_TS: This 2-bit field indicates the TS header compression mode used by the associated DP when DP_PAYLOAD_TYPE is set to TS (‘00’). The HC_MODE_TS is signaled according to the below table 25.

[339] Table 25

[Table 25]

Value	Header compression mode
00	HC_MODE_TS 1
01	HC_MODE_TS 2
10	HC_MODE_TS 3
11	HC_MODE_TS 4

[340] HC_MODE_IP: This 2-bit field indicates the IP header compression mode when DP_PAYLOAD_TYPE is set to IP (‘01’). The HC_MODE_IP is signaled according to the below table 26.

[341] Table 26

[Table 26]

Value	Header compression mode
00	No compression
01	HC_MODE_IP 1
10~11	reserved

[342] PID : This 13-bit field indicates the PID number for TS header compression when DP_PAYLOAD_TYPE is set to TS (‘00’) and HC_MODE_TS is set to ‘01’ or ‘10’.

[343] RESERVED: This 8-bit field is reserved for future use.

[344] The following field appears only if FIC_FLAG is equal to ‘1’:

[345] FIC_VERSION: This 8-bit field indicates the version number of the FIC.

[346] FIC_LENGTH_BYTE: This 13-bit field indicates the length, in bytes, of the FIC.

[347] RESERVED: This 8-bit field is reserved for future use.

[348] The following field appears only if AUX_FLAG is equal to ‘1’:

[349] NUM_AUX: This 4-bit field indicates the number of auxiliary streams. Zero means no auxiliary streams are used.

[350] AUX_CONFIG_RFU: This 8-bit field is reserved for future use.

[351] AUX_STREAM_TYPE: This 4-bit is reserved for future use for indicating the type of the current auxiliary stream.

[352] AUX_PRIVATE_CONFIG: This 28-bit field is reserved for future use for signaling auxiliary streams.

[353] FIG. 15 illustrates PLS2 data according to another embodiment of the present invention.

[354] FIG. 15 illustrates PLS2-DYN data of the PLS2 data. The values of the PLS2-DYN data may change during the duration of one frame-group, while the size of fields remains constant.

[355] The details of fields of the PLS2-DYN data are as follows:

[356] FRAME_INDEX: This 5-bit field indicates the frame index of the current frame within the super-frame. The index of the first frame of the super-frame is set to ‘0’.

[357] PLS_CHANGE_COUNTER: This 4-bit field indicates the number of super-frames ahead where the configuration will change. The next super-frame with changes in the configuration is indicated by the value signaled within this field. If this field is set to the value '0000', it means that no scheduled change is foreseen: e.g., value '1' indicates that there is a change in the next super-frame.

[358] FIC_CHANGE_COUNTER: This 4-bit field indicates the number of super-frames ahead where the configuration (i.e., the contents of the FIC) will change. The next super-frame with changes in the configuration is indicated by the value signaled within this field. If this field is set to the value '0000', it means that no scheduled change is

foreseen: e.g. value '0001' indicates that there is a change in the next super-frame..

[359] RESERVED: This 16-bit field is reserved for future use.

[360] The following fields appear in the loop over NUM_DP, which describe the parameters associated with the DP carried in the current frame.

[361] DP_ID: This 6-bit field indicates uniquely the DP within a PHY profile.

[362] DP_START: This 15-bit (or 13-bit) field indicates the start position of the first of the DPs using the DPU addressing scheme. The DP_START field has differing length according to the PHY profile and FFT size as shown in the below table 27.

[363] Table 27

[Table 27]

PHY profile	DP_START field size	
	64K	16K
Base	13 bit	15 bit
Handheld	-	13 bit
Advanced	13 bit	15 bit

[364] DP_NUM_BLOCK: This 10-bit field indicates the number of FEC blocks in the current TI group for the current DP. The value of DP_NUM_BLOCK ranges from 0 to 1023

[365] RESERVED: This 8-bit field is reserved for future use.

[366] The following fields indicate the FIC parameters associated with the EAC.

[367] EAC_FLAG: This 1-bit field indicates the existence of the EAC in the current frame. This bit is the same value as the EAC_FLAG in the preamble.

[368] EAS_WAKE_UP_VERSION_NUM: This 8-bit field indicates the version number of a wake-up indication.

[369] If the EAC_FLAG field is equal to ‘1’, the following 12 bits are allocated for EAC_LENGTH_BYTE field. If the EAC_FLAG field is equal to ‘0’, the following 12 bits are allocated for EAC_COUNTER.

[370] EAC_LENGTH_BYTE: This 12-bit field indicates the length, in byte, of the EAC. .

[371] EAC_COUNTER: This 12-bit field indicates the number of the frames before the frame where the EAC arrives.

[372] The following field appears only if the AUX_FLAG field is equal to ‘1':

[373] AUX_PRIVATE_DYN: This 48-bit field is reserved for future use for signaling auxiliary streams. The meaning of this field depends on the value of AUX_STREAM_TYPE in the configurable PLS2-STAT.

[374] CRC_32: A 32-bit error detection code, which is applied to the entire PLS2.

[375] FIG. 16 illustrates a logical structure of a frame according to an embodiment of the present invention.

[376] As above mentioned, the PLS, EAC, FIC, DPs, auxiliary streams and dummy cells are mapped into the active carriers of the OFDM symbols in the frame. The PLS1 and PLS2 are first mapped into one or more FSS(s). After that, EAC cells, if any, are mapped immediately following the PLS field, followed next by FIC cells, if any. The DPs are mapped next after the PLS or EAC, FIC, if any. Type 1 DPs follows first, and Type 2 DPs next. The details of a type of the DP will be described later. In some case, DPs may carry some special data for EAS or service signaling data. The auxiliary stream or streams, if any, follow the DPs, which in turn are followed by dummy cells. Mapping them all together in the above mentioned order, i.e. PLS, EAC, FIC, DPs, auxiliary streams and dummy data cells exactly fill the cell capacity in the frame.

[377] FIG. 17 illustrates PLS mapping according to an embodiment of the present invention.

[378] PLS cells are mapped to the active carriers of FSS(s). Depending on the number of cells occupied by PLS, one or more symbols are designated as FSS(s), and the number of FSS(s) N_{FSS} is signaled by NUM_FSS in PLS1. The FSS is a special symbol for carrying PLS cells. Since robustness and latency are critical issues in the PLS, the FSS(s) has higher density of pilots allowing fast synchronization and frequency-only interpolation within the FSS.

[379] PLS cells are mapped to active carriers of the N_{FSS} FSS(s) in a top-down manner as shown in an example in FIG. 17. The PLS1 cells are mapped first from the first cell of the first FSS in an increasing order of the cell index. The PLS2 cells follow immediately after the last cell of the PLS1 and mapping continues downward until the last cell index of the first FSS. If the total number of required PLS cells exceeds the number of active carriers of one FSS, mapping proceeds to the next FSS and continues in exactly the same manner as the first FSS.

[380] After PLS mapping is completed, DPs are carried next. If EAC, FIC or both are present in the current frame, they are placed between PLS and "normal" DPs.

[381] FIG. 18 illustrates EAC mapping according to an embodiment of the present invention.

[382] EAC is a dedicated channel for carrying EAS messages and links to the DPs for EAS. EAS support is provided but EAC itself may or may not be present in every frame. EAC, if any, is mapped immediately after the PLS2 cells. EAC is not preceded by any of the FIC, DPs, auxiliary streams or dummy cells other than the PLS cells. The procedure of mapping the EAC cells is exactly the same as that of the PLS.

[383] The EAC cells are mapped from the next cell of the PLS2 in increasing order of the cell index as shown in the example in FIG. 18. Depending on the EAS message size, EAC cells may occupy a few symbols, as shown in FIG. 18.

[384] EAC cells follow immediately after the last cell of the PLS2, and mapping continues

downward until the last cell index of the last FSS. If the total number of required EAC cells exceeds the number of remaining active carriers of the last FSS mapping proceeds to the next symbol and continues in exactly the same manner as FSS(s). The next symbol for mapping in this case is the normal data symbol, which has more active carriers than a FSS.

[385] After EAC mapping is completed, the FIC is carried next, if any exists. If FIC is not transmitted (as signaled in the PLS2 field), DPs follow immediately after the last cell of the EAC.

[386] FIG. 19 illustrates FIC mapping according to an embodiment of the present invention.

[387] shows an example mapping of FIC cell without EAC and (b) shows an example mapping of FIC cell with EAC.

[388] FIC is a dedicated channel for carrying cross-layer information to enable fast service acquisition and channel scanning. This information primarily includes channel binding information between DPs and the services of each broadcaster. For fast scan, a receiver can decode FIC and obtain information such as broadcaster ID, number of services, and BASE_DP_ID. For fast service acquisition, in addition to FIC, base DP can be decoded using BASE_DP_ID. Other than the content it carries, a base DP is encoded and mapped to a frame in exactly the same way as a normal DP. Therefore, no additional description is required for a base DP. The FIC data is generated and consumed in the Management Layer. The content of FIC data is as described in the Management Layer specification.

[389] The FIC data is optional and the use of FIC is signaled by the FIC_FLAG parameter in the static part of the PLS2. If FIC is used, FIC_FLAG is set to '1' and the signaling field for FIC is defined in the static part of PLS2. Signaled in this field are FIC_VERSION, and FIC_LENGTH_BYTE. FIC uses the same modulation, coding and time interleaving parameters as PLS2. FIC shares the same signaling parameters such as PLS2_MOD and PLS2_FEC. FIC data, if any, is mapped immediately after PLS2 or EAC if any. FIC is not preceded by any normal DPs, auxiliary streams or dummy cells. The method of mapping FIC cells is exactly the same as that of EAC which is again the same as PLS.

[390] Without EAC after PLS, FIC cells are mapped from the next cell of the PLS2 in an increasing order of the cell index as shown in an example in (a). Depending on the FIC data size, FIC cells may be mapped over a few symbols, as shown in (b).

[391] FIC cells follow immediately after the last cell of the PLS2, and mapping continues downward until the last cell index of the last FSS. If the total number of required FIC cells exceeds the number of remaining active carriers of the last FSS, mapping proceeds to the next symbol and continues in exactly the same manner as FSS(s). The

next symbol for mapping in this case is the normal data symbol which has more active carriers than a FSS.

[392] If EAS messages are transmitted in the current frame, EAC precedes FIC, and FIC cells are mapped from the next cell of the EAC in an increasing order of the cell index as shown in (b).

[393] After FIC mapping is completed, one or more DPs are mapped, followed by auxiliary streams, if any, and dummy cells.

[394] FIG. 20 illustrates a type of DP according to an embodiment of the present invention.

[395] FIG. 20 shows type 1 DP and (b) shows type 2 DP.

[396] After the preceding channels, i.e., PLS, EAC and FIC, are mapped, cells of the DPs are mapped. A DP is categorized into one of two types according to mapping method:

[397] Type 1 DP: DP is mapped by TDM

[398] Type 2 DP: DP is mapped by FDM

[399] The type of DP is indicated by DP_TYPE field in the static part of PLS2. FIG. 20 illustrates the mapping orders of Type 1 DPs and Type 2 DPs. Type 1 DPs are first mapped in the increasing order of cell index, and then after reaching the last cell index, the symbol index is increased by one. Within the next symbol, the DP continues to be mapped in the increasing order of cell index starting from p = 0. With a number of DPs mapped together in one frame, each of the Type 1 DPs are grouped in time, similar to TDM multiplexing of DPs.

[400] Type 2 DPs are first mapped in the increasing order of symbol index, and then after reaching the last OFDM symbol of the frame, the cell index increases by one and the symbol index rolls back to the first available symbol and then increases from that symbol index. After mapping a number of DPs together in one frame, each of the Type 2 DPs are grouped in frequency together, similar to FDM multiplexing of DPs.

[401] Type 1 DPs and Type 2 DPs can coexist in a frame if needed with one restriction; Type 1 DPs always precede Type 2 DPs. The total number of OFDM cells carrying Type 1 and Type 2 DPs cannot exceed the total number of OFDM cells available for transmission of DPs:

[402] MathFigure 2

[Math.2]

$$D_{DP1} + D_{DP2} \leq D_{DP}$$

[403] where D_{DP1} is the number of OFDM cells occupied by Type 1 DPs, D_{DP2} is the number of cells occupied by Type 2 DPs. Since PLS, EAC, FIC are all mapped in the same way as Type 1 DP, they all follow "Type 1 mapping rule". Hence, overall, Type 1 mapping always precedes Type 2 mapping.

[404] FIG. 21 illustrates DP mapping according to an embodiment of the present invention.

[405] (a) shows an addressing of OFDM cells for mapping type 1 DPs and (b) shows an an addressing of OFDM cells for mapping for type 2 DPs.

[406] Addressing of OFDM cells for mapping Type 1 DPs (0, ..., D_{DP1}-1) is defined for the active data cells of Type 1 DPs. The addressing scheme defines the order in which the cells from the TIs for each of the Type 1 DPs are allocated to the active data cells. It is also used to signal the locations of the DPs in the dynamic part of the PLS2.

[407] Without EAC and FIC, address 0 refers to the cell immediately following the last cell carrying PLS in the last FSS. If EAC is transmitted and FIC is not in the corresponding frame, address 0 refers to the cell immediately following the last cell carrying EAC. If FIC is transmitted in the corresponding frame, address 0 refers to the cell immediately following the last cell carrying FIC. Address 0 for Type 1 DPs can be calculated considering two different cases as shown in (a). In the example in (a), PLS, EAC and FIC are assumed to be all transmitted. Extension to the cases where either or both of EAC and FIC are omitted is straightforward. If there are remaining cells in the FSS after mapping all the cells up to FIC as shown on the left side of (a).

[408] Addressing of OFDM cells for mapping Type 2 DPs (0, ..., D_{DP2}-1) is defined for the active data cells of Type 2 DPs. The addressing scheme defines the order in which the cells from the TIs for each of the Type 2 DPs are allocated to the active data cells. It is also used to signal the locations of the DPs in the dynamic part of the PLS2.

[409] Three slightly different cases are possible as shown in (b). For the first case shown on the left side of (b), cells in the last FSS are available for Type 2 DP mapping. For the second case shown in the middle, FIC occupies cells of a normal symbol, but the number of FIC cells on that symbol is not larger than C_{FSS}. The third case, shown on the right side in (b), is the same as the second case except that the number of FIC cells mapped on that symbol exceeds C_{FSS}.

[410] The extension to the case where Type 1 DP(s) precede Type 2 DP(s) is straightforward since PLS, EAC and FIC follow the same "Type 1 mapping rule" as the Type 1 DP(s).

[411] A data pipe unit (DPU) is a basic unit for allocating data cells to a DP in a frame.

[412] A DPU is defined as a signaling unit for locating DPs in a frame. A cell Mapper 7010 may map the cells produced by the TIs for each of the DPs. A Time interleaver 5050 outputs a series of TI-blocks and each TI-block comprises a variable number of XFECBLOCKs which is in turn composed of a set of cells. The number of cells in an XFECBLOCK, N_{cells}, is dependent on the FECBLOCK size, N_{ldpc}, and the number of transmitted bits per constellation symbol. A DPU is defined as the greatest common divisor of all possible values of the number of cells in a XFECBLOCK, N_{cells}, supported in a given PHY profile. The length of a DPU in cells is defined as L_{DPU}. Since each PHY profile supports different combinations of FECBLOCK size and a

different number of bits per constellation symbol, L_{DPU} is defined on a PHY profile basis.

[413] FIG. 22 illustrates an FEC structure according to an embodiment of the present invention.

[414] FIG. 22 illustrates an FEC structure according to an embodiment of the present invention before bit interleaving. As above mentioned, Data FEC encoder may perform the FEC encoding on the input BBF to generate FECBLOCK procedure using outer coding (BCH), and inner coding (LDPC). The illustrated FEC structure corresponds to the FECBLOCK. Also, the FECBLOCK and the FEC structure have same value corresponding to a length of LDPC codeword.

[415] The BCH encoding is applied to each BBF (K_{bch} bits), and then LDPC encoding is applied to BCH-encoded BBF (K_{ldpc} bits = N_{bch} bits) as illustrated in FIG. 22.

[416] The value of N_{ldpc} is either 64800 bits (long FECBLOCK) or 16200 bits (short FECBLOCK).

[417] The below table 28 and table 29 show FEC encoding parameters for a long FECBLOCK and a short FECBLOCK, respectively.

[418] Table 28

[Table 28]

LDPC Rate	N_{ldpc}	K_{ldpc}	K_{bch}	BCH error correction capability	N_{bch}-K_{bch}
5/15	64800	21600	21408	12	192
6/15		25920	25728		
7/15		30240	30048		
8/15		34560	34368		
9/15		38880	38688		
10/15		43200	43008		
11/15		47520	47328		
12/15		51840	51648		
13/15		56160	55968		

[419] Table 29

[Table 29]

LDPC Rate	N_{ldpc}	K_{ldpc}	K_{bch}	BCH error correction capability	N_{bch}-K_{bch}
5/15	16200	5400	5232	12	168
6/15		6480	6312		
7/15		7560	7392		
8/15		8640	8472		
9/15		9720	9552		
10/15		10800	10632		
11/15		11880	11712		
12/15		12960	12792		
13/15		14040	13872		

[420] The details of operations of the BCH encoding and LDPC encoding are as follows:

[421] A 12-error correcting BCH code is used for outer encoding of the BBF. The BCH generator polynomial for short FECBLOCK and long FECBLOCK are obtained by multiplying together all polynomials.

[422] LDPC code is used to encode the output of the outer BCH encoding. To generate a completed B_{ldpc} (FECBLOCK), P_{ldpc} (parity bits) is encoded systematically from each I_{ldpc} (BCH-encoded BBF), and appended to I_{ldpc}. The completed B_{ldpc} (FECBLOCK) are expressed as follow Math figure.

[423] MathFigure 3

[Math.3]

$$B_{ldpc} = [\mathbf{I}_{ldpc} \ \mathbf{P}_{ldpc}] = [i_0, i_1, \ldots, i_{K_{ldpc}-1}, \ p_0, p_1, \ldots, p_{N_{ldpc}-K_{ldpc}-1}]$$

[424] The parameters for long FECBLOCK and short FECBLOCK are given in the above table 28 and 29, respectively.

[425] The detailed procedure to calculate N_{ldpc} - K_{ldpc} parity bits for long FECBLOCK, is as follows:

[426] 1) Initialize the parity bits,

[427] MathFigure 4

[Math.4]

$$p_0 = p_1 = p_2 = \ldots = p_{N_{ldpc}-K_{ldpc}-1} = 0$$

[428] 2) Accumulate the first information bit - i0, at parity bit addresses specified in the first row of an addresses of parity check matrix. The details of addresses of parity check matrix will be described later. For example, for rate 13/15:

[429] MathFigure 5

[Math.5]

$$p_{983} = p_{983} \oplus i_0 \qquad p_{2815} = p_{2815} \oplus i_0$$

$$p_{4837} = p_{4837} \oplus i_0 \qquad p_{4989} = p_{4989} \oplus i_0$$

$$p_{6138} = p_{6138} \oplus i_0 \qquad p_{6458} = p_{6458} \oplus i_0$$

$$p_{6921} = p_{6921} \oplus i_0 \qquad p_{6974} = p_{6974} \oplus i_0$$

$$p_{7572} = p_{7572} \oplus i_0 \qquad p_{8260} = p_{8260} \oplus i_0$$

$$p_{8496} = p_{8496} \oplus i_0$$

[430] 3) For the next 359 information bits, i_s, s=1, 2, …, 359 accumulate is at parity bit addresses using following Math figure.

[431] MathFigure 6

[Math.6]

$$\{x + (s \mod 360) \times Q_{ldpc}\} \bmod (N_{ldpc} - K_{ldpc})$$

[432] where x denotes the address of the parity bit accumulator corresponding to the first bit i0, and Q_{ldpc} is a code rate dependent constant specified in the addresses of parity check matrix. Continuing with the example, Q_{ldpc} = 24 for rate 13/15, so for information bit i1, the following operations are performed:

[433] MathFigure 7

[Math.7]

$$p_{1007} = p_{1007} \oplus i_1 \qquad p_{2839} = p_{2839} \oplus i_1$$

$$p_{4861} = p_{4861} \oplus i_1 \qquad p_{5013} = p_{5013} \oplus i_1$$

$$p_{6162} = p_{6162} \oplus i_1 \qquad p_{6482} = p_{6482} \oplus i_1$$

$$p_{6945} = p_{6945} \oplus i_1 \qquad p_{6998} = p_{6998} \oplus i_1$$

$$p_{7596} = p_{7596} \oplus i_1 \qquad p_{8284} = p_{8284} \oplus i_1$$

$$p_{8520} = p_{8520} \oplus i_1$$

[434] 4) For the 361st information bit i_{360}, the addresses of the parity bit accumulators are given in the second row of the addresses of parity check matrix. In a similar manner the addresses of the parity bit accumulators for the following 359 information bits i_s, s= 361, 362, …, 719 are obtained using the Math figure 6, where x denotes the address of the parity bit accumulator corresponding to the information bit i_{360}, i.e., the entries in the second row of the addresses of parity check matrix.

[435] 5) In a similar manner, for every group of 360 new information bits, a new row from addresses of parity check matrixes used to find the addresses of the parity bit accu-

mulators.

[436] After all of the information bits are exhausted, the final parity bits are obtained as follows:

[437] 6) Sequentially perform the following operations starting with i=1

[438] MathFigure 8

[Math.8]

$$p_i = p_i \oplus p_{i-1}, \qquad i = 1,2,\ldots, N_{ldpc} - K_{ldpc} - 1$$

[439] where final content of pi, i=0,1,...N_{ldpc} - K_{ldpc} - 1 is equal to the parity bit p_i.

[440] Table 30

[Table 30]

Code Rate	Q_{ldpc}
5/15	120
6/15	108
7/15	96
8/15	84
9/15	72
10/15	60
11/15	48
12/15	36
13/15	24

[441] This LDPC encoding procedure for a short FECBLOCK is in accordance with t LDPC encoding procedure for the long FECBLOCK, except replacing the table 30 with table 31, and replacing the addresses of parity check matrix for the long FECBLOCK with the addresses of parity check matrix for the short FECBLOCK.

[442] Table 31

[Table 31]

Code Rate	Q_{ldpc}
5/15	30
6/15	27
7/15	24
8/15	21
9/15	18
10/15	15
11/15	12
12/15	9
13/15	6

[443] FIG. 23 illustrates a bit interleaving according to an embodiment of the present invention.

[444] The outputs of the LDPC encoder are bit-interleaved, which consists of parity interleaving followed by Quasi-Cyclic Block (QCB) interleaving and inner-group interleaving.

[445] shows Quasi-Cyclic Block (QCB) interleaving and (b) shows inner-group interleaving.

[446] The FECBLOCK may be parity interleaved. At the output of the parity interleaving, the LDPC codeword consists of 180 adjacent QC blocks in a long FECBLOCK and 45 adjacent QC blocks in a short FECBLOCK. Each QC block in either a long or short FECBLOCK consists of 360 bits. The parity interleaved LDPC codeword is interleaved by QCB interleaving. The unit of QCB interleaving is a QC block. The QC blocks at the output of parity interleaving are permutated by QCB interleaving as illustrated in FIG. 23, where N_{cells} =64800/ η_{mod} or 16200/ η_{mod} according to the FECBLOCK length. The QCB interleaving pattern is unique to each combination of modulation type and LDPC code rate.

[447] After QCB interleaving, inner-group interleaving is performed according to modulation type and order (η_{mod}) which is defined in the below table 32. The number of QC blocks for one inner-group, N_{QCB_IG}, is also defined.

[448] Table 32

[Table 32]

Modulation type	η_{mod}	N_{QCB_IG}
QAM-16	4	2
NUC-16	4	4
NUQ-64	6	3
NUC-64	6	6
NUQ-256	8	4
NUC-256	8	8
NUQ-1024	10	5
NUC-1024	10	10

[449] The inner-group interleaving process is performed with N_{QCB_IG} QC blocks of the QCB interleaving output. Inner-group interleaving has a process of writing and reading the bits of the inner-group using 360 columns and NQCB_IG rows. In the write operation, the bits from the QCB interleaving output are written row-wise. The read operation is performed column-wise to read out m bits from each row, where m is equal to 1 for NUC and 2 for NUQ.

[450] FIG. 24 illustrates a cell-word demultiplexing according to an embodiment of the present invention.

[451] (a) shows a cell-word demultiplexing for 8 and 12 bpcu MIMO and (b) shows a cell-word demultiplexing for 10 bpcu MIMO.

[452] Each cell word (c0,l, c1,l, …, c ηmod mod-1,l) of the bit interleaving output is demultiplexed into (d1,0,m, d1,1,m…, d1, ηmod mod-1,m) and (d2,0,m, d2,1,m…, d2, ηmod mod-1,m) as shown in (a), which describes the cell-word de-multiplexing process for one XFECBLOCK.

[453] For the 10 bpcu MIMO case using different types of NUQ for MIMO encoding, the Bit Interleaver for NUQ-1024 is re-used. Each cell word (c0,l, c1,l, …, c9,l) of the Bit Interleaver output is demultiplexed into (d1,0,m, d1,1,m…, d1,3,m) and (d2,0,m, d2,1,m…, d2,5,m), as shown in (b).

[454] FIG. 25 illustrates a time interleaving according to an embodiment of the present invention.

[455] to (c) show examples of TI mode.

[456] The time interleaver operates at the DP level. The parameters of time interleaving

(TI) may be set differently for each DP.

[457] The following parameters, which appear in part of the PLS2-STAT data, configure the TI:

[458] DP_TI_TYPE (allowed values: 0 or 1): Represents the TI mode; '0' indicates the mode with multiple TI blocks (more than one TI block) per TI group. In this case, one TI group is directly mapped to one frame (no inter-frame interleaving). '1' indicates the mode with only one TI block per TI group. In this case, the TI block may be spread over more than one frame (inter-frame interleaving).

[459] DP_TI_LENGTH: If DP_TI_TYPE = '0', this parameter is the number of TI blocks NTI per TI group. For DP_TI_TYPE = '1', this parameter is the number of frames PI spread from one TI group.

[460] DP_NUM_BLOCK_MAX (allowed values: 0 to 1023): Represents the maximum number of XFECBLOCKs per TI group.

[461] DP_FRAME_INTERVAL (allowed values: 1, 2, 4, 8): Represents the number of the frames IJUMP between two successive frames carrying the same DP of a given PHY profile.

[462] DP_TI_BYPASS (allowed values: 0 or 1): If time interleaving is not used for a DP, this parameter is set to '1'. It is set to '0' if time interleaving is used.

[463] Additionally, the parameter DP_NUM_BLOCK from the PLS2-DYN data is used to represent the number of XFECBLOCKs carried by one TI group of the DP.

[464] When time interleaving is not used for a DP, the following TI group, time interleaving operation, and TI mode are not considered. However, the Delay Compensation block for the dynamic configuration information from the scheduler will still be required. In each DP, the XFECBLOCKs received from the SSD/MIMO encoding are grouped into TI groups. That is, each TI group is a set of an integer number of XFECBLOCKs and will contain a dynamically variable number of XFECBLOCKs. The number of XFECBLOCKs in the TI group of index n is denoted by $N_{xBLOCK_Group}(n)$ and is signaled as DP_NUM_BLOCK in the PLS2-DYN data. Note that $N_{xBLOCK_Group}(n)$ may vary from the minimum value of 0 to the maximum value $N_{xBLOCK_Group_MAX}$ (corresponding to DP_NUM_BLOCK_MAX) of which the largest value is 1023.

[465] Each TI group is either mapped directly onto one frame or spread over PI frames. Each TI group is also divided into more than one TI blocks(NTI), where each TI block corresponds to one usage of time interleaver memory. The TI blocks within the TI group may contain slightly different numbers of XFECBLOCKs. If the TI group is divided into multiple TI blocks, it is directly mapped to only one frame. There are three options for time interleaving (except the extra option of skipping the time interleaving) as shown in the below table 33.

[466] Table 33

[Table 33]

Modes	Descriptions
Option-1	Each TI group contains one TI block and is mapped directly to one frame as shown in (a). This option is signaled in the PLS2-STAT by DP_TI_TYPE='0' and DP_TI_LENGTH ='1'(N_{TI}=1).
Option-2	Each TI group contains one TI block and is mapped to more than one frame. (b) shows an example, where one TI group is mapped to two frames, i.e., DP_TI_LENGTH ='2' (P_I=2) and DP_FRAME_INTERVAL (I_{JUMP} = 2). This provides greater time diversity for low data-rate services. This option is signaled in the PLS2-STAT by DP_TI_TYPE ='1'.
Option-3	Each TI group is divided into multiple TI blocks and is mapped directly to one frame as shown in (c). Each TI block may use full TI memory, so as to provide the maximum bit-rate for a DP. This option is signaled in the PLS2-STAT signaling by DP_TI_TYPE='0' and DP_TI_LENGTH = N_{TI}, while P_I=1.

[467] In each DP, the TI memory stores the input XFECBLOCKs (output XFECBLOCKs from the SSD/MIMO encoding block). Assume that input XFECBLOCKs are defined as

[468] $$(d_{n,s,0,0},d_{n,s,0,1},\ldots,d_{n,s,0,N_{cells}-1},d_{n,s,1,0},\ldots,d_{n,s,1,N_{cells}-1},\ldots,d_{n,s,N_{xBLOCK_TI}(n,s)-1,0},\ldots,d_{n,s,N_{xBLOCK_TI}(n,s)-1,N_{cells}-1}),$$

[469] where $d_{n,s,r,q}$ is the q_{th} cell of the r^{th} XFECBLOCK in the s^{th} TI block of the n^{th} TI group and represents the outputs of SSD and MIMO encodings as follows

[470] $$d_{n,s,r,q}=\begin{cases} f_{n,s,r,q} & \text{, the output of SSD} \cdots \text{encoding} \\ g_{n,s,r,q} & \text{, the output of MIMO encoding} \end{cases}$$

[471] In addition, assume that output XFECBLOCKs from the time interleaver 5050 are defined as

[472] $$(h_{n,s,0},h_{n,s,1},\ldots,h_{n,s,i},\ldots,h_{n,s,N_{xBLOCK_TI}(n,s)\times N_{cells}-1})$$

[473] where $h_{n,s,i}$ is the i^{th} output cell (for $i=0,\ldots,N_{xBLOCK_TI}(n,s)\times N_{cells}-1$) in the s^{th} TI block of the n^{th} TI group.

[474] Typically, the time interleaver will also act as a buffer for DP data prior to the process of frame building. This is achieved by means of two memory banks for each DP. The first TI-block is written to the first bank. The second TI-block is written to the second bank while the first bank is being read from and so on.

[475] The TI is a twisted row-column block interleaver. For the s^{th} TI block of the n^{th} TI group, the number of rows N_r of a TI memory is equal to the number of cells N_{cell} , i.e., $N_r=N_{cell}$ while the number of columns N_c is equal to the number N_{xBLCOK_TI} (n,s).

[476] FIG. 26 shows a parity check matrix of a QC-IRA (quasi-cyclic irregular repeat accumulate) LDPC code.

[477] The above-described LDPC encoder may encode a parity of an LDPC encoding block using the parity check matrix.

[478] The parity check matrix according to the present invention is a parity check matrix of the QC-IRA LDPC code and may have the form of a quasi-cyclic matrix called an H matrix and be represented as Hqc.

[479] (a) shows a parity check matrix according to an embodiment of the present invention. As shown in (a), the parity check matrix is a matrix having a horizontal size of Qx(K+M) and a vertical size of QxM and may include an information part and a parity part. The information part may include a matrix having a horizontal size of QxK and a vertical size of QxM and the parity part may include a matrix having a horizontal size of QxM and a vertical size of QxM. In this case, an LDPC code rate corresponds to K/(K+M).

[480] The parity check matrix according to an embodiment of the present invention may include randomly distributed 1s and 0s and 1 may be referred to as an "edge". The position of 1 in the parity check matrix, that is, the position of each edge may be represented in the form of a circulant shifted identity matrix per submatrix having a horizontal size of Q and a vertical size of Q. That is, a submatrix can be represented as a QxQ circulant-shifted identity matrix including only 1 and 0. Specifically, the submatrix according to an embodiment of the present invention is represented as identity matrices Ix including I0, I1, I2, ˇI1…, which have different positions of 1s according to the number of circulant shifts. The number of submatrices according to an embodiment of the present invention may be (K+M)xM.

[481] (b) shows the circulant-shifted identity matrices Ix which represent submatrices according to an embodiment of the present invention.

[482] The subscript x of Ix indicates the number of circulant shifts of columns of a circulant-shifted identity matrix. That is, I1 represents an identify matrix in which columns are circulant-shifted once and I2 represents an identity matrix in which columns are circulant-shifted twice. IQ which is an identity matrix circulant-shifted Q times corresponding to the total number of columns, Q, may be the same matrix as I0 due to circulant characteristic thereof.

[483] I0+2 represents a submatrix corresponding to a combination of two circulant-shifted identity matrices. In this case, the submatrix corresponds to a combination of the identity matrix I0 and an identity matrix circulant-shifted twice.

[484] ˇI1 represents a circulant-shifted identity matrix in which the edge of the last column of the corresponding submatrix, that is, 1 has been removed while corresponding to the submatrix I1.

[485] The parity part of the parity check matrix of the QC-IRA LDPC code may include only submatrices I0 and ˇI1 and the position of submatrices I0 may be fixed. As shown in (a), submatrices I0 may be distributed in a diagonal direction in the parity part.

[486] An edge in the parity check matrix represents that the corresponding row (checksum node) and the corresponding column (variable node) are physically connected. In this case, the number of 1s included in each column (variable node) may be referred to as a degree and columns may have the same degree or different degrees. Accordingly, the number, positions and value x of identity matrices Ix that represent edges grouped per submatrix are important factors in determining QC-IRA LDPC encoding performance and unique values may be determined per code rate.

[487] (c) shows a base matrix of the parity check matrix according to an embodiment of the present invention. The base matrix represents only the number and positions of identity matrices Ix as specific numbers, ignoring the value x of Ix. As shown in (c), a base matrix may have a horizontal size of K+M and a vertical size of M and be represented as Hbase. When Ix is not a matrix corresponding to a combination of submatrices, the position of the corresponding submatrix may be represented as 1. When a submatrix is represented as I0+2, this submatrix is a matrix corresponding to a combination of two circulant-shifted identity matrices and thus the submatrix needs to be discriminated from a submatrix represented as one circulant-shifted identity matrix. In this case, the position of the submatrix may be represented as 2 which is the number of the combined circulant-shifted identity matrices. In the same manner, the position of a submatrix corresponding to a combination of N circulant-shifted identity matrices can be represented as N.

[488] FIG. 27 shows a process of encoding the QC-IRA LDPC code according to an embodiment of the present invention.

[489] The QC-IRA LDPC code may be encoded per submatrix, distinguished from conventional sequential encoding, to reduce processing complexity.

[490] (a) shows arrangement of a QC-IRA parity check matrix in a QC form. The QC-IRA parity check matrix may be divided into 6 regions A, B, C, D, E and T when arranged in the QC form. When a QxK information vector s, a parity vector p1 having a length of Q and a parity vector p2 having a length of Qx(M-1) are used, a codeword x can be represented as x={s, p1, p2}.

[491] When the efficient encoding math figure of Richardson is used, the codeword x can be obtained by directly acquiring p1 and p2 from the parity check matrix arranged in the QC form. The efficient encoding math figure of Richardson is as follows.

[492] MathFigure 9

[Math.9]

$$\phi = -ET^{-1}B + D$$

$$p_1^T = -\phi^{-1}(-ET^{-1}A + C)s^T$$

$$p_2^T = -T^{-1}(As^T + Bp_1^T)$$

[493] (b) shows matrices

$$\varphi$$

and

$$\varphi^{-1}$$

derived according to the efficient encoding math figure.

[494] As shown in (b),

$$\varphi^{-1}$$

can be represented as a left low triangular (sub) matrix. The parity vector p2 can be obtained by calculating s and p1 according to the above-described math figure. When the QC-IRA parity check matrix is encoded according to the efficient encoding math figure of Richardson, at least Q parity nodes can be simultaneously processed in parallel according to characteristics of a QxQ submatrix.

[495] FIGS. 28 to 31 illustrate a process of sequentially encoding the QC-IRA LDPC code according to an embodiment of the present invention. This sequentially encoding may correspond to the above mentioned LDPC encoding.

[496] FIG. 28 illustrates a parity check matrix permutation process according to an embodiment of the present invention.

[497] (a) shows a QC-IRA LDPC parity check matrix H1 arranged in QC form. As shown in (a), a parity part of the matrix H1 may include submatrices distributed in a stepped form, which corresponds to the above-described QC-IRA LDPC parity check matrix. To easily perform sequential encoding, rows and columns of the matrix H1 are moved such that the matrix H1 is modified into a matrix H2 according to an embodiment of the present invention.

[498] (b) shows the modified matrix H2. As shown in (b), a parity part of the matrix H2 may include a dual diagonal matrix. In this case, an applied row and column per-

mutation math figure is as follows.

[499] MathFigure 10

[Math.10]

$$r_y = (r_x \bmod Q)M + \lfloor r_x / Q \rfloor \quad \text{where} \quad r_x = 0, 1, 2, \ldots, QM - 1$$

$$c_y = \{((c_x - QK) \bmod Q\}M + \lfloor (c_x - QK) / Q \rfloor + QK \quad \text{where} \quad c_x = QK, QK + 1, \ldots, Q(K + M) - 1$$

[500] According to the above permutation math figure, the rx-th row of the matrix H1 can be moved to the ry-th row of the matrix H2 and the cx-th column of the matrix H1 can be moved to the cy-th column of the matrix H2. In this case, column permutation can be applied only to a parity processing period (QK≤cx≤Q(K+M)-1) and LDPC code characteristics can be maintained even if permutation is applied.

[501] FIG. 29 is a table showing addresses of parity check matrix according to an embodiment of the present invention.

[502] The table shown in FIG. 29 represents a parity check matrix (or matrix H) having a codeword length of 16200 and a code rate of 9/15. The table represents addresses of 1 in the parity check matrix. In this case, the table according to an embodiment of the present invention can be referred to as addresses of a parity check matrix.

[503] In the table of (a), i indicates the blocks generated when the length of the matrix H or codeword by the length of a submatrix. A submatrix according to an embodiment of the present invention is a 360x360 matrix having a codeword length of 16200, and thus the number of blocks can be 45 obtained by dividing 16200 by 360. The each block can be sequentially indicated from 0. Accordingly, i can have a value in the range of 0 to 44. Also, i can indicate information bit corresponding to first column in each block.

[504] (b) shows the positions (or addresses) of 1s (or edges) in the first column in each block.

[505] The matrix H can be represented as H(r,c) using all rows and columns thereof. The following math figure 11 is used to derive H(r,c).

[506] MathFigure 11

[Math.11]

$$r = \lfloor x(i,j) / Q \rfloor \times Q + (x(i,j) + m) \bmod Q$$

$$c = i \times Q + m$$

$$H(r,c) = \begin{cases} 0, & \text{if } r = 0 \text{ and } c = 16199 \\ 1, & \text{else} \end{cases}$$

$\lfloor x \rfloor$ the largest integer less than or equal to x

$j = 0, \ldots,$ length of x(i)

$m = 0, \ldots, Q - 1$

$Q = 360$

[507] In the math figure, X(i,j) represents the j-th value of the i-th line in the table. Specifically, x(0,0)=1, x(0,1)=158 and x(1,0)=1, which correspond to the positions of rows having 1 (or addresses of 1) corresponding to i-th line of the matrix H. In this case, maximum values of r and c can be 9719 and 16199, respectively.

[508] The performance of the LDPC code may depend on distribution of degrees of nodes

of the parity check matrix, the girth according to the positions of 1s or edges of the parity check matrix, cycle characteristic, connection between check nodes and variable nodes, etc. The matrix H shown optimizes node degree distribution in the case of the codeword of 16200, Q=360 and code rate=6/15 and optimizes the positions of 1s or edges under the condition of optimized degree distribution, Q and code rate.

[509] The matrix H configured according to the table has the above-described QC-IRA LDPC structure. Hqc can be obtained using H(r,c) derived using the math figure and a base matrix Hbase can be derived from Hqc.

[510] In addition, the matrix H according to an embodiment of the present invention may include a matrix H in a different from, which has the same degree distribution as the lengths of x(i) (or degrees of corresponding variable nodes) of the table shown in FIG. 4. Furthermore, when a transmitter performs encoding using the corresponding matrix H, the above-described efficient encoding for QC-IRA LDPC can be employed.

[511] Accordingly, a transmitting side can implement an encoder having high encoding performance, low complexity and high throughput and a receiving side can perform parallel decoding up to 360 level using Q and effectively design a receiver with high throughput using the proposed matrix H.

[512] The following table 34 shows degree distribution.

[513] Table 34

[Table 34]

Variable node degree	16	10	9	3	2
(# of variable node)/Q	3	2	3	19	18

[514] When i is 0 to 2, the numbers of 1s in the 0-th block to 2nd block are all 16. Accordingly, when the variable node degree is 16, the number of blocks having the same degree is represented as 3. When i corresponds to 27 to 44, the numbers of 1s in the twenty-seventh block to forty-fourth block are 2. Accordingly, when the variable node degree is 2, the number of blocks having the same degree is 18. As described above, since the parity part of the matrix H includes only submatrices represented as I0 diagonally distributed in a stepped form, the variable node degree is always 2. Hence, blocks having a variable node degree of 2 can be regarded as blocks corresponding to the parity part. The number of actual variable nodes corresponding to each variable

node degree can be obtained by multiplying the number of blocks shown in the table by Q of the submatrix.

[515] FIG. 30 is a table showing addresses of parity check matrix according to another embodiment of the present invention.

[516] The table shown in FIG. 30 shows the matrix H2 obtained by modifying the matrix H1.

[517] In sequential encoding, edges used in a parity processing period are typically represented by an math figure and thus the edges can be omitted from the table. That is, 27 blocks having a degree of 2 corresponding to the parity part are not represented in the table.

[518] Since the property of the matrix is maintained even if the matrix is modified, as described above, node degree characteristic, cycle, girth, connection between check nodes and variable nodes, etc. are maintained. Accordingly, the equal encoding performance can be obtained and sequential encoding can be performed using the matrix H2 according to the table.

[519] FIG. 31 illustrates a method for sequentially encoding the QC-IRA LDPC code according to an embodiment of the present invention.

[520] When the parity check matrix is modified into the matrix H2 through the above-described permutation process, sequential encoding can be performed through updating of each parity checksum using information bits of a codeword and checksum updating between parity checksums.

[521] As shown in FIG. 31, the codeword can be represented using QK information bits and QM parity checksums. The information bits can be represented as iz according to position and parity checksums can be represented as ps.

[522] A parity checksum update process through the information bits can be represented by the following math figure 12.

[523] MathFigure 12

[Math.12]

$$p_w = p_w \oplus i_z \quad \text{... (1)}$$

$$w = \{v + (z \bmod Q)M\} \bmod (QM) \quad \text{where } z = 0, 1, 2, \ldots, QK-1 \quad \text{... (2)}$$

[524] Here, iz represents a z-th information bit and pw denotes a parity checksum that needs to be updated using iz. Math figure (1) represents that parity checksum pw corresponding to the w-th row is updated through an XOR operation performed on the z-th information and parity checksum pw. According to math figure (2), the position of w is calculated using the above-described table representing the matrix H2. Here, v denotes a number corresponding to each row in the table representing the matrix H2. As

described above, a row in the table representing the matrix H2 corresponds to the position of a block generated when the length of the matrix H or codeword is divided by the submatrix length. Accordingly, the information processing period shown in FIG. 6 is divided by the submatrix length Q and then the numbers of rows corresponding to every Q-th iz are read. Upon completion of checksum update using the information bits of the information processing period, checksum update of the parity processing period can be performed. Checksum update of the parity processing period may be represented by the following math figure 13.

[525] MathFigure 13

[Math.13]

$$p_s = p_s \oplus p_{s-1} \quad \text{where } s = 1, 2, \ldots, QM - 1$$

[526] When S is 0, parity checksum corresponds to parity p0 and parity values from p1 to pQM-1 can be sequentially derived through XOR operations performed on the parity values and parity values immediately prior thereto.

[527] FIG. 32 illustrates an LDPC decoder according to an embodiment of the present invention.

[528] The LDPC decoder 700 according to an embodiment of the present invention may include a variable node update block 710, a check node update block 720, a barrel shift block 730 and a check sum block 740. Each block will now be described.

[529] The variable node block 710 may update each variable node of the matrix H using an input of the LDPC decoder and a message delivered through edges from the check node block.

[530] The check node block 720 may update a check node of the matrix H using a message transmitted through edges from a variable node. A node update algorithm according to an embodiment of the present invention may include sum product algorithm, belief-propagation algorithm, min-sum algorithm, modified min-sum algorithm, etc. and may be changed according to designer. In addition, since connection between variable nodes and check nodes is represented in the form of a QxQ circulant identity matrix due to characteristics of QC-IRA LDPC, Q messages between variable nodes and the check node block can be simultaneously processed in parallel. The barrel shift block 730 may control circulant connection.

[531] The check sum block 740 is an optional block which hard-decides a decoding message for each variable node update and performs parity checksum operation to reduce the number of decoding iterations necessary for error correction. In this case, the LDPC decoder 700 according to an embodiment of the present invention can output a final LDPC decoding output through soft decision even if the check sum block 740 hard-decides the decoding message.

[532] FIG. 33 is a flowchart illustrating a method for transmitting broadcast signals according to an embodiment of the present invention.

[533] The apparatus for transmitting broadcast signals according to an embodiment of the present invention can encode service data (S33000). As described above, service data is transmitted through a data pipe which is a logical channel in the physical layer that carries service data or related metadata, which may carry one or multiple service(s) or service component(s). Data carried on a data pipe can be referred to as the DP data or the service data. The detailed process of step S33000 is as described in FIGs. 1, 5, 22 to 26, 32.

[534] As described in FIG. 26 to 32, the apparatus for transmitting broadcast signals according to an embodiment of the present invention may encode a parity of an LDPC encoding block using the parity check matrix. Also, the FEC structure according to an embodiment of the present invention before bit interleaving by using the FEC encoding parameters for a long FECBLOCK and a short FECBLOCK.

[535] The apparatus for transmitting broadcast signals according to an embodiment of the present invention can build at least one signal frame including the encoded service data (S33010). The detailed process of step S33010 is as described in FIGs. 7, 10 to 11, 16 to 21.

[536] Then, the apparatus for transmitting broadcast signals according to an embodiment of the present invention can modulate data in the built at least one signal frame by an OFDM (Orthogonal Frequency Division Multiplexing) scheme (S33020). The detailed process of this step is as described in FIG 1 and FIG. 8.

[537] Subsequently, the apparatus for transmitting broadcast signals according to an embodiment of the present invention can transmit the broadcast signals including the modulated at least one signal frame (S33030). The detailed process of this step is as described in FIG. 1 and FIG. 8.

[538] FIG. 34 is a flowchart illustrating a method for receiving broadcast signals according to an embodiment of the present invention.

[539] The flowchart shown in FIG. 34 corresponds to a reverse process of the broadcast signal transmission method according to an embodiment of the present invention, described with reference to FIG. 33.

[540] The apparatus for receiving broadcast signals according to an embodiment of the present invention can receive the broadcast signals (S34000).

[541] The apparatus for receiving broadcast signals according to an embodiment of the present invention can demodulate received broadcast signals using an OFDM (Orthogonal Frequency Division Multiplexing) scheme (S34010). The detailed process of this step is as described in FIG. 9.

[542] The apparatus for receiving broadcast signals according to an embodiment of the

present invention can parse at least one signal frame from the demodulated broadcast signals (S34020). Details are as described in FIG. 9. Also, the signal frame according to an embodiment of the present invention have a structure described in FIGs 11 to 21.

[543] Subsequently, the apparatus for receiving broadcast signals according to an embodiment of the present invention can decode service data in the parsed at least one signal frame (S34030). Details are as described in FIG. 9. As described above, service data is transmitted through a data pipe which is a logical channel in the physical layer that carries service data or related metadata, which may carry one or multiple service(s) or service component(s). Data carried on a data pipe can be referred to as the DP data or the service data.

[544] FIG. 35 illustrates the basic operation of a twisted row-column block interleaver according to an embodiment of the present invention.

[545] shows a writing operation in the time interleaver and (b) shows a reading operation in the time interleaver The first XFECBLOCK is written column-wise into the first column of the TI memory, and the second XFECBLOCK is written into the next column, and so on as shown in (a). Then, in the interleaving array, cells are read out diagonal-wise. During diagonal-wise reading from the first row (rightwards along the row beginning with the left-most column) to the last row, cells are read out as shown in (b). In detail, assuming $Z_{n,s,i}$(i=0,,,,,,N_r,N_c) as the TI memory cell position to be read sequentially, the reading process in such an interleaving array is performed by calculating the row index $R_{n,s,i}$, the column index $C_{n,s,i}$, and the associated twisting parameter $T_{n,s,i}$ as follows math figure.

[546] MathFigure 14

[Math.14]

$$GENERATE(R_{n,s,i},C_{n,s,j})=$$
$$\{$$
$$R_{n,s,i}=\mathrm{mod}(i,N_r),$$
$$T_{n,s,i}=\mathrm{mod}(S_{shift}\times R_{n,s,i},N_c),$$
$$C_{n,s,i}=\mathrm{mod}(T_{n,s,i}+\left\lfloor\frac{i}{N_r}\right\rfloor,N_c)$$
$$\}$$

[547] where S_{shift} is a common shift value for the diagonal-wise reading process regardless of N_{xBLOCK_TI}(n,s), and it is determined by $N_{xBLOCK_TI_MAx}$ given in the PLS2-STAT as follows math figure.

[548] MathFigure 15

[Math.15]

$$for \begin{cases} N'_{xBLOCK_TI_MAX} = N_{xBLOCK_TI_MAX} + 1, & if\ N_{xBLOCK_TI_MAX} \bmod 2 = 0 \\ N'_{xBLOCK_TI_MAX} = N_{xBLOCK_TI_MAX}, & if\ N_{xBLOCK_TI_MAX} \bmod 2 = 1 \end{cases},$$

$$S_{shift} = \frac{N'_{xBLOCK_TI_MAX} - 1}{2}$$

[549] As a result, the cell positions to be read are calculated by a coordinate as $Z_{n,s,i} = N_r C_{n,s,i} + R_{n,s,i}$.

[550] FIG. 36 illustrates an operation of a twisted row-column block interleaver according to another embodiment of the present invention.

[551] More specifically, FIG. 36 illustrates the interleaving array in the TI memory for each TI group, including virtual XFECBLOCKs when $N_{xBLOCK_TI}(0,0) = 3$, $N_{xBLOCK_TI}(1,0) = 6$, $N_{xBLOCK_TI}(2,0) = 5$.

[552] The variable number $N_{xBLOCK_TI}(n,s) = N_r$, will be less than or equal to $N_{xBLOCK_TI_MAx}$. Thus, in order to achieve a single-memory deinterleaving at the receiver side, regardless of $N_{xBLOCK_TI}(n,s)$, the interleaving array for use in a twisted row-column block interleaver is set to the size of $N_r \times N_c = N_{cells} \times N_{xBLOCK_TI_MAx}$ by inserting the virtual XFECBLOCKs into the TI memory and the reading process is accomplished as follow math figure.

[553] MathFigure 16

[Math.16]

$$\begin{aligned}
&p = 0; \\
&for\ i = 0; i < N_{cells} N'_{xBLOCK_TI_MAX}; i = i + 1 \\
&\{GENERATE(R_{n,s,i}, C_{n,s,i}); \\
&V_i = N_r C_{n,s,j} + R_{n,s,j} \\
&\quad if\ V_i < N_{cells} N_{xBLOCK_TI}(n,s) \\
&\quad \{ \\
&\quad\ Z_{n,s,p} = V_i;\ p = p + 1; \\
&\quad \} \\
&\}
\end{aligned}$$

[554] The number of TI groups is set to 3. The option of time interleaver is signaled in the PLS2-STAT data by DP_TI_TYPE='0', DP_FRAME_INTERVAL='1', and DP_TI_LENGTH='1', i.e., $N_{TI} = 1$, $I_{JUMP} = 1$, and $P_I = 1$. The number of XFECBLOCKs, each of which has $N_{cells} = 30$, per TI group is signaled in the PLS2-DYN data by $N_{xBLOCK_TI}(0,0) = 3$, $N_{xBLOCK_TI}(1,0) = 6$, $N_{xBLOCK_TI}(2,0) = 5$, respectively. he maximum number of XFECBLOCK is signaled in the PLS2-STAT data by $N_{xBLOCK_Groyp_MAx}$, which leads to

$$\lfloor N_{xBLOCK_Group_MAX} / N_{TI} \rfloor = N_{xBLOCK_TI_MAX} = 6$$

.

[555] FIG. 37 illustrates a diagonal-wise reading pattern of a twisted row-column block interleaver according to an embodiment of the present invention.

[556] More specifically FIG. 37 shows a diagonal-wise reading pattern from each interleaving array with parameters of $N_{xBLOCK_TI_MAX} = 7$ and $S_{shift} = (7-1)/2 = 3$. Note that in the reading process shown as pseudocode above, if $V_i \geq N_{cells} N_{xBLOCK_TI}(n,s)$, the value of V_i is skipped and the next calculated value of V_i is used.

[557] FIG. 38 illustrates interlaved XFECBLOCKs from each interleaving array according to an embodiment of the present invention.

[558] FIG. 38 illustrates the interleaved XFECBLOCKs from each interleaving array with parameters of $N_{xBLOCK_TI_MAX} = 7$ and $S_{shift} = 3$.

[559] FIG. 39 is a table showing addresses of parity check matrix according to another embodiment of the present invention.

[560] The table shown in FIG. 39 represents a parity check matrix (or matrix H) having a codeword length of 16200 and a code rate of 8/15. The details of the table are equal to the details described in FIG. 29.The following table shows degree distribution.

[561] Table 35

[Table 35]

Variable node degree	16	10	9	3	2
(# of variable node)/Q	3	5	13	19	18

[562] When i is 0 to 2, the numbers of 1s in the 0-th block to 2-nd block are all 16. Accordingly, when the variable node degree is 16, the number of blocks having the same degree is represented as 3. When i corresponds to 3 to 7, the numbers of 1s in the third block to seventh block are 10. Accordingly, when the variable node degree is 10, the number of blocks having the same degree is 5. As described above, since the parity part of the matrix H includes only submatrices represented as I0 diagonally distributed in a stepped form, the variable node degree is always 2. Hence, blocks having a variable node degree of 2 can be regarded as blocks corresponding to the parity part. The number of actual variable nodes corresponding to each variable node degree can be obtained by multiplying the number of blocks shown in the table by Q of the submatrix.

[563] FIG. 40 is a table showing addresses of parity check matrix according to another embodiment of the present invention.

[564] The table shown in FIG. 40 shows the matrix H2 obtained by modifying the matrix H1.

[565] In sequential encoding, edges used in a parity processing period are typically represented by an equation and thus the edges can be omitted from the table. That is, 18 blocks having a degree of 2 corresponding to the parity part are not represented in the table.

[566] Since the property of the matrix is maintained even if the matrix is modified, as described above, node degree characteristic, cycle, girth, connection between check nodes and variable nodes, etc. are maintained. Accordingly, the equal encoding performance can be obtained and sequential encoding can be performed using the matrix H2 according to the table.

[567] Two-dimensional enhanced SFN (2D-eSFN) processing:

[568] The system supports the SFN network, where distributed MISO scheme is optionally used to support very robust transmission mode. The 2D-eSFN is a distributed MISO scheme that uses multiple TX antennas, each of which is located in the different transmitter site in the SFN network.

[569] In the SFN configuration, the 2D-eSFN processing independently distorts the phase of the signals transmitted from multiple transmitters, in order to create both time and frequency diversity. Hence, burst errors due to low flat fading or deep-fading for a long time can be mitigated. The time-frequency dimensional phase-distorted signals are given by

[570] $$r_{m,l,k} = q_{m,l,k}\Psi(l,k)$$

[571] wherein $q_{m,l,k}$ and $r_{m,l,k}$ are the inptu and ouput signals of 2D-esfn processing, respectively.

[572] $\Psi(l,k)$ denotes a phase-distortion value for the kth carrier of the lth symbol and is defined as $\Psi(l,k) = e^{j\theta_t(l)} \times e^{j\theta_f(k)}$,

[573] where $\theta_t(l)$ and $\theta_f(k)$ indicate the time- and frequency-dimensional phase terms, respectively.

[574] The time-dimensional phase term $\theta_t(l)$ for the lth symbol carrier (for) is calculated as following math figure.

[575] MathFigure 17

[Math.17]

$$\theta_t(l) = \theta_{base} + \frac{1}{2}\theta_{\text{var}}\left(1 - \cos\left(\frac{2\pi l}{N_R} + \varepsilon_{offset}\right)\right)$$

[576] where

$$\theta_{base} \in [0, 2\pi)$$

is a base phase [radian],

$$\theta_{\text{var}} \in [0, 2\pi)$$

is the amount of phase variation, and N_R determines a resolution value of the sinusoidal wave.

$$\varepsilon_{offset} \in [0, 2\pi)$$

denotes a phase offset for different transmitter.

[577] The frequency-dimensional phase term

$$\theta_f(k)$$

for the kth carrier (for $K_{min} \leq k \leq K_{max}$) is calculated as following math figure.

[578] MathFigure 18

[Math.18]

$$m = \left\lfloor \frac{k}{b} \right\rfloor, \quad p = \left\lfloor \frac{k + b/2}{b} \right\rfloor,$$

$$q = b \cdot m + b/2,$$

$$k' = k - (q - a),$$

$$\theta_f(k) = \begin{cases} \varphi(p) + \dfrac{\varphi(p+1) - \varphi(p)}{2a}(k' \bmod (2a)), & if\ (q-a) \leq k \leq (q+a) \\ \varphi(p) & else \end{cases}$$

[579] where the parameters a and b are set to a =128 and b= 512, respectively. The phase term

$$\varphi(p) \quad (p = 0, \ldots, L-1)$$

is recursively defined as

[580] $$\varphi(p)=\begin{cases} TxID_0(0)\cdot 2\pi/3, & if\ \ p=0 \\ \varphi(p-1)+TxID_0(p)\cdot \pi/4, & else \end{cases},$$

[581] where the values

$$TxID_0(p)\in\{-1,0,1\}$$

of the basic TxID identify each transmitter within the network and are defined within one frame. Note that the exchange of TxID every frame also causes a time-dimensional phase variation. The exchange of TxID in each frame will be performed by applying the left circular shift or right circular shift method to

$$TxID_0(p)$$

:

[582] $$TxID_m(p)=\begin{cases} TxID_0((p+mJ)\bmod L) & :\text{left circular shift} \\ TxID_0((p-mJ)\bmod L) & :\text{right circular shift} \end{cases}$$

[583] where the index m denotes the mth frame and J.is an integer factor controlling the shifting value mJ. Note that if only one transmitter identification sequence in the network is used, it consists of zeros, i.e,

$$TxID_0=\{0,\ldots,0\}$$

.

[584] It will be appreciated by those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

[585] Both apparatus and method inventions are mentioned in this specification and descriptions of both of the apparatus and method inventions may be complementarily applicable to each other.

Mode for the Invention

[586] Various embodiments have been described in the best mode for carrying out the invention.

Industrial Applicability

[587] The present invention is available in a series of broadcast signal provision fields.

[588] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Claims

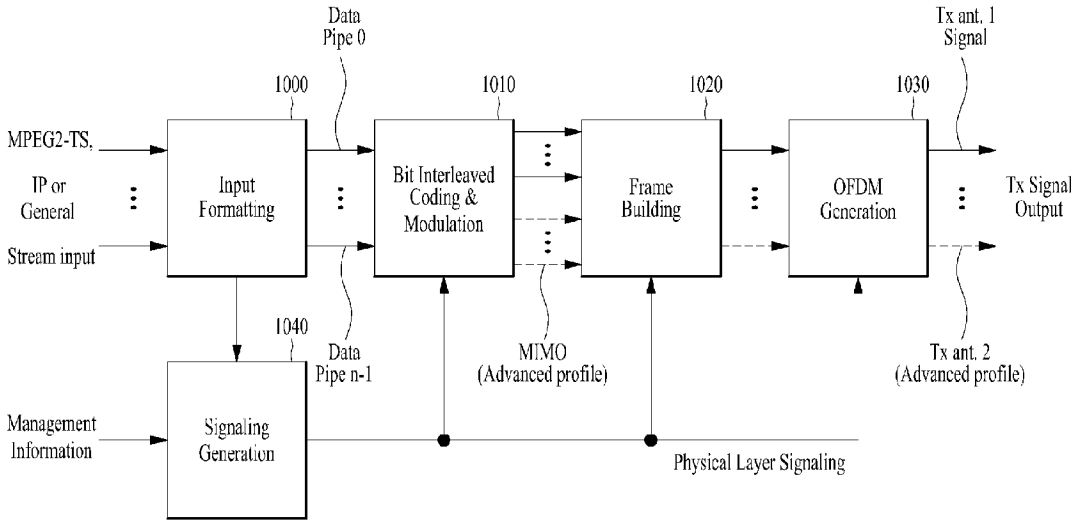
[Claim 1] A method of transmitting broadcast signals, the method including:
encoding service data;
building at least one signal frame by mapping the encoded service data;
modulating data in the built at least one signal frame by an Orthogonal Frequency Division Multiplexing, OFDM, scheme; and
transmitting the broadcast signals having the modulated data.

[Claim 2] The method of claim 1,
wherein the encoding is processed according to a code rate to output an FEC frame corresponding to a codeword, wherein the codeword have information bits and parity bits, wherein the parity bits are calculated using the information bits based on addresses of a parity check matrix, wherein the addresses of the parity check matrix indicate addresses of the parity bits to be calculated.

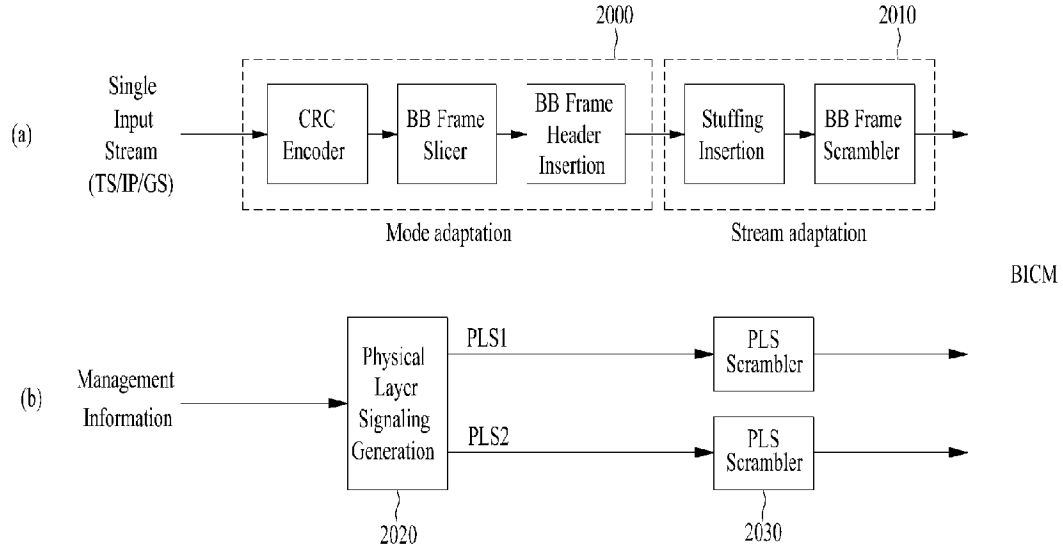
[Claim 3] A method of receiving broadcast signals, the method including:
receiving the broadcast signals;
demodulating the received broadcast signals by an Orthogonal Frequency Division Multiplexing, OFDM, scheme;
parsing at least one signal frame from the demodulated broadcast signals; and
decoding data in the parsed at least one signal frame to output service data.

[Claim 4] The method of claim 3,
wherein the decoding is processed according to code rate and a codeword, wherein the codeword have information bits and parity bits, wherein the parity bits are calculated using the information bits based on addresses of a parity check matrix, wherein the addresses of the parity check matrix indicate addresses of the calculated parity bits.

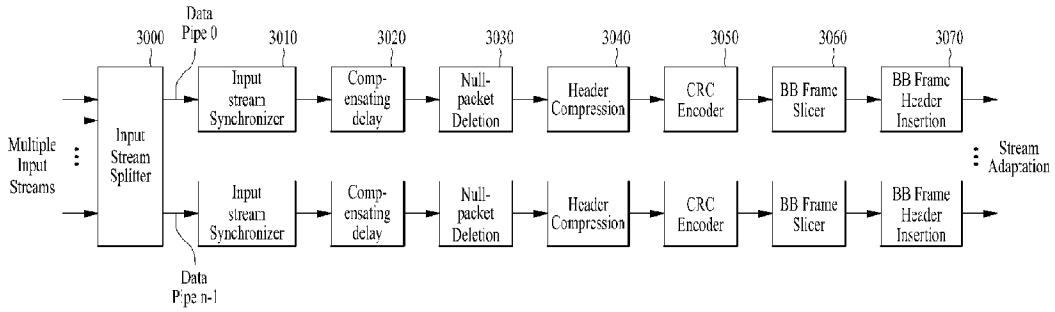
[Fig. 1]



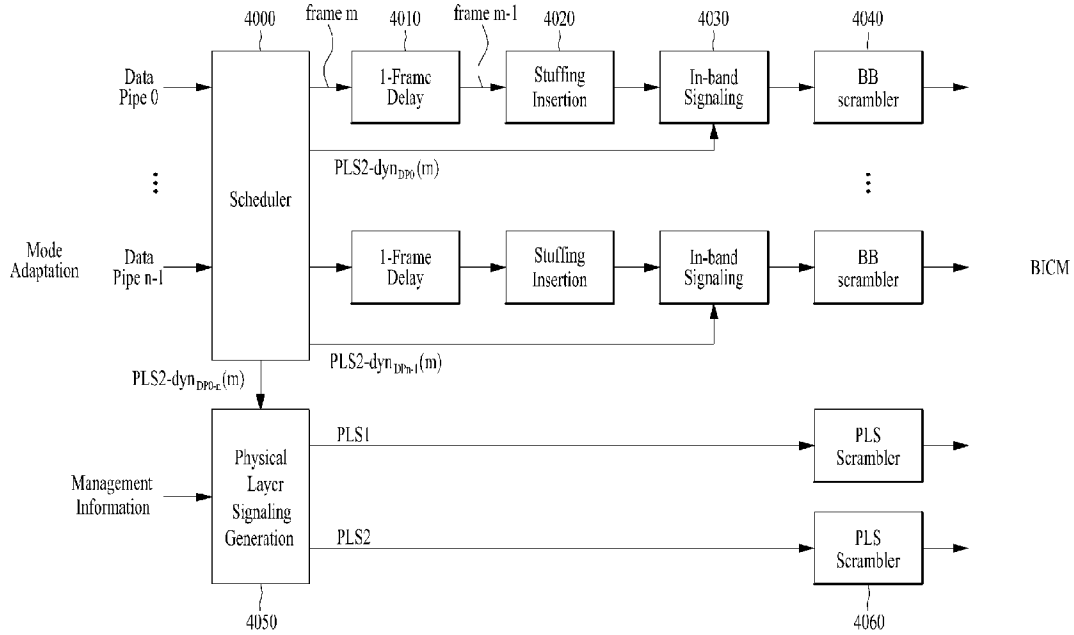
[Fig. 2]



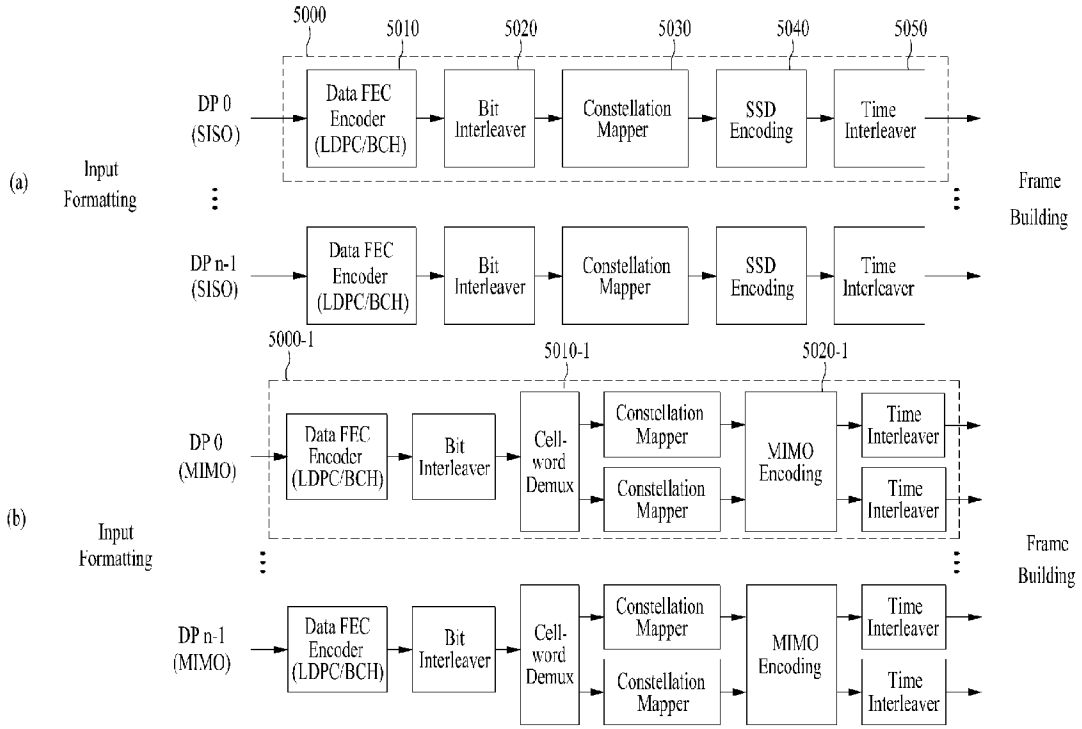
[Fig. 3]



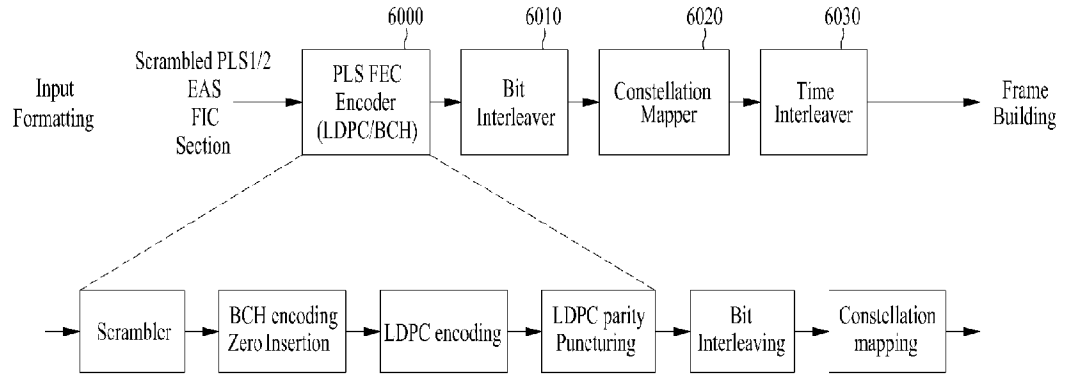
[Fig. 4]



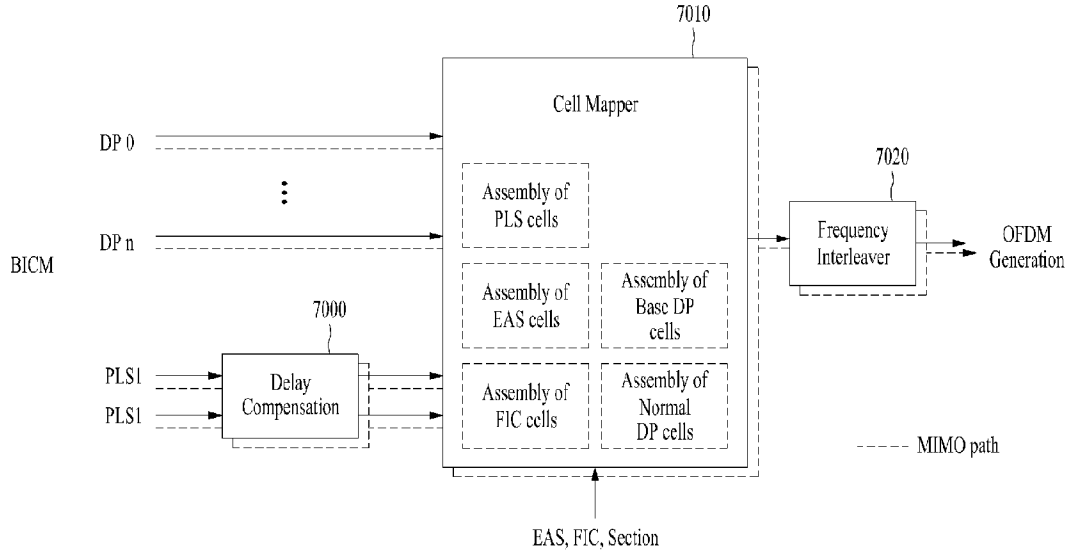
[Fig. 5]



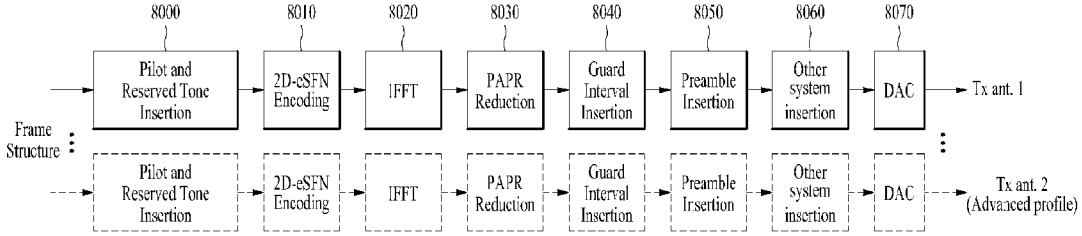
[Fig. 6]



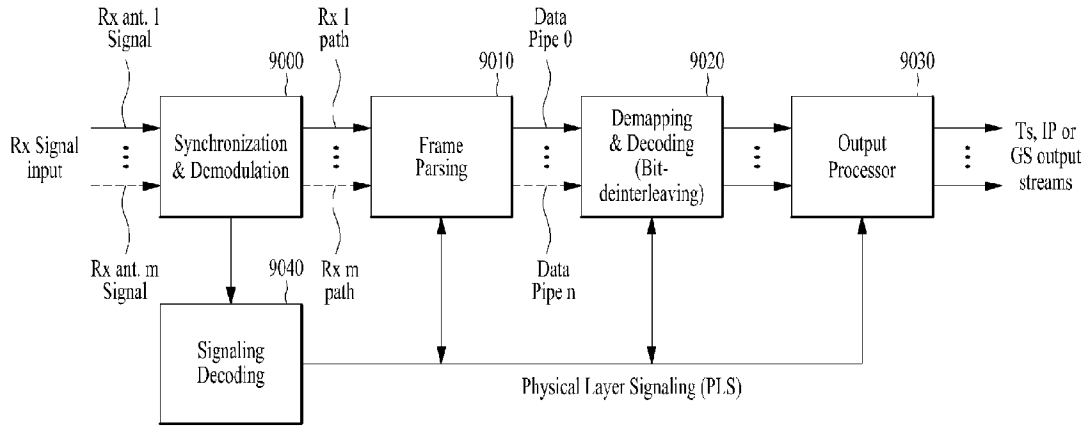
[Fig. 7]



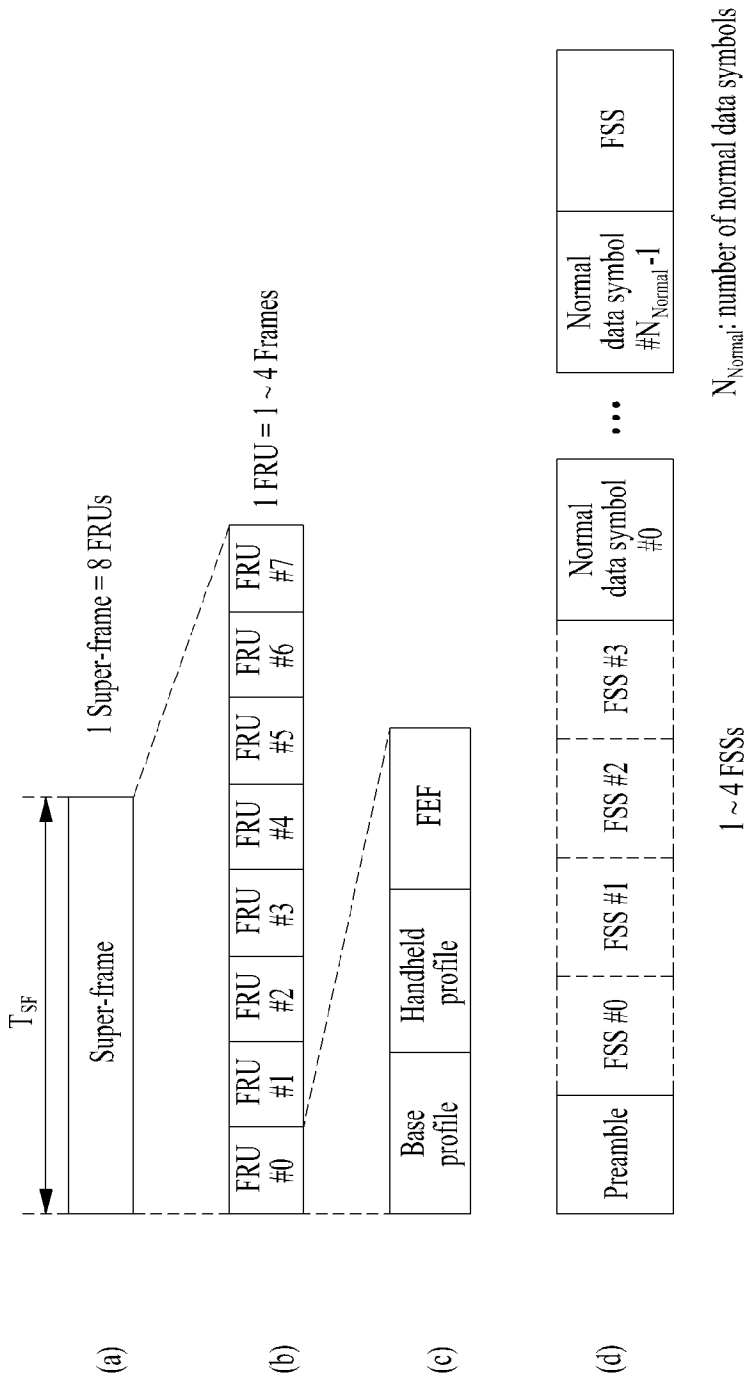
[Fig. 8]



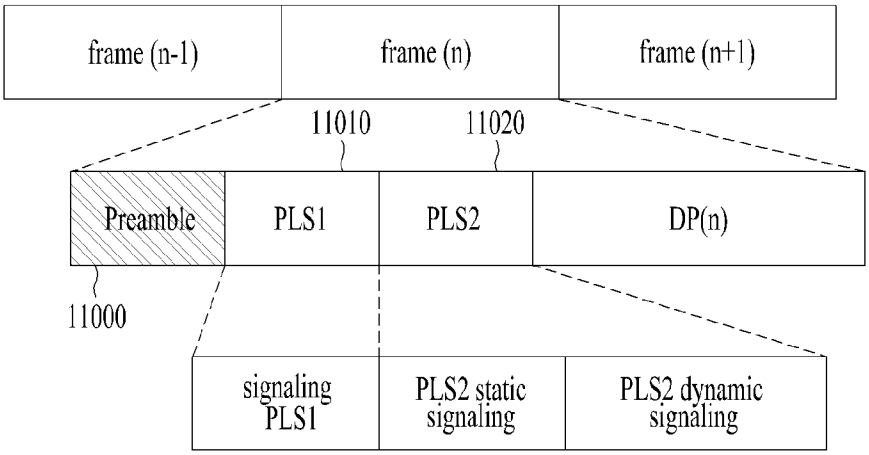
[Fig. 9]



[Fig. 10]


(a)
T_{SF}
Super-frame
1 Super-frame = 8 FRUs
(b)
FRU #0
FRU #1
FRU #2
FRU #3
FRU #4
FRU #5
FRU #6
FRU #7
1 FRU = 1 ~ 4 Frames
(c)
Base profile
Handheld profile
FEF
(d)
Preamble
FSS #0
FSS #1
FSS #2
FSS #3
Normal data symbol #0
Normal data symbol #N_{Normal}-1
FSS
1 ~ 4 FSSs
N_{Normal}: number of normal data symbols

[Fig. 11]



[Fig. 12]

Content	Bits
PHY_PROFILE	3
FFT_SIZE	2
GI_FRACTION	3
EAC_FLAG	1
PILOT_MODE	1
PAPR_FLAG	1
FRU_CONFIGURE	3
RESERVED	7

[Fig. 13]

Content	Bits
PREAMBLE_DATA	20
NUM_FRAME_FRU	2
PAYLOAD_TYPE	3
NUM_FSS	2
SYSTEM_VERSION	8
CELL_ID	16
NETWORK_ID	16
SYSTEM_ID	16
for i = 0:3	
FRU_PHY_PROFILE	3
FRU_FRAME_LENGTH	2
FRU_GI_FRACTION	3
RESERVED	4
end	
PLS2_FEC_TYPE	2
PLS2_MOD	3
PLS2_SIZE_CELL	15
PLS2_STAT_SIZE_BIT	14
PLS2_SYN_SIZE_BIT	14
PLS2_REP_FLAG	1
PLS2_REP_SIZE_CELL	15
PLS2_NEXT_FEC_TYPE	2
PLS2_NEXT_MODE	3
PLS2_NEXT_REP_FLAG	1
PLS2_NEXT_REP_SIZE_CELL	15
PLS2_NEXT_REP_STAT_SIZE_BIT	14
PLS2_NEXT_REP_DYN_SIZE_BIT	14
PLS2_AP_MODE	2
PLS2_AP_SIZE_CELL	15
PLS2_NEXT_AP_MODE	2
PLS2_NEXT_AP_SIZE_CELL	15
RESERVED	32
CRC 32	32

[Fig. 14]

Content	Bits
FIC_FLAG	1
AUX_FLAG	1
NUM_DP	6
for i = 1: NUM_DP	
DP_ID	6
DP_TYPE	3
DP_GROUP_ID	8
BASE_DP_ID	6
DP_FEC_TYPE	2
DP_COD	4
DP_MOD	4
DP_SSD_FLAG	1
if PHY_PROFILE = '010'	
DP_MIMO	3
end	
DP_TI_TYPE	1
DP_TI_LENGTH	2
DP_TI_BYPASS	1
DP_FRAME_INTERVAL	2
DP_FIRST_FRAME_IDX	5
DP_NUM_BLOCK_MAX	10
DP_PAYLOAD_TYPE	2
DP_INBAND_MODE	2
DP_PROTOCOL_TYPE	2
DP_CRC_MODE	2
if DP_PAYLOAD_TYPE = = TS('00')	
DNP_MODE	2
ISSY_MODE	2
HC_MODE_TS	2
if HC_MODE_TS = = '01' or '10'	
PID	13
end	
if DP_PAYLOAD_TYPE == IP('01')	
HC_MODE_IP	2
end	
RESERVED	8
end	
if FIC_FLAG = = 1	
FIC_VERSION	8
FIC_LENGTH_BYTE	13
RESERVED	8
end	
if AUX_FLAG = = 1	
NUM_AUX	4
AUX_CONFIG_RFU	8
for - 1 : NUM_AUX	
AUX_STREAM_TYPE	4
AUX_PRIVATE_CONF	28
end	
end	

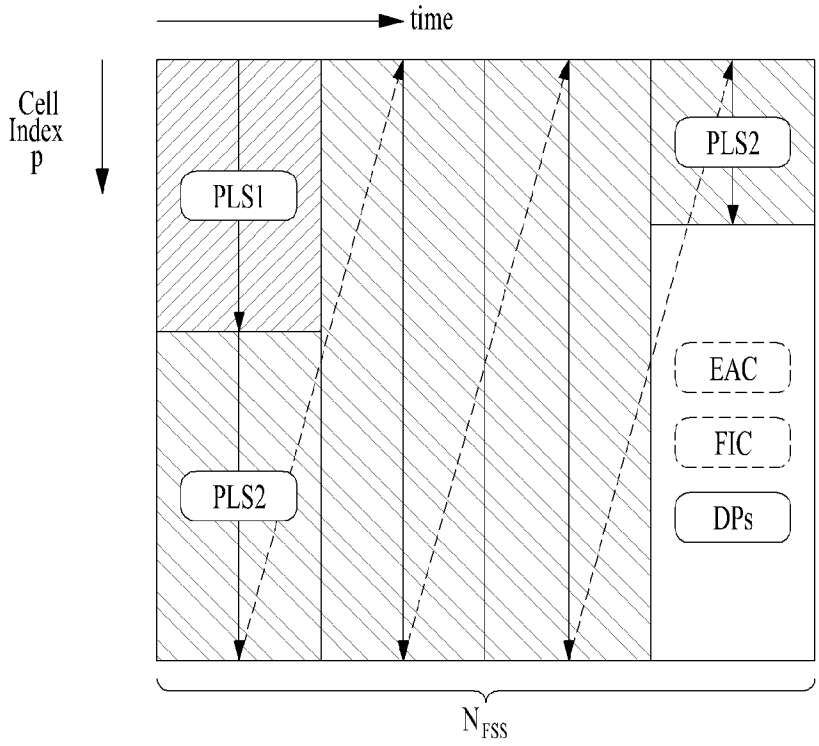
[Fig. 15]

Content		Bit
FRAME_INDEX		5
PLS_CHANGE_COUNTER		4
FIC_CHANGE_COUNTER		4
RESERVED		16
for i = 1: NUM_DP		
	DP_ID DP_START	6 15 (or13)
	DP_NUM_BLOCK	10
end	RESERVED	8
EAC_FLAG		1
EAS_WAKE_UP_VERSION_NUM		8
if EAC_FLAG == 1		
	EAC_LENGTH_BYTE	12
else		
	EAC_COUNTER	12
end		
for i=1:NUM_AUX		
	AUX_PRIVATE_DYN	48
end		
CRC 32		32

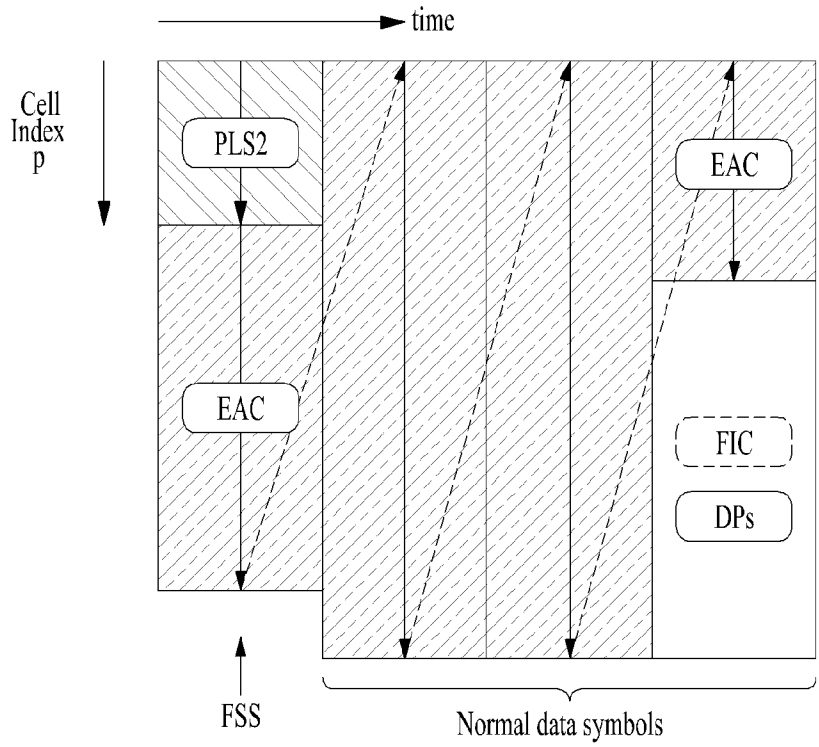
[Fig. 16]



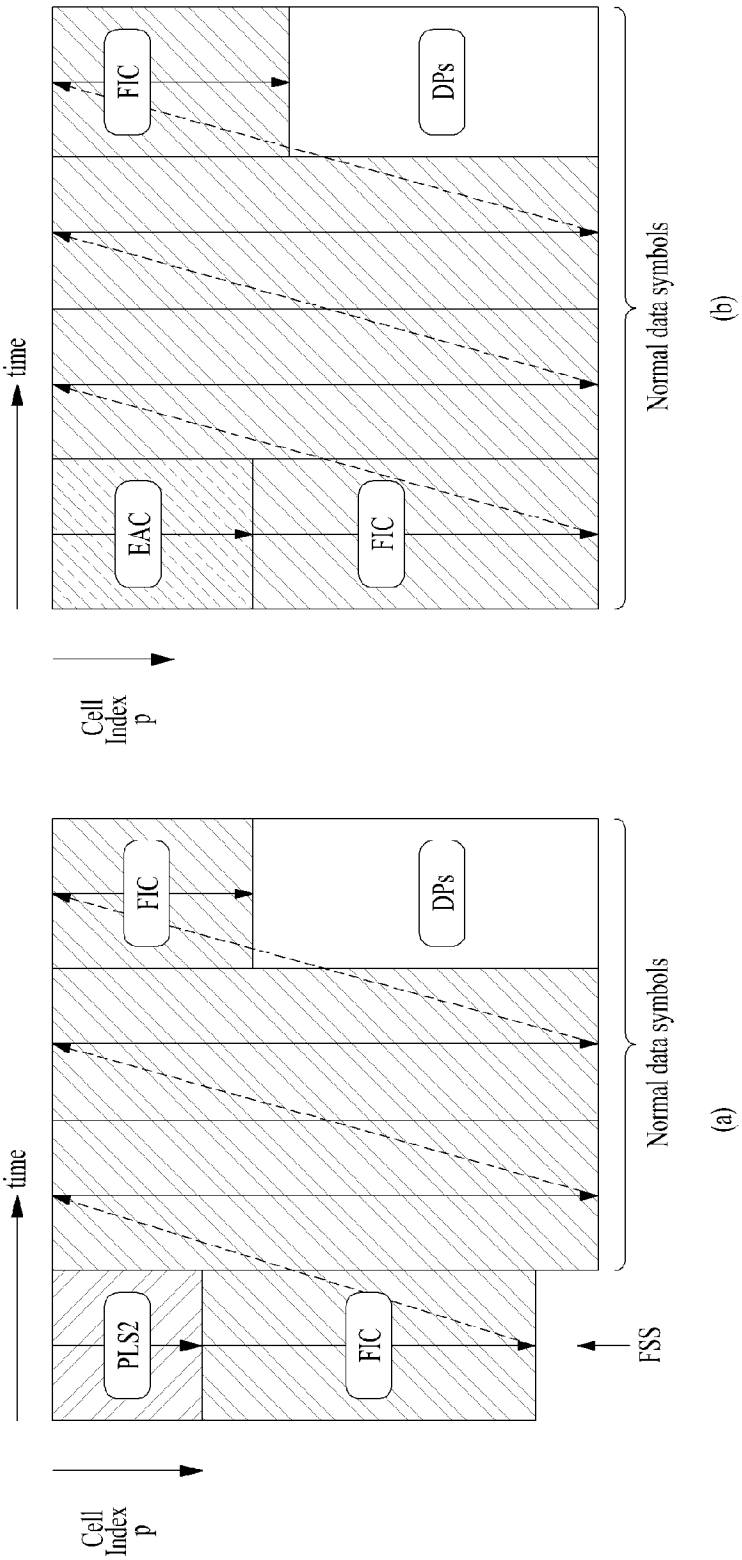
[Fig. 17]


time
Cell Index p
PLS1
PLS2
PLS2
EAC
FIC
DPs
N_{FSS}

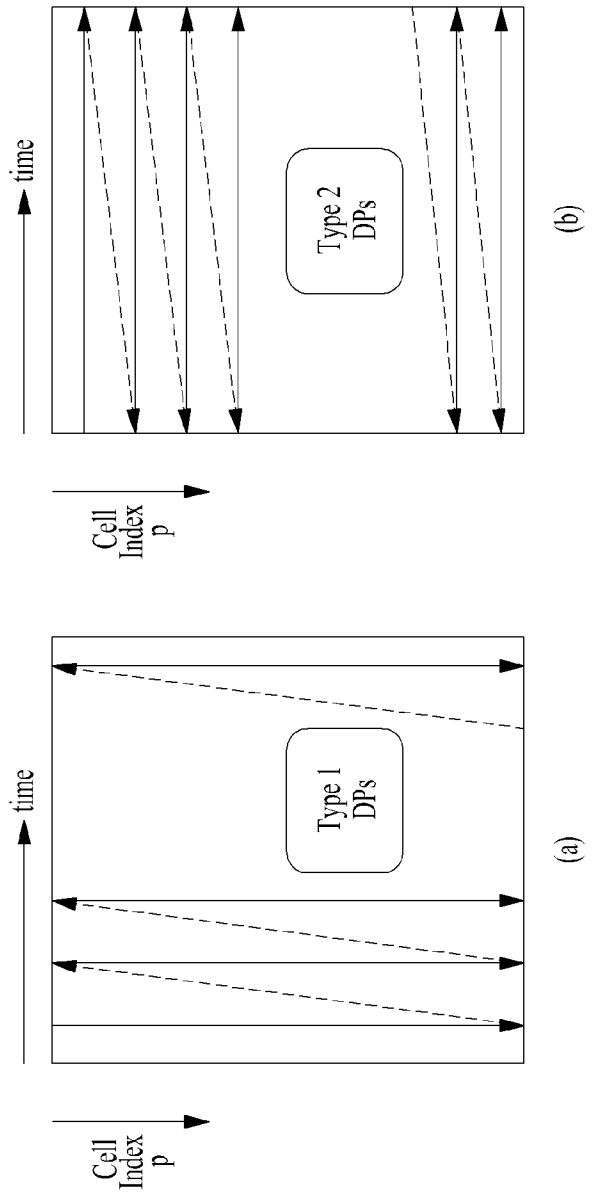
[Fig. 18]


time
Cell Index p
PLS2
EAC
EAC
FIC
DPs
FSS
Normal data symbols

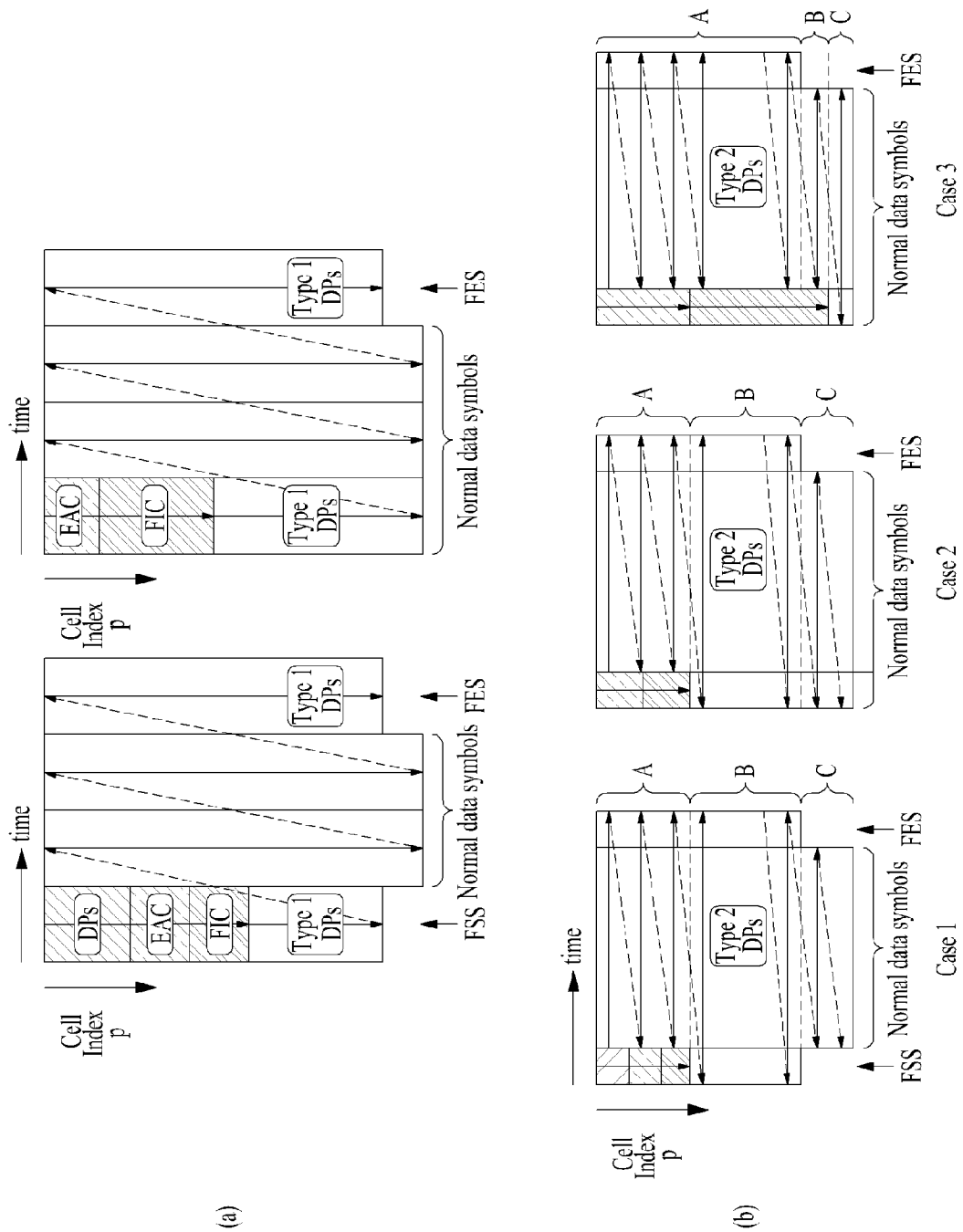
[Fig. 19]


time
Cell Index p
PLS2
FIC
FIC
DPs
FSS
Normal data symbols
(a)
time
Cell Index p
EAC
FIC
FIC
DPs
Normal data symbols
(b)

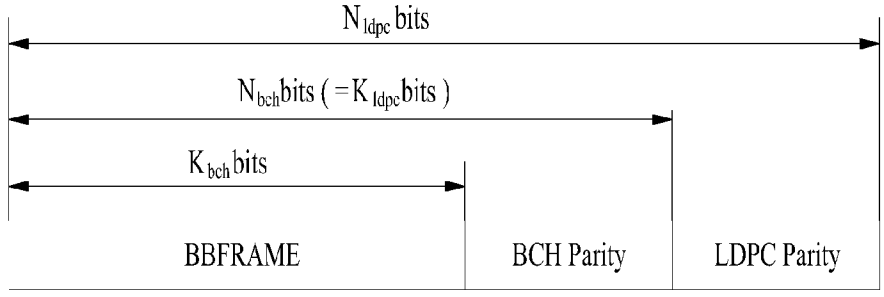
[Fig. 20]



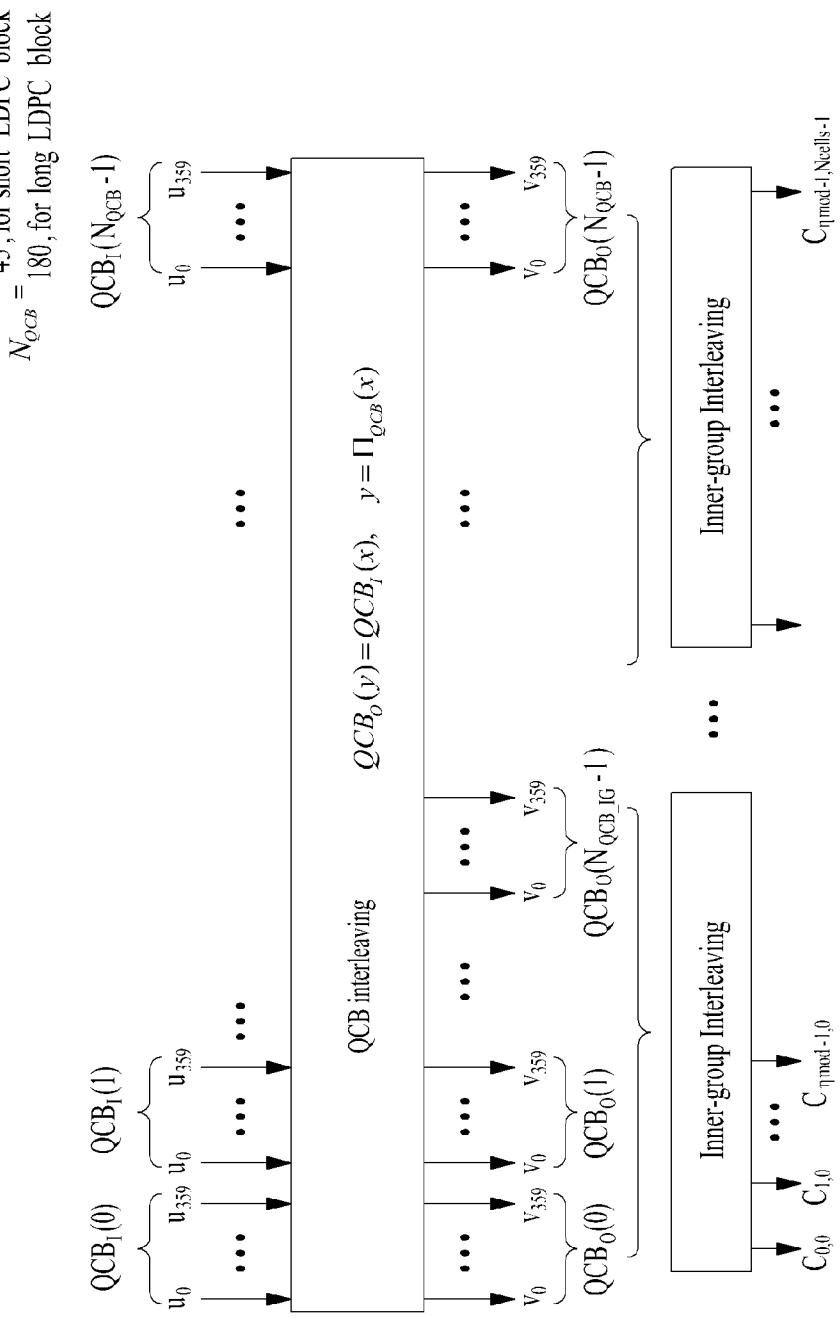
[Fig. 21]


time
Cell Index p
DPs
EAC
FIC
Type 1 DPs
Type 2 DPs
FSS
FES
Normal data symbols
A
B
C
Case 1
Case 2
Case 3
(a)
(b)

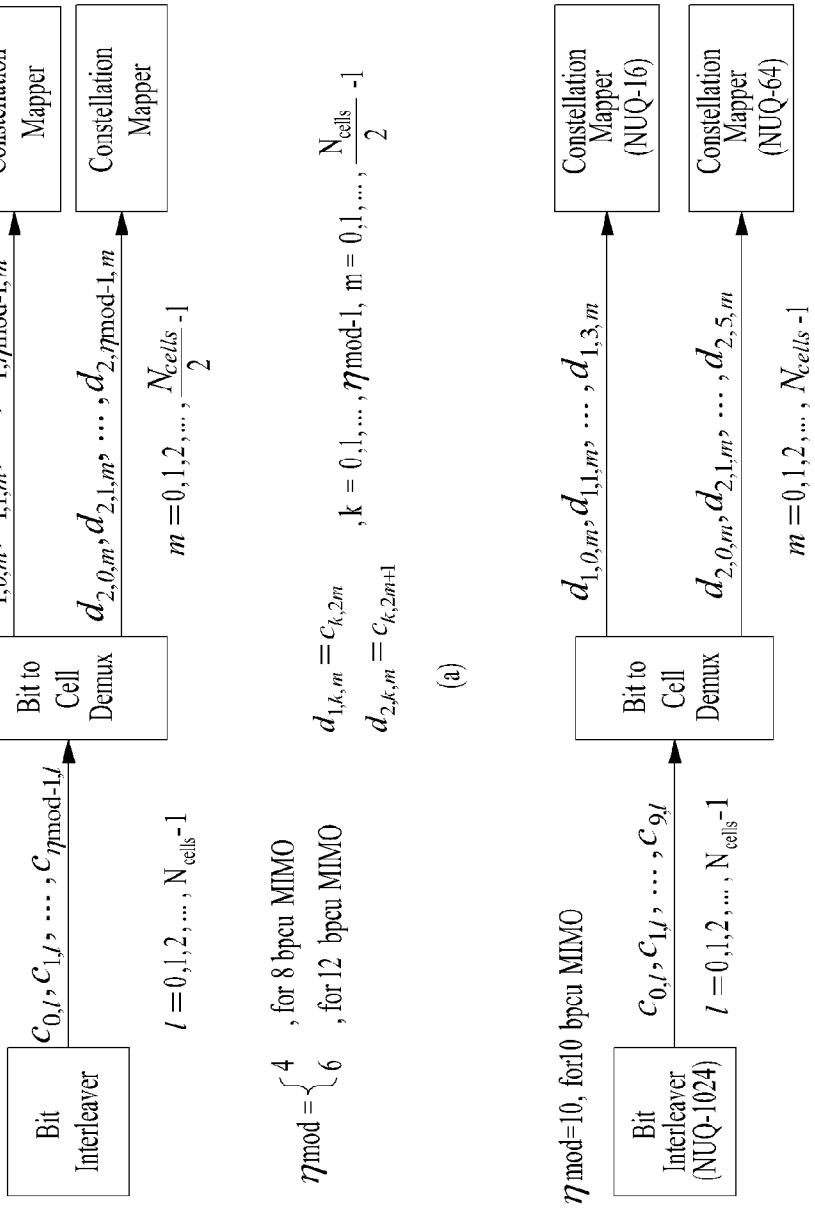
[Fig. 22]


N_{ldpc} bits
N_{bch} bits ($=K_{ldpc}$ bits)
K_{bch} bits
BBFRAME
BCH Parity
LDPC Parity

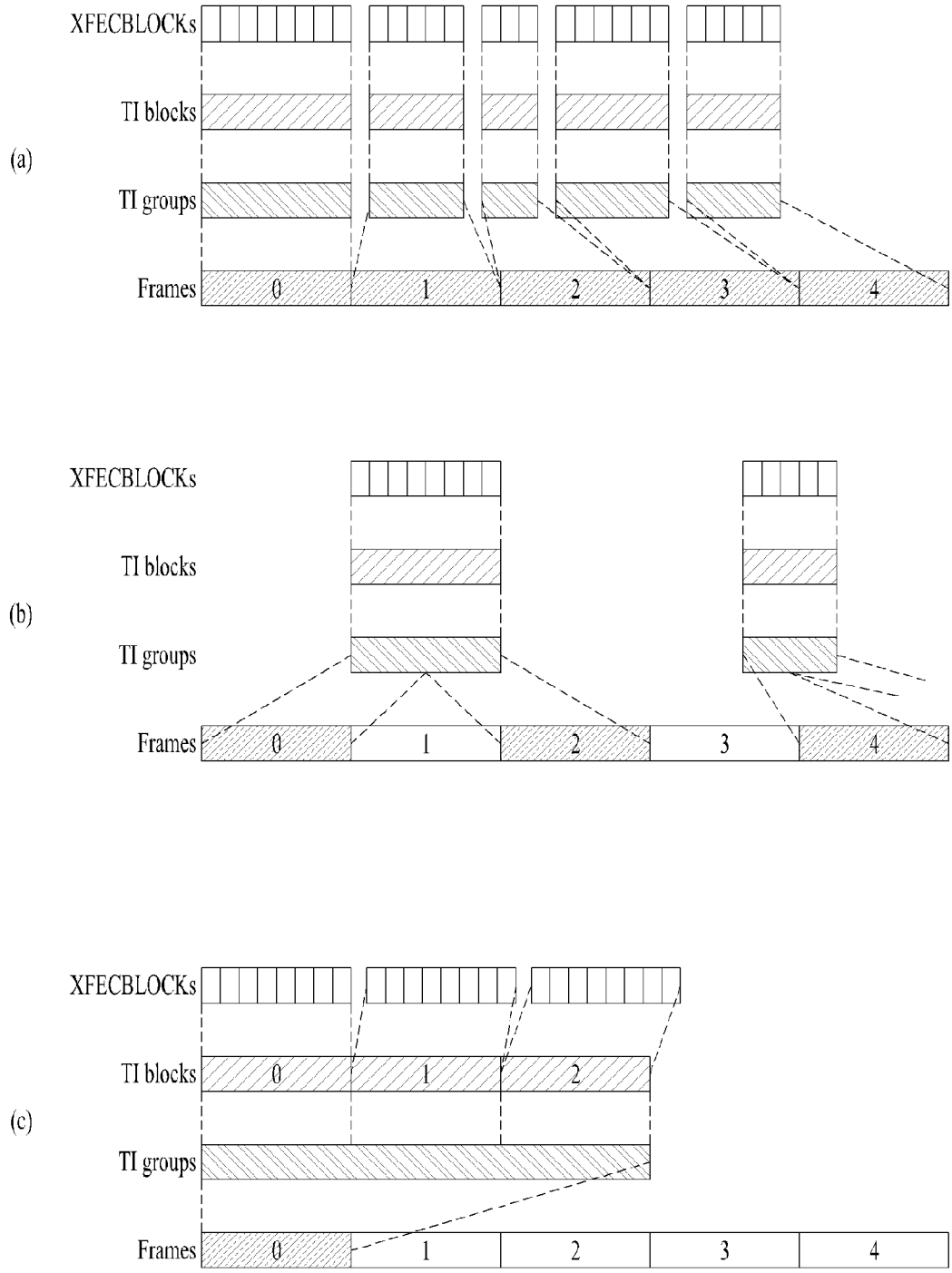
[Fig. 23]


N_{QCB} = 45, for short LDPC block
180, for long LDPC block
$QCB_I(N_{QCB}-1)$
$QCB_I(1)$
$QCB_I(0)$
u_0 u_{359}
QCB interleaving
$QCB_O(y)=QCB_I(x), \quad y=\Pi_{QCB}(x)$
v_0 v_{359}
$QCB_O(N_{QCB}-1)$
$QCB_O(1)$
$QCB_O(0)$
$QCB_O(N_{QCB_IG}-1)$
Inner-group Interleaving
Inner-group Interleaving
$C_{0,0}$ $C_{1,0}$ $C_{\eta mod-1,0}$
$C_{\eta mod-1,Ncells-1}$

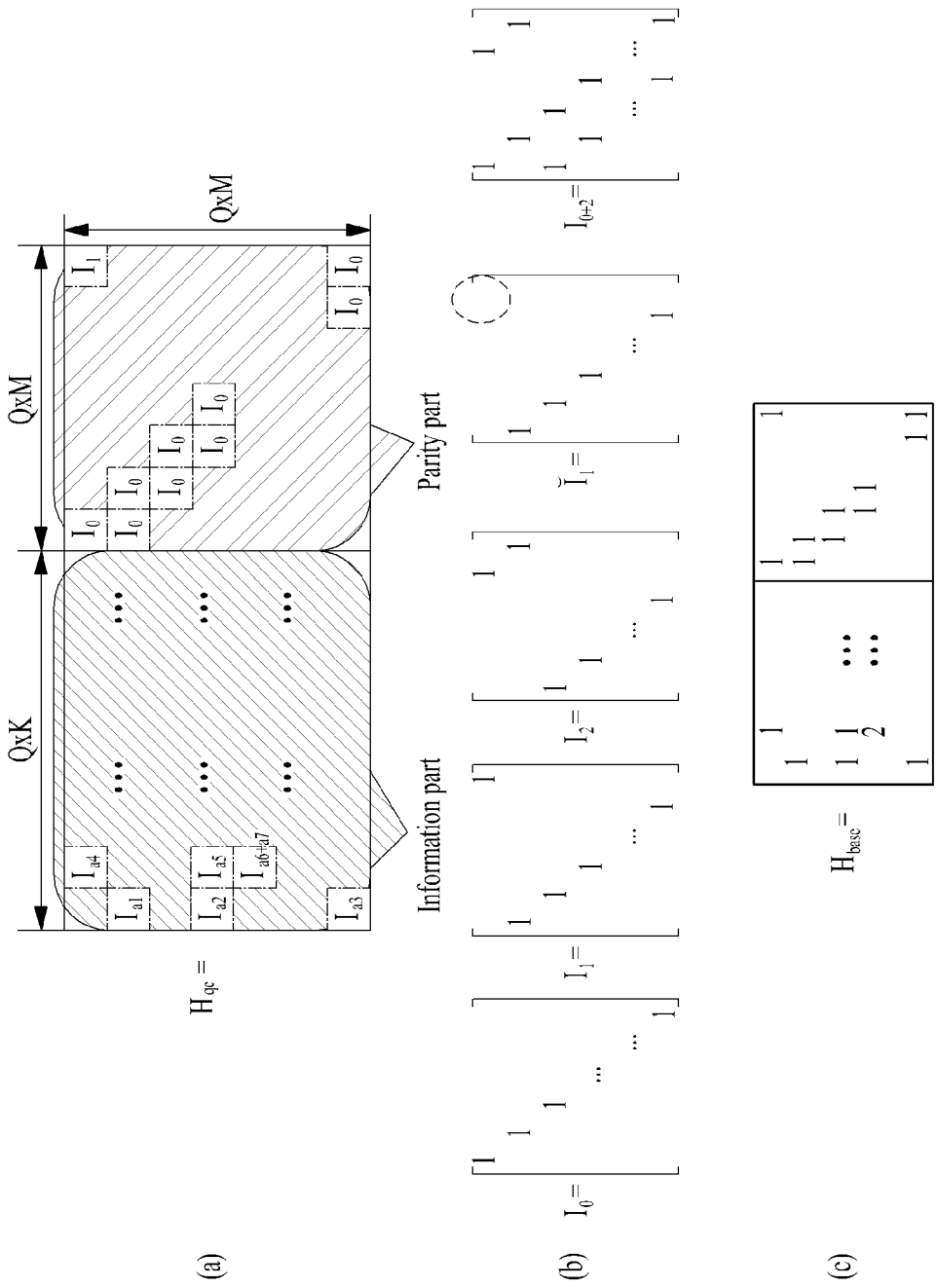
[Fig. 24]


Bit Interleaver
$c_{0,l}, c_{1,l}, \cdots, c_{\eta\text{mod-}1,l}$
$l = 0,1,2,\cdots, N_{cells}-1$
Bit to Cell Demux
$d_{1,0,m}, d_{1,1,m}, \cdots, d_{1,\eta\text{mod-}1,m}$
$d_{2,0,m}, d_{2,1,m}, \cdots, d_{2,\eta\text{mod-}1,m}$
$m = 0,1,2,\cdots, \frac{N_{cells}}{2}-1$
Constellation Mapper
Constellation Mapper
$\eta\text{mod} = \begin{cases} 4 & \text{, for 8 bpcu MIMO} \\ 6 & \text{, for 12 bpcu MIMO} \end{cases}$
$d_{1,k,m} = c_{k,2m}$
$d_{2,k,m} = c_{k,2m+1}$
$k = 0,1,\cdots \eta\text{mod-}1,\ m = 0,1,\cdots, \frac{N_{cells}}{2}-1$
(a)
$\eta\text{mod}=10$, for10 bpcu MIMO
Bit Interleaver (NUQ-1024)
$c_{0,l}, c_{1,l}, \cdots, c_{9,l}$
$l = 0,1,2,\cdots, N_{cells}-1$
Bit to Cell Demux
$d_{1,0,m}, d_{1,1,m}, \cdots, d_{1,3,m}$
$d_{2,0,m}, d_{2,1,m}, \cdots, d_{2,5,m}$
$m = 0,1,2,\cdots, N_{cells}-1$
Constellation Mapper (NUQ-16)
Constellation Mapper (NUQ-64)
$\{d_{1,0,m}, d_{1,1,m}, d_{1,2,m}, d_{1,3,m}\} = \{c_{0,m}, c_{1,m}, c_{4,m}, c_{5,m}\}$
$\{d_{2,0,m}, d_{2,1,m}, d_{2,2,m}, d_{2,3,m}, d_{2,4,m}, d_{2,5,m}\} = \{c_{2,m}, c_{3,m}, c_{6,m}, c_{7,m}, c_{8,m}, c_{9,m}\}$
$m = 0,1,\cdots, N_{cells}-1$
(b)

[Fig. 25]

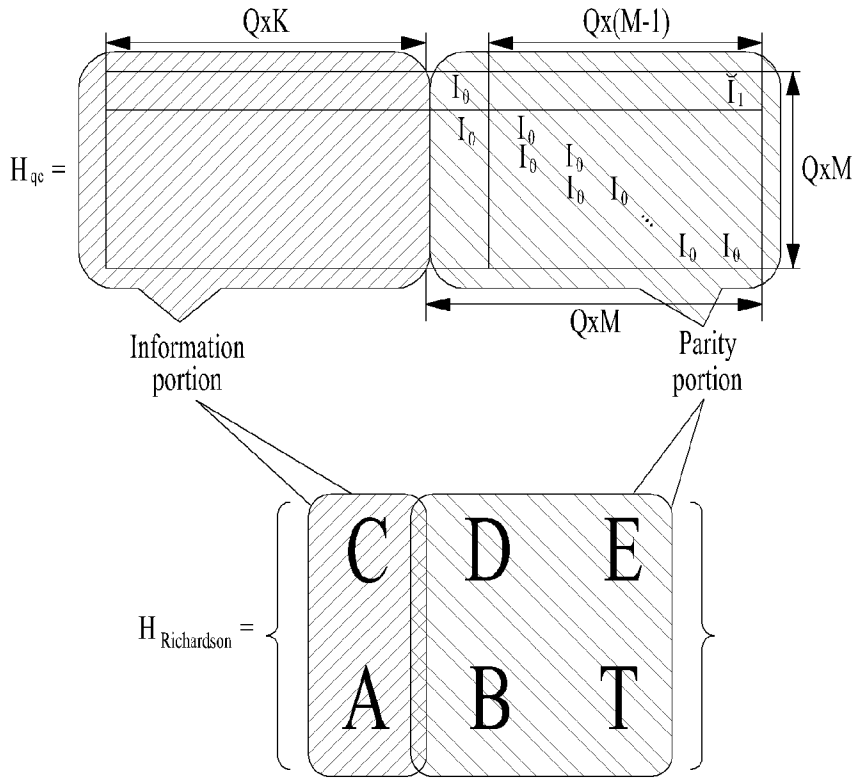

(a)
XFECBLOCKs
TI blocks
TI groups
Frames
0
1
2
3
4
(b)
XFECBLOCKs
TI blocks
TI groups
Frames
0
1
2
3
4
(c)
XFECBLOCKs
TI blocks
TI groups
Frames
0
1
2
3
4

[Fig. 26]


QxM
QxM
QxK
Parity part
Information part
H_{qc} =
(a)
I_0 =
I_1 =
I_2 =
$\breve{I}_1$ =
$I_{(1+2)}$ =
(b)
H_{base} =
(c)

[Fig. 27]

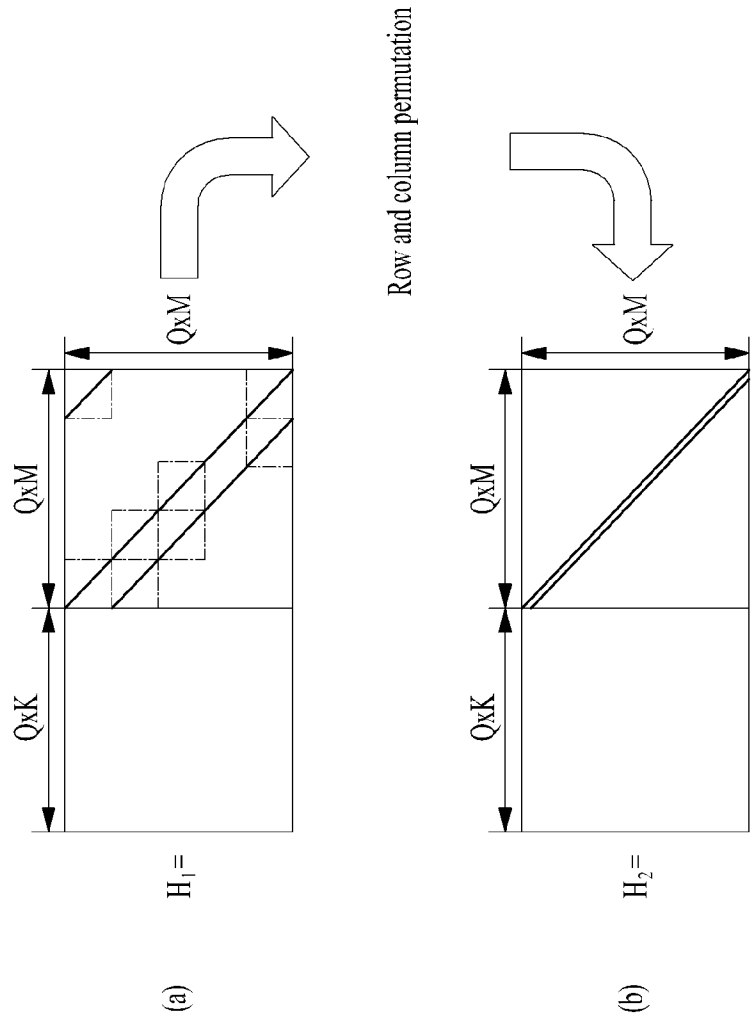
(a)



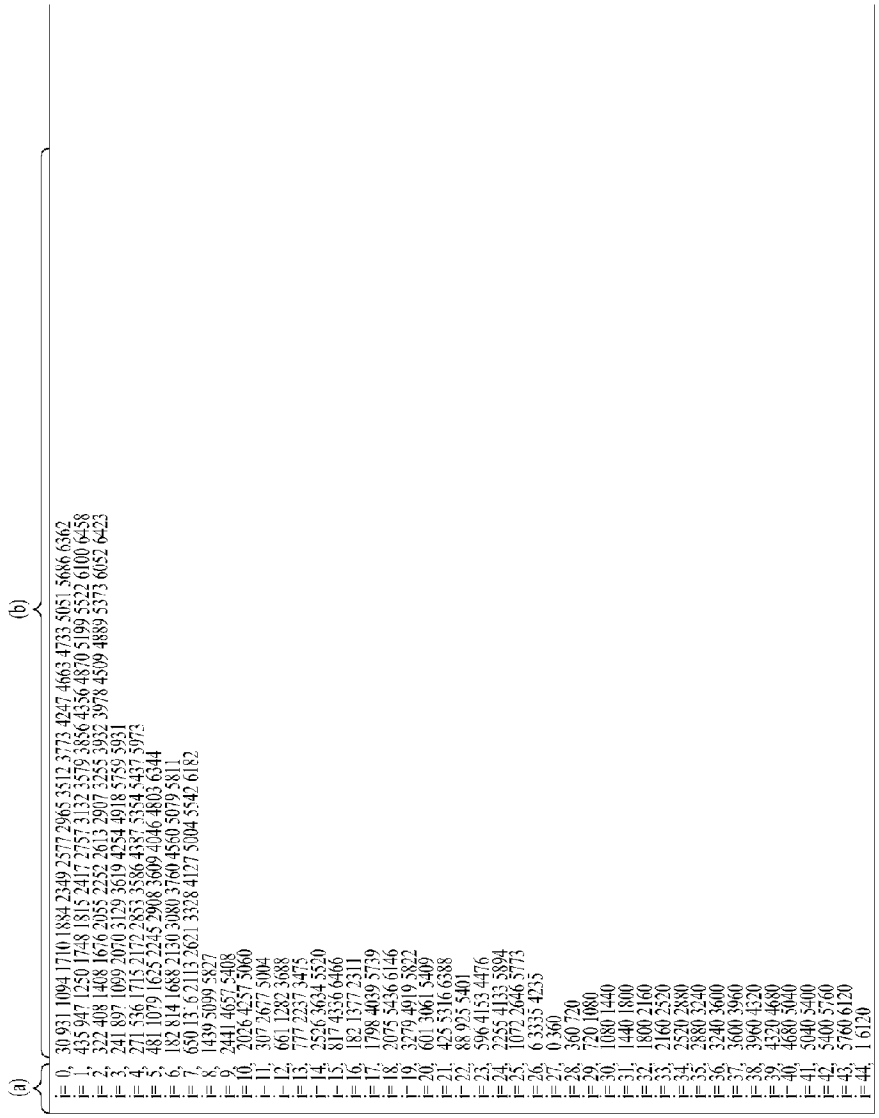
(b)

$$\phi = \begin{bmatrix} 1 & & & & & \\ 1 & 1 & & & & \\ & 1 & 1 & & & \\ & & 1 & 1 & & \\ & & & \cdots & \cdots & \\ & & & & 1 & 1 \end{bmatrix} \qquad \phi^{-1} = \begin{bmatrix} 1 & & & & & \\ 1 & 1 & & & & \\ 1 & 1 & 1 & & & \\ 1 & 1 & 1 & 1 & & \\ \cdots & \cdots & \cdots & \cdots & \cdots & \\ 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}$$

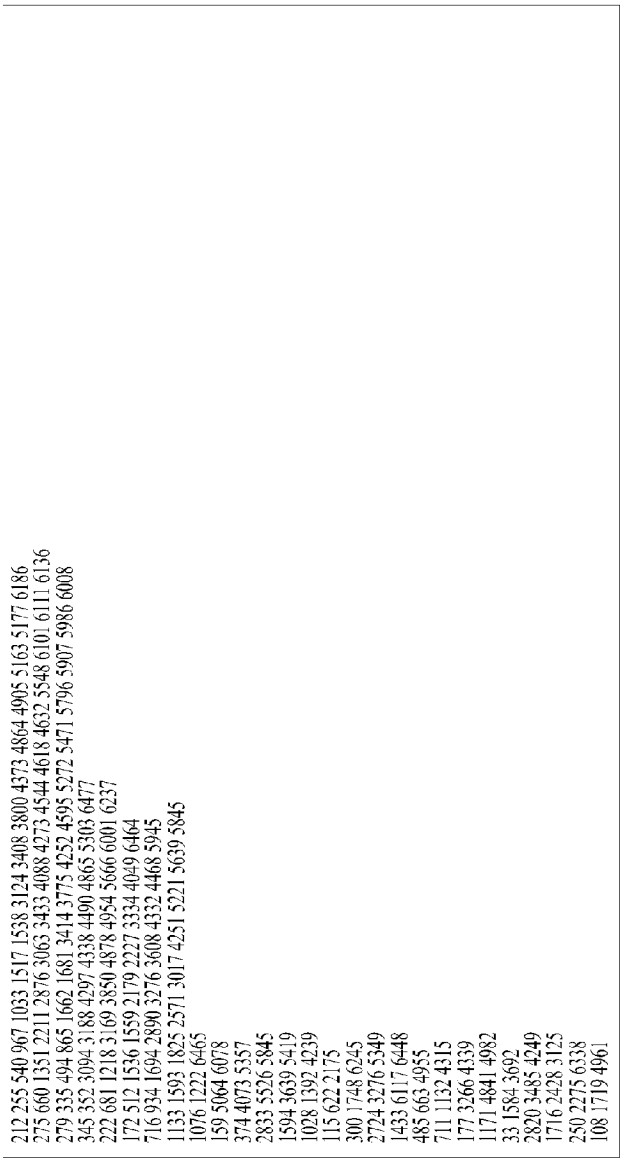
[Fig. 28]



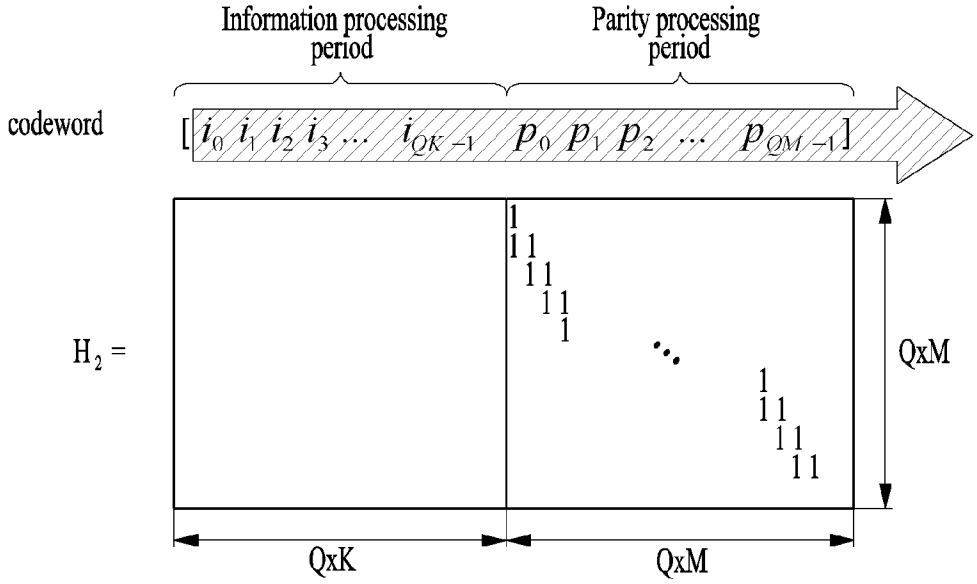
[Fig. 29]


(a)
(b)
i= 0, 30 93 1 1094 1710 1884 2349 2577 2965 3512 3773 4247 4663 4733 5051 5686 6362
i= 1, 435 947 1250 1748 1815 2417 2757 3132 3579 3856 4356 4870 5199 5522 6100 6458
i= 2, 322 408 1408 1676 2055 2252 2613 2907 3255 3932 3978 4509 4889 5373 6052 6423
i= 3, 241 897 1099 2070 3129 3619 4254 4918 5756 5931
i= 4, 271 536 1715 2172 2823 3586 4337 5354 5437 5973
i= 5, 481 1079 1625 2245 2908 3609 4046 4803 6344
i= 6, 182 814 1688 2130 3080 3760 4560 5079 5811
i= 7, 650 1316 2113 2621 3328 4127 5004 5542 6182
i= 8, 1439 3099 5827
i= 9, 2441 4657 5408
i= 10, 2026 4257 5060
i= 11, 307 2677 3004
i= 12, 661 1282 3688
i= 13, 777 2237 3475
i= 14, 2526 3634 5520
i= 15, 817 4336 6466
i= 16, 182 1377 2311
i= 17, 1798 4039 5739
i= 18, 2075 5436 6146
i= 19, 3279 4919 5822
i= 20, 601 3061 5409
i= 21, 425 5316 6388
i= 22, 88 935 5401
i= 23, 596 4153 4476
i= 24, 2255 4133 5894
i= 25, 1072 2646 5773
i= 26, 6 3335 4235
i= 27, 0 360
i= 28, 360 720
i= 29, 720 1080
i= 30, 1080 1440
i= 31, 1440 1800
i= 32, 1800 2160
i= 33, 2160 2520
i= 34, 2520 2880
i= 35, 2880 3240
i= 36, 3240 3600
i= 37, 3600 3960
i= 38, 3960 4320
i= 39, 4320 4680
i= 40, 4680 5040
i= 41, 5040 5400
i= 42, 5400 5760
i= 43, 5760 6120
i= 44, 1 6120

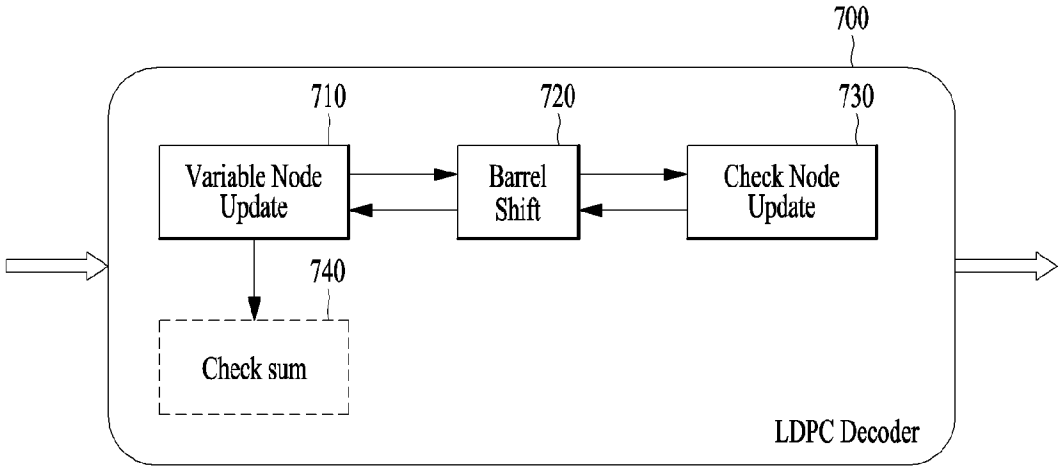
[Fig. 30]


212 255 540 967 1033 1517 1538 3124 3408 3800 4373 4864 4905 5163 5177 6186
275 660 1351 2211 2876 3063 3433 4088 4273 4544 4618 4632 5548 6101 6111 6136
279 335 494 865 1662 1681 3414 3775 4252 4595 5272 5471 5796 5907 5986 6008
345 352 3094 3188 4297 4338 4490 4865 5303 6477
222 681 1218 3169 3850 4878 4954 5666 6001 6237
172 512 1536 1559 2179 2227 3334 4049 6464
716 934 1694 2890 3276 3608 4332 4468 5945
1133 1593 1825 2571 3017 4251 5221 5639 5845
1076 1222 6465
159 5064 6078
374 4073 5357
2833 5526 5845
1594 3639 5419
1028 1392 4239
115 622 2175
300 1748 6245
2724 3276 5349
1433 6117 6448
485 663 4955
711 1132 4315
177 3266 4339
1171 4841 4982
33 1584 3692
2820 3485 4249
1716 2428 3125
250 2275 6338
108 1719 4961

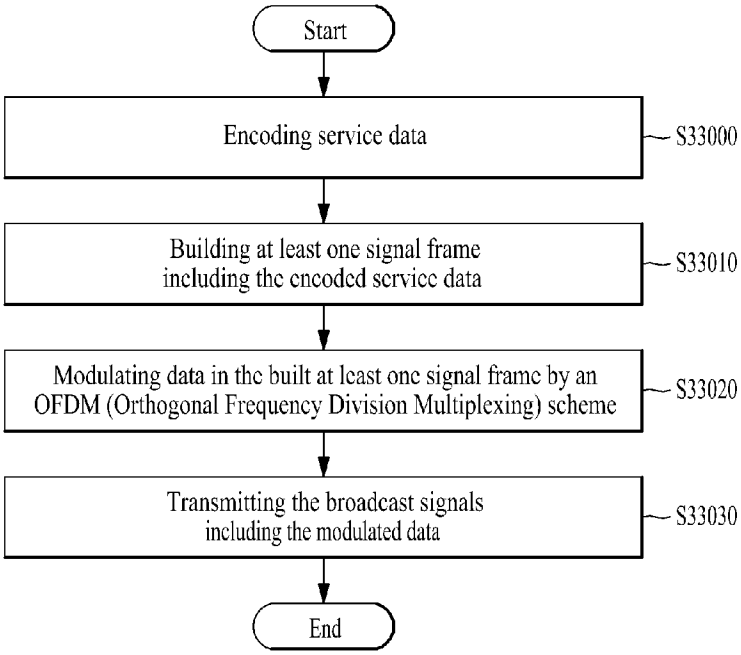
[Fig. 31]


Information processing period
Parity processing period
codeword
$[i_0\ i_1\ i_2\ i_3 \cdots\ i_{QK-1}\ \ p_0\ p_1\ p_2 \cdots\ p_{QM-1}]$
H_2 =
QxM
QxK
QxM

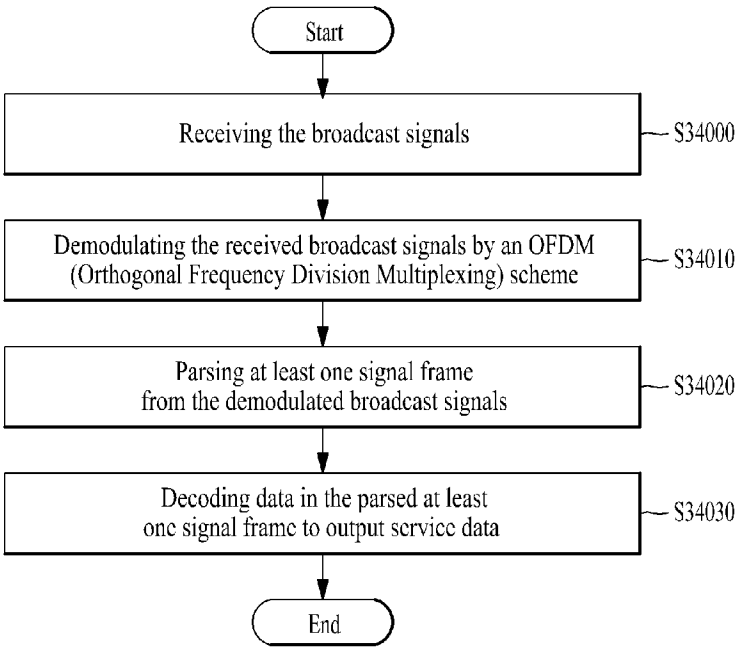
[Fig. 32]



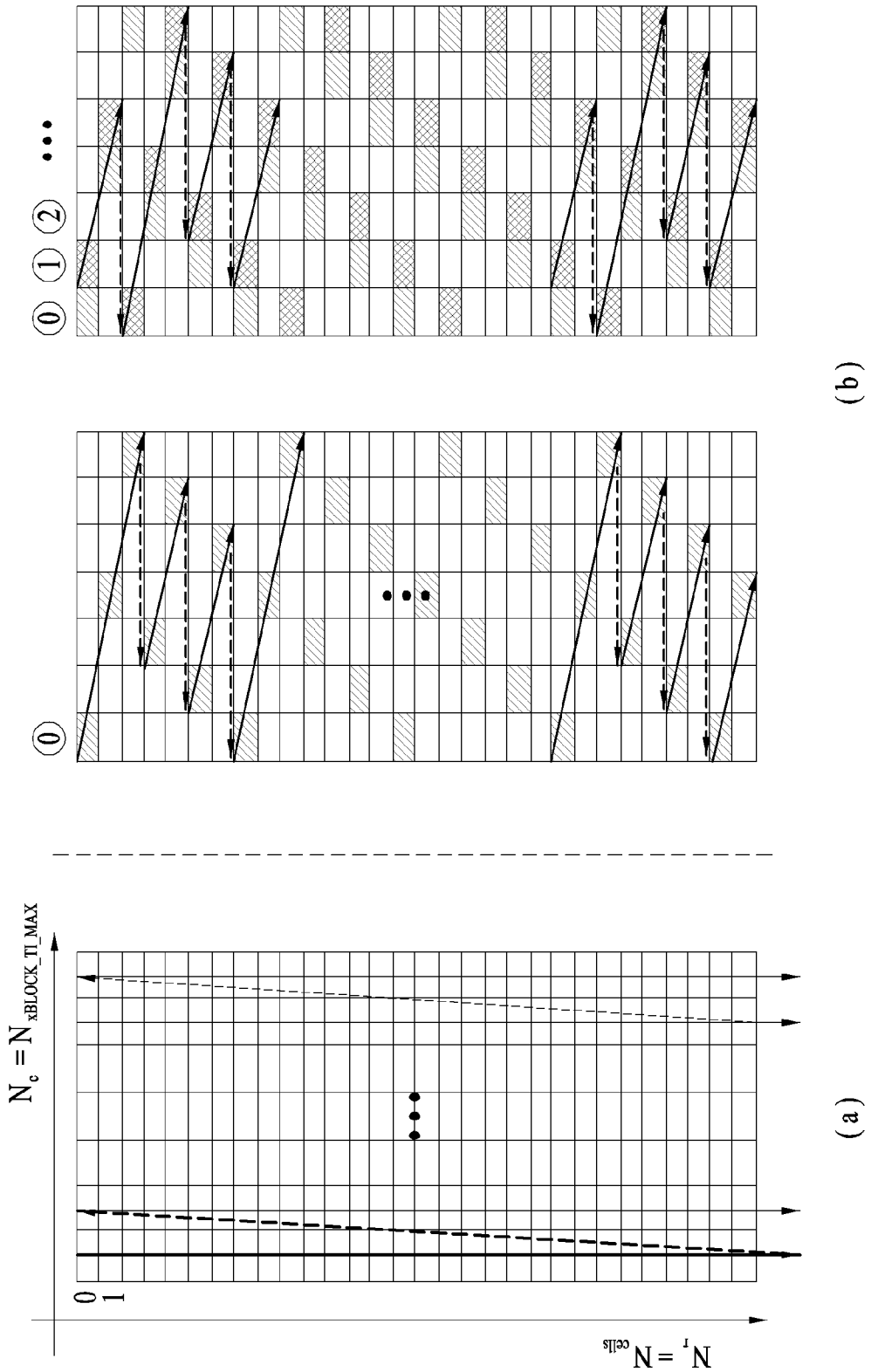
[Fig. 33]



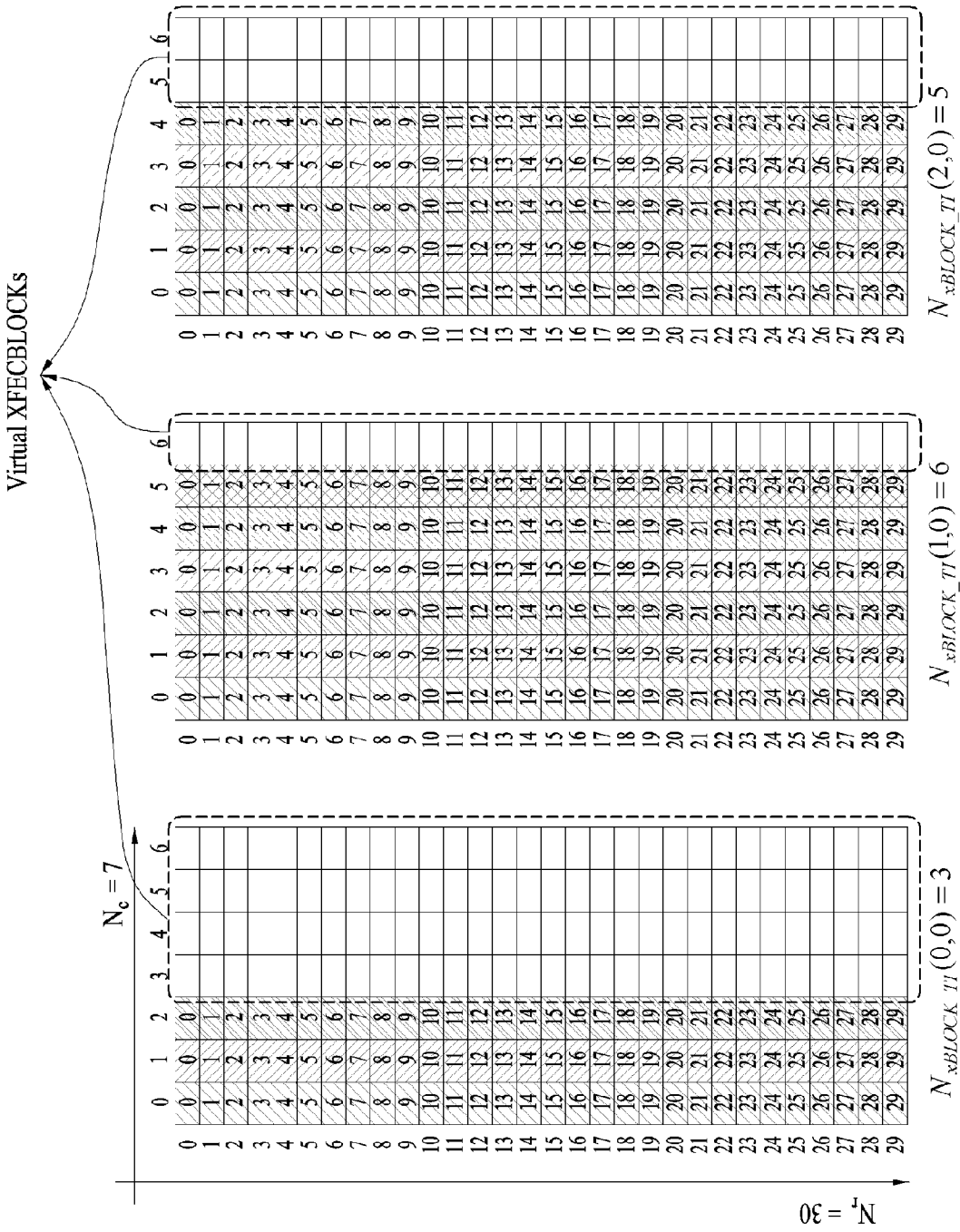
[Fig. 34]



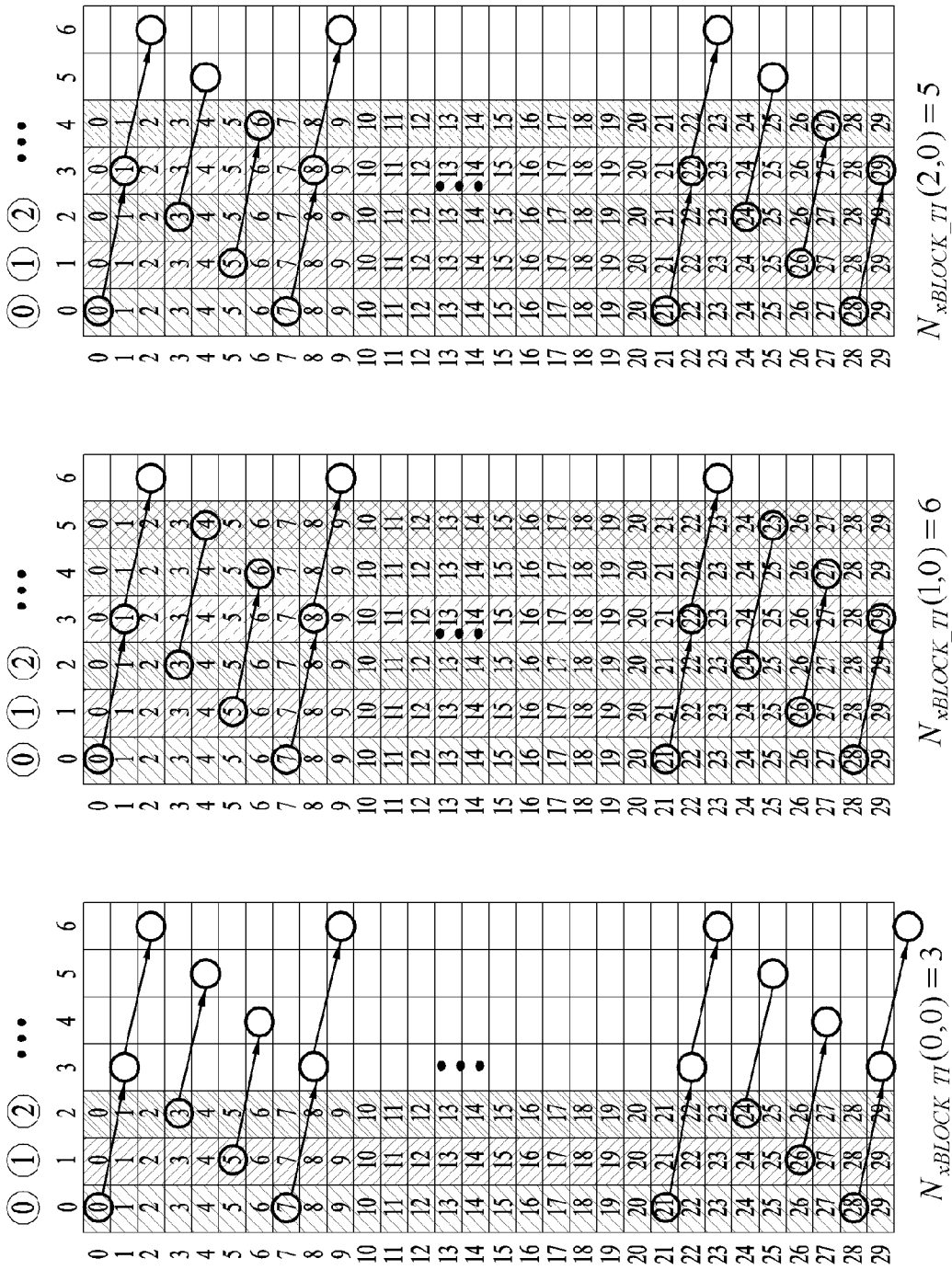
[Fig. 35]



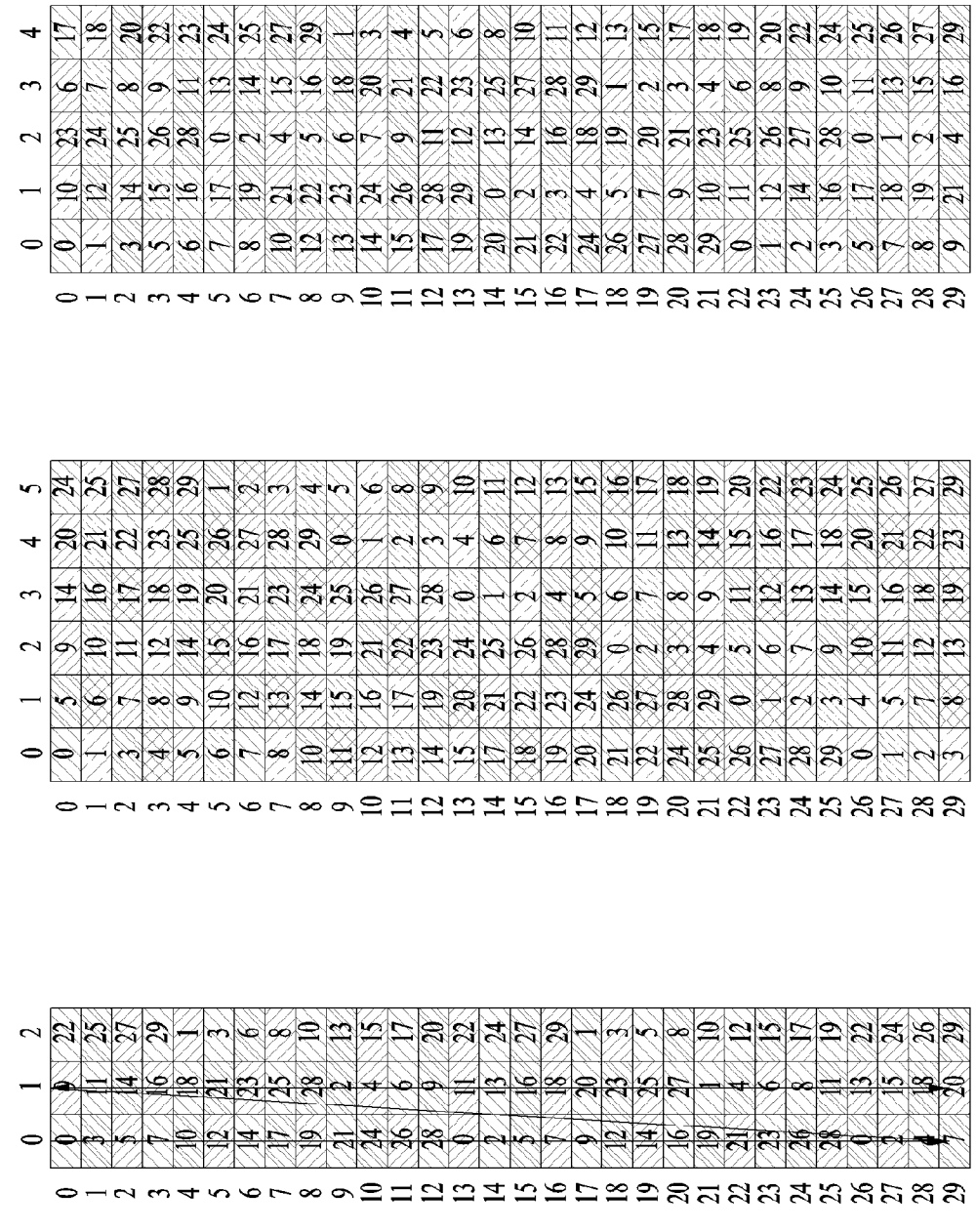
[Fig. 36]


Virtual XFECBLOCKs
$N_c = 7$
$N_r = 30$
$N_{xBLOCK_TI}(0,0) = 3$
$N_{xBLOCK_TI}(1,0) = 6$
$N_{xBLOCK_TI}(2,0) = 5$

[Fig. 37]



[Fig. 38]



[Fig. 39]

```
i = 0,  348 751 1280 1606 1893 2307 2802 3203 3529 3658 4233 4503 5026 5097 5509 6128
i = 1,  454 726 1098 1488 1961 2271 2698 3052 3297 3834 4575 4806 5233 5469 6032 6402
i = 2,  37 361 1326 1457 1808 2479 2874 3097 3459 3773 4217 4326 4720 5287 5760 6217
i = 3,  172 963 1382 1846 3031 3824 4019 4711 5468 5995
i = 4,  120 525 1648 2216 2595 3516 4395 5201 5616 6066
i = 5,  644 937 1750 2296 2912 3840 4257 4931 6382
i = 6,  149 881 1589 1916 2884 3837 4584 5257 6042
i = 7,  605 1150 1881 2595 3380 4067 4690 5678 6267
i = 8,  1333 5333 6114
i = 9,  2365 4494 5539
i = 10, 1817 4128 5336
i = 11, 56 2685 4824
i = 12, 401 1352 3743
i = 13, 845 2207 3265
i = 14, 2564 3842 5646
i = 15, 813 4391 6238
i = 16, 56 1408 2399
i = 17, 1740 4070 5426
i = 18, 2017 5505 6285
i = 19, 3570 4858 5879
i = 20, 568 3060 5454
i = 21, 661 5074 6252
i = 22, 50 999 5692
i = 23, 529 4174 4442
i = 24, 2458 4270 5939
i = 25, 826 2762 6113
i = 26, 76 3405 4215
i = 27, 0 360
i = 28, 360 720
i = 29, 720 1080
i = 30, 1080 1440
i = 31, 1440 1800
i = 32, 1800 2160
i = 33, 2160 2520
i = 34, 2520 2880
i = 35, 2880 3240
i = 36, 3240 3600
i = 37, 3600 3960
i = 38, 3960 4320
i = 39, 4320 4680
i = 40, 4680 5040
i = 41, 5040 5400
i = 42, 5400 5760
i = 43, 5760 6120
i = 44, 1 6120
```

[Fig. 40]

```
161 560 1040 1054 1679 1977 2652 2992 3306 3603 4925 5083 5211 5822 6241 6264
110 327 868 1035 1257 1693 2004 2281 2903 3104 3211 3488 4222 4602 4912 5093
16 19 120 149 310 666 733 1763 3124 3914 3951 4431 4460 4637 5748 6379
571 833 1073 1239 2726 3096 4042 4246 4376 5439
1014 1357 1362 2160 2912 2971 3748 3903 4977 5524
584 2454 3908 4330 4531 4733 5113 5357 5584
80 2093 2682 2686 2900 3920 4276 4764 5092
193 1263 1357 1463 1937 2529 2663 4411 5019
4557 5288 6388
2517 3144 3696
311 3035 5342
1008 2605 2977
739 2584 4899
459 852 2252
799 4366 4443
1290 1676 2141
1008 4308 5907
483 1991 5404
1905 2987 3911
2158 3217 5949
987 3248 3745
626 2393 5419
900 5024 5271
2208 3043 3863
3238 5370 5591
1910 4363 6370
1368 2979 4601
```

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2014/007130

A. CLASSIFICATION OF SUBJECT MATTER

H04N 7/08(2006.01)i, H04N 21/234(2011.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N 7/08; H03M 13/09; H03M 13/11; H03M 13/00; H04L 27/28; G06F 11/10; H04W 72/04; H04L 27/34; H04N 21/234

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: encode, decode, parity bit, code rate, codeword

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0064314 A1 (WOO SUK KO et al.) 14 March 2013 See abstract, paragraphs [0108]-[0112], [0262]-[0263], [0299], [0327], [0402], claims 16, 20 and figures 4, 49.	1,3
Y		2,4
Y	WO 2004-006443 A1 (HUGHES ELECTRONICS CORPORATION) 15 January 2004 See paragraphs [44], [46]-[49], [69], claims 1, 12, 18 and figure 10.	2,4
A	KR 10-2007-0058480 A (LG ELECTRONICS INC.) 08 June 2007 See paragraphs [0042]-[0045], [0059]-[0065], claim 13 and figures 1, 4.	1-4
A	US 2008-0256425 A1 (MIN SEOK OH et al.) 16 October 2008 See paragraphs [0035]-[0043] and figure 1.	1-4
A	US 2012-0327879 A1 (LOTHAR STADELMEIER et al.) 27 December 2012 See paragraphs [0108]-[0119], [0204]-[0217], claims 47, 49 and figures 2, 19.	1-4

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
11 November 2014 (11.11.2014)	**12 November 2014 (12.11.2014)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2014/007130

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