Title: DRIVE CIRCUIT AND METHOD FOR MOSFET

Abstract: A triggering circuit (10) for an insulated gate semiconductor device such as a MOSFET (12) comprises a charge storage device (14) and a fast switching device (16) connected in a circuit to a gate (20) of the MOSFET. The fast switching device is able to switch between an off and an on state in a first time period shorter than a specified turn-on delay time of the MOSFET and the fast switching device is further controllable to move charge between the storage device and the gate, so that the MOSFET switches between an off state and an on state in a second time period shorter than a specified rise time or fall time for the MOSFET.
DRIVE CIRCUIT AND METHOD FOR MOSFET

TECHNICAL FIELD

This invention relates to a circuit and method for improving the switching speed of insulated gate semiconductor devices such as metal oxide field effect transistors (MOSFET’s), more particularly power MOSFET’s.

BACKGROUND ART

Capacitance inherent in transistor junctions limits the speed at which a voltage within a circuit can switch. It is also well known that the Miller effect has an influence on the capacitance at the gate of devices of the aforementioned kind.

Prior art teaches a number of methods of alleviating the Miller effect in high frequency transistor switching circuits, for example by reducing source impedance or reducing feedback capacitance, or both.

Even with such improvements, an output of a MOSFET such as an IRF740 typically switches through 200 volts in a rise time of approximately 27ns at a peak current of 10 amperes and in a fall
time of approximately 24ns. These times may be too long for many applications.

OBJECT OF THE INVENTION

Accordingly, it is an object of the present invention to provide a triggering circuit and method for improving the rise and/or fall times of insulated gate semiconductor devices with which the applicant believes the aforementioned disadvantages will at least be alleviated.

SUMMARY OF THE INVENTION

According to the invention there is provided a triggering circuit for an insulated gate semiconductor device comprising as a first terminal a gate and further comprising at least a second and a third terminal, the circuit comprising:

- a charge storage device and a fast switching means connected in a circuit to the gate of the device;
- the fast switching means being able to switch between an off and an on state in a first time period shorter than a specified turn-on delay time of the insulated gate device; and
- the fast switching means being controllable to move charge between the storage device and the gate of the insulated gate device, so that the insulated gate device switches between
an off state and an on state in a second time period shorter than a specified rise time or fall time for the insulated gate device.

The insulated gate semiconductor device may be a metal oxide semiconductor field effect transistor (MOSFET), such as a power MOSFET.

Alternatively, the insulated gate semiconductor device may be an insulated gate bipolar transistor.

The first time period is preferably shorter than 2ns.

The fast switching means may comprise one of: a SIDAC, a break-over diode, a bipolar transistor, another insulated gate semiconductor device and a high voltage fast switching device.

The specified turn-on time is typically a minimum turn-on time specified in a publicly available data sheet relating to the insulated gate semiconductor device.

The fast switching means may be electronically controllable.
The charge storage device may be a capacitor.

The insulated gate semiconductor device may switch from the off state to the on state as well as from the on state to the off state in periods shorter than specified rise and fall times respectively.

An inductor may be provided in the circuit between the fast switching means and the gate.

The triggering circuit may be integrated on a single chip.

The chip may further comprise additional circuitry also integrated thereon.

According to another aspect of the invention, a method of driving an insulated gate semiconductor device comprises the steps of:

- utilizing a fast switching means to transfer charge to a gate of the device;
- switching the fast switching means on in a first time period shorter than a specified turn-on delay time of the insulated gate device;
moving charge to and from the gate to cause the insulated gate device to switch between an off and an on state in a second time period shorter than a specified rise time or fall time for the insulated gate device.

5

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described, by way of example only, with reference to the accompanying drawings wherein:

figure 1 is a basic circuit diagram of a triggering circuit according to the invention for a MOSFET;

figure 2 is a diagram of one embodiment of the circuit comprising a SIDAC as fast switching device;

figure 3 includes a diagram in dotted lines of gate voltage against time of normal specified operation of the MOSFET and a diagram in solid lines of operation according to the method of the invention;

figure 4 includes a diagram in dotted lines of gate current against time of normal specified operation of the MOSFET and a diagram in solid lines of operation according to the method of the invention;

figure 5 is a diagram of another embodiment of the circuit according to the invention;
figure 6 is a waveform of voltage against time at a first terminal of a charge storage capacitor in figure 5;

figure 7 is a waveform of voltage against time at the source of the MOSFET in figure 5;

figure 8 is a diagram of a triggering circuit for an insulated gate bipolar transistor;

figure 9 is a waveform of voltage against time at a first terminal of a charge storage capacitor in the circuit in figure 8;

figure 10 is a waveform of voltage against time at an emitter of the transistor in figure 8; and

figure 11 is a basic circuit diagram of yet another embodiment of the triggering circuit.

**DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION**

In figure 1, there is shown a basic diagram of a triggering circuit 10 according to the invention for an insulated gate semiconductor device 12 such as a metal oxide semiconductor field effect transistor (MOSFET).

In the diagram a power MOSFET is shown and which is available from International Rectifier under the trademark HEXFET number IRF740. A 10% to 90% rise time of an output voltage is specified
in publicly available user data sheets of the device as being about
27ns and a corresponding fall time is specified as being in the order
of 24ns. These times may be too long for some applications of the
MOSFET. The turn-on delay time is specified at 14ns and the turn-
off delay time as 50ns.

The triggering circuit 10 comprises a charge storage device in the
form of a capacitor 14 having first and second terminals 14.1 and
14.2 respectively. The first terminal 14.1 is connected in a circuit 17
to a fast switching device 16. An optional inductor 18 is connected
between the fast switching device 16 and a gate 20 of the MOSFET.
The drain and source of the MOSFET are shown at 22 and 24
respectively.

The fast switching device 16 may be any suitable device having a
switching speed faster than the data sheet specified turn-on delay
time and/or turn-off delay time of the MOSFET, preferably better
than 2ns. Such devices may include a SIDAC, a break-over diode, a
suitably configured bipolar transistor arrangement, or any other
suitable fast switching device or circuit.
To switch the MOSFET on, the fast switching device is switched on electronically which rapidly transfers sufficient charge from the capacitor 14 to the gate 20 of the MOSFET, to switch the MOSFET on.

Time diagrams for the circuit in figure 1 are shown in figures 3 and 4. The diagrams in broken lines indicate normal specified operation of the MOSFET 12. Hence, diagram 30 in figure 3 shows the gate voltage of the MOSFET during conventional switching on. The MOSFET is switched on at 32 and the diagram illustrates a turn-on delay time of about 34ns. The associated gate current is shown at 34 in figure 4.

The diagrams for the method according to the invention are shown at 36 and 38 in figures 3 and 4 respectively. At 40 in figure 3, the aforementioned rapid transfer of charge from capacitor 14 through switch 16 and consequent build up of voltage on the gate of the MOSFET are shown. The subsequent fall in the gate voltage shown at 42 is attributable to the aforementioned Miller effect. What is clear though is that the device switches on at 44, after a mere 4ns. The associated current at the gate 20 is shown at 38 in figure 4. Initially, during the charge transfer stage, the gate current is high
and thereafter it drops to a negligible level. It is also believed that
with drain currents within the data specification of the MOSFET,
switching losses with the switching method and circuit according to
the invention are also reduced.

The value (C) of the capacitor 14, the voltage (V_c) required on the
capacitor before switching and hence the breakthrough voltage of
the switching device 16, the gate threshold voltage (V_t) of the
MOSFET 12 and the gate charge (Q_s) required for complete
switching of the MOSFET are related according to the following
equation \[ \frac{C \cdot V_c}{(Q_s/V_t + C)} > V_t. \]

In figure 2 a circuit diagram of the triggering circuit 10 is shown
wherein the first switching device 16 is a SIDAC.

A periodic voltage is applied across a capacitor 14, in parallel with a
SIDAC 16 and a MOSFET 12. Initially, during a first half cycle, the
voltage supplied at the input 19 is insufficient to switch the SIDAC
14 on and the capacitor 12 is hence charged up. When the supplied
voltage reaches the threshold of the SIDAC 16 it switches on,
resulting in a closed circuit from the capacitor 14 to the gate 20 of
the MOSFET 12, partially discharging the capacitor 14 and hence charging the gate 20. The result is that a charge will now be shared between the capacitor 14 and the gate 20, so that some voltage, preferably above the gate threshold voltage relative to ground, is applied to the gate.

Using this method, the gate voltage may for short intervals be driven approximately three to four times beyond the maximum threshold rating of some MOSFET's 12 without destroying the device.

Similarly, when during the other half cycle the gate voltage exceeds the reverse threshold of the SIDAC 16 and current is conducted in the opposite direction, the gate voltage of the MOSFET 12 drops to substantially below the threshold voltage of the MOSFET 12 shortly after the charge dissipates from the gate 20 of the MOSFET 12. As a result, the MOSFET 12 will turn off and the drain current will no longer flow.

In figure 5, an alternative and self-oscillating triggering circuit for the MOSFET 12 is shown. Components thereof corresponding to components of the circuits in figures 1 and 2 are designated utilizing
like reference numerals. In this embodiment, the fast switching means 16 comprises a bipolar transistor arrangement.

The voltage waveform at 50 is shown in figure 6. The voltage waveform at source 24 is shown in figure 7. From the latter waveform it can be seen at 52 that the source 24 of the aforementioned MOSFET 12 switches between an “off”-state to an “on”-state through about 400V in a rise time t, of about 4ns, which is substantially quicker than the specified rise time of 27ns. Similarly, and as shown at 54 it switches from the “on”-state to the “off”-state in a fall time t, of about 15ns, which is also substantially shorter than a specified fall time of about 24ns.

In figure 8, the same triggering circuit 10 is shown for an insulated gate bipolar transistor 60 having a gate 62, a collector 64 and an emitter 66. The transistor is an IRG4PC50W device which is being manufactured and sold by International Rectifier. The waveform at 68 in figure 8 is shown in figure 9 and the waveform at emitter 66 adjacent load 70 is shown in figure 10.

From the latter waveform it can be seen at 72 that the emitter 66 switches between an “off”-state and an “on”-state through about
400V in a rise time \( t \), of about 4ns, which is substantially less than a specified rise time of 33ns.

In figure 11 a further embodiment of the triggering circuit is shown. The switching means comprises a low output impedance, high voltage, fast switching driving circuit 116. The device 116 must be able to switch between OV and Vd in a first time period shorter than a specified turn-on delay time of the device 12. Vd is preferably bigger than 20xVt. Devices of this nature are available on the market.

It will be appreciated that there are many variations in detail on the triggering circuit and method according to the invention, without departing from the scope and spirit of the appended claims.
CLAIMS:

1. A triggering circuit for an insulated gate semiconductor device comprising as a first terminal a gate and further comprising at least a second and a third terminal, the circuit comprising:

   - a charge storage device and a fast switching means connected in a circuit to the gate of the device;

   - the fast switching means being able to switch between an off and an on state in a first time period shorter than a specified turn-on delay time of the insulated gate device; and

   - the fast switching means being controllable to move charge between the storage device and the gate of the insulated gate device, so that the insulated gate device switches between an off state and an on state in a second time period shorter than a specified rise time or fall time for the insulated gate device.
2. A triggering circuit as claimed in claim 1 wherein the insulated gate semiconductor device is a metal oxide semiconductor field effect transistor (MOSFET).

3. A triggering circuit as claimed in claim 2 wherein the MOSFET is a power MOSFET.

4. A triggering circuit as claimed in claim 1 wherein the insulated gate semiconductor device is an insulated gate bipolar transistor.

5. A triggering circuit as claimed in any one of the preceding claims wherein the first time period is shorter than 2ns.

6. A triggering circuit as claimed in any one of claims 1 to 5 wherein the fast switching means comprises one of: a SIDAC, a break-over diode, a bipolar transistor, another insulated gate semiconductor device and a high voltage fast switching device.

7. A triggering circuit as claimed in any one of claims 1 to 6 wherein the specified turn-on time is a minimum turn-on time
specified in a data sheet relating to the insulated gate semiconductor device.

8. A triggering circuit as claimed in any one of claims 1 to 7 wherein the fast switching means is electronically controllable.

9. A triggering circuit as claimed in any one of the preceding claims wherein the charge storage device is a capacitor.

10. A triggering circuit as claimed in any of the preceding claims wherein the insulated gate semiconductor device switches from the off state to the on state as well as from the on state to the off state in periods shorter than specified rise and fall times respectively.

11. A triggering circuit as claimed in any one of claims 1 to 10 comprising an inductor between the fast switching means and the gate.

12. A triggering circuit as claimed in any one of claims 1 to 11 which is integrated on a single chip.
13. A triggering circuit as claimed in claim 12 wherein the chip comprises additional circuitry also integrated thereon.

14. A method of driving an insulated gate semiconductor device comprising the steps of:

- utilizing a fast switching means to transfer charge to or from a gate of the device;

- switching the fast switching means on in a first time period shorter than a specified turn-on delay time of the insulated gate device;

- moving charge to or from the gate to cause the insulated gate device to switch between an off and an on state in a second time period shorter than a specified rise time or fall time for the insulated gate device.

15. A triggering circuit for an insulated gate semiconductor device substantially as herein described with reference to the accompanying diagrams.

16. A method of driving an insulated gate semiconductor device substantially as herein described with reference to the accompanying diagrams.
**FIGURE 3**

**FIGURE 4**
Figure 5

Figure 6

Figure 7