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[Continued on next page]

(54) Title: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

FIG. 1A

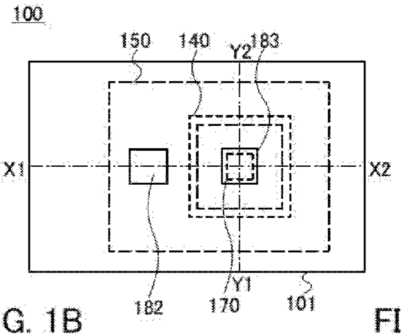


FIG. 1B

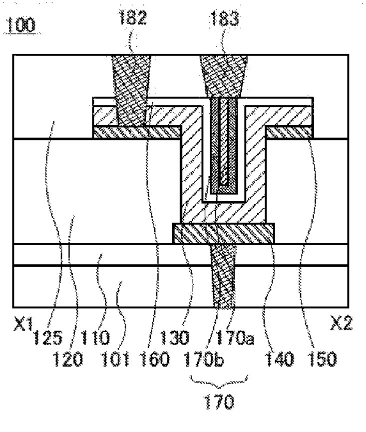
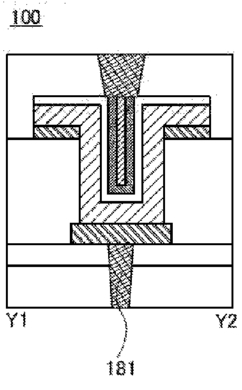


FIG. 1C



(57) Abstract: A miniaturized transistor having highly stable electrical characteristics is provided. Furthermore, high performance and high reliability of a semiconductor device including the transistor is achieved. The transistor includes a first electrode, a second electrode, a third electrode, an oxide semiconductor layer, a first insulating layer, and a second insulating layer. The transistor includes a first region and a second region surrounded by the first region. In the first region, the first insulating layer, the second electrode, the oxide semiconductor layer, and the second insulating layer are stacked. In the second region, the first electrode, the oxide semiconductor layer, the second insulating layer, and the third electrode are stacked.

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DESCRIPTION

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

TECHNICAL FIELD

[0001]

The present invention relates to, for example, an oxide, a transistor, a semiconductor device, and manufacturing methods thereof. The present invention relates to, for example, a display device, a liquid crystal display device, a light-emitting device, a lighting device, a power storage device, a memory device, a processor, an imaging device, and an electronic device. The present invention relates to methods for manufacturing a display device, a liquid crystal display device, a light-emitting device, a lighting device, a power storage device, a memory device, a processor, an imaging device, and an electronic device. The present invention relates to methods for driving a display device, a liquid crystal display device, a light-emitting device, a lighting device, a power storage device, a memory device, a processor, an imaging device, and an electronic device.

[0002]

Note that one embodiment of the present invention is not limited to the above technical field. The technical field of one embodiment of the invention disclosed in this specification and the like relates to an object, a method, or a manufacturing method. One embodiment of the present invention relates to a process, a machine, manufacture, or a composition of matter.

[0003]

In this specification and the like, a semiconductor device refers to any device that can function by utilizing semiconductor characteristics. A display device, a light-emitting device, a lighting device, an electro-optical device, a semiconductor circuit, and an electronic device include a semiconductor device in some cases.

BACKGROUND ART

[0004]

A technique for forming a transistor by using a semiconductor over a substrate having an insulating surface has attracted attention. The transistor is applied to a wide range of semiconductor devices such as an integrated circuit and a display device. Silicon is known as a semiconductor applicable to a transistor.

[0005]

As silicon which is used as a semiconductor of a transistor, either amorphous silicon or polycrystalline silicon is used depending on the purpose. For example, in the case of a transistor included in a large display device, it is preferable to use amorphous silicon, which can be used to form a film on a large substrate with the established technique. In the case of a transistor included in a high-performance display device where driver circuits are formed over the same substrate, it is preferable to use polycrystalline silicon, which can be used to form a transistor having high field-effect mobility. As a method for forming polycrystalline silicon, high-temperature heat treatment or laser light treatment which is performed on amorphous silicon has been known.

[0006]

In recent years, transistors including oxide semiconductors (typically, In-Ga-Zn oxide) have been actively developed.

[0007]

Oxide semiconductors have been researched since early times. In 1988, there was a disclosure of a crystal In-Ga-Zn oxide that can be used for a semiconductor element (see Patent Document 1). In 1995, a transistor including an oxide semiconductor was invented, and its electrical characteristics were disclosed (see Patent Document 2).

[0008]

In addition, a transistor including an amorphous oxide semiconductor is disclosed (see Patent Document 3). An oxide semiconductor can be formed by a sputtering method or the like, and thus can be used for a semiconductor of a transistor in a large display device. A transistor including an oxide semiconductor has high field-effect mobility; therefore, a high-performance display device where driver circuits are formed over the same substrate can be obtained. Moreover, there is an advantage that capital investment can be reduced because part of production equipment for a transistor including amorphous silicon can be retrofitted and utilized.

[0009]

It is known that a transistor including an oxide semiconductor has an extremely small leakage current in an off state. For example, a low-power-consumption CPU utilizing the small leakage current characteristic of a transistor including an oxide semiconductor is disclosed (see Patent Document 4). It is also disclosed that a transistor having high field-effect mobility can be obtained by a well potential formed using an active layer including an oxide semiconductor (see Patent Document 5).

[Reference]

[Patent Document]

[0010]

[Patent Document 1] Japanese Published Patent Application No. S63-239117

[Patent Document 2] Japanese translation of PCT international application No. H11-505377

[Patent Document 3] Japanese Patent No. 5215589

[Patent Document 4] Japanese Published Patent Application No. 2012-257187

[Patent Document 5] Japanese Published Patent Application No. 2012-59860

DISCLOSURE OF INVENTION

[0011]

However, miniaturization of transistors makes the manufacturing process complicated, leading to variations in characteristics of transistors.

[0012]

With use of an oxide semiconductor layer, the amount of off-state current of the transistor can be reduced. However, when oxygen vacancies are included in the oxide semiconductor layer, the electrical characteristics of the transistor might deteriorate.

[0013]

An object of one embodiment of the disclosed invention is to provide a transistor that can be miniaturized and highly integrated and has stable electrical characteristics. Another object of one embodiment of the disclosed invention is to provide a transistor whose channel length is easily controlled. Another object of one embodiment of the disclosed invention is to provide a transistor with a large channel width. Another object of one embodiment of the disclosed invention is to provide a transistor with large on-state current.

[0014]

Another object of one embodiment of the disclosed invention is to achieve high performance, high reliability, and high productivity of a semiconductor device including the transistor. Alternatively, an object of one embodiment of the disclosed invention is to provide a semiconductor device to which oxygen is easily supplied. Another object is to provide a novel semiconductor device. Note that the descriptions of these objects do not disturb the existence of other objects. Note that one embodiment of the disclosed invention does not necessarily achieve all the objects listed above. Other objects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

[0015]

A transistor provided in a semiconductor device includes a first electrode, a second electrode, a third electrode, an oxide semiconductor layer, a first insulating layer, and a second insulating layer. The transistor includes a first region and a second region surrounded by the first region. In the first region, the first insulating layer, the second electrode, the oxide semiconductor layer, and the second insulating layer are stacked. In the second region, the first electrode, the oxide semiconductor layer, the second insulating layer, and the third electrode are stacked.

[0016]

A transistor provided in a semiconductor device includes a first electrode, a second electrode having an opening, a third electrode, an oxide semiconductor layer, a first insulating layer, and a second insulating layer. The transistor includes a first region overlapping with the second electrode and a second region overlapping with the opening. In the first region, the first insulating layer, the second electrode, the oxide semiconductor layer, and the second insulating layer are stacked. In the second region, the first electrode, the oxide semiconductor layer, the second insulating layer, and the third electrode are stacked.

[0017]

A transistor provided in a semiconductor device includes a first electrode, a second electrode, a third electrode, an oxide semiconductor layer, a first insulating layer, and a second insulating layer. The second electrode and the first insulating layer have an opening. A side surface and a bottom surface of the third electrode are covered with the second insulating layer. The third electrode is embedded in the opening.

[0018]

In each of the above structures, the first insulating layer preferably contains oxygen.

[0019]

In each of the above structures, the first electrode functions as one of a source electrode and a drain electrode, and the second electrode functions as the other of the source electrode and the drain electrode.

[0020]

One embodiment of the present invention is an electronic device including any of the above semiconductor devices.

[0021]

In a vertical transistor, the channel length can be easily controlled by adjusting the thickness of the oxide semiconductor layer even when the transistor is miniaturized. Moreover, with a structure in which one of a source electrode and a drain electrode surrounds a side surface of a gate electrode with a gate insulating film and an oxide semiconductor layer provided therebetween, the effective channel width of the transistor can be increased. Accordingly, the amount of on-state current of the transistor can be increased.

[0022]

Furthermore, with a structure in which a region in the oxide semiconductor layer to be a channel is in contact with an insulating layer containing oxygen, oxygen can be supplied to the oxide semiconductor layer. Oxygen vacancies in the oxide semiconductor layer are filled with supplied oxygen, whereby the reliability of a transistor using the oxide semiconductor layer can be increased.

[0023]

With the above structures, a transistor with high and stable electrical characteristics can be provided even when the transistor is miniaturized.

[0024]

Also in a semiconductor device including the transistor, high performance, high reliability, and high productivity can be achieved. Alternatively, a novel semiconductor device can be provided. Note that the description of these effects does not disturb the existence of other effects. One embodiment of the present invention does not necessarily achieve all the effects listed above. Other effects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

BRIEF DESCRIPTION OF DRAWINGS

[0025]

FIG. 1A is a top view and FIGS. 1B and 1C are cross-sectional views illustrating one embodiment of a semiconductor device.

FIGS. 2A to 2C are cross-sectional views each illustrating one embodiment of a semiconductor device.

FIGS. 3A to 3C are top views each illustrating one embodiment of a semiconductor device.

FIGS. 4A and 4B are top views and FIG. 4C is a cross-sectional view illustrating embodiments of a semiconductor device.

FIGS. 5A to 5E are cross-sectional views illustrating one embodiment of a method for manufacturing a semiconductor device.

FIGS. 6A to 6D are cross-sectional views illustrating one embodiment of a method for manufacturing a semiconductor device.

FIGS. 7A to 7C are cross-sectional views illustrating one embodiment of a method for manufacturing a semiconductor device.

FIGS. 8A and 8B each illustrate an atomic ratio of an oxide semiconductor film of one embodiment of the present invention.

FIGS. 9A to 9C are Cs-corrected high-resolution TEM images of a cross section of a CAAC-OS and FIG. 9D is a cross-sectional schematic view of the CAAC-OS.

FIGS. 10A to 10D are Cs-corrected high-resolution TEM images of a plane of a CAAC-OS.

FIGS. 11A to 11C show structural analysis of a CAAC-OS and a single crystal oxide semiconductor by XRD.

FIGS. 12A and 12B show electron diffraction patterns of a CAAC-OS.

FIG. 13 shows changes in crystal parts of an In-Ga-Zn oxide by electron irradiation.

FIGS. 14A to 14D illustrate a deposition method of a CAAC-OS.

FIG. 15 illustrates a crystal structure of $\mathrm{In}M\mathrm{ZnO}_4$.

FIGS. 16A to 16E illustrate a deposition method of a CAAC-OS.

FIGS. 17A to 17C illustrate a deposition method of a CAAC-OS.

FIG. 18 illustrates a deposition method of an nc-OS.

FIGS. 19A, 19B, 19E, and 19F are cross-sectional views and FIGS. 19C and 19D are circuit diagrams illustrating embodiments of semiconductor devices.

FIG. 20 is a cross-sectional view illustrating one embodiment of a semiconductor device.

FIGS. 21A and 21B are cross-sectional views each illustrating one embodiment of a semiconductor device.

FIG. 22A is a cross-sectional view and FIGS. 22B and 22C are circuit diagrams illustrating embodiments of semiconductor devices.

FIG. 23 is a block diagram illustrating a CPU of one embodiment of the present invention.

FIG. 24 is a circuit diagram illustrating a memory element of one embodiment of the present invention.

FIG. 25A is a top view and FIGS. 25B and 25C are circuit diagrams of a display device of one embodiment of the present invention.

FIGS. 26A to 26F illustrate electronic devices of embodiments of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0026]

Embodiments will be described below with reference to the drawings. Note that the embodiments can be implemented with various modes, and it will be readily appreciated by those skilled in the art that modes and details can be changed in various ways without departing from the spirit and scope of the present invention. Thus, the present invention should not be interpreted as being limited to the following description of the embodiments.

[0027]

In the drawings, the size, the layer thickness, or the region is exaggerated for clarity in some cases. Therefore, embodiments of the present invention are not limited to such a scale. Note that the drawings are schematic views showing ideal examples, and embodiments of the present invention are not limited to shapes or values shown in the drawings. In the drawings, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and explanation thereof will not be repeated. The same hatching pattern is applied to portions having similar functions, and the portions are not especially denoted by reference numerals in some cases.

[0028]

Note that the ordinal numbers such as "first" and "second" in this specification and the like are used for convenience and do not denote the order of steps or the stacking order of layers. Therefore, for example, description can be made even when "first" is replaced with "second" or "third", as appropriate. In addition, the ordinal numbers in this specification and the like are not necessarily the same as those which specify one embodiment of the present invention.

[0029]

In this specification and the like, terms for explaining arrangement, such as over and under, are used for convenience to describe the positional relation between components with reference to drawings. The positional relation between components is changed as appropriate in accordance with a direction in which each component is described. Thus, the positional relation is not limited to that described with a term used in this specification and can be explained with another term as appropriate depending on the situation.

[0030]

The “semiconductor device” in this specification and the like means all devices which can operate by utilizing semiconductor characteristics. A semiconductor element such as a transistor, a semiconductor circuit, an arithmetic device, and a memory device are each an embodiment of a semiconductor device. An imaging device, a display device, a liquid crystal display device, a light-emitting device, an electro-optical device, a power generation device (including a thin film solar cell, an organic thin film solar cell, and the like), and an electronic device may each include a semiconductor device.

[0031]

In this specification and the like, a transistor is an element having at least three terminals: a gate, a drain, and a source. The transistor has a channel region between the drain (a drain terminal, a drain region, or a drain electrode) and the source (a source terminal, a source region, or a source electrode), and current can flow through the drain, the channel region, and the source. Note that in this specification and the like, a channel region refers to a region through which current mainly flows.

[0032]

Functions of a source and a drain are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flowing is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be replaced with each other in this specification and the like.

[0033]

Note that in this specification and the like, a silicon oxynitride film refers to a film in which the proportion of oxygen is higher than that of nitrogen. The silicon oxynitride film preferably contains oxygen, nitrogen, silicon, and hydrogen at concentrations ranging from 55 atomic% to 65 atomic%, 1 atomic% to 20 atomic%, 25 atomic% to 35 atomic%, and 0.1 atomic% to 10 atomic%, respectively. A silicon nitride oxide film refers to a film in which the proportion of nitrogen is higher than that of oxygen. The silicon nitride oxide film preferably contains nitrogen, oxygen, silicon, and hydrogen at concentrations ranging from 55 atomic% to 65 atomic%, 1 atomic% to 20 atomic%, 25 atomic% to 35 atomic%, and 0.1 atomic% to 10 atomic%, respectively.

[0034]

In this specification and the like, the terms “film” and “layer” can be interchanged with each other. For example, the term “conductive layer” can be changed into the term “conductive film” in some cases. Also, the term “insulating film” can be changed into the term “insulating layer” in some cases.

[0035]

In this specification and the like, the term "parallel" indicates that the angle formed between two straight lines is greater than or equal to −10° and less than or equal to 10°, and accordingly also includes the case where the angle is greater than or equal to −5° and less than or equal to 5°. In addition, the term "substantially parallel" indicates that the angle formed between two straight lines is greater than or equal to −30° and less than or equal to 30°. In addition, the term "perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 80° and less than or equal to 100°, and accordingly also includes the case where the angle is greater than or equal to 85° and less than or equal to 95°. In addition, the term "substantially perpendicular" indicates that the angle formed between two straight lines is greater than or equal to 60° and less than or equal to 120°.

[0036]

For example, in this specification and the like, an explicit description "*X* and *Y* are connected" means that *X* and *Y* are electrically connected, *X* and *Y* are functionally connected, and *X* and *Y* are directly connected. Accordingly, without being limited to a predetermined connection relationship, for example, a connection relationship shown in drawings or texts, another connection relationship is included in the drawings or the texts.

[0037]

Here, each of *X* and *Y* denotes an object (e.g., a device, an element, a circuit, a wiring, an electrode, a terminal, a conductive film, or a layer).

[0038]

Examples of the case where *X* and *Y* are directly connected include the case where an element that enables electrical connection between *X* and *Y* (e.g., a switch, a transistor, a capacitor, an inductor, a resistor, a diode, a display element, a light-emitting element, or a load) is not connected between *X* and *Y*, and the case where *X* and *Y* are connected without the element that enables electrical connection between *X* and *Y* provided therebetween.

[0039]

For example, in the case where *X* and *Y* are electrically connected, one or more elements that enable electrical connection between *X* and *Y* (e.g., a switch, a transistor, a capacitor, an inductor, a resistor, a diode, a display element, a light-emitting element, or a load) can be connected between *X* and *Y*. Note that the switch is controlled to be turned on or off. That is, the switch is conducting or not conducting (is turned on or off) to determine whether current flows therethrough or not. Alternatively, the switch has a function of selecting and changing a current path. Note that the case where *X* and *Y* are electrically connected includes the case where *X* and *Y* are directly connected.

[0040]

For example, in the case where *X* and *Y* are functionally connected, one or more circuits that enable functional connection between *X* and *Y* (e.g., a logic circuit such as an inverter, a NAND circuit, or a NOR circuit; a signal converter circuit such as a D/A converter circuit, an A/D converter circuit, or a gamma correction circuit; a potential level converter circuit such as a power supply circuit (e.g., a step-up circuit or a step-down circuit) or a level shifter circuit for changing the potential level of a signal; a voltage source; a current source; a switching circuit; an amplifier circuit such as a circuit that can increase signal amplitude, the amount of current, or the like, an operational amplifier, a differential amplifier circuit, a source follower circuit, or a buffer circuit; a signal generation circuit; a storage circuit; or a control circuit) can be connected between *X* and *Y*. Note that for example, in the case where a signal output from *X* is transmitted to *Y* even when another circuit is provided between *X* and *Y*, *X* and *Y* are functionally connected. The case where *X* and *Y* are functionally connected includes the case where *X* and *Y* are directly connected and *X* and *Y* are electrically connected.

[0041]

Note that in this specification and the like, an explicit description "*X* and *Y* are electrically connected" means that *X* and *Y* are electrically connected (i.e., the case where *X* and *Y* are connected with another element or another circuit provided therebetween), *X* and *Y* are functionally connected (i.e., the case where *X* and *Y* are functionally connected with another circuit provided therebetween), and *X* and *Y* are directly connected (i.e., the case where *X* and *Y* are connected without another element or another circuit provided therebetween). That is, in this specification and the like, the explicit description "*X* and *Y* are electrically connected" is the same as the explicit description "*X* and *Y* are connected."

[0042]

For example, the case where a source (or a first terminal or the like) of a transistor is electrically connected to *X* through (or not through) *Z*1 and a drain (or a second terminal or the like) of the transistor is electrically connected to *Y* through (or not through) *Z*2, or the case where a source (or a first terminal or the like) of a transistor is directly connected to part of *Z*1 and another part of *Z*1 is directly connected to *X* while a drain (or a second terminal or the like) of the transistor is directly connected to part of *Z*2 and another part of *Z*2 is directly connected to *Y*, can be expressed by using any of the following expressions.

[0043]

The expressions include, for example, "*X*, *Y*, a source (or a first terminal or the like) of a transistor, and a drain (or a second terminal or the like) of the transistor are electrically connected to each other, and *X*, the source (or the first terminal or the like) of the transistor, the drain (or the second terminal or the like) of the transistor, and *Y* are electrically connected to each other in that order," "a source (or a first terminal or the like) of a transistor is electrically connected to *X*, a drain (or a second terminal or the like) of the transistor is electrically connected to *Y*, and *X*, the source (or the first terminal or the like) of the transistor, the drain (or the second terminal or the like) of the transistor, and *Y* are electrically connected to each other in that order," and "*X* is electrically connected to *Y* through a source (or a first terminal or the like) and a drain (or a second terminal or the like) of a transistor, and *X*, the source (or the first terminal or the like) of the transistor, the drain (or the second terminal or the like) of the transistor, and *Y* are connected in that order." When the connection order in a circuit structure is defined by an expression similar to the above examples, a source (or a first terminal or the like) and a drain (or a second terminal or the like) of a transistor can be distinguished from each other to specify the technical scope.

[0044]

Other examples of the expressions include "a source (or a first terminal or the like) of a transistor is electrically connected to *X* through at least a first connection path, the first connection path does not include a second connection path, the second connection path is a path between the source (or the first terminal or the like) of the transistor and a drain (or a second terminal or the like) of the transistor, *Z*1 is on the first connection path, the drain (or the second terminal or the like) of the transistor is electrically connected to *Y* through at least a third connection path, the third connection path does not include the second connection path, and *Z*2 is on the third connection path." It is also possible to use the expression "a source (or a first terminal or the like) of a transistor is electrically connected to *X* through at least *Z*1 on a first connection path, the first connection path does not include a second connection path, the second connection path includes a connection path through the transistor, a drain (or a second terminal or the like) of the transistor is electrically connected to *Y* through at least *Z*2 on a third connection path, and the third connection path does not include the second connection path." Still another example of the expressions is "a source (or a first terminal or the like) of a transistor is electrically connected to *X* through at least *Z*1 on a first electrical path, the first electrical path does not include a second electrical path, the second electrical path is an electrical path from the source (or the first terminal or the like) of the transistor to a drain (or a second terminal or the like) of the transistor, the drain (or the second terminal or the like) of the transistor is electrically connected to *Y* through at least *Z*2 on a third electrical path, the third electrical path does not include a fourth electrical path, and the fourth electrical path is an electrical path from the drain (or the second terminal or the like) of the transistor to the source (or the first terminal or the like) of the transistor." When the connection path in a circuit structure is defined by an expression similar to the above examples, a source (or a first terminal or the like) and a drain (or a second terminal or the like) of a transistor can be distinguished from each other to specify the technical scope.

[0045]

Note that these expressions are examples and there is no limitation on the expressions. Here, *X*, *Y*, *Z*1, and *Z*2 each denote an object (e.g., a device, an element, a circuit, a wiring, an electrode, a terminal, a conductive film, or a layer).

[0046]

Even when independent components are electrically connected to each other in a circuit diagram, one component has functions of a plurality of components in some cases. For example, when part of a wiring also functions as an electrode, one conductive film functions as the wiring and the electrode. Thus, the term "electrical connection" in this specification also means such a case where one conductive film has functions of a plurality of components.

[0047]

(Embodiment 1)

In this embodiment, one embodiment of a semiconductor device is described with reference to FIGS. 1A to 1C, FIGS. 2A to 2C, FIGS. 3A to 3C, and FIGS. 4A to 4C.

[0048]

<Example of structure of semiconductor device>

FIG. 1A illustrates an example of a top view of a transistor 100. For simplicity, some films are not illustrated in FIG. 1A. FIG. 1B is a cross-sectional view taken along the dashed-dotted line X1-X2 in FIG. 1A, and FIG. 1C is a cross-sectional view taken along the dashed-dotted line Y1-Y2 in FIG. 1A.

[0049]

The transistor 100 is a vertical transistor which includes a first electrode 140 electrically connected to a wiring 181, a first insulating layer 120, a second electrode 150 electrically connected to a wiring 182, and an oxide semiconductor layer 130. The first electrode 140, the first insulating layer 120, and the second electrode 150 are stacked. The oxide semiconductor layer 130 is in contact with a top surface of the first electrode 140, a side surface of the first insulating layer 120, a side surface and a top surface of the second electrode 150. The second electrode 150 surrounds a third electrode 170 electrically connected to a wiring 183. Between the second electrode 150 and the third electrode 170, the oxide semiconductor layer 130 and a second insulating layer 160 are provided.

[0050]

The first electrode 140 has a function of one of a source and a drain, the second electrode 150 has a function of the other of the source and the drain, and the third electrode 170 has a function of a gate. Therefore, a channel is formed between the first electrode 140 and the second electrode 150.

[0051]

The second electrode 150 preferably surrounds a side surface of the third electrode 170 with the second insulating layer 160 and the oxide semiconductor layer 130 provided therebetween. The shape of the second electrode 150 is not limited to a polygonal ring shape as in FIG. 1A, and may be a ring shape with a rounded portion. The shape of the second electrode 150 is not limited to the ring shape, and may be a U-like shape, an L-like shape, an I-like shape, or a shape obtained by combining these shapes, for example.

[0052]

The third electrode 170 is preferably embedded in an opening in the second electrode 150. However, depending on the designed channel length and the thickness of the oxide semiconductor layer 130, the oxide semiconductor layer 130 and the second insulating layer 160 may fill the opening.

[0053]

The wiring 182 is electrically connected to the second electrode 150. The wiring 183 is electrically connected to the third electrode 170. The wiring 182 is provided over the second electrode 150 in FIGS. 1A to 1C, but not limited to this structure. For example, a bottom portion of the wiring 182 may be in contact with the first insulating layer 120. In addition, the wiring 183 is in contact with the second insulating layer 160 and the third electrode 170 in FIGS 1A to 1C, but not limited to this structure. A bottom portion of the wiring 183 may be in contact with only the third electrode 170.

[0054]

The first insulating layer 120 has an opening that reaches at least part of a top surface of the first electrode 140. The first insulating layer 120 is preferably an insulating layer containing oxygen, such as a silicon oxide film or a silicon oxynitride film.

[0055]

Note that as the first insulating layer 120, an insulating layer containing excessive oxygen (containing oxygen in excess of stoichiometric composition) is preferably used. When such an insulating layer containing excess oxygen is provided in contact with the oxide semiconductor layer 130, oxygen vacancies in the oxide semiconductor layer 130 are compensated.

[0056]

The oxide semiconductor layer 130 is in contact with the top surface of the first electrode 140, a side surface of the first insulating layer 120 in the opening, and the top and side surfaces of the second electrode 150.

[0057]

An oxide semiconductor that forms the oxide semiconductor layer 130 has a wide energy gap of 3.0 eV or more. A transistor including an oxide semiconductor film obtained by processing of the oxide semiconductor in an appropriate condition and a sufficient reduction in carrier density of the oxide semiconductor can have much smaller leakage current between a source and a drain in an off state (off-state current) than a conventional transistor including silicon.

[0058]

An influence of impurities in the oxide semiconductor layer 130 is described below. In order to obtain stable electrical characteristics of a transistor, it is effective to reduce the concentration of impurities in the oxide semiconductor layer 130 to have lower carrier density so that the oxide semiconductor layer 130 is highly purified. The carrier density of the oxide semiconductor layer 130 is set to be higher than or equal to 1×10^{-9} /cm^3, and lower than 8×10^{11} /cm^3, preferably lower than 1×10^{11} /cm^3, further preferably lower than 1×10^{10} /cm^3. In order to reduce the concentration of impurities in the oxide semiconductor layer 130, the concentration of impurities in a film adjacent to the oxide semiconductor layer 130 is preferably reduced.

[0059]

When nitrogen is contained in the oxide semiconductor layer 130, the carrier density is increased in some cases. The concentration of nitrogen in the oxide semiconductor layer 130 measured by SIMS is set to be lower than 5×10^{19} atoms/cm^3, preferably lower than or equal to 5×10^{18} atoms/cm^3, further preferably lower than or equal to 1×10^{18} atoms/cm^3, still further preferably lower than or equal to 5×10^{17} atoms/cm^3.

[0060]

When hydrogen is contained in the oxide semiconductor layer 130, the carrier density is increased in some cases. Furthermore, hydrogen contained in the oxide semiconductor layer 130 as an impurity is moved to the surface of the semiconductor layer and bonds to oxygen near the surface, whereby a water molecule is formed and released in some cases. At this time, an oxygen vacancy V_0 is formed in a site of O that has been released as a water molecule. For this reason, it is preferable to reduce sufficiently the concentration of hydrogen in the oxide semiconductor layer 130. Therefore, the amount of water molecules in the oxide semiconductor layer 130 detected by thermal desorption spectroscopy (TDS) (converted into the number of water molecules) is 1.0×10^{21} /cm^3 (1.0 /nm^3) or less, preferably 1.0×10^{20} /cm^3 (0.1 /nm^3) or less at a surface temperature ranging from 100 °C to 700 °C or 100 °C to 500 °C.

[0061]

Here, the method of measuring the amount of released oxygen using TDS analysis is described below.

[0062]

The total amount of released gas from a measurement sample in TDS analysis is proportional to the integral value of the ion intensity of the released gas. Then, comparison with a reference sample is made, whereby the total amount of released gas can be calculated.

[0063]

For example, the number of released water molecules (N_{H2O}) from a measurement sample can be calculated according to the following formula using the TDS results of a silicon substrate containing hydrogen at a predetermined density, which is a reference sample, and the TDS results of the measurement sample. Here, all gases having a mass-to-charge ratio of 18 which are obtained in the TDS analysis are assumed to originate from an water molecule. Note that CH_4, which is a gas having the mass-to-charge ratio of 18, is not taken into consideration because it is unlikely to be present. Furthermore, an oxygen molecule including an oxygen atom having a mass number of 17 or 18 which is an isotope of an oxygen atom is also not taken into consideration because the proportion of such a molecule in the natural world is minimal.

Further, a water molecule including a hydrogen molecule having a mass number of 2 or 3 which is an isotope of hydrogen and a water molecule including an oxygen atom having a mass number of 17 or 18 which is an isotope of an oxygen atom are not taken into consideration because the proportions of such molecules in the natural world are minimal.

[0064]

[Formula 1]

$$N_{\mathrm{H2O}} = \frac{N_{\mathrm{H2}}}{\mathrm{S}_{\mathrm{H2}}} \times \mathrm{S}_{\mathrm{H20}} \times \alpha$$

[0065]

The value N_{H2} is obtained by conversion of the number of hydrogen molecules desorbed from the reference sample into densities. The value S_{H2} is the integral value of ion intensity in the case where the reference sample is subjected to the TDS analysis. Here, the reference value of the reference sample is set to N_{H2}/S_{H2}. The value S_{H2O} is the integral value of ion intensity when the measurement sample is analyzed by TDS. The value α is a coefficient affecting the ion intensity in the TDS analysis. Refer to Japanese Published Patent Application No. H6-275697 for details of the above formula. The amount of released oxygen is measured with, for example, a thermal desorption spectroscopy apparatus produced by ESCO Ltd., EMD-WA1000S/W using a silicon substrate containing a certain amount of hydrogen atoms as the reference sample.

[0066]

Note that N_{H2O} is the number of the released water molecules. The number of released water molecules in the case of being converted into hydrogen atoms is twice the number of the released water molecules.

[0067]

Note that it is difficult for hydrogen as an impurity in the semiconductor to exist as a water molecule because the hydrogen is in a state of a hydrogen atom, a hydrogen ion, a hydrogen molecule, a hydroxy group, a hydroxide ion, and the like in the semiconductor.

[0068]

By using an oxide semiconductor including a crystal whose hydrogen concentration is sufficiently lowered for a channel formation region in a transistor, the transistor can have stable electric characteristics. That is, a change in electrical characteristics can be inhibited and reliability can be improved. Furthermore, a semiconductor device with low power consumption can be provided.

[0069]

In the semiconductor device illustrated in FIG. 1A, the transistor 100 is provided over a substrate 101. A base film 110 may be formed over the substrate 101. In addition to the base film 110, a barrier film may be stacked. An insulating layer 125 is provided to cover the transistor 100. In addition to the insulating layer 125, a barrier film may be stacked.

[0070]

As the barrier film, an insulating film having barrier properties against oxygen and hydrogen is preferably used. Examples of such an insulating film can include an aluminum oxide film. When such a material is used, the barrier film has a function of suppressing release of oxygen from the oxide semiconductor layer 130 and diffusion of oxygen to portions other than the oxide semiconductor layer 130 from the first insulating layer 120, and also have a function of preventing entry of impurities such as hydrogen from the outside.

[0071]

The insulating film containing excess oxygen is provided in contact with the oxide semiconductor layer and surrounded by the barrier films, whereby the composition of the oxide semiconductor layer can be almost the same as the stoichiometric composition or in a supersaturated state containing more oxygen than the stoichiometric composition. It is also possible to prevent entry of impurities such as hydrogen into the oxide semiconductor layer.

[0072]

<Modification example 1 of semiconductor device>

FIGS. 2A to 2C are cross-sectional views illustrating modification examples of the transistor 100.

[0073]

As illustrated in FIG. 2A, the first insulating layer 120 and the second electrode 150 in the opening may have a sloped side surface. Owing to this sloped side surface, the channel length can be longer than the thickness obtained by subtracting the thickness of the first electrode 140 from the thickness of the first insulating layer 120. Moreover, the distance between the first electrode 140 and the second electrode 150 can be adjusted with the sloped side surface; whereby the generation of the parasitic capacitance can be prevented.

[0074]

In the case where the thickness of the first insulating layer 120 is small as illustrated in FIG. 2B, the sloped side surface of the first insulating layer 120 and the second electrode 150 in the opening is made gentle, whereby a reduction in the channel length can be prevented. In addition, the film coverage with a film to be formed at a subsequent step can be improved when the side surface is gently sloped. Therefore, an angle θ formed between the top surface of the first electrode 140 and the side surface of the first insulating layer 120 is greater than or equal to 5° and less than or equal to 85°, preferably greater than or equal to 25° and less than or equal to 75°.

[0075]

As illustrated in FIG. 2C, an insulator 190 and an insulator 195 (an insulator 195a and an insulator 195b) may be formed. These insulators serves as layers that prevent oxygen release from the oxide semiconductor layer 130, oxygen diffusion from the first insulating layer 120 to a layer other than the oxide semiconductor layer 130, and entry of an impurity (e.g., hydrogen) from the outside.

[0076]

Note that the insulator 195 in FIG. 2C includes the insulator 195a and the insulator 195b, but is not limited to this structure. For example, the insulator may be formed also in a region along the side surface of the first insulating layer 120 in the opening, that is, the insulator 195 may be a continuous film in which a gap between the insulator 195a and the insulator 195b is filled. The insulator 195 functions as a layer that prevents oxygen release from the oxide semiconductor layer 130 and supplies oxygen to the oxide semiconductor layer 130.

[0077]

The insulating film containing excess oxygen is provided in contact with the oxide semiconductor layer and surrounded by the barrier films, whereby the composition of the oxide semiconductor layer can be almost the same as the stoichiometric composition or in a supersaturated state containing more oxygen than the stoichiometric composition. It is also possible to prevent entry of impurities such as hydrogen into the oxide semiconductor layer.

[0078]

As illustrated in FIGS. 3A to 3C, the shapes of the electrodes and the layers may be a rectangular shape, a circular shape, an elliptical shape, a polygonal shape, or a shape having a curve. As illustrated in FIGS. 3B and 3C, part of the second electrode 150 may be projected. For example, when part of the second electrode 150 is projected, a portion in contact with a wiring or the like can be easily formed even in a miniaturized transistor.

[0079]

The top surface shape of the second electrode 150 may be a circular ring shape or a polygonal ring shape. The shape of the second electrode 150 is not limited to the ring shapes, and may be a U-like shape, an L-like shape, or an I-like shape, or a shape obtained by combining these shapes, for example.

[0080]

<Modification example 2 of semiconductor device>

FIGS. 4A to 4C illustrate a transistor 200 and a transistor 300. FIGS. 4A and 4B are top views illustrating examples of the transistor 200 and the transistor 300. FIG. 4C is a cross-sectional view taken along the dashed-dotted line X1-X2 in FIG. 4A.

[0081]

The first electrode 140, the second electrode 150, and the oxide semiconductor layer 130 included in the transistor 100 are divided to form two transistors, whereby a semiconductor device with higher integration degree of transistors can be manufactured.

[0082]

For example, as illustrated in FIG. 4A, first electrodes, second electrodes, and oxide semiconductor layers are line-symmetrically disposed and the second insulating layer 160, and the third electrode 170 are commonly used in the transistor 200 and the transistor 300. Thus, a wiring 281 electrically connected to the first electrode and a wiring 282 electrically connected to the second electrode are formed in the transistor 200; a wiring 381 electrically connected to the first electrode and a wiring 382 electrically connected to the second electrode are provided in the transistor 300. Note that the transistor 200 and the transistor 300 can operate in different manners by dividing the third electrode 170.

[0083]

Alternatively, as illustrated in FIG. 4B, the first electrodes, the second electrodes, and the oxide semiconductor layers are point-symmetrically disposed, and the second insulating layer 160 and the third electrode 170 are commonly used in the transistor 200 and the transistor 300.

[0084]

The shape of the second electrode is not limited to an L-like shape, and may be a U-like shape, a circular shape, or the like. Part of the second electrode may be projected to be connected to a wiring. When part of the second electrode is projected, a portion in contact with a wiring or the like can be easily formed even in a miniaturized transistor.

[0085]

In Embodiment 1, one embodiment of the present invention has been described. Other embodiments of the present invention are described in Embodiments 2 to 4. Note that one embodiment of the present invention is not limited to these. That is, since various embodiments of the present invention are disclosed in Embodiments 1 to 4, one embodiment of the present invention is not limited to a specific embodiment. For example, examples in which channel formation regions, source and drain regions, and the like of the transistors 100, 200, and 300 include an oxide semiconductor are described as embodiments of the present invention; however, one embodiment of the present invention is not limited to these examples. Depending on circumstances or conditions, the channel formation regions, the source and drain regions, and the like of the transistors 100, 200, and 300 in embodiments of the present invention may include various semiconductors. Depending on circumstances or conditions, for example, the channel formation regions, the source and drain regions, and the like of the transistors 100, 200, and 300 may include at least one of silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, aluminum gallium arsenide, indium phosphide, gallium nitride, an organic semiconductor, and the like. Alternatively, depending on circumstances or conditions, the channel formation regions, the source and drain regions, and the like of the transistors 100, 200, and 300 do not necessarily include an oxide semiconductor in embodiments of the present invention.

[0086]

(Embodiment 2)

In this embodiment, an example of a method for manufacturing a semiconductor device is described with reference to FIGS. 5A to 5E, FIGS. 6A to 6D, and FIGS. 7A to 7C.

[0087]

Note that common portions to those in FIGS. 1A to 1C, FIGS. 2A to 2C, FIGS. 3A to 3C, and FIGS. 4A to 4C are denoted by the same reference numerals, and description thereof is omitted.

[0088]

An example of a method for manufacturing the semiconductor device illustrated in FIG. 2C is described with reference to FIGS. 5A to 5E, FIGS. 6A to 6D, and FIGS. 7A to 7C.

[0089]

First, the substrate 101 is prepared. There is no particular limitation on a substrate that can be used as the substrate 101 as long as it has heat resistance high enough to withstand heat treatment performed later. For example, a glass substrate of barium borosilicate glass, aluminoborosilicate glass, or the like, a ceramic substrate, a quartz substrate, or a sapphire substrate can be used. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate of silicon or silicon carbide; a compound semiconductor substrate of silicon germanium, gallium arsenide, indium arsenide, or indium gallium arsenide; a silicon-on-insulator (SOI) substrate; a germanium-on-insulator (GOI) substrate; or the like can be used. Further alternatively, any of these substrates provided with a semiconductor element may be used.

[0090]

A flexible substrate may be used as the substrate to manufacture the semiconductor device. To manufacture a flexible semiconductor device, a transistor may be directly formed over a flexible substrate; or alternatively, a transistor may be formed over a substrate and then separated from the substrate and transferred to a flexible substrate. For separation of the transistor from the substrate and transfer to the flexible substrate, a separation layer is preferably provided between the substrate and the transistor including the oxide semiconductor film.

[0091]

First, the base film 110 is formed over the substrate 101. The base film 110 can be formed to have a single-layer structure or a stacked-layer structure using, for example, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, aluminum oxide, aluminum oxynitride, aluminum nitride oxide, aluminum nitride, or the like. The base film 110 is preferably formed using silicon nitride containing oxygen and hydrogen (SiNOH) because the amount of hydrogen released by heating can be increased. Alternatively, the base film 110 can also be formed using silicon oxide with high step coverage that is formed by reacting tetraethyl orthosilicate (TEOS), silane, or the like with oxygen, nitrous oxide, or the like.

[0092]

The base film 110 can be formed by, for example, a sputtering method, a CVD method (including a thermal CVD method, an MOCVD method, a PECVD method, and the like), an MBE method, an ALD method, a PLD method, or the like. In particular, it is preferable that the insulating film be formed by a CVD method, more preferably, a plasma CVD method because coverage can be improved. It is preferable to use a thermal CVD method, an MOCVD method, or an ALD method in order to reduce plasma damage.

[0093]

Next, the insulator 190 is formed. As the insulator 190, it is preferable to form an insulating film having barrier properties against oxygen and hydrogen, for example. Examples of such an insulating film includes an aluminum oxide film, an aluminum oxynitride film, a gallium oxide film, a gallium oxynitride film, an yttrium oxide film, an yttrium oxynitride film, a hafnium oxide film, a hafnium oxynitride film, and a silicon nitride film.

[0094]

The wiring 181 electrically connected to the first electrode 140 may be formed. Note that the wiring 181 can be formed with a conductive material, such as a metal material, an alloy material, or a metal oxide material. In particular, the wiring 181 is preferably formed with a low-resistance conductive material, such as aluminum or copper. The use of the material as described above can reduce the wiring resistance. In consideration of the formation of the transistor 100 at a subsequent step, the wiring 181 is preferably formed as an embedded wiring with high planarity.

[0095]

Next, as illustrated in FIG. 5A, a conductive film 140A to be the electrode 140 is formed. As the conductive film 140A, a metal film containing an element selected from molybdenum, titanium, tantalum, tungsten, aluminum, copper, chromium, neodymium, and scandium; a metal nitride film containing any of the above elements as its component (e.g., a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film); or the like can be used. Alternatively, a semiconductor film typified by a polycrystalline silicon film doped with an impurity element such as phosphorus, or a silicide film such as a nickel silicide film may be used as the conductive film 140A. Alternatively, a conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added can be used. Moreover, the conductive film 140A can have a stacked structure of the above conductive material and the above metal material. For example, a 5-nm-thick titanium film, a 10-nm-thick titanium nitride film, and a 100-nm-thick tungsten film may be stacked.

[0096]

The conductive film 140A can be formed by, for example, a sputtering method, an evaporation method, or a CVD method (including a thermal CVD method, an MOCVD method, a PECVD method, and the like). To reduce plasma damage, a thermal CVD method, an MOCVD method, or an ALD method is preferred.

[0097]

Next, a resist mask 145 is formed over the conductive film 140A by a lithography process or the like, and an unnecessary portion of the conductive film 140A is removed. After that, the resist mask 145 is removed. In this manner, the first electrode 140 can be formed (FIGS. 5B and 5C).

[0098]

A method for processing a film is described. In the case of finely processing a film, a variety of fine processing techniques can be used. For example, a method may be used in which a resist mask formed by a lithography process or the like is subjected to slimming treatment. Alternatively, a dummy pattern is formed by a lithography process or the like, the dummy pattern is provided with a sidewall and then removed, and a film is etched using the remaining sidewall as a resist mask. To achieve a high aspect ratio, anisotropic dry etching is preferably used for etching of a film. Alternatively, a hard mask formed of an inorganic film or a metal film may be used.

[0099]

As light used to form the resist mask, for example, light with an i-line (with a wavelength of 365 nm), light with a g-line (with a wavelength of 436 nm), light with an h-line (with a wavelength of 405 nm), or light in which the i-line, the g-line, and the h-line are mixed can be used. Alternatively, ultraviolet light, KrF laser light, ArF laser light, or the like can be used. Exposure may also be performed by a liquid immersion exposure technique. As the light for the exposure, extreme ultra-violet light (EUV) or X-rays may be used. Instead of the light for the exposure, an electron beam can be used. It is preferable to use EUV, X-rays, or an electron beam because extremely fine processing can be performed. Note that in the case of performing exposure by scanning of a beam, such as an electron beam, a photomask is not needed.

[0100]

Before a resist film that is processed into the resist mask is formed, an organic resin film having a function of improving adhesion between a film and the resist film may be formed. The organic resin film can be formed by, for example, a spin coating method to planarize a surface by covering a step thereunder and thus can reduce variation in thickness of the resist mask over the organic resin film. In the case of fine processing, in particular, a material serving as an anti-reflection film against light for the exposure is preferably used for the organic resin film. Examples of such an organic resin film serving as an anti-reflection film include a bottom anti-reflection coating

(BARC) film. The organic resin film may be removed at the same time as the removal of the resist mask or after the removal of the resist mask.

[0101]

Next, an insulating film 120A is formed over the first electrode 140. The insulating film 120A is an insulating film containing oxygen, such as a silicon oxide film or a silicon oxynitride film.

[0102]

The insulating film 120A is preferably an insulating film containing excess oxygen. As the insulating film containing excess oxygen, a silicon oxide film or a silicon oxynitride film containing a large amount of oxygen can be formed by a plasma CVD method or a sputtering method under the conditions that are set as appropriate. After the silicon oxide film or the silicon oxynitride film is formed, oxygen may be added by an ion implantation method, an ion doping method, or plasma treatment.

[0103]

The insulating film 120A may have a stacked-layer structure. For example, it is preferable that an oxide film formed by a sputtering method be stacked over an insulating film formed by a plasma CVD method. By the sputtering method, an oxygen-excess region can be formed easily in a silicon oxide film formed by the plasma CVD method.

[0104]

In the film formation by a sputtering method, ions in plasma are accelerated and collide with a target, so that particles sputtered from the target are ejected. These sputtered particles attach to a deposition surface, thereby forming a film. Some ions recoil by the target and might be taken into a component below the formed film as recoil ions. The ions in the plasma might collide with the deposition surface. Some ions reach the inside of the component below the formed film. The ions are taken into the component, whereby a region into which the ions are excessively taken is formed in the component. That is, an oxygen-excess region is formed in the component in the case where the ions include oxygen.

[0105]

Next, a conductive film 150A and a conductive film 150B are formed over the insulating film 120A by a sputtering method, an evaporation method, a CVD method, or the like. The insulating film 120A, the conductive film 150A, and the conductive film 150B are etched to form an opening; whereby the first insulating layer 120 and the conductive films 150A and 150B having the opening are formed. From the opening, the first electrode 140 is exposed (see FIGS. 5D and 5E).

[0106]

The conductive films 150A and 150B can be formed using a metal film containing an element selected from molybdenum, titanium, tantalum, tungsten, aluminum, copper, chromium, neodymium, and scandium; a metal nitride film containing any of the above elements as its component (e.g., a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film); or the like. Alternatively, a semiconductor film typified by a polycrystalline silicon film doped with an impurity element such as phosphorus, or a silicide film such as a nickel silicide film may be used as a material of the conductive films 150A and 150B. Alternatively, a conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added can also be used. Moreover, a stacked structure of the above conductive material and the above metal material may be employed. For example, a 5-nm-thick titanium film, a 10-nm-thick titanium nitride film, and a 100-nm-thick tungsten film may be stacked.

[0107]

In this embodiment, the conductive film 150A is preferably formed with tungsten. The conductive film 150B is preferably formed with a material that can be etched together with the conductive film 150A. In the case where tungsten is used for the conductive film 150A and for a hard mask 135 that is used at a subsequent step of etching an oxide semiconductor film 130A, the conductive film 150A and the conductive film 150B can be etched simultaneously when the hard mask 135 is removed. That is, the second electrode 150 can be formed at the same time when the hard mask 135 is removed.

[0108]

Next, the oxide semiconductor film 130A is formed over and in contact with the first insulating layer 120, the conductive films 150A and 150B provided with the opening, and the exposed first electrode 140. For the formation of the oxide semiconductor film 130A, a sputtering method, a coating method, a molecular beam epitaxy (MBE) method, a CVD method, a pulsed laser deposition method, an atomic layer deposition (ALD) method, or the like can be used as appropriate.

[0109]

For example, in the case where the oxide semiconductor film 130A is formed by a sputtering method, the substrate temperature is set to higher than or equal to 100 °C and lower than or equal to 500 °C, preferably higher than or equal to 150°C and lower than or equal to 450 °C, and the parcentage of oxygen in a deposition gas is set to higher than or equal to 30 vol%, preferably 100 vol%.

[0110]

An applicable oxide semiconductor preferably contains at least one of indium (In) and zinc (Zn), and more preferably contains In and Zn. In addition, as a stabilizer for reducing variation in electric characteristics of the transistor including an oxide semiconductor, one or more selected from gallium (Ga), tin (Sn), hafnium (Hf), zirconium (Zr), titanium (Ti), scandium (Sc), yttrium (Y), and an lanthanoid (e.g., cerium (Ce), neodymium (Nd), or gadolinium (Gd)) are preferably contained.

[0111]

Here, the case where an oxide semiconductor film contains indium, an element M, and zinc is considered. Here, the element M is preferably aluminum, gallium, yttrium, tin, or the like. Other elements that can be used as the element M are boron, silicon, titanium, iron, nickel, germanium, zirconium, molybdenum, lanthanum, cerium, neodymium, hafnium, tantalum, tungsten, and the like. Note that two or more of the above elements may be used in combination as the element M. A favorable range of the atomic ratio of indium to the element M and zinc (x:y:z) of the oxide semiconductor film is described with reference to FIGS. 8A and 8B.

[0112]

FIGS. 8A and 8B show the range of the atomic ratio of indium to the element M and zinc of the oxide semiconductor film. Here, FIGS. 8A and 8B show an example in which the element M is Ga. Note that the proportion of oxygen atoms is not shown in FIGS. 8A and 8B.

[0113]

For example, it is known that there is a homologous series represented by $\mathrm{In}M\mathrm{O}_3(\mathrm{ZnO})_m$ (m is a natural number) as one of oxides containing indium, the element M, and zinc. Here, for example, the case where the element M is Ga is considered. It is known that regions denoted by thick lines in FIGS. 8A and 8B indicate compositions which allow a single-phase solid solution range when powders of $\mathrm{In_2O_3}$, $\mathrm{Ga_2O_3}$, and ZnO are mixed and sintered at 1350 °C, for example. Coordinates denoted by square symbols in FIGS. 8A and 8B correspond to known compositions with which a spinel crystal structure is likely to be mixed.

[0114]

For example, a compound represented by $\mathrm{Zn}M_2\mathrm{O}_4$, such as $\mathrm{ZnGa_2O_4}$, is known as having a spinel crystal structure. Furthermore, when a composition is in the neighborhood of $\mathrm{ZnGa_2O_4}$ as illustrated in FIGS. 8A and 8B, that is, the ratio of x to y and z is close to 0:1:2, a spinel crystal structure is likely to be formed or mixed.

[0115]

Here, the oxide semiconductor film is preferably a CAAC-OS film. Specifically, the CAAC-OS film having no spinel crystal structure is preferred. In addition, to increase carrier mobility, the indium content is preferably increased. In an oxide semiconductor containing indium, the element M, and zinc, the s orbital of heavy metal mainly contributes to carrier transfer, and when the indium content in the oxide semiconductor is increased, overlaps of the s orbitals of In atoms are increased; therefore, an oxide having a high content of indium has higher mobility than an oxide having a low content of indium. Therefore, an oxide having a high content of indium is used as an oxide semiconductor film, whereby the carrier mobility can be increased.

[0116]

Accordingly, the atomic ratio of indium to the element M and zinc, x:y:z, of the oxide semiconductor film is preferably within the range of an area 11 shown in FIG. 8B, for example. Here, the area 11 includes atomic ratios within the range of an area surrounded by line segments that connect first coordinates K (x:y:z = 8:14:7), second coordinates L (x:y:z = 2:5:7), third coordinates M (x:y:z = 51:149:300), fourth coordinates N (x:y:z = 46:288:833), fifth coordinates O (x:y:z = 0:2:11), sixth coordinates P (x:y:z = 0:0:1), seventh coordinates Q (x:y:z = 1:0:0) and the first coordinates K, in this order. Note that the area 11 also includes coordinates positioned on the line segments.

[0117]

When x:y:z is within the area 11 in FIG. 8B, a spinel crystal structure is not observed or is hardly observed by nanobeam electron diffraction. Thus, an excellent CAAC-OS film can be obtained. Furthermore, carrier scattering or the like at the boundary between a CAAC structure and a spinel crystal structure can be reduced; therefore, when the oxide semiconductor film is used for a transistor, the transistor can have high field-effect mobility. In addition, the transistor can have high reliability.

[0118]

In the case where the oxide semiconductor film is formed by a sputtering method, a film having an atomic ratio deviated from the atomic ratio of the target is formed in some cases. Especially for zinc, the proportion of zinc atoms of a deposited film is smaller than that of zinc atoms of the target in some cases. Specifically, the proportion of zinc atoms of the film may be approximately 40 % to 90 % of the proportion of zinc atoms of the target. The target used here is preferably polycrystalline.

[0119]

The oxide semiconductor film 130A may have a stacked-layer structure of n layers (n is two or more) instead of a single-layer structure. Furthermore, the films may differ in the CAAC proportion. In addition, at least one of the stacked films preferably has a CAAC proportion of higher than 90 %, further preferably higher than or equal to 95 %, still further preferably higher than or equal to 97 % and lower than or equal to 100 %.

[0120]

For example, when a second semiconductor is formed over a first semiconductor in which impurities are reduced, the second semiconductor can have fewer impurities than the first semiconductor and prevent diffusion of impurities from layers positioned below the second semiconductor. In the case where a layer is additionally stacked over the oxide semiconductor film 130A in a subsequent step, forming a third semiconductor with a small thickness over the second semiconductor can prevent diffusion of impurities from the upper layer of the oxide semiconductor film 130A to the second semiconductor. By using a transistor formed such that the second semiconductor in which impurities are reduced serves as a channel region, a highly reliable semiconductor device can be provided.

[0121]

The thickness of the oxide semiconductor film 130A is greater than or equal to 1 nm and less than or equal to 500 nm, preferably greater than or equal to 1 nm and less than or equal to 300 nm, for example.

[0122]

After the oxide semiconductor film 130A is formed, heat treatment is preferably performed. The heat treatment is performed at a temperature higher than or equal to 250 °C and lower than or equal to 650 °C, preferably higher than or equal to 300 °C and lower than or equal to 500 °C, in an inert gas atmosphere, an atmosphere containing an oxidizing gas at 10 ppm or more, or a reduced pressure atmosphere. Alternatively, the heat treatment may be performed in such a manner that heat treatment is performed in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more in order to compensate released oxygen. The heat treatment here can remove impurities such as hydrogen and water from the oxide semiconductor film 130A. By this heat treatment, oxygen can be supplied from the first insulating layer 120 to the oxide semiconductor film 130A. At this time, the first insulating film 120 and the insulating layer 104 preferably contain excess oxygen, in which case oxygen can be supplied efficiently to the oxide semiconductor film 130A. Note that the heat treatment may be performed after the oxide semiconductor film 130A is processed into an island shape to form the oxide semiconductor layer 130.

[0123]

Next, an insulating film 160A is formed over the oxide semiconductor film 130A. The insulating film 160A has a thickness greater than or equal to 1 nm and less than or equal to 20 nm and can be formed by a sputtering method, an MBE method, a CVD method, a pulsed laser deposition method, an ALD method, or the like as appropriate. The insulating film 160A may be formed with a sputtering apparatus which performs deposition in the state where surfaces of a plurality of substrates are substantially perpendicular to a surface of a sputtering target. A metal organic chemical vapor deposition (MOCVD) method may be used. For example, a gallium oxide film formed by an MOCVD method can be used as the insulating film 160A.

[0124]

The insulating film 160A can be formed using a silicon oxide film, a gallium oxide film, a gallium zinc oxide film, a zinc oxide film, an aluminum oxide film, a silicon nitride film, a silicon oxynitride film, an aluminum oxynitride film, or a silicon nitride oxide film. It is preferable that the insulating film 160A contain oxygen in a portion in contact with the oxide semiconductor film 130A. In particular, the insulating film 160A preferably contains an amount of oxygen which exceeds the stoichiometric composition in the film (bulk). In this embodiment, a silicon oxynitride film formed by a CVD method is used as an insulating film. By using a silicon oxynitride film containing excess oxygen as a gate insulating film, oxygen can be supplied to the oxide semiconductor film 130A, leading to good characteristics. Furthermore, the insulating film 160A is processed into the second insulating layer 160 in a subsequent step; thus, formation of the insulating film 160A is preferably performed in consideration of the size and the like, of the transistor 100.

[0125]

Alternatively, the insulating film 160A can be formed using a high-k material such as hafnium oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0, y > 0$)), hafnium silicate to which nitrogen is added ($HfSi_xO_yN_z$ ($x > 0, y > 0, z > 0$)), hafnium aluminate ($HfAl_xO_y$ ($x > 0, y > 0$)), or lanthanum oxide. The insulating film 160A may have a single-layer structure or a stacked-layer structure (FIG. 6A).

[0126]

Then, the insulators 195A and 195b are formed. The insulator 195 is preferably formed with an insulator having barrier properties. Each of the insulators 195A and 195b can be formed with a single layer or stacked layers using, for example, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, aluminum oxide, aluminum oxynitride, aluminum nitride oxide, aluminum nitride, or the like.

[0127]

An insulator is not formed on a surface of the insulating film 160A that covers a region in the oxide semiconductor film 130A to be a channel, that is, a region in the oxide semiconductor film 130A in contact with the side surface of the first insulating layer 120 in the opening (also referred to as a side surface of the opening) (FIG. 6B).

[0128]

For this reason, for example, the insulator 195A and the insulator 195b are formed by a collimated sputtering method, a long throw sputtering method, or the like, in which case the insulator the insulator can be formed only in regions other than a region along the side surfaces of the opening.

[0129]

The method for forming the insulator 195A and the insulator 195b is not limited to the methods described above. For example, the insulator 195A and the insulator 195b may be formed in such a manner that an insulator is formed to cover the entire surface of the insulating film 160A by a sputtering method, a chemical vapor deposition (CVD) method (including a thermal CVD method, a plasma enhanced CVD (PECVD) method, and the like), a metal organic CVD (MOCVD) method, a molecular beam epitaxy (MBE) method, an atomic layer deposition (ALD) method, a pulsed laser deposition (PLD) method, a high density plasma CVD method, a low pressure CVD (LP-CVD) method, or an atmospheric pressure CVD (AP-CVD) method, and then the insulator in the opening is removed. In that case, it is possible to remove the insulator 195b as long as at least a region in the oxide semiconductor film 130A overlapping with the second electrode is protected by the insulator 195A. This is because the opening is filled with the third electrode 170 at a subsequent step, and therefore the oxide semiconductor film 130A in the opening is protected by the third electrode 170.

[0130]

A conductive film 170A and a conductive film 170B are formed over the insulators 195A and 195b and the insulating film 160A. The conductive films 170A and 170B can be formed with a material similar to that of the conductive films 150A and 150B and the first electrode 140. Although two-layer structure is described here, the conductive film to be the third electrode 170 may have a single-layer structure or a stacked-layer structure of three or more layers.

[0131]

The conductive films 170A and 170B are partly removed by CMP treatment or the like to form the third electrode 170. At this step, the insulator 195A is partly removed and thus the thickness thereof is reduced in some cases. The insulator 195A can be used as a stopper layer. Note that the CMP treatment is performed under such a condition that the root-mean-square (RMS) roughness of a surface of the insulator 195A becomes 1 nm or less (preferably 0.5 nm or less). By the CMP treatment performed under such a condition, the planarity of a surface where a wiring and the like are formed later can be improved, and the characteristics of the transistor 100 can be improved.

[0132]

The CMP treatment is treatment for planarizing a surface of an object to be processed by a combination of chemical and mechanical actions. More specifically, the CMP treatment is a method in which a polishing cloth is attached to a polishing stage, the polishing stage and an object to be processed are each rotated or swung while a slurry (an abrasive) is supplied between the object to be processed and the polishing cloth, and the surface of the object to be processed is polished by a chemical reaction between the slurry and the surface of the object to be processed and by a mechanical polishing action of the polishing cloth on the object to be processed.

[0133]

Note that the CMP treatment may be performed only once or plural times. When the CMP treatment is performed plural times, it is preferable that first polishing be performed at a high polishing rate and final polishing be performed at a low polishing rate. By polishing with different polishing rates, the planarity of the surfaces of the insulator 195A and the third electrode 170 can be further improved.

[0134]

A conductive film is formed over the third electrode 170 and the insulator 195A, a resist mask is formed by the above-mentioned method, and an unnecessary portion of the conductive film is removed by etching, whereby the hard mask 135 is formed. In the case where the same material as the conductive film 170B is used for the conductive film to be the hard mask 135, the hard mask 135 can be formed by half etching of the conductive film 170B (FIG. 6D).

[0135]

After that, unnecessary portions of the insulator 195A, the oxide semiconductor film 130A, and the insulating film 160A are removed by etching using the hard mask 135 as a mask (FIG. 7A). By the etching treatment, part of the conductive films 150A and 150B is exposed with respect to the hard mask 135. In the case where the hard mask 135 and the conductive films 150A and 150B can be etched at the same time, the exposed region of the conductive films 150A and 150B can be removed together with the hard mask 135, whereby the second electrode 150 is formed. At this time, a top surface of the third electrode is removed and thus the thickness thereof is reduced in some cases.

[0136]

Through the above steps, a stacked-layer structure of the second electrode 150 having an opening, the oxide semiconductor layer 130, the second insulating layer 160, the insulator 195, and the third electrode 170 in the opening can be formed (FIG. 7B). Through the above steps, the transistor 100 can be manufactured.

[0137]

In FIG. 7C, the insulating layer 125 is further formed to cover the transistor 100. The insulating layer 125 may have a single-layer structure or a stacked-layer structure. In addition to the insulating layer 125, an insulator may be formed. As the insulator, an insulating film having barrier properties against oxygen and hydrogen can be used as in the cases of the insulator 190 and the insulator 195. The insulator covering the transistor 100 can prevent release of oxygen contained in the first insulating layer 120, the insulating layer 125, and the oxide semiconductor layer 130. In addition, entry of impurities such as hydrogen to the oxide semiconductor layer 130 from the outside can be prevented.

[0138]

The wiring 182 electrically connected to the second electrode 150 and the wiring 183 electrically connected to the third electrode 170 may be formed. The wiring 182 and the wiring 183 can be formed using a conductive material, such as a metal material, an alloy material, or a metal oxide material as well as the wiring 181. In particular, the wirings are preferably formed with a low-resistance conductive material, such as aluminum or copper. The use of the material as described above can reduce the wiring resistance. In consideration of the subsequent steps, the wiring 182 is preferably formed as an embedded wiring with high planarity (FIG. 7C).

[0139]

The etching conditions may be adjusted such that an end portion of at least one of the first insulating layer 120 and the second electrode 150 has a tapered shape. FIGS. 2A and 2B are cross-sectional views illustrating modification examples of the transistor 100 in which end portions of the first electrode 140, the first insulating layer 120, and the second electrode 150 have tapered shapes. With the tapered end portions, coverage with a film to be formed at a subsequent step in a process for forming the transistor can be improved.

[0140]

According to this embodiment, the channel length of the transistor 100 can be easily controlled by adjusting the thickness of the insulating layer 120 even when the transistor is miniaturized. Furthermore, with a structure in which the second electrode 150 surrounds the side surface of the third electrode with the second insulating layer 160 and the oxide semiconductor layer 130 interposed therebetween, the effective channel width of the transistor can be made large, and accordingly, the amount of on-state current of the transistor can be increased.

[0141]

According to this embodiment, when an insulating layer containing oxygen is used as the first insulating layer 120, the first insulating layer 120 is in contact with a region in the oxide semiconductor layer to be a channel; thus, oxygen can be supplied to the oxide semiconductor layer 130. Oxygen vacancies in the oxide semiconductor layer are filled with supplied oxygen, whereby the oxygen vacancies are reduced, and the reliability of the transistor using the oxide semiconductor layer 130 can be increased.

[0142]

Thus, a miniaturized transistor having highly stable electrical characteristics can be provided.

[0143]

The structures, the methods, and the like described in this embodiment can be combined as appropriate with any of the structures, the methods, and the like described in the other embodiments.

[0144]

(Embodiment 3)

<Structure of oxide semiconductor>

A structure of an oxide semiconductor is described below.

[0145]

An oxide semiconductor is classified into a single crystal oxide semiconductor and a non-single-crystal oxide semiconductor. Examples of a non-single-crystal oxide semiconductor include a c-axis aligned crystalline oxide semiconductor (CAAC-OS), a polycrystalline oxide semiconductor, a nanocrystalline oxide semiconductor (nc-OS), an amorphous-like oxide semiconductor (a-like OS), and an amorphous oxide semiconductor.

[0146]

From another perspective, an oxide semiconductor is classified into an amorphous oxide semiconductor and a crystalline oxide semiconductor. Examples of a crystalline oxide semiconductor include a single crystal oxide semiconductor, a CAAC-OS, a polycrystalline oxide semiconductor, and an nc-OS.

[0147]

It is known that an amorphous structure is generally defined as being metastable and unfixed, and being isotropic and having no non-uniform structure. In other words, an amorphous structure has a flexible bond angle and a short-range order but does not have a long-range order.

[0148]

This means that an inherently stable oxide semiconductor cannot be regarded as a completely amorphous oxide semiconductor. Moreover, an oxide semiconductor that is not isotropic (e.g., an oxide semiconductor that has a periodic structure in a microscopic region) cannot be regarded as a completely amorphous oxide semiconductor. Note that an a-like OS has a periodic structure in a microscopic region, but at the same time has a void and has an unstable structure. For this reason, an a-like OS has physical properties similar to those of an amorphous oxide semiconductor.

[0149]

<CAAC-OS>

First, a CAAC-OS is described.

[0150]

A CAAC-OS is one of oxide semiconductors having a plurality of c-axis aligned crystal parts (also referred to as pellets).

[0151]

In a combined analysis image (also referred to as a high-resolution TEM image) of a bright-field image and a diffraction pattern of a CAAC-OS, which is obtained using a transmission electron microscope (TEM), a plurality of pellets can be observed. However, in the high-resolution TEM image, a boundary between pellets, that is, a grain boundary is not clearly observed. Thus, in the CAAC-OS, a reduction in electron mobility due to the grain boundary is less likely to occur.

[0152]

A CAAC-OS observed with TEM is described below. FIG. 9A shows a high-resolution TEM image of a cross section of the CAAC-OS which is observed from a direction substantially parallel to the sample surface. The high-resolution TEM image is obtained with a spherical aberration corrector function. The high-resolution TEM image obtained with a spherical aberration corrector function is particularly referred to as a Cs-corrected high-resolution TEM image. The Cs-corrected high-resolution TEM image can be obtained with, for example, an atomic resolution analytical electron microscope JEM-ARM200F manufactured by JEOL Ltd.

[0153]

FIG. 9B is an enlarged Cs-corrected high-resolution TEM image of a region (1) in FIG. 9A. FIG. 9B shows that metal atoms are arranged in a layered manner in a pellet. Each metal atom layer has a configuration reflecting unevenness of a surface over which the CAAC-OS is formed (hereinafter, the surface is referred to as a formation surface) or the top surface of the CAAC-OS, and is arranged parallel to the formation surface or the top surface of the CAAC-OS.

[0154]

As shown in FIG. 9B, the CAAC-OS has a characteristic atomic arrangement. The characteristic atomic arrangement is denoted by an auxiliary line in FIG. 9C.

FIGS. 9B and 9C prove that the size of a pellet is greater than or equal to 1 nm or greater than or equal to 3 nm, and the size of a space caused by tilt of the pellets is approximately 0.8 nm. Therefore, the pellet can also be referred to as a nanocrystal (nc). Furthermore, the CAAC-OS can also be referred to as an oxide semiconductor including c-axis aligned nanocrystals (CANC).

[0155]

Here, according to the Cs-corrected high-resolution TEM images, the schematic arrangement of pellets 5100 of a CAAC-OS over a substrate 5120 is illustrated by such a structure in which bricks or blocks are stacked (see FIG. 9D). The part in which the pellets are tilted as observed in FIG. 9C corresponds to a region 5161 shown in FIG. 9D.

[0156]

FIG. 10A shows a Cs-corrected high-resolution TEM image of a plane of the CAAC-OS observed from a direction substantially perpendicular to the sample surface. FIGS. 10B, 10C, and 10D are enlarged Cs-corrected high-resolution TEM images of regions (1), (2), and (3) in FIG. 10A, respectively. FIGS. 10B, 10C, and 10D indicate that metal atoms are arranged in a triangular, quadrangular, or hexagonal configuration in a pellet. However, there is no regularity of arrangement of metal atoms between different pellets.

[0157]

Next, a CAAC-OS analyzed by X-ray diffraction (XRD) is described. For example, when the structure of a CAAC-OS including an $InGaZnO_4$ crystal is analyzed by an out-of-plane method, a peak appears at a diffraction angle (2θ) of around 31° as shown in FIG. 11A. This peak is assigned to the (009) plane of the $InGaZnO_4$ crystal, which indicates that crystals in the CAAC-OS have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS.

[0158]

Note that in structural analysis of the CAAC-OS by an out-of-plane method, another peak may appear when 2θ is around 36°, in addition to the peak at 2θ of around 31°. The peak at 2θ of around 36° indicates that a crystal having no c-axis alignment is included in part of the CAAC-OS. It is preferable that in the CAAC-OS analyzed by an out-of-plane method, a peak appear when 2θ is around 31° and that a peak not appear when 2θ is around 36°.

[0159]

On the other hand, in structural analysis of the CAAC-OS by an in-plane method in which an X-ray beam is incident on a sample in a direction substantially perpendicular to the c-axis, a peak appears when 2θ is around 56°. This peak is attributed to the (110) plane of the $InGaZnO_4$ crystal. In the case of the CAAC-OS, when analysis (ϕ scan) is performed with 2θ fixed at around 56° and with the sample rotated using a normal vector of the sample surface as an axis (ϕ axis), as shown in FIG. 11B, a peak is not clearly observed. In contrast, in the case of a single crystal oxide semiconductor of $InGaZnO_4$, when ϕ scan is performed with 2θ fixed at around 56°, as shown in FIG. 11C, six peaks which are assigned to crystal planes equivalent to the (110) plane are observed. Accordingly, the structural analysis using XRD shows that the directions of the a-axes and b-axes are irregularly oriented in the CAAC-OS.

[0160]

Next, a CAAC-OS analyzed by electron diffraction is described. For example, when an electron beam with a probe diameter of 300 nm is incident on a CAAC-OS including an $InGaZnO_4$ crystal in a direction parallel to the sample surface, a diffraction pattern (also referred to as a selected-area transmission electron diffraction pattern) shown in FIG. 12A can be obtained. In this diffraction pattern, spots assigned to the (009) plane of an $InGaZnO_4$ crystal are included. Thus, the electron diffraction also indicates that pellets included in the CAAC-OS have c-axis alignment and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS. Meanwhile, FIG. 12B shows a diffraction pattern obtained in such a manner that an electron beam with a probe diameter of 300 nm is incident on the same sample in a direction perpendicular to the sample surface. As shown in FIG. 12B, a ring-like diffraction pattern is observed. Thus, the electron diffraction also indicates that the a-axes and b-axes of the pellets included in the CAAC-OS do not have regular alignment. The first ring in FIG. 12B is considered to be assigned to the (010) plane, the (100) plane, and the like of the $InGaZnO_4$ crystal. The second ring in FIG. 12B is considered to be assigned to the (110) plane and the like.

[0161]

As described above, the CAAC-OS is an oxide semiconductor with high crystallinity. Entry of impurities, formation of defects, or the like might decrease the crystallinity of an oxide semiconductor. This means that the CAAC-OS has small amounts of impurities and defects (e.g., oxygen vacancies).

[0162]

Note that the impurity means an element other than the main components of the oxide semiconductor, such as hydrogen, carbon, silicon, or a transition metal element. For example, an element (specifically, silicon or the like) having higher strength of bonding to oxygen than a metal element included in an oxide semiconductor extracts oxygen from the oxide semiconductor, which results in disorder of the atomic arrangement and reduced crystallinity of the oxide semiconductor. A heavy metal such as iron or nickel, argon, carbon dioxide, or the like has a large atomic radius (or molecular radius), and thus disturbs the atomic arrangement of the oxide semiconductor and decreases crystallinity.

[0163]

The characteristics of an oxide semiconductor having impurities or defects might be changed by light, heat, or the like. Impurities contained in the oxide semiconductor might serve as carrier traps or carrier generation sources, for example. Furthermore, oxygen vacancies in the oxide semiconductor serve as carrier traps or serve as carrier generation sources when hydrogen is captured therein.

[0164]

The CAAC-OS having small amounts of impurities and oxygen vacancies is an oxide semiconductor with low carrier density (specifically, lower than $8 \times 10^{11}/cm^3$, preferably lower than $1 \times 10^{11}/cm^3$, further preferably lower than $1 \times 10^{10}/cm^3$, and is higher than or equal to $1 \times 10^{-9}/cm^3$). Such an oxide semiconductor is referred to as a highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor. A CAAC-OS has a low impurity concentration and a low density of defect states.

Thus, the CAAC-OS can be referred to as an oxide semiconductor having stable characteristics.

[0165]

<nc-OS>

Next, an nc-OS is described.

[0166]

An nc-OS has a region in which a crystal part is observed and a region in which a crystal part is not clearly observed in a high-resolution TEM image. In most cases, the size of a crystal part included in the nc-OS is greater than or equal to 1 nm and less than or equal to 10 nm, or greater than or equal to 1 nm and less than or equal to 3 nm. Note that an oxide semiconductor including a crystal part whose size is greater than 10 nm and less than or equal to 100 nm is sometimes referred to as a microcrystalline oxide semiconductor. In a high-resolution TEM image of the nc-OS, for example, a grain boundary is not clearly observed in some cases. Note that there is a possibility that the origin of the nanocrystal is the same as that of a pellet in a CAAC-OS. Therefore, a crystal part of the nc-OS may be referred to as a pellet in the following description.

[0167]

In the nc-OS, a microscopic region (for example, a region with a size greater than or equal to 1 nm and less than or equal to 10 nm, in particular, a region with a size greater than or equal to 1 nm and less than or equal to 3 nm) has a periodic atomic arrangement. There is no regularity of crystal orientation between different pellets in the nc-OS. Thus, the orientation of the whole film is not ordered. Accordingly, the nc-OS cannot be distinguished from an a-like OS or an amorphous oxide semiconductor, depending on an analysis method. For example, when the nc-OS is analyzed by an out-of-plane method using an X-ray beam having a diameter larger than the size of a pellet, a peak indicating a crystal plane does not appear. Furthermore, a diffraction pattern like a halo pattern is observed when the nc-OS is subjected to electron diffraction using an electron beam with a probe diameter (e.g., 50 nm or larger) that is larger than the size of a pellet. Meanwhile, spots appear in a nanobeam electron diffraction pattern of the nc-OS when an electron beam having a probe diameter close to or smaller than the size of a pellet is applied. Moreover, in a nanobeam electron diffraction pattern of the nc-OS, regions with high luminance in a circular (ring) pattern are shown in some cases. Also in a nanobeam electron diffraction pattern of the nc-OS, a plurality of spots is shown in a ring-like region in some cases.

[0168]

Since there is no regularity of crystal orientation between the pellets (nanocrystals) as mentioned above, the nc-OS can also be referred to as an oxide semiconductor including random aligned nanocrystals (RANC) or an oxide semiconductor including non-aligned nanocrystals (NANC).

[0169]

The nc-OS is an oxide semiconductor that has high regularity as compared with an amorphous oxide semiconductor. Therefore, the nc-OS is likely to have a lower density of defect states than an a-like OS and an amorphous oxide semiconductor. Note that there is no regularity of crystal orientation between different pellets in the nc-OS. Therefore, the nc-OS has a higher density of defect states than the CAAC-OS.

[0170]

<a-like OS>

An a-like OS has a structure intermediate between those of the nc-OS and the amorphous oxide semiconductor.

[0171]

In a high-resolution TEM image of the a-like OS, a void may be observed. Furthermore, in the high-resolution TEM image, there are a region where a crystal part is clearly observed and a region where a crystal part is not observed.

[0172]

The a-like OS has an unstable structure because it includes a void. To verify that an a-like OS has an unstable structure as compared with a CAAC-OS and an nc-OS, a change in structure caused by electron irradiation is described below.

[0173]

An a-like OS (referred to as Sample A), an nc-OS (referred to as Sample B), and a CAAC-OS (referred to as Sample C) are prepared as samples subjected to electron irradiation. Each of the samples is an In-Ga-Zn oxide.

[0174]

First, a high-resolution cross-sectional TEM image of each sample is obtained. The high-resolution cross-sectional TEM images show that all the samples have crystal parts.

[0175]

Note that which part is regarded as a crystal part is determined as follows. It is known that a unit cell of an $InGaZnO_4$ crystal has a structure in which nine layers including three In-O layers and six Ga-Zn-O layers are stacked in the c-axis direction. The distance between the adjacent layers is equivalent to the lattice spacing on the (009) plane (also referred to as d value). The value is calculated to be 0.29 nm from crystal structural analysis. Accordingly, a portion where the lattice spacing between lattice fringes is greater than or equal to 0.28 nm and less than or equal to 0.30 nm is regarded as a crystal part of $InGaZnO_4$. Each of lattice fringes corresponds to the a-b plane of the $InGaZnO_4$ crystal.

[0176]

FIG. 13 shows change in the average size of crystal parts (at 22 points to 45 points) in each sample. Note that the crystal part size corresponds to the length of a lattice fringe. FIG. 13 indicates that the crystal part size in the a-like OS increases with an increase in the cumulative electron dose. Specifically, as shown by (1) in FIG. 13, a crystal part of approximately 1.2 nm (also referred to as an initial nucleus) at the start of TEM observation grows to a size of approximately 2.6 nm at a cumulative electron dose of 4.2×10^8 e^-/nm^2. In contrast, the crystal part size in the nc-OS and the CAAC-OS shows little change from the start of electron irradiation to a cumulative electron dose of 4.2×10^8 e^-/nm^2. Specifically, as shown by (2) and (3) in FIG. 13, the average crystal sizes in an nc-OS and a CAAC-OS are approximately 1.4 nm and approximately 2.1 nm, respectively, regardless of the cumulative electron dose.

[0177]

In this manner, growth of the crystal part in the a-like OS is induced by electron irradiation. In contrast, in the nc-OS and the CAAC-OS, growth of the crystal part is hardly induced by electron irradiation. Therefore, the a-like OS has an unstable structure as compared with the nc-OS and the CAAC-OS.

[0178]

The a-like OS has a lower density than the nc-OS and the CAAC-OS because it includes a void. Specifically, the density of the a-like OS is higher than or equal to 78.6 % and lower than 92.3 % of the density of the single crystal oxide semiconductor having the same composition. The density of each of the nc-OS and the CAAC-OS is higher than or equal to 92.3 % and lower than 100 % of the density of the single crystal oxide semiconductor having the same composition. Note that it is difficult to deposit an oxide semiconductor having a density of lower than 78 % of the density of the single crystal oxide semiconductor.

[0179]

For example, in the case of an oxide semiconductor having an atomic ratio of In:Ga:Zn = 1:1:1, the density of single crystal $InGaZnO_4$ with a rhombohedral crystal structure is 6.357 g/cm^3. Accordingly, in the case of the oxide semiconductor having an atomic ratio of In:Ga:Zn = 1:1:1, the density of the a-like OS is higher than or equal to 5.0 g/cm^3 and lower than 5.9 g/cm^3. For example, in the case of the oxide semiconductor having an atomic ratio of In:Ga:Zn = 1:1:1, the density of each of the nc-OS and the CAAC-OS is higher than or equal to 5.9 g/cm^3 and lower than 6.3 g/cm^3.

[0180]

Note that there is a possibility that an oxide semiconductor having a certain composition cannot exist in a single crystal structure. In that case, single crystal oxide semiconductors with different compositions are combined at an adequate ratio, which makes it possible to calculate density equivalent to that of a single crystal oxide semiconductor with the desired composition. The density of a single crystal oxide semiconductor having the desired composition can be calculated using a weighted average according to the combination ratio of the single crystal oxide semiconductors with different compositions. Note that it is preferable to use as few kinds of single crystal oxide semiconductors as possible to calculate the density.

[0181]

As described above, oxide semiconductors have various structures and various properties. Note that an oxide semiconductor may be a stacked layer including two or more of an amorphous oxide semiconductor, an a-like OS, an nc-OS, and a CAAC-OS, for example.

[0182]

<Deposition method>

An example of a method for depositing a CAAC-OS film is described below.

[0183]

FIG. 14A is a schematic view of the inside of a deposition chamber. The CAAC-OS can be deposited by a sputtering method.

[0184]

As shown in FIG. 14A, a substrate 5220 and a target 5230 are arranged to face each other. Plasma 5240 is generated between the substrate 5220 and the target 5230. A heating mechanism 5260 is under the substrate 5220. The target 5230 is attached to a backing plate although not shown in the drawing. A plurality of magnets is arranged to face the target 5230 with the backing plate positioned therebetween. A sputtering method in which the deposition speed is increased by utilizing a magnetic field of magnets is referred to as a magnetron sputtering method.

[0185]

The distance *d* between the substrate 5220 and the target 5230 (also referred to as a target-substrate distance (T-S distance)) is greater than or equal to 0.01 m and less than or equal to 1 m, preferably greater than or equal to 0.02 m and less than or equal to 0.5 m. The deposition chamber is mostly filled with a deposition gas (e.g., an oxygen gas, an argon gas, or a mixed gas containing oxygen at 5 vol% or more) and controlled to be higher than or equal to 0.01 Pa and lower than or equal to 100 Pa, preferably higher than or equal to 0.1 Pa and lower than or equal to 10 Pa. Here, discharge starts by application of a voltage at a certain value or higher to the target 5230, and plasma 5240 is observed. Note that the magnetic field in the vicinity of the target 5230 forms a high-density plasma region. In the high-density plasma region, the deposition gas is ionized, so that an ion 5201 is generated. Examples of the ion 5201 include an oxygen cation (O^+) and an argon cation (Ar^+).

[0186]

The target 5230 has a polycrystalline structure which includes a plurality of crystal grains and in which a cleavage plane exists in any of the crystal grains. FIG. 15 shows a crystal structure of $InMZnO_4$ (M is an element such as aluminum, gallium, yttrium, or tin) included in the target 5230 as an example. Note that the crystal structure shown in FIG. 15 is In*M*ZnO$_4$ observed from a direction parallel to a b-axis. In the crystal of In*M*ZnO$_4$, oxygen atoms are negatively charged, whereby repulsive force is generated between the two adjacent *M*-Zn-O layers. Thus, the In*M*ZnO$_4$ crystal has a cleavage plane between the two adjacent *M*-Zn-O layers.

[0187]

The ion 5201 generated in the high-density plasma region is accelerated to move toward the target 5230 side by an electric field, and then collides with the target 5230. At this time, a pellet 5200 which is a flat-plate-like or pellet-like sputtered particle is separated from the cleavage plane (see FIG. 14A). The pellet 5200 corresponds to a portion between the two cleavage planes shown in FIG. 15. Thus, when the pellet 5200 is observed, the cross-section thereof is as shown in FIG. 14B, and the top surface thereof is as shown in FIG. 14C. Note that structure of the pellet 5200 may be distorted by an impact of collision of the ion 5201. Note that along with the separation of the pellet 5200, a particle 5203 is also sputtered from the target 5230. The particle 5203 has an atom or an aggregate of several atoms. Therefore, the particle 5203 can be referred to as an atomic particle.

[0188]

The pellet 5200 is a flat-plate-like (pellet-like) sputtered particle having a triangle plane, e.g., regular triangle plane. Alternatively, the pellet 5200 is a flat-plate-like (pellet-like) sputtered particle having a hexagon plane, e.g., regular hexagon plane. However, the shape of a flat plane of the pellet 5200 is not limited to a triangle or a hexagon. For example, the flat plane may have a shape formed by combining two or more triangles. For example, a quadrangle (e.g., rhombus) may be formed by combining two triangles (e.g., regular triangles).

[0189]

The thickness of the pellet 5200 is determined depending on the kind of deposition gas and the like. For example, the thickness of the pellet 5200 is greater than or equal to 0.4 nm and less than or equal to 1 nm, preferably greater than or equal to 0.6 nm and less than or equal to 0.8 nm. In addition, the width of the pellet 5200 is, for example, greater than or equal to 1 nm and less than or equal to 3 nm, preferably greater than or equal to 1.2 nm and less than or equal to 2.5 nm. For example, the ion

5201 collides with the target 5230 including the In-*M*-Zn oxide. Then, the pellet 5200 including three layers of an *M*-Zn-O layer, an In-O layer, and an *M*-Zn-O layer is separated.

[0190]

The pellet 5200 may receive a charge when passing through the plasma 5240, so that surfaces thereof are negatively or positively charged. For example, the pellet 5200 receives a negative charge from O^{2-} in the plasma 5240. As a result, oxygen atoms on the surfaces of the pellet 5200 may be negatively charged. In addition, when passing through the plasma 5240, the pellet 5200 is sometimes combined with indium, the element *M*, zinc, oxygen, or the like in the plasma 5240 to grow up.

[0191]

The pellet 5200 and the particle 5203 that have passed through the plasma 5240 reach the surface of the substrate 5220. Note that part of the particle 5203 is discharged to the outside by a vacuum pump or the like because the particle 5203 is small in mass.

[0192]

Next, deposition of the pellet 5200 and the particle 5203 over the surface of the substrate 5220 is described with reference to FIGS. 16A to 16E.

[0193]

First, a first of the pellets 5200 is deposited over the substrate 5220. Since the pellet 5200 has a flat-plate-like shape, it is deposited so that the flat plane faces the surface of the substrate 5220 (FIG. 16A). Here, a charge on a surface of the pellet 5200 on the substrate 5220 side is lost through the substrate 5220.

[0194]

Next, a second of the pellets 5200 reaches the substrate 5220. Here, since the surface of the first of the pellets 5200 and the surface of the second of the pellets 5200 are charged, they repel each other (FIG. 16B).

[0195]

As a result, the second of the pellets 5200 avoids being deposited over the first of the pellets 5200, and is deposited over the surface of the substrate 5220 so as to be a little distance away from the first of the pellets 5200 (FIG. 16C). With repetition of this, millions of the pellets 5200 are deposited over the surface of the substrate 5220 to have a thickness of one layer. A region where any pellet 5200 is not deposited is generated between adjacent pellets 5200.

[0196]

Next, the particle 5203 reaches the surface of the substrate 5220 (FIG. 16D).

[0197]

The particle 5203 cannot be deposited over an active region such as the surface of the pellet 5200. Therefore, the particle 5203 is deposited so as to fill a region where the pellets 5200 are not deposited. The particles 5203 grow in the horizontal (lateral) direction between the pellets 5200, thereby connecting the pellets 5200. In this way, the particles 5203 are deposited until they fill regions where the pellets 5200 are not deposited. This mechanism is similar to a deposition mechanism of an atomic layer deposition (ALD) method.

[0198]

Note that there can be several mechanisms for the lateral growth of the particles 5203 between the pellets 5200. For example, as shown in FIG. 16E, the pellets 5200 can be connected from side surfaces of the first *M*-Zn-O layers. In this case, after the first *M*-Zn-O layers make connection, the In-O layers and the second *M*-Zn-O layers are connected in this order (the first mechanism).

[0199]

Alternatively, as shown in FIG. 17A, first, the particles 5203 are connected to the sides of the first *M*-Zn-O layers so that each side of the first *M*-Zn-O layer has one particle 5203. Then, as shown in FIG. 17B, the particle 5203 is connected to each side of the In-O layers. After that, as shown in FIG. 17C, the particle 5203 is connected to each side of the second *M*-Zn-O layers (the second mechanism). Note that the connection can also be made by the simultaneous occurrence of the deposition in FIGS. 17A, 17B, and 17C (the third mechanism).

[0200]

As shown in the above, the above three mechanisms are considered as the mechanisms of the lateral growth of the particles 5203 between the pellets 5200. However, the particles 5203 may grow up laterally between the pellets 5200 by other mechanisms.

[0201]

Therefore, even when the orientations of a plurality of pellets 5200 are different from each other, generation of crystal boundaries can be suppressed since the particles 5203 laterally grow to fill gaps between the plurality of pellets 5200. In addition, as the particles 5203 make smooth connection between the plurality of pellets 5200, a crystal structure different from a single crystal and a polycrystal is formed. In other words, a crystal structure including distortion between minute crystal regions (pellets 5200) is formed. The regions filling the gaps between the crystal regions are distorted crystal regions, and thus, it will be not appropriate to say that the regions have an amorphous structure.

[0202]

When the particles 5203 completely fill the regions between the pellets 5200, a first layer with a thickness almost the same as that of the pellet 5200 is formed. Then, a new first of the pellets 5200 is deposited over the first layer, and a second layer is formed. With repetition of this cycle, the stacked-layer thin film structure is formed (FIG. 14D).

[0203]

A deposition way of the pellets 5200 changes depending on the surface temperature of the substrate 5220 or the like. For example, if the surface temperature of the substrate 5220 is high, migration of the pellets 5200 occurs over the substrate 5220. As a result, a proportion of the pellets 5200 that are directly connected with each other without the particles 5203 increases, whereby a CAAC-OS with high orientation is made. The surface temperature of the substrate 5220 for the deposition of the CAAC-OS is higher than or equal to 100 °C and lower than 500 °C, preferably higher than or equal to 140 °C and lower than 450 °C, or further preferably higher than or equal to 170 °C and lower than 400 °C. Therefore, even when a large-sized substrate of the 8th generation or more is used as the substrate 5220, a warp or the like hardly occurs.

[0204]

On the other hand, if the surface temperature of the substrate 5220 is low, the migration of the pellets 5200 over the substrate 5220 does not easily occur. As a result, the pellets 5200 overlap with each other, whereby a nanocrystalline oxide semiconductor (nc-OS) with low orientation or the like is made (see FIG. 18). In the nc-OS, the pellets 5200 are deposited with certain gaps because the pellets 5200 are negatively charged. Therefore, the nc-OS film has low orientation but some regularity, and thus it has a denser structure than an amorphous oxide semiconductor.

[0205]

When gaps between the pellets are extremely small in a CAAC-OS, the pellets may form a large pellet. The inside of the large pellet has a single crystal structure. For example, the size of the pellet may be greater than or equal to 10 nm and less than or equal to 200 nm, greater than or equal to 15 nm and less than or equal to 100 nm, or greater than or equal to 20 nm and less than or equal to 50 nm, when seen from the above.

[0206]

According to such a model, the pellets 5200 are considered to be deposited on the surface of the substrate 5220. Thus, a CAAC-OS can be deposited even when a formation surface does not have a crystal structure; therefore, a growth mechanism in this case is different from epitaxial growth. In addition, uniform deposition of a CAAC-OS or an nc-OS can be performed even over a large-sized glass substrate or the like. For example, even when the surface of the substrate 5220 (formation surface) has an amorphous structure (e.g., such as amorphous silicon oxide), a CAAC-OS can be deposited.

[0207]

In addition, even when the surface of the substrate 5220 (formation surface) has uneven shape, the pellets 5200 are aligned along the shape.

[0208]

(Embodiment 4)

In this embodiment, a structural example of a semiconductor device including the transistor of one embodiment of the present invention is described with reference to drawings.

[0209]

[Cross-sectional structure]

FIGS. 19A and 19B are cross-sectional views of a semiconductor device of one embodiment of the present invention. The semiconductor device illustrated in FIGS.

19A and 19B includes a transistor 2200 including a first semiconductor material in a lower portion and a transistor 2100 including a second semiconductor material in an upper portion. FIG. 19A illustrates a cross-sectional view of the transistors in the channel length direction, and FIG. 19B illustrates a cross-sectional view of the transistors in the channel width direction.

[0210]

Note that the transistor 2100 may be provided with a back gate.

[0211]

The first and second semiconductor materials preferably have different energy gaps. For example, the first semiconductor material can be a semiconductor material other than an oxide semiconductor (examples of such a semiconductor material include silicon (including strained silicon), germanium, silicon germanium, silicon carbide, gallium arsenide, aluminum gallium arsenide, indium phosphide, gallium nitride, and an organic semiconductor), and the second semiconductor material can be an oxide semiconductor. A transistor including a material other than an oxide semiconductor, such as single crystal silicon, can operate at high speed easily. On the other hand, a transistor including an oxide semiconductor has a small off-state current.

[0212]

The transistor 2200 may be either an n-channel transistor or a p-channel transistor, and an appropriate transistor may be used in accordance with a circuit. Furthermore, the specific structure of the semiconductor device, such as the material or the structure used for the semiconductor device, is not necessarily limited to those described here except for the use of the transistor of one embodiment of the present invention which includes an oxide semiconductor.

[0213]

FIGS. 19A and 19B illustrate a structure in which the transistor 2100 is provided over the transistor 2200 with an insulating film 2201 and an insulating film 2207 provided therebetween. A plurality of wirings 2202 are provided between the transistor 2200 and the transistor 2100. Furthermore, wirings and electrodes provided over and under the insulating films are electrically connected to each other through a plurality of plugs 2203 embedded in the insulating films. In addition, an interlayer insulating film 2204 covering the transistor 2100 is provided.

[0214]

The stack of the two kinds of transistors reduces the area occupied by the circuit, allowing a plurality of circuits to be highly integrated.

[0215]

In the case where a silicon-based semiconductor material is used for the transistor 2200 provided in the lower portion, hydrogen in an insulating film provided in the vicinity of the semiconductor film of the transistor 2200 terminates dangling bonds of silicon; accordingly, the reliability of the transistor 2200 can be improved. Meanwhile, in the case where an oxide semiconductor is used for the transistor 2100 provided in the upper portion, hydrogen in an insulating film provided in the vicinity of the semiconductor film of the transistor 2100 becomes a factor of generating carriers in the oxide semiconductor; thus, the reliability of the transistor 2100 might be decreased. Therefore, in the case where the transistor 2100 including an oxide semiconductor is provided over the transistor 2200 including a silicon-based semiconductor material, it is particularly effective that the insulating film 2207 having a function of preventing diffusion of hydrogen is provided between the transistors 2100 and 2200. The insulating film 2207 makes hydrogen remain in the lower portion, thereby improving the reliability of the transistor 2200. In addition, since the insulating film 2207 suppresses diffusion of hydrogen from the lower portion to the upper portion, the reliability of the transistor 2100 can also be improved.

[0216]

The insulating film 2207 can be formed using, for example, aluminum oxide, aluminum oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, hafnium oxide, hafnium oxynitride, or yttria-stabilized zirconia (YSZ).

[0217]

Furthermore, a blocking film having a function of preventing entry of hydrogen may be formed over the transistor 2100 so as to cover the transistor 2100 including an oxide semiconductor film. For the blocking film, a material that is similar to that of the insulating film 2207 can be used, and in particular, aluminum oxide is preferably used. The aluminum oxide film has a high shielding (blocking) effect of preventing penetration of both oxygen and impurities, such as hydrogen and moisture. Thus, by using the aluminum oxide film as the blocking film covering the transistor 2100, release of oxygen from the oxide semiconductor film included in the transistor 2100 and entry of water and hydrogen into the oxide semiconductor film can be prevented.

[0218]

Note that the transistor 2200 can be a transistor of various types without being limited to a planar type transistor. For example, the transistor 2200 can be a fin-type transistor, a tri-gate transistor, or the like. An example of a cross-sectional view in that case is illustrated in FIGS. 19E and 19F. An insulating film 2212 is provided over a semiconductor substrate 2211. The semiconductor substrate 2211 includes a protruding portion with a thin tip (also referred to a fin). Note that an insulating film may be provided over the protruding portion. The insulating film serves as a mask for preventing the semiconductor substrate 2211 from being etched when the protruding portion is formed. Alternatively, the protruding portion does not necessarily have a thin tip; a cuboid-like protruding portion or a protruding portion with a thick tip can be used, for example. A gate insulating film 2214 is provided over the protruding portion of the semiconductor substrate 2211, and a gate electrode 2213 is provided over the gate insulating film 2214. Although the gate electrode 2213 has a single-layer structure in this embodiment, one embodiment of the present invention is not limited to this example, and the gate electrode 2213 may have a stacked-layer structure of two or more layers. Source and drain regions 2215 are formed in the semiconductor substrate 2211. Note that here is illustrated an example in which the semiconductor substrate 2211 includes a protruding portion; however, the semiconductor device of one embodiment of the present invention is not limited thereto. For example, a semiconductor region including a protruding portion may be formed by processing an SOI substrate.

[0219]

[Examples of circuit configuration]

In the above structure, electrodes of the transistors 2100 and 2200 can be connected in a variety of ways; thus, a variety of circuits can be formed. Examples of a circuit configuration which can be achieved by using the semiconductor device of one embodiment of the present invention are shown below.

[0220]

A circuit diagram in FIG. 19C shows a configuration of a “CMOS circuit” in which the p-channel transistor 2200 and the n-channel transistor 2100 are connected to each other in series and in which gates of them are connected to each other.

[0221]

A circuit diagram in FIG. 19D shows a configuration in which a source and a drain of the transistor 2100 are connected to a source and a drain of the transistor 2200. With such a configuration, the transistors can function as a so-called analog switch.

[0222]

FIG. 20 is a cross-sectional view of a semiconductor device in which a CMOS circuit is formed using the transistor 2200 and a transistor 2300 each including a channel formed using the first semiconductor material.

[0223]

The transistor 2300 includes impurity regions 2301 serving as source and drain regions, a gate electrode 2303, a gate insulating film 2304, and a sidewall insulating film 2305. The transistor 2300 may also include an impurity region 2302 serving as an LDD region under the sidewall insulating film 2305. The description for FIGS. 19A and 19B can be referred to for other components in FIG. 20.

[0224]

The transistors 2200 and 2300 preferably have opposite polarities. For example, when the transistor 2200 is a p-channel transistor, the transistor 2300 is preferably an n-channel transistor.

[0225]

A photoelectric conversion element, such as a photodiode, may be provided in the semiconductor devices illustrated in FIGS. 19A and 19B and FIG. 20.

[0226]

The photodiode can be formed using a single crystal semiconductor or a polycrystalline semiconductor. The photodiode formed using a single crystal semiconductor or a polycrystalline semiconductor is preferable because of its high light detection sensitivity.

[0227]

FIG. 21A is a cross-sectional view of a semiconductor device in which a substrate 2001 is provided with a photodiode 2400. The photodiode 2400 includes a conductive film 2401 having a function as one of an anode and a cathode, a conductive film 2402 having a function as the other of the anode and the cathode, and a conductive film 2403 electrically connecting the conductive film 2402 and a plug 2004. The conductive films 2401 to 2403 may be formed by injecting an impurity into the substrate 2001.

[0228]

Although the photodiode 2400 is provided so that a current flows in the vertical direction with respect to the substrate 2001 in FIG. 21A, the photodiode 2400 may be provided so that a current flows in the lateral direction with respect to the substrate 2001.

[0229]

FIG. 21B is a cross-sectional view of a semiconductor device in which a photodiode 2500 is provided over the transistor 2100. The photodiode 2500 includes a conductive film 2501 having a function as one of an anode and a cathode, a conductive film 2502 having a function as the other of the anode and the cathode, and a semiconductor 2503. The photodiode 2500 is electrically connected to the transistor 2100 through a plug 2504.

[0230]

In FIG. 21B, the photodiode 2500 may also be provided at the same level as the transistor 2100. Alternatively, the photodiode 2500 may also be provided at the level between the transistor 2200 and the transistor 2100.

[0231]

The description for FIGS. 19A and 19B and FIG. 20 can be referred to for the details of other components in FIGS. 21A and 21B.

[0232]

The photodiode 2400 or the photodiode 2500 may be formed using a material capable of generating charge by absorbing a radiation. Examples of a material capable of generating charge by absorbing a radiation include selenium, lead iodide, mercury iodide, gallium arsenide, CdTe, and CdZn.

[0233]

The use of selenium for the photodiode 2400 or the photodiode 2500 can provide a photoelectric conversion element having a light absorption coefficient in a wide wavelength range of visible light, ultraviolet light, X-rays, and gamma rays, for example.

[0234]

<Memory device>

An example of a semiconductor device (memory device) which includes the transistor of one embodiment of the present invention, which can retain stored data even when not powered, and which has an unlimited number of write cycles is shown in FIGS. 22A to 22C. Note that FIG. 22B is a circuit diagram of the structure in FIG. 22A.

[0235]

The semiconductor device illustrated in FIGS. 22A and 22B includes a transistor 3200 using a first semiconductor material, a transistor 3300 using a second semiconductor material, and a capacitor 3400. Note that any of the transistors described in Embodiment 1 can be used as the transistor 3300.

[0236]

The transistor 3300 is a transistor in which a channel is formed in a semiconductor including an oxide semiconductor. Since the off-state current of the transistor 3300 is small, stored data can be retained for a long period. In other words, power consumption can be sufficiently reduced because a semiconductor device in which refresh operation is unnecessary or the frequency of refresh operation is extremely low can be provided.

[0237]

In FIG. 22B, a first wiring 3001 is electrically connected to a source electrode of the transistor 3200. A second wiring 3002 is electrically connected to a drain electrode of the transistor 3200. A third wiring 3003 is electrically connected to one of a source electrode and a drain electrode of the transistor 3300. A fourth wiring 3004 is electrically connected to a gate electrode of the transistor 3300. A gate electrode of the transistor 3200 and the other of the source electrode and the drain electrode of the transistor 3300 are electrically connected to the one electrode of the capacitor 3400. A fifth wiring 3005 is electrically connected to the other electrode of the capacitor 3400.

[0238]

The semiconductor device in FIG. 22A has a feature that the potential of the gate electrode of the transistor 3200 can be retained, and thus enables writing, retaining, and reading of data as follows.

[0239]

Writing and retaining of data are described. First, the potential of the fourth wiring 3004 is set to a potential at which the transistor 3300 is turned on, so that the transistor 3300 is turned on. Accordingly, the potential of the third wiring 3003 is supplied to the gate electrode of the transistor 3200 and the capacitor 3400. That is, a predetermined charge is supplied to the gate electrode of the transistor 3200 (writing). Here, one of two kinds of charges providing different potential levels (hereinafter referred to as a low-level charge and a high-level charge) is supplied. After that, the potential of the fourth wiring 3004 is set to a potential at which the transistor 3300 is turned off, so that the transistor 3300 is turned off. Thus, the charge supplied to the gate electrode of the transistor 3200 is held (retaining).

[0240]

Since the off-state current of the transistor 3300 is extremely small, the charge of the gate electrode of the transistor 3200 is retained for a long time.

[0241]

Next, reading of data is described. An appropriate potential (a reading potential) is supplied to the fifth wiring 3005 while a predetermined potential (a constant potential) is supplied to the first wiring 3001, whereby the potential of the second wiring 3002 varies depending on the amount of charge retained in the gate electrode of the transistor 3200. This is because in the case of using an n-channel transistor as the transistor 3200, an apparent threshold voltage V_{th_H} at the time when the high-level charge is given to the gate electrode of the transistor 3200 is lower than an apparent threshold voltage V_{th_L} at the time when the low-level charge is given to the gate electrode of the transistor 3200. Here, an apparent threshold voltage refers to the potential of the fifth wiring 3005 which is needed to turn on the transistor 3200. Thus, the potential of the fifth wiring 3005 is set to a potential V_0 which is between V_{th_H} and V_{th_L}, whereby charge supplied to the gate electrode of the transistor 3200 can be determined. For example, in the case where the high-level charge is supplied to the gate electrode of the transistor 3200 in writing and the potential of the fifth wiring 3005 is V_0 (> V_{th_H}), the transistor 3200 is turned on. On the other hand, in the case where the low-level charge is supplied to the gate electrode of the transistor 3200 in writing, even when the potential of the fifth wiring 3005 is V_0 (< V_{th_L}), the transistor 3200 remains off. Thus, the data retained in the gate electrode of the transistor 3200 can be read by determining the potential of the second wiring 3002.

[0242]

Note that in the case where memory cells are arrayed, it is necessary that data of a desired memory cell is read. For example, the fifth wiring 3005 of memory cells from which data is not read may be supplied with a potential at which the transistor 3200 is turned off regardless of the state of the gate electrode, that is, a potential lower than V_{th_H}, whereby only data of a desired memory cell can be read. Alternatively, the fifth wiring 3005 of memory cells from which data is not read may be supplied with a potential at which the transistor 3200 is turned on regardless of the state of the gate electrode, that is, a potential higher than V_{th_L}, whereby only data of a desired memory cell can be read.

[0243]

The semiconductor device illustrated in FIG. 22C is different from the semiconductor device illustrated in FIG. 22A in that the transistor 3200 is not provided. Also in this case, writing and retaining operation of data can be performed in a manner similar to the semiconductor device illustrated in FIG. 22A.

[0244]

Next, reading of data of the semiconductor device illustrated in FIG. 22C is described. When the transistor 3300 is turned on, the third wiring 3003 which is in a floating state and the capacitor 3400 are electrically connected to each other, and the charge is redistributed between the third wiring 3003 and the capacitor 3400. As a result, the potential of the third wiring 3003 is changed. The amount of change in potential of the third wiring 3003 varies depending on the potential of the one electrode of the capacitor 3400 (or the charge accumulated in the capacitor 3400).

[0245]

For example, the potential of the third wiring 3003 after the charge redistribution is $(C_B \times V_{B0} + C \times V) / (C_B + C)$, where V is the potential of the one electrode of the capacitor 3400, C is the capacitance of the capacitor 3400, C_B is the capacitance component of the third wiring 3003, and V_{B0} is the potential of the third wiring 3003 before the charge redistribution. Thus, it can be found that, assuming that the memory cell is in either of two states in which the potential of the one electrode of the capacitor 3400 is V_1 and V_0 ($V_1 > V_0$), the potential of the third wiring 3003 in the case of retaining the potential V_1 ($= (C_B \times V_{B0} + C \times V_1) / (C_B + C)$) is higher than the potential of the third wiring 3003 in the case of retaining the potential V_0 ($= (C_B \times V_{B0} + C \times V_0) / (C_B + C)$).

[0246]

Then, by comparing the potential of the third wiring 3003 with a predetermined potential, data can be read.

[0247]

In this case, a transistor including the first semiconductor material may be used for a driver circuit for driving a memory cell, and a transistor including the second semiconductor material may be stacked over the driver circuit as the transistor 3300.

[0248]

When including a transistor in which a channel formation region is formed using an oxide semiconductor and which has an extremely small off-state current, the semiconductor device described in this embodiment can retain stored data for an extremely long time. In other words, refresh operation becomes unnecessary or the frequency of the refresh operation can be extremely low, which leads to a sufficient reduction in power consumption. Moreover, stored data can be retained for a long time even when power is not supplied (note that a potential is preferably fixed).

[0249]

Further, in the semiconductor device described in this embodiment, high voltage is not needed for writing data and there is no problem of deterioration of elements. Unlike in a conventional nonvolatile memory, for example, it is not necessary to inject and extract electrons into and from a floating gate; thus, a problem such as deterioration of a gate insulating film is not caused. That is, the semiconductor device of the disclosed invention does not have a limit on the number of times data can be rewritten, which is a problem of a conventional nonvolatile memory, and the reliability thereof is drastically improved. Furthermore, data is written depending on the state of the transistor (on or off), whereby high-speed operation can be easily achieved.

[0250]

The memory device described in this embodiment can also be used in an LSI such as a central processing unit (CPU), a digital signal processor (DSP), a custom LSI, or a programmable logic device (PLD), for example.

[0251]

<CPU>

A CPU including a semiconductor device such as any of the above-described transistors or the above-described memory device is described below.

[0252]

FIG. 23 is a block diagram illustrating a configuration example of a CPU including any of the above-described transistors as a component.

[0253]

The CPU illustrated in FIG. 23 includes, over a substrate 1190, an arithmetic logic unit (ALU) 1191, an ALU controller 1192, an instruction decoder 1193, an interrupt controller 1194, a timing controller 1195, a register 1196, a register controller 1197, a bus interface 1198, a rewritable ROM 1199, and a ROM interface 1189. A semiconductor substrate, an SOI substrate, a glass substrate, or the like is used as the substrate 1190. The ROM 1199 and the ROM interface 1189 may be provided over a separate chip. Needless to say, the CPU in FIG. 23 is just an example in which the configuration has been simplified, and an actual CPU may have a variety of configurations depending on the application. For example, the CPU may have the following configuration: a structure including the CPU illustrated in FIG. 23 or an arithmetic circuit is considered as one core; a plurality of such cores are included; and the cores operate in parallel. The number of bits that the CPU can process in an internal arithmetic circuit or in a data bus can be 8, 16, 32, or 64, for example.

[0254]

An instruction that is input to the CPU through the bus interface 1198 is input to the instruction decoder 1193 and decoded therein, and then, input to the ALU controller 1192, the interrupt controller 1194, the register controller 1197, and the timing controller 1195.

[0255]

The ALU controller 1192, the interrupt controller 1194, the register controller 1197, and the timing controller 1195 conduct various controls in accordance with the decoded instruction. Specifically, the ALU controller 1192 generates signals for controlling the operation of the ALU 1191. While the CPU is executing a program, the interrupt controller 1194 judges an interrupt request from an external input/output device or a peripheral circuit on the basis of its priority or a mask state, and processes the request. The register controller 1197 generates an address of the register 1196, and reads/writes data from/to the register 1196 in accordance with the state of the CPU.

[0256]

The timing controller 1195 generates signals for controlling operation timings of the ALU 1191, the ALU controller 1192, the instruction decoder 1193, the interrupt controller 1194, and the register controller 1197. For example, the timing controller 1195 includes an internal clock generator for generating an internal clock signal based on a reference clock signal, and supplies the internal clock signal to the above circuits.

[0257]

In the CPU illustrated in FIG. 23, a memory cell is provided in the register 1196. For the memory cell of the register 1196, any of the above-described transistors, the above-described memory device, or the like can be used.

[0258]

In the CPU illustrated in FIG. 23, the register controller 1197 selects operation of retaining data in the register 1196 in accordance with an instruction from the ALU 1191. That is, the register controller 1197 selects whether data is retained by a flip-flop or by a capacitor in the memory cell included in the register 1196. When data retention by the flip-flop is selected, a power supply voltage is supplied to the memory cell in the register 1196. When data retention by the capacitor is selected, the data is rewritten in the capacitor, and supply of a power supply voltage to the memory cell in the register 1196 can be stopped.

[0259]

FIG. 24 is an example of a circuit diagram of a memory element that can be used as the register 1196. A memory element 1200 includes a circuit 1201 in which stored data is volatile when power supply is stopped, a circuit 1202 in which stored data is nonvolatile even when power supply is stopped, a switch 1203, a switch 1204, a logic element 1206, a capacitor 1207, and a circuit 1220 having a selecting function. The circuit 1202 includes a capacitor 1208, a transistor 1209, and a transistor 1210. Note that the memory element 1200 may further include another element such as a diode, a resistor, or an inductor, as needed.

[0260]

Here, the above-described memory device can be used as the circuit 1202. When supply of a power supply voltage to the memory element 1200 is stopped, GND (0 V) or a potential at which the transistor 1209 in the circuit 1202 is turned off continues to be input to a gate of the transistor 1209. For example, the gate of the transistor 1209 is grounded through a load such as a resistor.

[0261]

Shown here is an example in which the switch 1203 is a transistor 1213 having one conductivity type (e.g., an n-channel transistor) and the switch 1204 is a transistor 1214 having a conductivity type opposite to the one conductivity type (e.g., a p-channel transistor). A first terminal of the switch 1203 corresponds to one of a source and a drain of the transistor 1213, a second terminal of the switch 1203 corresponds to the other of the source and the drain of the transistor 1213, and conduction or non-conduction between the first terminal and the second terminal of the switch 1203 (i.e., the on/off state of the transistor 1213) is selected by a control signal RD input to a gate of the transistor 1213. A first terminal of the switch 1204 corresponds to one of a source and a drain of the transistor 1214, a second terminal of the switch 1204 corresponds to the other of the source and the drain of the transistor 1214, and conduction or non-conduction between the first terminal and the second terminal of the switch 1204 (i.e., the on/off state of the transistor 1214) is selected by the control signal RD input to a gate of the transistor 1214.

[0262]

One of a source and a drain of the transistor 1209 is electrically connected to one of a pair of electrodes of the capacitor 1208 and a gate of the transistor 1210. Here, the connection portion is referred to as a node M2. One of a source and a drain of the transistor 1210 is electrically connected to a line which can supply a low power supply potential (e.g., a GND line), and the other thereof is electrically connected to the first terminal of the switch 1203 (the one of the source and the drain of the transistor 1213). The second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) is electrically connected to the first terminal of the switch 1204 (the one of the source and the drain of the transistor 1214). The second terminal of the switch 1204 (the other of the source and the drain of the transistor 1214) is electrically connected to a line which can supply a power supply potential VDD. The second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213), the first terminal of the switch 1204 (the one of the source and the drain of the transistor 1214), an input terminal of the logic element 1206, and one of a pair of electrodes of the capacitor 1207 are electrically connected to each other. Here, the connection portion is referred to as a node M1. The other of the pair of electrodes of the capacitor 1207 can be supplied with a constant potential. For example, the other of the pair of electrodes of the capacitor 1207 can be supplied with a low power supply potential (e.g., GND) or a high power supply potential (e.g., VDD). The other of the pair of electrodes of the capacitor 1207 is electrically connected to the line which can supply a low power supply potential (e.g., a GND line). The other of the pair of electrodes of the capacitor 1208 can be supplied with a constant potential. For example, the other of the pair of electrodes of the capacitor 1208 can be supplied with the low power supply potential (e.g., GND) or the high power supply potential (e.g., VDD). The other of the pair of electrodes of the capacitor 1208 is electrically connected to the line which can supply a low power supply potential (e.g., a GND line).

[0263]

The capacitor 1207 and the capacitor 1208 are not necessarily provided as long as the parasitic capacitance of the transistor, the wiring, or the like is actively utilized.

[0264]

A control signal WE is input to the gate of the transistor 1209. As for each of the switch 1203 and the switch 1204, a conduction state or a non-conduction state between the first terminal and the second terminal is selected by the control signal RD which is different from the control signal WE. When the first terminal and the second terminal of one of the switches are in the conduction state, the first terminal and the second terminal of the other of the switches are in the non-conduction state.

[0265]

A signal corresponding to data retained in the circuit 1201 is input to the other of the source and the drain of the transistor 1209. FIG. 24 illustrates an example in which a signal output from the circuit 1201 is input to the other of the source and the drain of the transistor 1209. The logic value of a signal output from the second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) is inverted by the logic element 1206, and the inverted signal is input to the circuit 1201 through the circuit 1220.

[0266]

In the example of FIG. 24, a signal output from the second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) is input to the circuit 1201 through the logic element 1206 and the circuit 1220; however, one embodiment of the present invention is not limited thereto. The signal output from the second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) may be input to the circuit 1201 without its logic value being inverted. For example, in the case where the circuit 1201 includes a node in which a signal obtained by inversion of the logic value of a signal input from the input terminal is retained, the signal output from the second terminal of the switch 1203 (the other of the source and the drain of the transistor 1213) can be input to the node.

[0267]

In FIG. 24, the transistors included in the memory element 1200 except for the transistor 1209 can each be a transistor in which a channel is formed in a film formed using a semiconductor other than an oxide semiconductor or in the substrate 1190. For example, the transistor can be a transistor whose channel is formed in a silicon film or a silicon substrate. Alternatively, all the transistors in the memory element 1200 may be a transistor in which a channel is formed in an oxide semiconductor. Further alternatively, in the memory element 1200, a transistor in which a channel is formed in an oxide semiconductor may be included besides the transistor 1209, and a transistor in which a channel is formed in a layer formed using a semiconductor other than an oxide semiconductor or in the substrate 1190 can be used for the rest of the transistors.

[0268]

As the circuit 1201 in FIG. 24, for example, a flip-flop circuit can be used. As the logic element 1206, for example, an inverter or a clocked inverter can be used.

[0269]

In a period during which the memory element 1200 is not supplied with the power supply voltage, the semiconductor device of one embodiment of the present invention can retain data stored in the circuit 1201 by the capacitor 1208 which is provided in the circuit 1202.

[0270]

The off-state current of a transistor in which a channel is formed in an oxide semiconductor is extremely small. For example, the off-state current of a transistor in which a channel is formed in an oxide semiconductor is significantly smaller than that of a transistor in which a channel is formed in silicon having crystallinity. Thus, when the transistor is used as the transistor 1209, a signal held in the capacitor 1208 is retained for a long time also in a period during which the power supply voltage is not supplied to the memory element 1200. The memory element 1200 can accordingly retain the stored content (data) also in a period during which the supply of the power supply voltage is stopped.

[0271]

Since the above-described memory element performs pre-charge operation with the switch 1203 and the switch 1204, the time required for the circuit 1201 to retain original data again after the supply of the power supply voltage is restarted can be shortened.

[0272]

In the circuit 1202, a signal retained by the capacitor 1208 is input to the gate of the transistor 1210. Thus, after supply of the power supply voltage to the memory element 1200 is restarted, the signal retained by the capacitor 1208 can be converted into the one corresponding to the state (the on state or the off state) of the transistor 1210 to be read from the circuit 1202. Consequently, an original signal can be accurately read even when a potential corresponding to the signal retained by the capacitor 1208 varies to some degree.

[0273]

By applying the above-described memory element 1200 to a memory device such as a register or a cache memory included in a processor, data in the memory device can be prevented from being lost owing to the stop of the supply of the power supply voltage. Furthermore, shortly after the supply of the power supply voltage is restarted, the memory device can be returned to the same state as that before the power supply is stopped. Thus, the power supply can be stopped even for a short time in the processor or one or a plurality of logic circuits included in the processor, resulting in lower power consumption.

[0274]

Although the memory element 1200 is used in a CPU, the memory element 1200 can also be used in an LSI such as a digital signal processor (DSP), a custom LSI, or a programmable logic device (PLD), and a radio frequency identification (RF-ID).

[0275]

<Display device>

The following shows configuration examples of a display device of one embodiment of the present invention.

[0276]

[Configuration example]

FIG. 25A is a top view of a display device of one embodiment of the present invention. FIG. 25B illustrates a pixel circuit where a liquid crystal element is used for a pixel of a display device of one embodiment of the present invention. FIG. 25C illustrates a pixel circuit where an organic EL element is used for a pixel of a display device of one embodiment of the present invention.

[0277]

Any of the above-described transistors can be used as a transistor used for the pixel. Here, an example in which an n-channel transistor is used is shown. Note that a transistor manufactured through the same steps as the transistor used for the pixel may be used for a driver circuit. Thus, by using any of the above-described transistors for a pixel or a driver circuit, the display device can have high display quality and/or high reliability.

[0278]

FIG. 25A illustrates an example of an active matrix display device. A pixel portion 5001, a first scan line driver circuit 5002, a second scan line driver circuit 5003, and a signal line driver circuit 5004 are provided over a substrate 5000 in the display device. The pixel portion 5001 is electrically connected to the signal line driver circuit 5004 through a plurality of signal lines and is electrically connected to the first scan line driver circuit 5002 and the second scan line driver circuit 5003 through a plurality of scan lines. Pixels including display elements are provided in respective regions divided by the scan lines and the signal lines. The substrate 5000 of the display device is electrically connected to a timing control circuit (also referred to as a controller or a control IC) through a connection portion such as a flexible printed circuit (FPC).

[0279]

The first scan line driver circuit 5002, the second scan line driver circuit 5003, and the signal line driver circuit 5004 are formed over the substrate 5000 where the pixel portion 5001 is formed. Therefore, a display device can be manufactured at cost lower than that in the case where a driver circuit is separately formed. Further, in the case where a driver circuit is separately formed, the number of wiring connections is increased. By providing the driver circuit over the substrate 5000, the number of wiring connections can be reduced. Accordingly, the reliability and/or yield can be improved.

[0280]

[Liquid crystal display device]

FIG. 25B illustrates an example of a circuit configuration of the pixel. Here, a pixel circuit which is applicable to a pixel of a VA liquid crystal display device, or the like is illustrated.

[0281]

This pixel circuit can be applied to a structure in which one pixel includes a plurality of pixel electrodes. The pixel electrodes are connected to different transistors, and the transistors can be driven with different gate signals. Accordingly, signals applied to individual pixel electrodes in a multi-domain pixel can be controlled independently.

[0282]

A scan line 5012 of a transistor 5016 and a scan line 5013 of a transistor 5017 are separated so that different gate signals can be supplied thereto. In contrast, a signal line 5014 is shared by the transistors 5016 and 5017. Any of the above-described transistors can be used as appropriate as each of the transistors 5016 and 5017. Thus, the liquid crystal display device can have high display quality and/or high reliability.

[0283]

A first pixel electrode is electrically connected to the transistor 5016 and a second pixel electrode is electrically connected to the transistor 5017. The first pixel electrode and the second pixel electrode are separated. A shape of the first pixel electrode and the second pixel electrode is not especially limited, and for example, the first pixel electrode may have a V-like shape.

[0284]

A gate electrode of the transistor 5016 is electrically connected to the scan line 5012, and a gate electrode of the transistor 5017 is electrically connected to the scan line 5013. When different gate signals are supplied to the scan line 5012 and the scan line 5013, operation timings of the transistor 5016 and the transistor 5017 can be varied. As a result, alignment of liquid crystals can be controlled.

[0285]

Further, a capacitor may be formed using a capacitor line 5010, a gate insulator functioning as a dielectric, and a capacitor electrode electrically connected to the first pixel electrode or the second pixel electrode.

[0286]

The multi-domain pixel includes a first liquid crystal element 5018 and a second liquid crystal element 5019 in one pixel. The first liquid crystal element 5018 includes the first pixel electrode, a counter electrode, and a liquid crystal layer therebetween. The second liquid crystal element 5019 includes the second pixel electrode, a counter electrode, and a liquid crystal layer therebetween.

[0287]

Note that a pixel circuit in the display device of one embodiment of the present invention is not limited to that shown in FIG. 25B. For example, a switch, a resistor, a capacitor, a transistor, a sensor, a logic circuit, or the like may be added to the pixel circuit shown in FIG. 25B.

[0288]

[Organic EL display device]

FIG. 25C illustrates another example of a circuit configuration of the pixel. Here, a pixel structure of a display device using an organic EL element is shown.

[0289]

In an organic EL element, by application of voltage to a light-emitting element, electrons are injected from one of a pair of electrodes included in the organic EL element and holes are injected from the other of the pair of electrodes, into a layer containing a light-emitting organic compound; thus, current flows. The electrons and holes are recombined, and thus, the light-emitting organic compound is excited. The light-emitting organic compound returns to a ground state from the excited state, thereby emitting light. Owing to such a mechanism, this light-emitting element is referred to as a current-excitation light-emitting element.

[0290]

FIG. 25C illustrates an example of a pixel circuit. Here, one pixel includes two n-channel transistors. Note that any of the above-described transistors can be used as the n-channel transistors. Further, digital time grayscale driving can be employed for the pixel circuit.

[0291]

The configuration of the applicable pixel circuit and operation of a pixel employing digital time grayscale driving are described.

[0292]

A pixel 5020 includes a switching transistor 5021, a driver transistor 5022, a light-emitting element 5024, and a capacitor 5023. A gate electrode of the switching transistor 5021 is connected to a scan line 5026, a first electrode (one of a source electrode and a drain electrode) of the switching transistor 5021 is connected to a signal line 5025, and a second electrode (the other of the source electrode and the drain electrode) of the switching transistor 5021 is connected to a gate electrode of the driver transistor 5022. The gate electrode of the driver transistor 5022 is connected to a power supply line 5027 through the capacitor 5023, a first electrode of the driver transistor 5022 is connected to the power supply line 5027, and a second electrode of the driver transistor 5022 is connected to a first electrode (a pixel electrode) of the light-emitting element 5024. A second electrode of the light-emitting element 5024 corresponds to a common electrode 5028. The common electrode 5028 is electrically connected to a common potential line provided over the same substrate.

[0293]

As each of the switching transistor 5021 and the driver transistor 5022, any of the above-described transistors can be used as appropriate. In this manner, an organic EL display device having high display quality and/or high reliability can be provided.

[0294]

The potential of the second electrode (the common electrode 5028) of the light-emitting element 5024 is set to be a low power supply potential. Note that the low power supply potential is lower than a high power supply potential supplied to the power supply line 5027. For example, the low power supply potential can be GND, 0 V, or the like. The high power supply potential and the low power supply potential are set to be higher than or equal to the forward threshold voltage of the light-emitting element 5024, and the difference between the potentials is applied to the light-emitting element 5024, whereby current is supplied to the light-emitting element 5024, leading to light emission. The forward voltage of the light-emitting element 5024 refers to a voltage at which a desired luminance is obtained, and includes at least forward threshold voltage.

[0295]

Note that gate capacitance of the driver transistor 5022 may be used as a substitute for the capacitor 5023 in some cases, so that the capacitor 5023 can be omitted. The gate capacitance of the driver transistor 5022 may be formed between the channel formation region and the gate electrode.

[0296]

Next, a signal input to the driver transistor 5022 is described. In the case of a voltage-input voltage driving method, a video signal for turning on or off the driver transistor 5022 is input to the driver transistor 5022. In order for the driver transistor

5022 to operate in a linear region, voltage higher than the voltage of the power supply line 5027 is applied to the gate electrode of the driver transistor 5022. Note that voltage higher than or equal to voltage which is the sum of power supply line voltage and the threshold voltage V_{th} of the driver transistor 5022 is applied to the signal line 5025.

[0297]

In the case of performing analog grayscale driving, a voltage higher than or equal to a voltage which is the sum of the forward voltage of the light-emitting element 5024 and the threshold voltage V_{th} of the driver transistor 5022 is applied to the gate electrode of the driver transistor 5022. A video signal by which the driver transistor 5022 is operated in a saturation region is input, so that current is supplied to the light-emitting element 5024. In order for the driver transistor 5022 to operate in a saturation region, the potential of the power supply line 5027 is set higher than the gate potential of the driver transistor 5022. When an analog video signal is used, it is possible to supply current to the light-emitting element 5024 in accordance with the video signal and perform analog grayscale driving.

[0298]

Note that in the display device of one embodiment of the present invention, a pixel configuration is not limited to that shown in FIG. 25C. For example, a switch, a resistor, a capacitor, a sensor, a transistor, a logic circuit, or the like may be added to the pixel circuit shown in FIG. 25C.

[0299]

In the case where any of the above-described transistors is used for the circuit shown in FIGS. 25A to 25C, the source electrode (the first electrode) is electrically connected to the low potential side and the drain electrode (the second electrode) is electrically connected to the high potential side. Further, the potential of the first gate electrode may be controlled by a control circuit or the like and the potential described above as an example, e.g., a potential lower than the potential applied to the source electrode, may be input to the second gate electrode.

[0300]

For example, in this specification and the like, a display element, a display device which is a device including a display element, a light-emitting element, and a light-emitting device which is a device including a light-emitting element can employ various modes or can include various elements. The display element, the display device, the light-emitting element, or the light-emitting device includes at least one of an electroluminescence (EL) element (e.g., an EL element including organic and inorganic materials, an organic EL element, or an inorganic EL element), an LED (e.g., a white LED, a red LED, a green LED, or a blue LED), a transistor (a transistor that emits light depending on current), an electron emitter, a liquid crystal element, electronic ink, an electrophoretic element, a grating light valve (GLV), a plasma display panel (PDP), a display element using micro electro mechanical systems (MEMS), a digital micromirror device (DMD), a digital micro shutter (DMS), an interferometric modulator display (IMOD) element, a MEMS shutter display element, an optical-interference-type MEMS display element, an electrowetting element, a piezoelectric ceramic display, a display element including a carbon nanotube, and the like. Other than the above, a display medium whose contrast, luminance, reflectance, transmittance, or the like is changed by an electrical or magnetic effect may be included. Note that examples of a display device including an EL element include an EL display. Examples of a display device having an electron emitter include a field emission display (FED), an SED-type flat panel display (SED: surface-conduction electron-emitter display), and the like. Examples of display devices including liquid crystal elements include a liquid crystal display (e.g., a transmissive liquid crystal display, a transflective liquid crystal display, a reflective liquid crystal display, a direct-view liquid crystal display, or a projection liquid crystal display). Display devices having electronic ink or electrophoretic elements include electronic paper and the like. In the case of a transflective liquid crystal display or a reflective liquid crystal display, some of or all of pixel electrodes function as reflective electrodes. For example, some or all of pixel electrodes are formed to contain aluminum, silver, or the like. In such a case, a memory circuit such as an SRAM can be provided under the reflective electrodes. Thus, the power consumption can be further reduced. Note that in the case of using an LED, graphene or graphite may be provided under an electrode or a nitride semiconductor of the LED. Graphene or graphite may be a multilayer film in which a plurality of layers are stacked. As described above, provision of graphene or graphite enables easy formation of a nitride semiconductor thereover, such as an n-type GaN semiconductor including crystals. Furthermore, a p-type GaN semiconductor including crystals or the like can be provided thereover, and thus the LED can be formed. Note that AlN may be provided between the n-type GaN semiconductor including crystals and graphene or graphite. The GaN semiconductors included in the LED may be formed by MOCVD. Note that when the graphene is provided, the GaN semiconductors included in the LED can also be formed by a sputtering method.

[0301]

<Electronic device>

The semiconductor device of one embodiment of the present invention can be used for display devices, personal computers, or image reproducing devices provided with recording media (typically, devices which reproduce the content of recording media such as digital versatile discs (DVDs) and have displays for displaying the reproduced images). Other examples of electronic devices that can be equipped with the semiconductor device of one embodiment of the present invention are mobile phones, game machines including portable game consoles, portable data appliances, e-book readers, cameras such as video cameras and digital still cameras, goggle-type displays (head mounted displays), navigation systems, audio reproducing devices (e.g., car audio systems and digital audio players), copiers, facsimiles, printers, multifunction printers, automated teller machines (ATM), and vending machines. FIGS. 26A to 26F illustrate specific examples of these electronic devices.

[0302]

FIG. 26A illustrates a portable game console including a housing 901, a housing 902, a display portion 903, a display portion 904, a microphone 905, a speaker 906, an operation key 907, a stylus 908, and the like. Although the portable game machine in FIG. 26A has the two display portions 903 and 904, the number of display portions included in a portable game machine is not limited to this.

[0303]

FIG. 26B illustrates a portable data terminal including a first housing 911, a second housing 912, a first display portion 913, a second display portion 914, a joint 915, an operation key 916, and the like. The first display portion 913 is provided in the first housing 911, and the second display portion 914 is provided in the second housing 912. The first housing 911 and the second housing 912 are connected to each other with the joint 915, and the angle between the first housing 911 and the second housing 912 can be changed with the joint 915. An image on the first display portion 913 may be switched depending on the angle between the first housing 911 and the second housing 912 at the joint 915. A display device with a position input function may be used as at least one of the first display portion 913 and the second display portion 914. Note that the position input function can be added by providing a touch panel in a display device. Alternatively, the position input function can be added by provision of a photoelectric conversion element called a photosensor in a pixel portion of a display device.

[0304]

FIG. 26C illustrates a laptop personal computer, which includes a housing 921, a display portion 922, a keyboard 923, a pointing device 924, and the like.

[0305]

FIG. 26D illustrates the electric refrigerator-freezer including a housing 931, a door for a refrigerator 932, a door for a freezer 933, and the like.

[0306]

FIG. 26E illustrates a video camera, which includes a first housing 941, a second housing 942, a display portion 943, operation keys 944, a lens 945, a joint 946, and the like. The operation keys 944 and the lens 945 are provided for the first housing 941, and the display portion 943 is provided for the second housing 942. The first housing 941 and the second housing 942 are connected to each other with the joint 946, and the angle between the first housing 941 and the second housing 942 can be changed with the joint 946. Images displayed on the display portion 943 may be switched in accordance with the angle at the joint 946 between the first housing 941 and the second housing 942.

[0307]

FIG. 26F illustrates a vehicle including a car body 951, wheels 952, a dashboard 953, lights 954, and the like.

[0308]

The structures, the methods, and the like described in this embodiment can be combined as appropriate with any of the structures, the methods, and the like described in the other embodiments.

EXPLANATION OF REFERENCE

[0309]

11: area, 100: transistor, 101: substrate, 104: insulating layer, 110: a base film, 120: insulating layer, 120A: insulating film, 125: insulating layer, 130: oxide semiconductor layer, 130A: oxide semiconductor film, 135: hard mask, 140: electrode, 140A: conductive film, 145: resist mask, 150: electrode, 150A: conductive film, 150B: conductive film, 160: insulating layer, 160A: insulating film, 170: electrode, 170A: conductive film, 170B: conductive film, 181: wiring, 182: wiring, 183: wiring, 190: insulator, 195: insulator, 195A: insulator, 195a: insulator, 195b: insulator, 200: transistor, 231: wiring, 282: wiring, 300: transistor, 381: wiring, 382: wiring, 901: housing, 902: housing, 903: display portion, 904: display portion, 905: microphone, 906: speaker, 907: operation key, 908: stylus, 911: housing, 912: housing, 913: display portion, 914: display portion, 915: joint, 916: operation key, 921: housing, 922: display portion, 923: keyboard, 924: pointing device, 931: housing, 932: refrigerator, 933: refrigerator, 941: housing, 942: housing, 943: display portion, 944: operation key, 945: lens, 946: joint, 951: car body, 952: wheel, 953: dashboard, 954: light, 1189: ROM interface, 1190: substrate, 1191: ALU, 1192: ALU controller, 1193: instruction decoder, 1194: interrupt controller, 1195: timing controller, 1196: register, 1197: register controller, 1198: bus interface, 1199: ROM, 1200: memory element, 1201: circuit, 1202: circuit, 1203: switch, 1204: switch, 1206: logic element, 1207: capacitor, 1208: capacitor, 1209: transistor, 1210: transistor, 1213: transistor, 1214: transistor, 1220: circuit, 2001: substrate, 2004: plug, 2100: transistor, 2200: transistor, 2201: insulating film, 2202: wiring, 2203: plug, 2204: interlayer insulating film, 2207: insulating film, 2211: semiconductor substrate, 2212: insulating film, 2213: gate electrode, 2214: gate insulating film, 2215: drain region, 2300: transistor, 2301: impurity region, 2302: impurity region, 2303: gate electrode, 2304: gate insulating film, 2305: sidewall insulating film, 2400: photodiode, 2401: conductive film, 2402: conductive film, 2403: conductive film, 2500: photodiode, 2501: conductive film, 2502: conductive film, 2503: semiconductor, 2504: plug, 3001: wiring, 3002: wiring, 3003: wiring, 3004: wiring, 3005: wiring, 3200: transistor, 3300: transistor, 3400: capacitor, 5000: substrate, 5001: pixel portion, 5002: scan line driver circuit, 5003: scan line driver circuit, 5004: signal line driver circuit, 5010: capacitor line, 5012: scan line, 5013: scan line, 5014: signal line, 5016: transistor, 5017: transistor, 5018: liquid crystal element, 5019: liquid crystal element, 5020: pixel, 5021: switching transistor, 5022: driver transistor, 5023: capacitor, 5024: light-emitting element, 5025: signal line, 5026: scan line, 5027: power supply line, 5028: common electrode, 5100: pellet, 5120: substrate, 5161: region, 5200: pellet, 5201: ion, 5203: particle, 5220: substrate, 5230: target, 5240: plasma, 5260: heating mechanism.

This application is based on Japanese Patent Application serial no. 2015-024836 filed with Japan Patent Office on February 11, 2015, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising a transistor, the transistor comprising:

a first electrode;

a second electrode;

a third electrode;

an oxide semiconductor layer;

a first insulating layer; and

a second insulating layer,

wherein the transistor includes a first region and a second region surrounded by the first region,

wherein in the first region, the first insulating layer, the second electrode, the oxide semiconductor layer, and the second insulating layer are stacked, and

wherein in the second region, the first electrode, the oxide semiconductor layer, the second insulating layer, and the third electrode are stacked.

2. A semiconductor device comprising a transistor, the transistor comprising:

a first electrode;

a second electrode having an opening;

a third electrode;

an oxide semiconductor layer;

a first insulating layer; and

a second insulating layer,

wherein the transistor includes a first region overlapping with the second electrode and a second region overlapping with the opening,

wherein in the first region, the first insulating layer, the second electrode, the oxide semiconductor layer, and the second insulating layer are stacked, and

wherein in the second region, the first electrode, the oxide semiconductor layer, the second insulating layer, and the third electrode are stacked.

3. A semiconductor device comprising a transistor, the transistor comprising:

a first electrode;

a second electrode;

a third electrode;

an oxide semiconductor layer;

a first insulating layer; and

a second insulating layer,

wherein the second electrode and the first insulating layer have an opening,

wherein a side surface and a bottom surface of the third electrode are covered with the second insulating layer, and

wherein the third electrode is embedded in the opening.

4. The semiconductor device according to claim 1, wherein the first insulating layer contains oxygen.

5. The semiconductor device according to claim 1,

wherein the first electrode functions as one of a source electrode and a drain electrode, and

wherein the second electrode functions as the other of the source electrode and the drain electrode.

6. An electronic device comprising the semiconductor device according to claim 1.

FIG. 1A

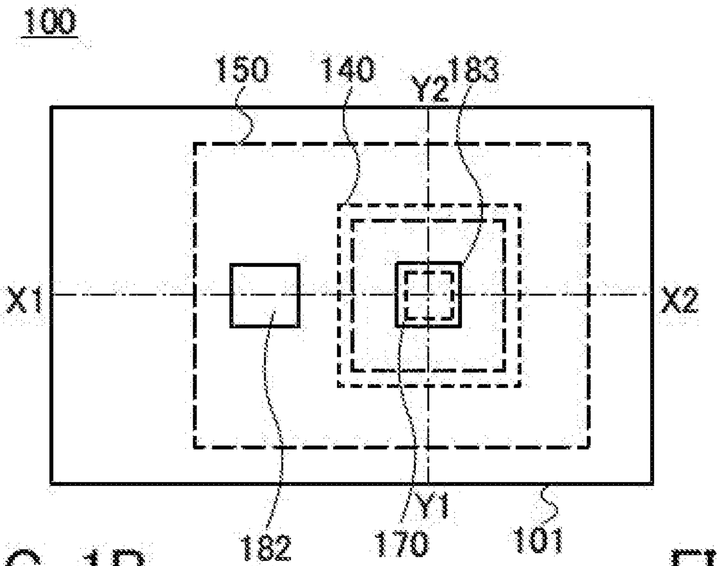


FIG. 1B

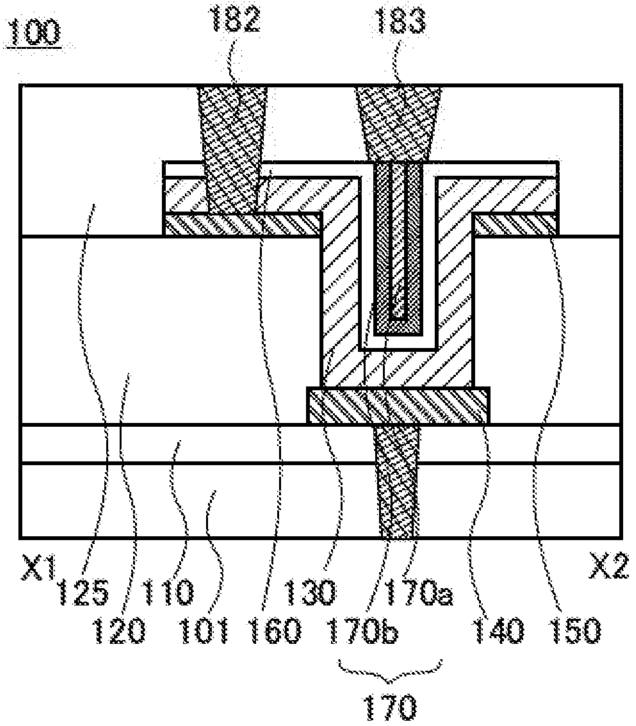


FIG. 1C

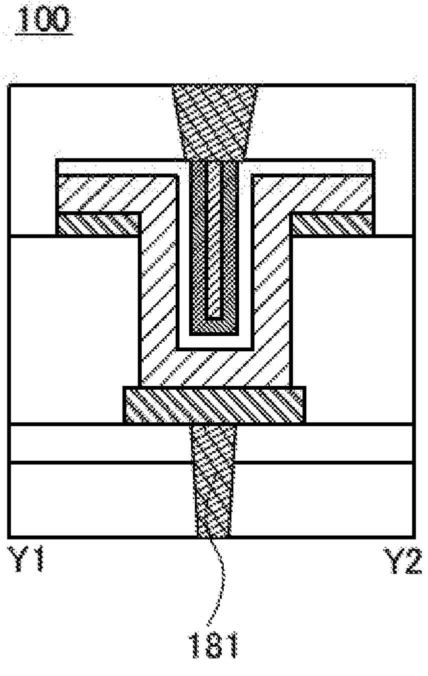


FIG. 2A

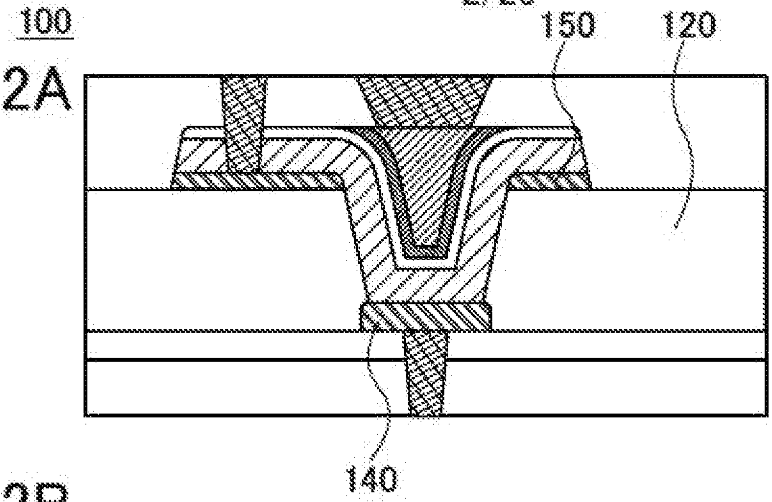


FIG. 2B

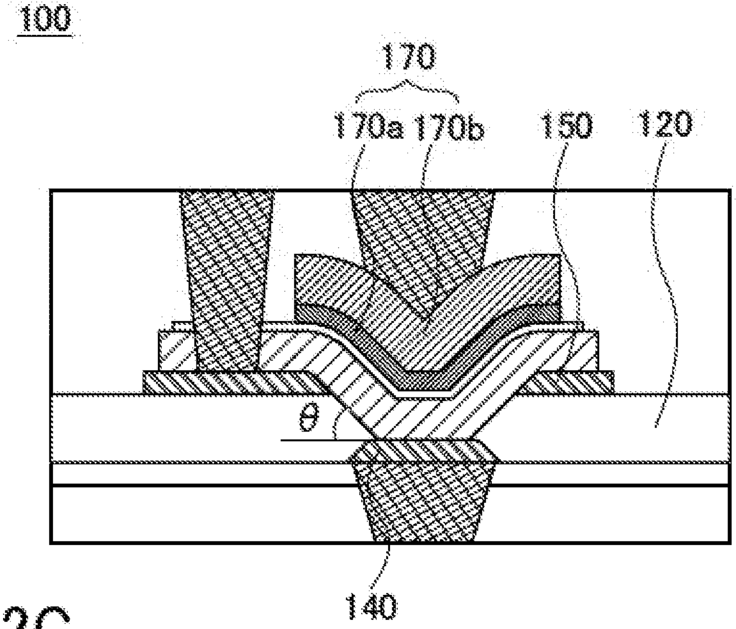


FIG. 2C

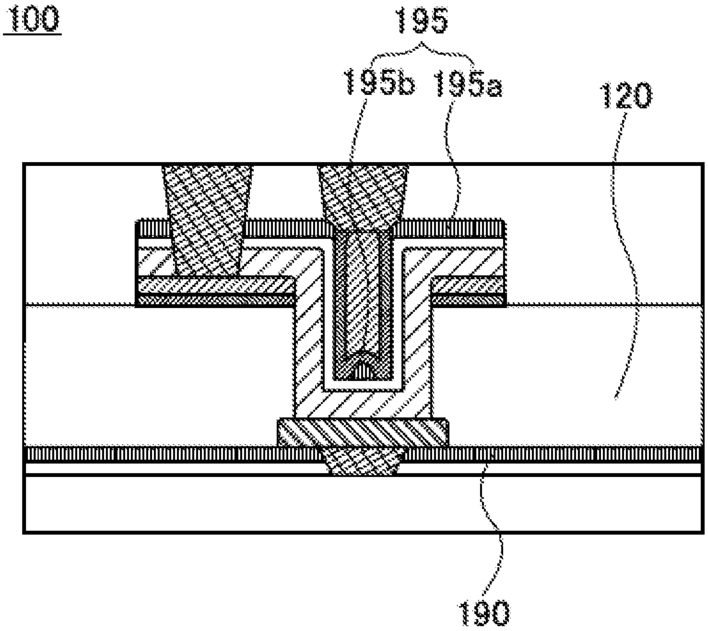


FIG. 3A

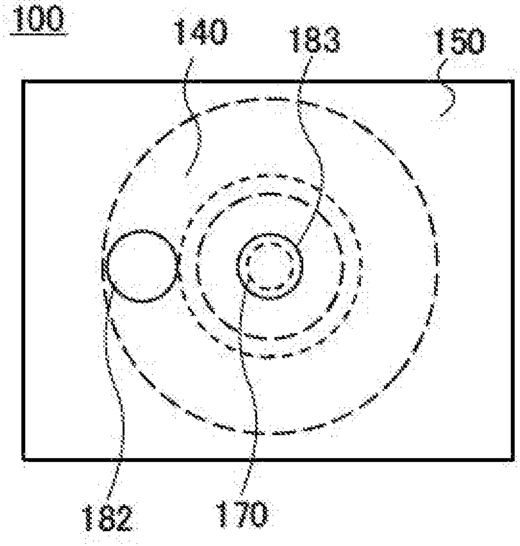


FIG. 3B

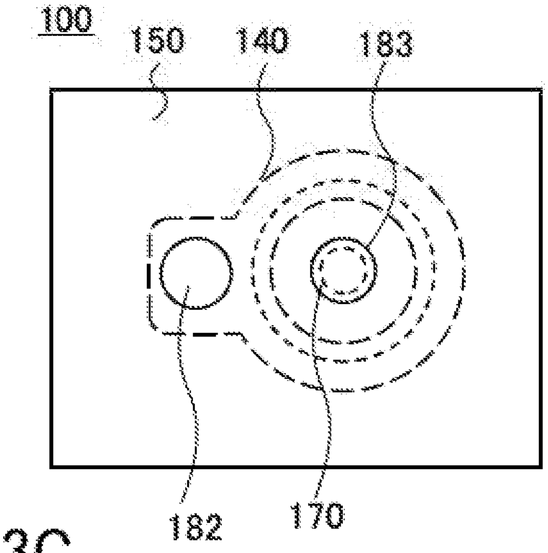


FIG. 3C

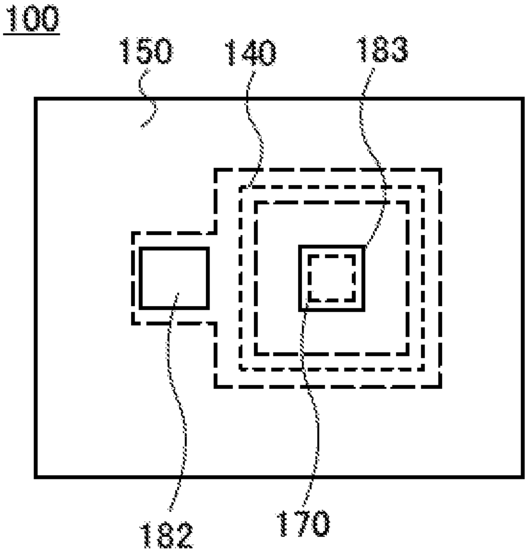


FIG. 4A

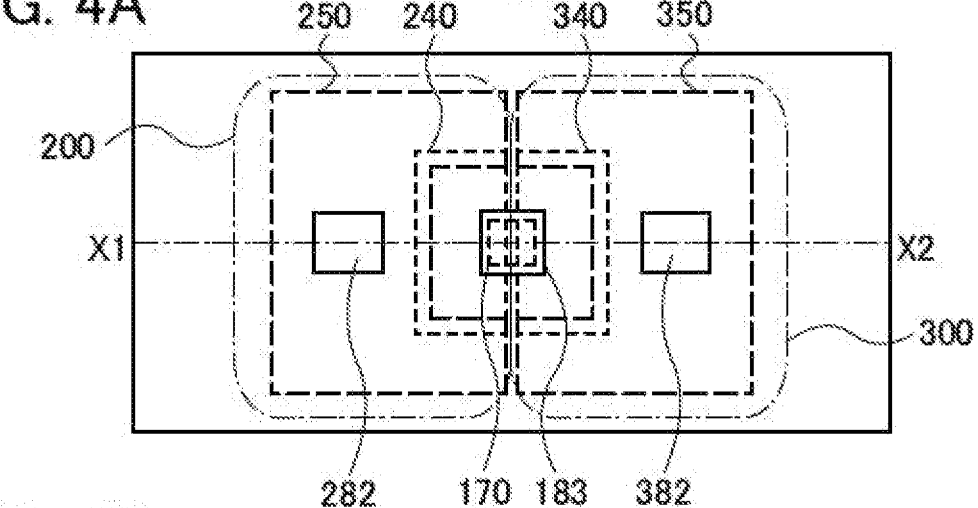


FIG. 4B

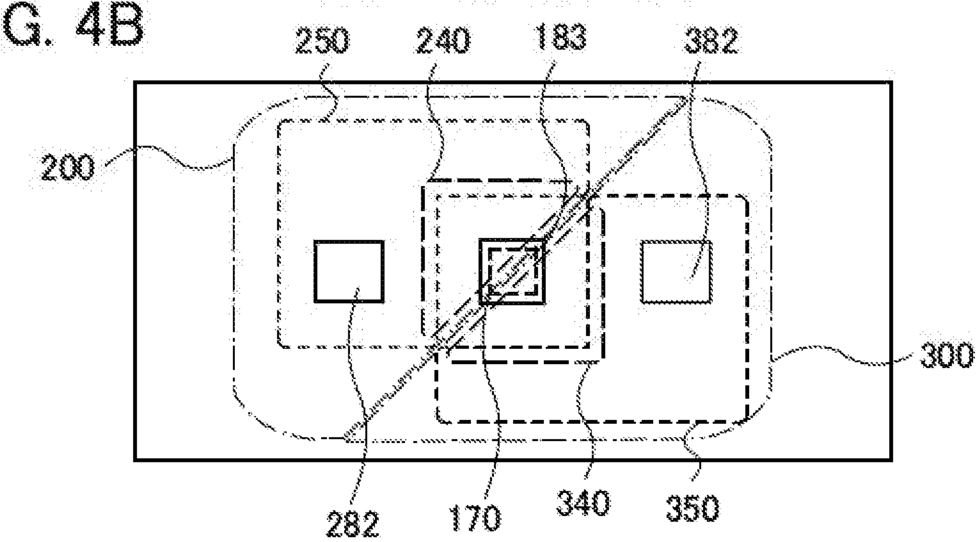


FIG. 4C

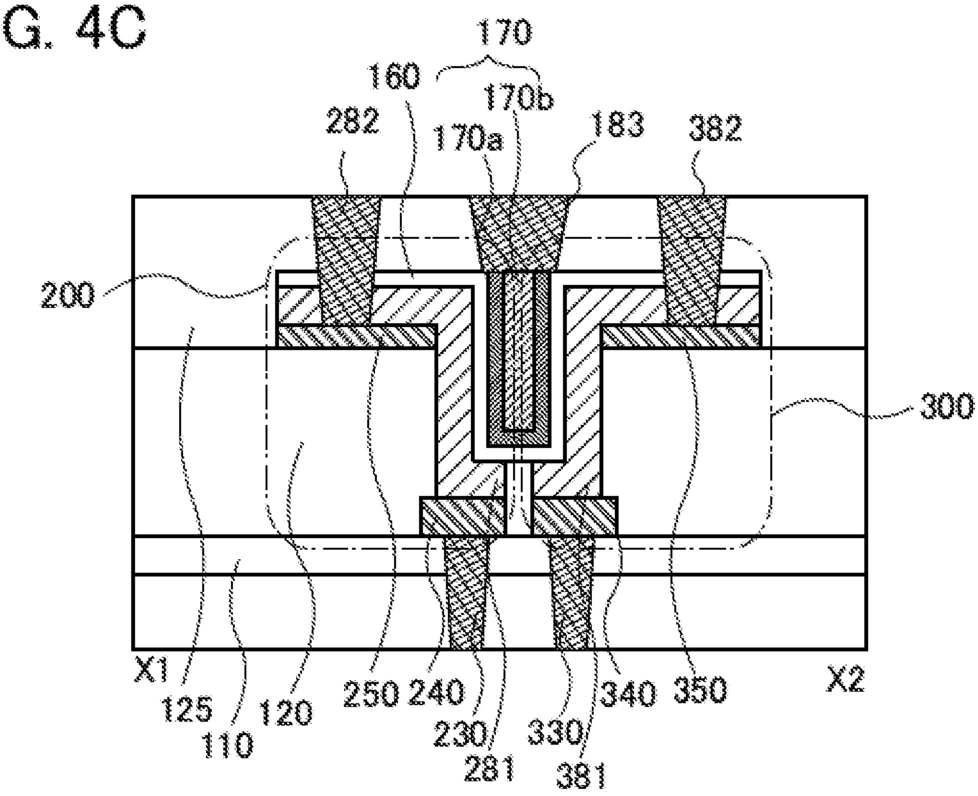


FIG. 5A

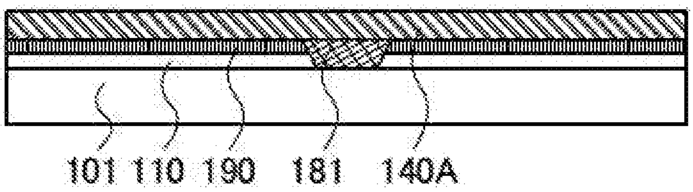


FIG. 5B

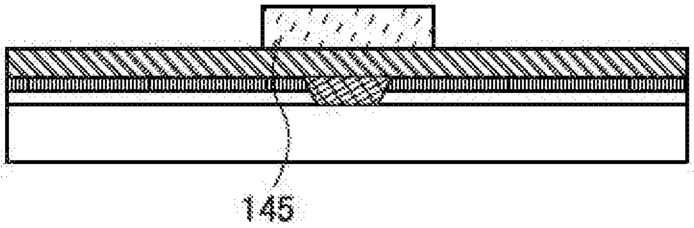


FIG. 5C

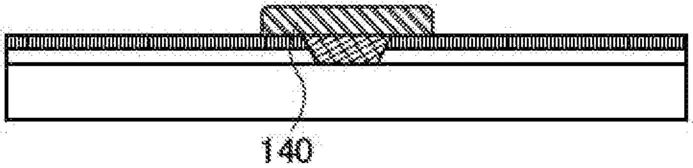


FIG. 5D

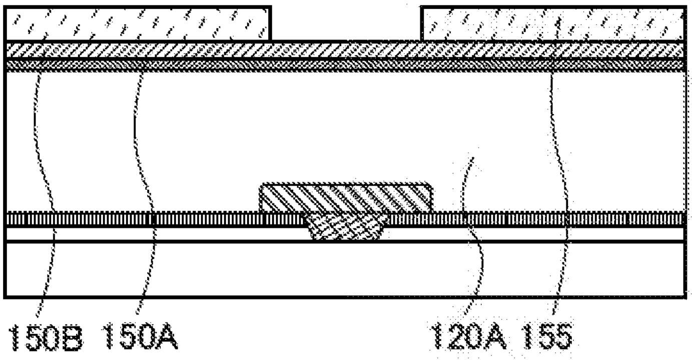


FIG. 5E

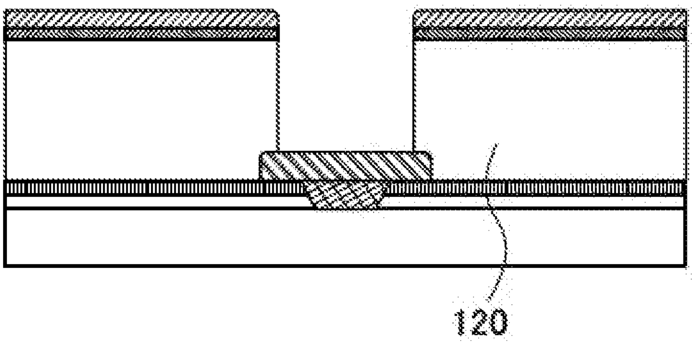


FIG. 6A

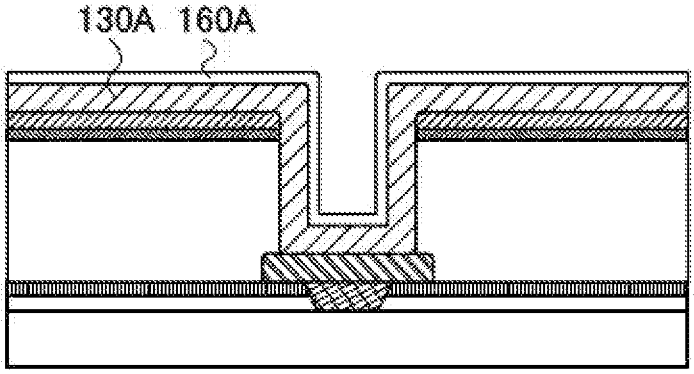


FIG. 6B

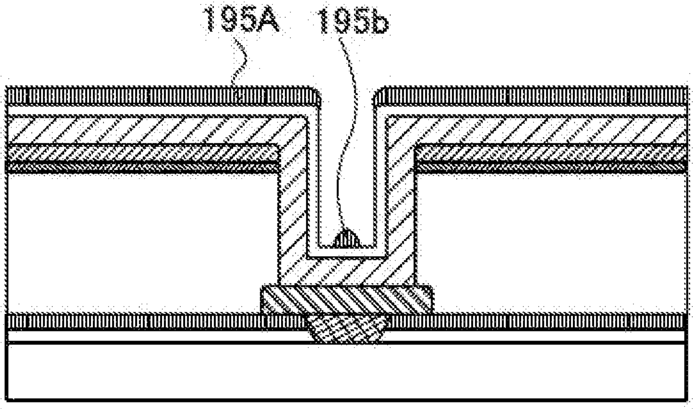


FIG. 6C

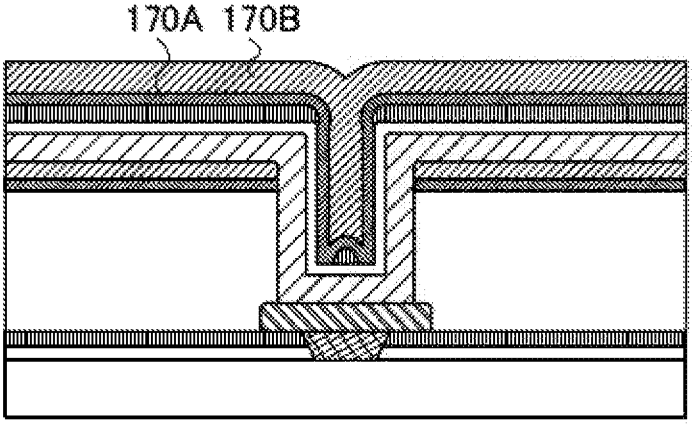


FIG. 6D

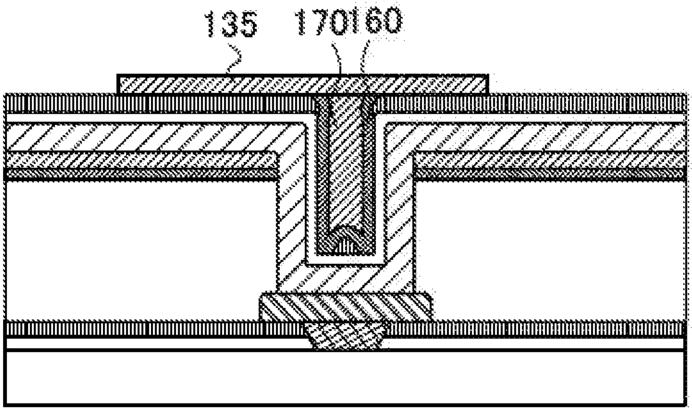


FIG. 7A

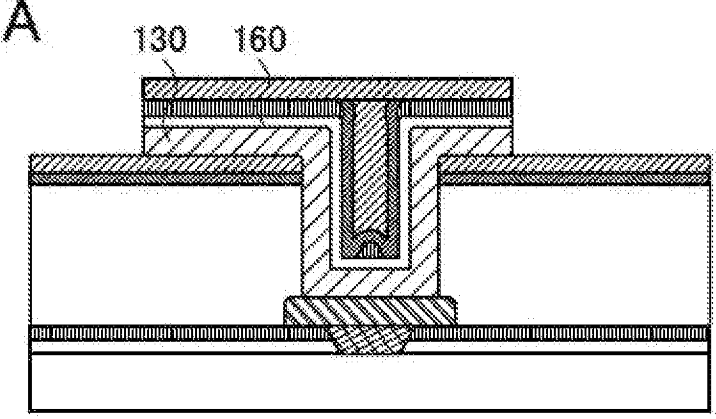


FIG. 7B

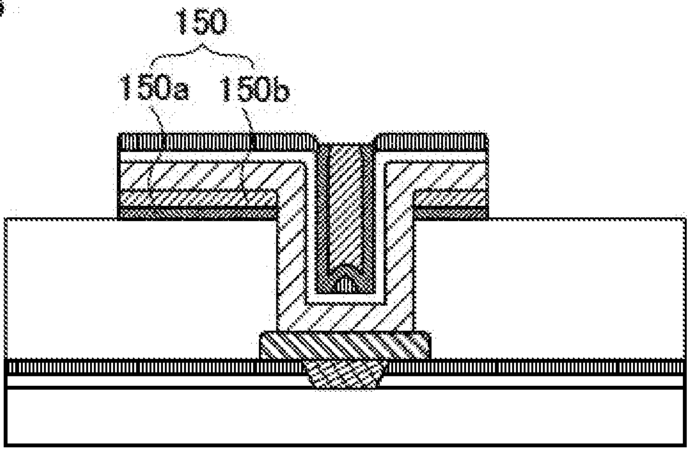


FIG. 7C

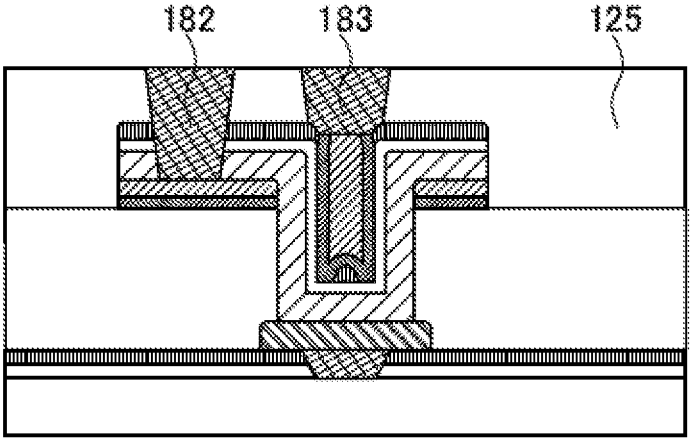


FIG. 8A

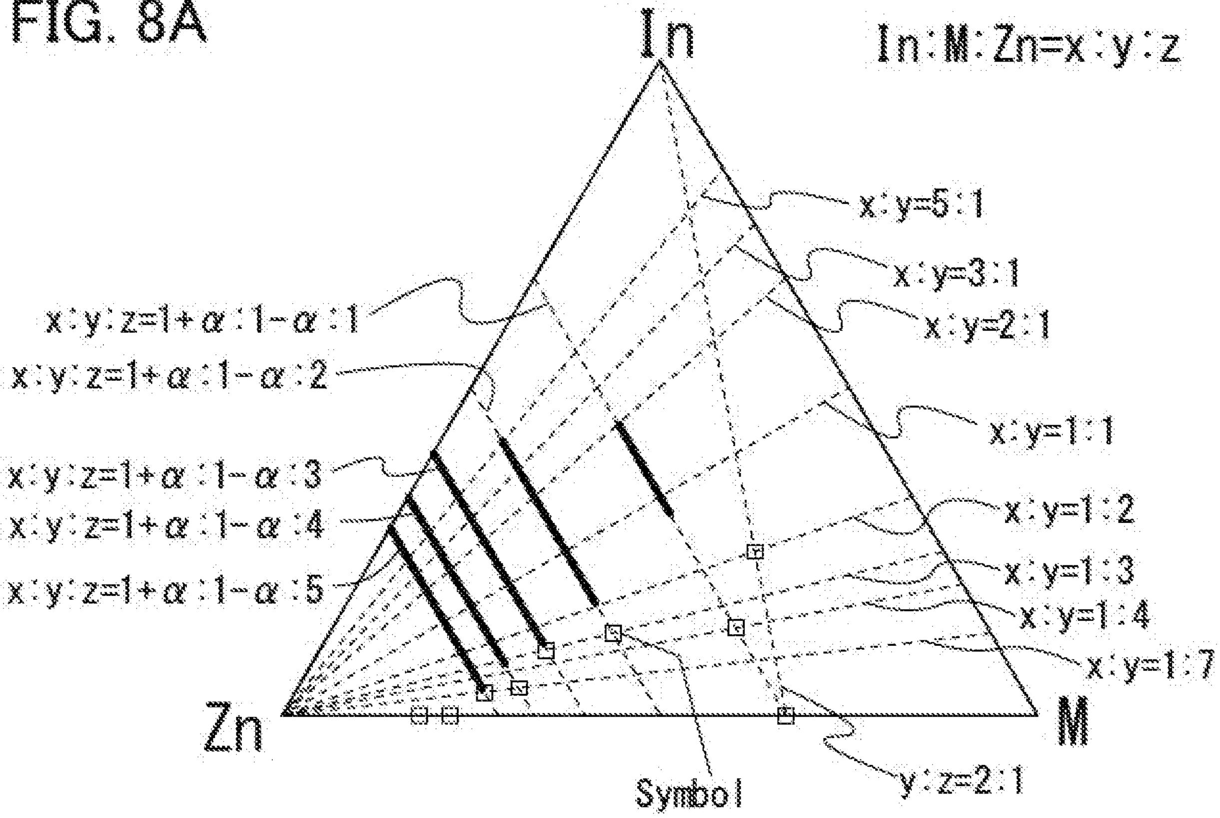

In
In:M:Zn=x:y:z
x:y=5:1
x:y=3:1
x:y=2:1
x:y:z=1+α:1-α:1
x:y:z=1+α:1-α:2
x:y=1:1
x:y:z=1+α:1-α:3
x:y:z=1+α:1-α:4
x:y=1:2
x:y=1:3
x:y:z=1+α:1-α:5
x:y=1:4
x:y=1:7
Zn
M
Symbol
y:z=2:1

FIG. 8B

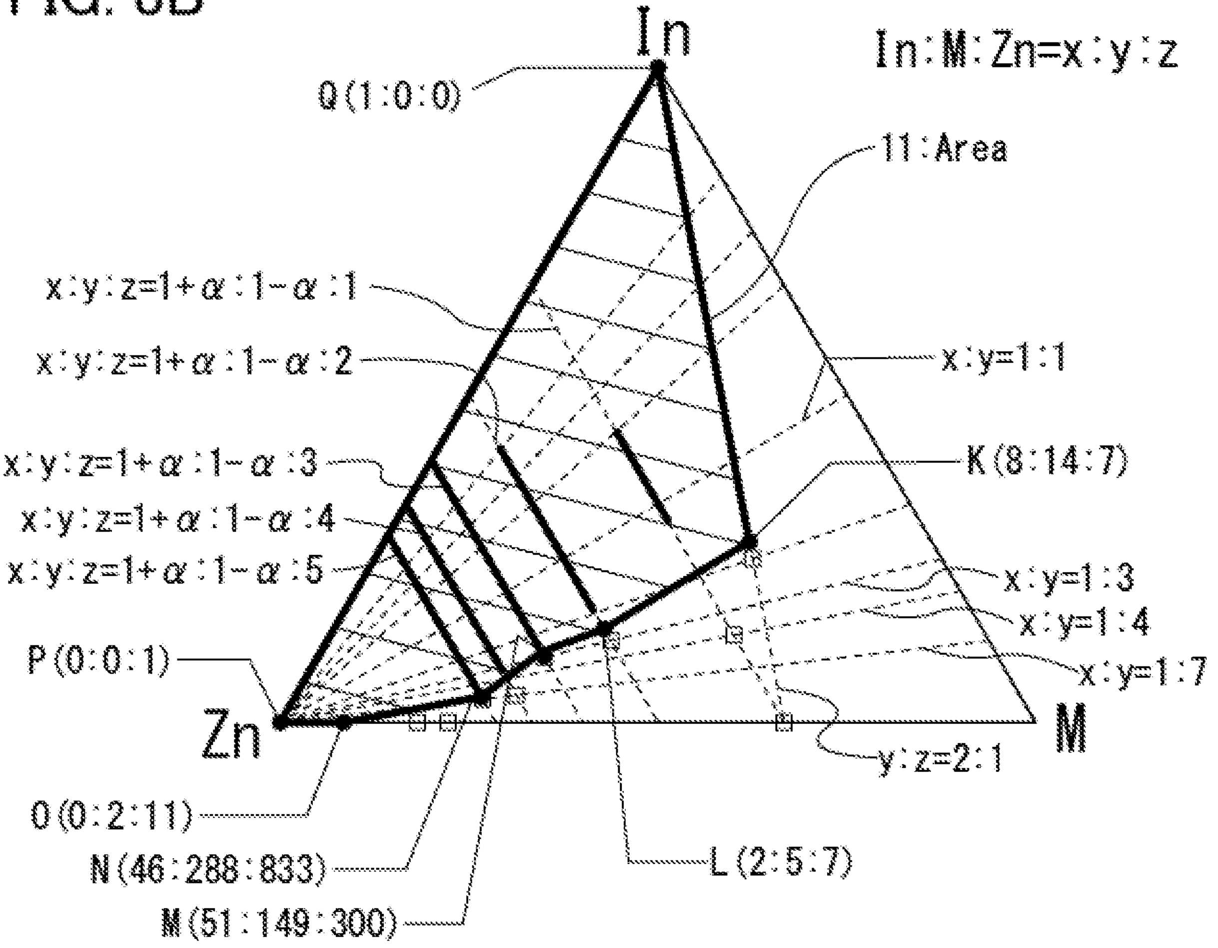

In
In:M:Zn=x:y:z
Q(1:0:0)
11:Area
x:y:z=1+α:1-α:1
x:y:z=1+α:1-α:2
x:y=1:1
x:y:z=1+α:1-α:3
K(8:14:7)
x:y:z=1+α:1-α:4
x:y:z=1+α:1-α:5
x:y=1:3
x:y=1:4
P(0:0:1)
x:y=1:7
Zn
M
y:z=2:1
O(0:2:11)
N(46:288:833)
L(2:5:7)
M(51:149:300)

FIG. 9A

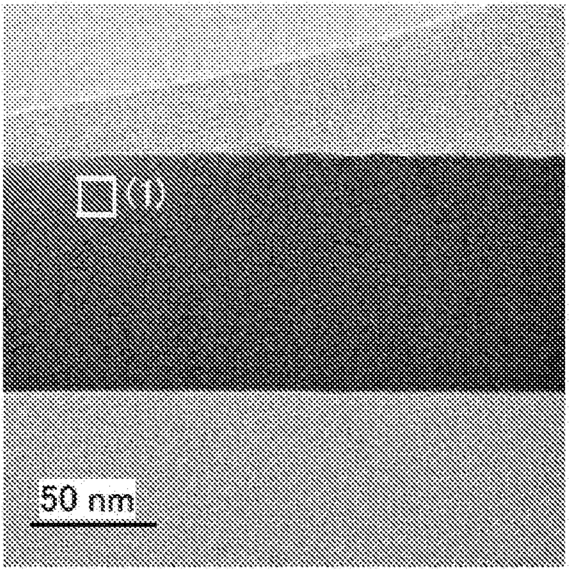


FIG. 9B

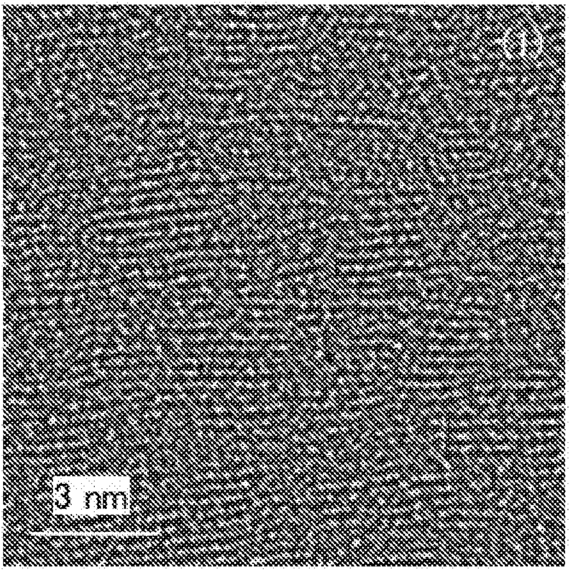


FIG. 9C

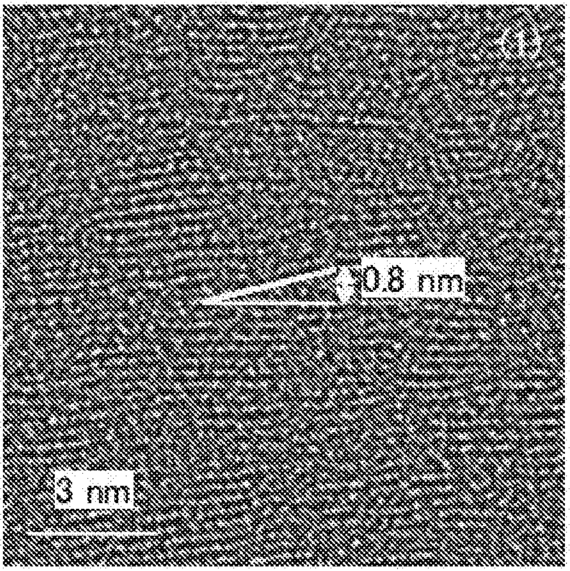


FIG. 9D

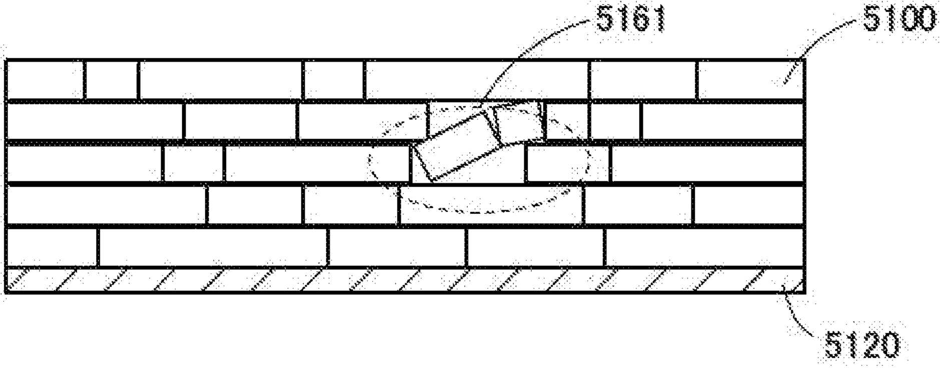


FIG. 10A

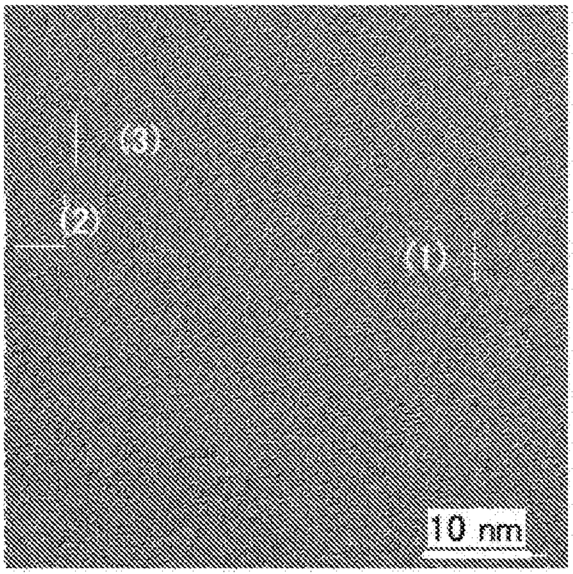


FIG. 10B

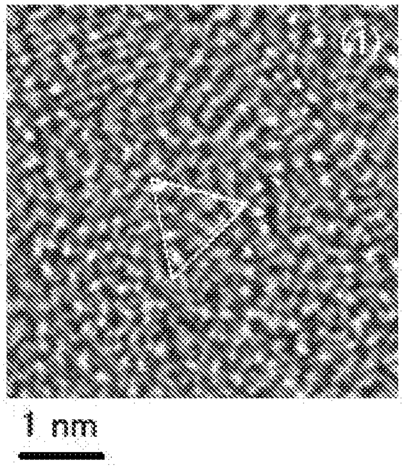


FIG. 10C

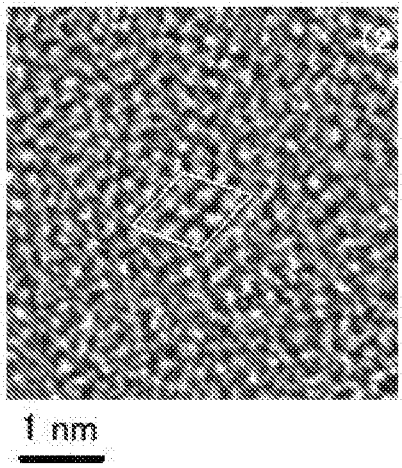


FIG. 10D

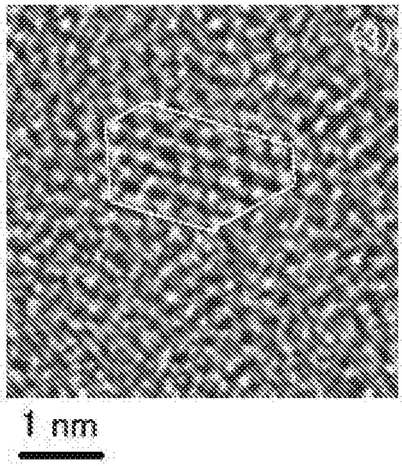


FIG. 11A

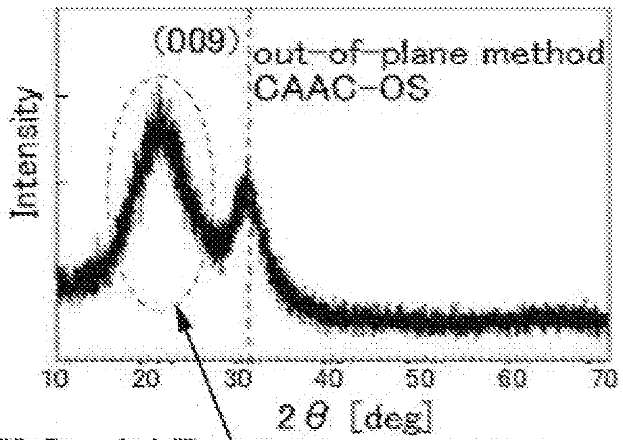


FIG. 11B

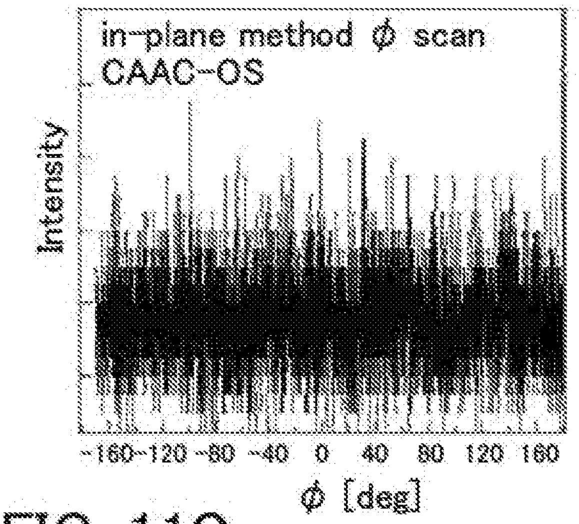


FIG. 11C

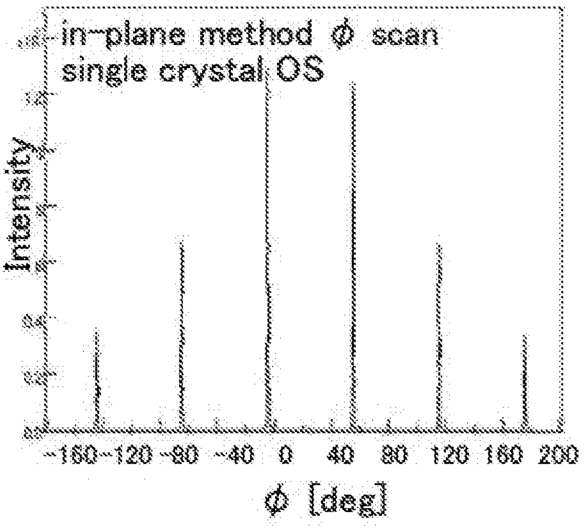


FIG. 12A

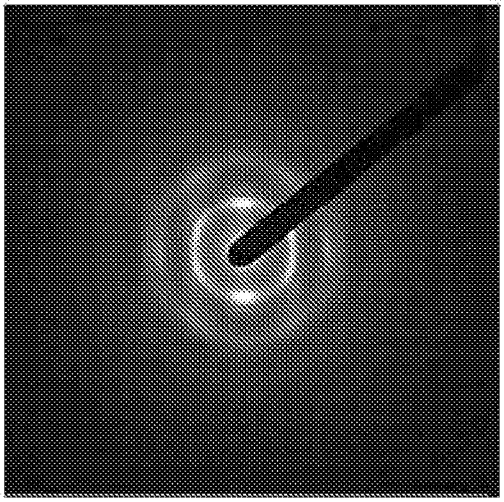


FIG. 12B

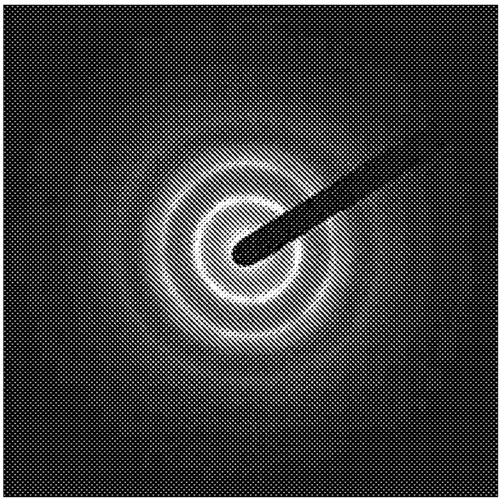


FIG. 13

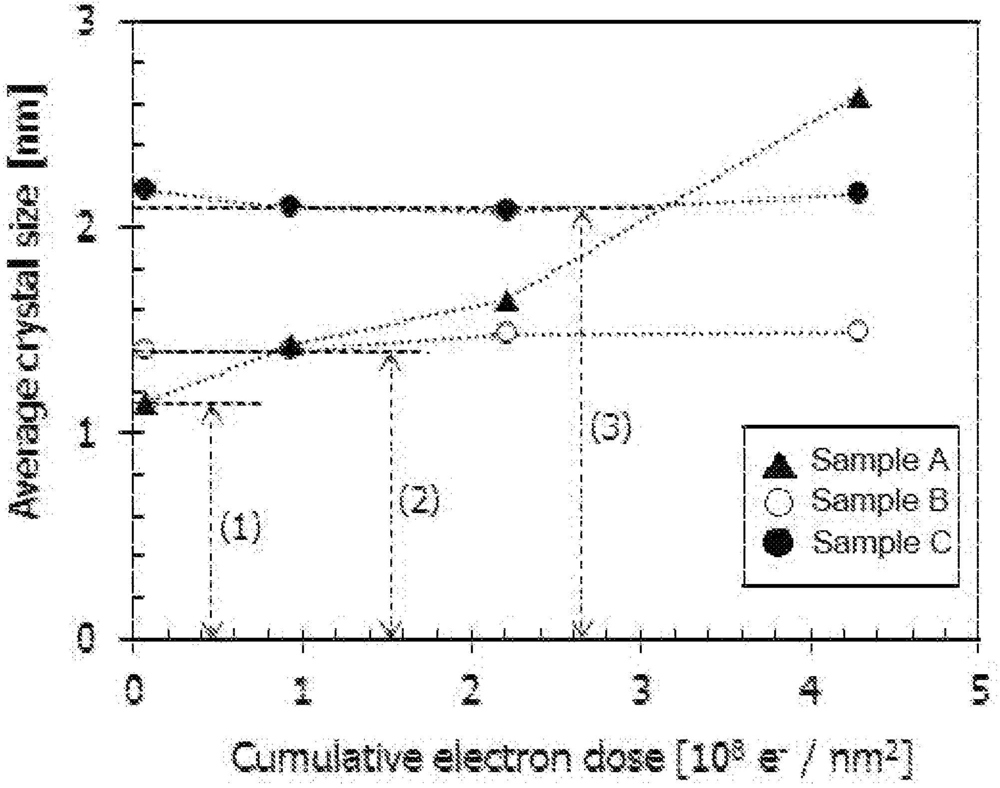

Average crystal size [nm]
3
2
1
0
0
1
2
3
4
5
Cumulative electron dose [10⁸ e⁻ / nm²]
(1)
(2)
(3)
Sample A
Sample B
Sample C

FIG. 14A

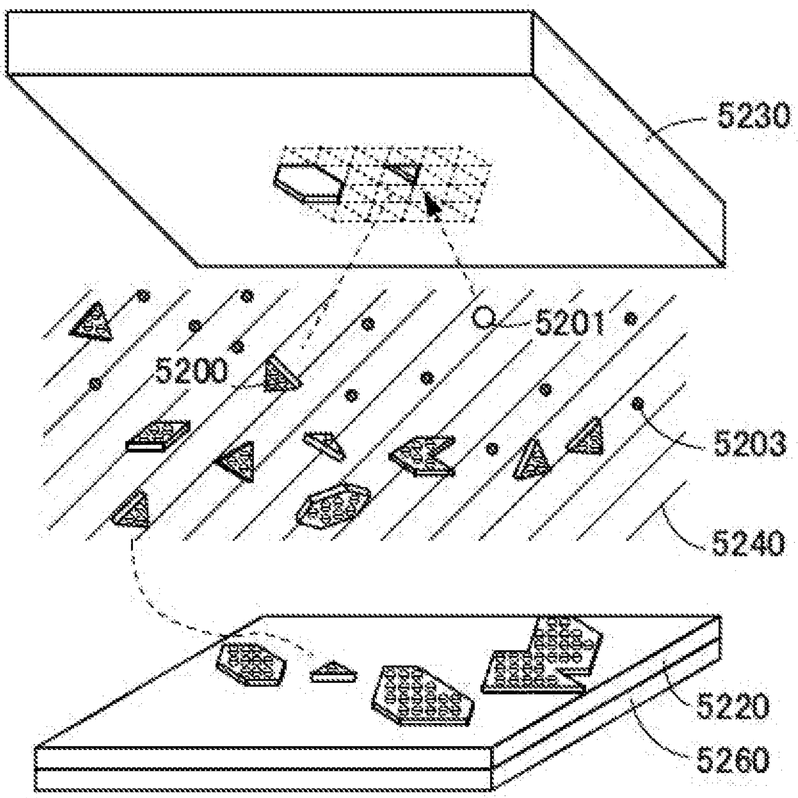


FIG. 14B

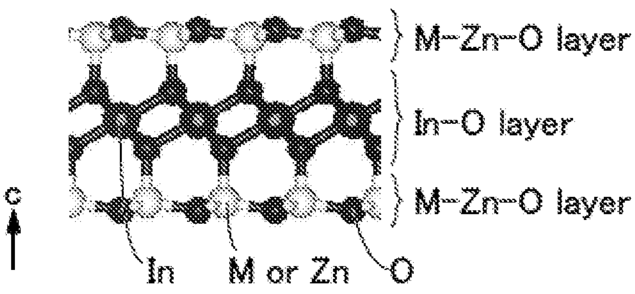


FIG. 14C

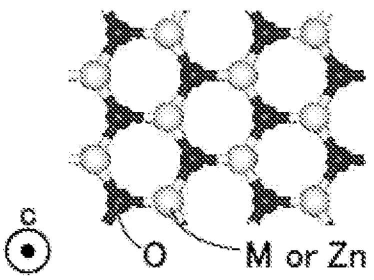


FIG. 14D

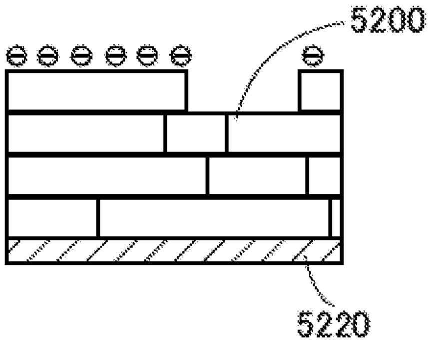


FIG. 15

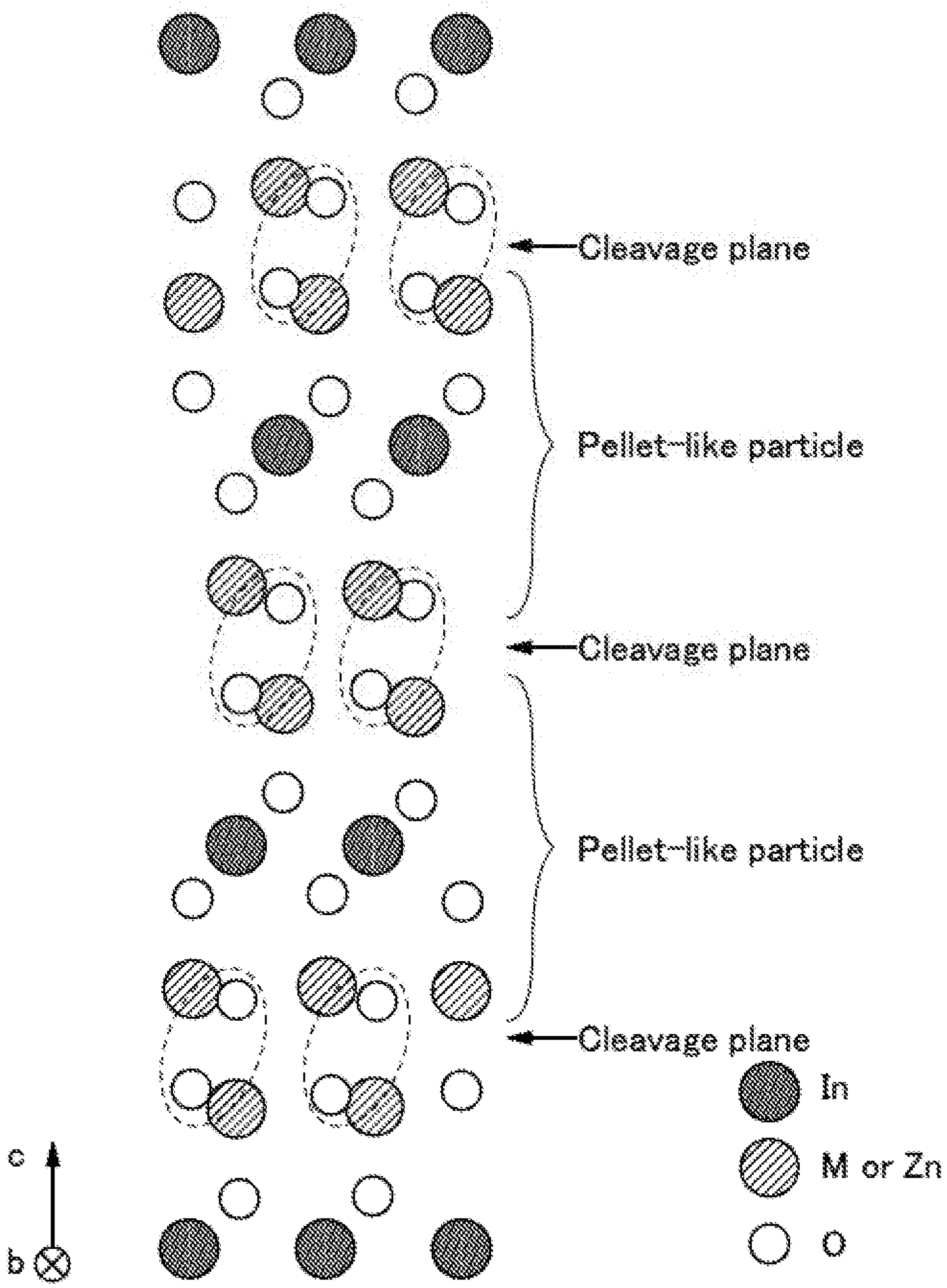

Cleavage plane
Pellet-like particle
Cleavage plane
Pellet-like particle
Cleavage plane
In
M or Zn
O
c
b

FIG. 16A

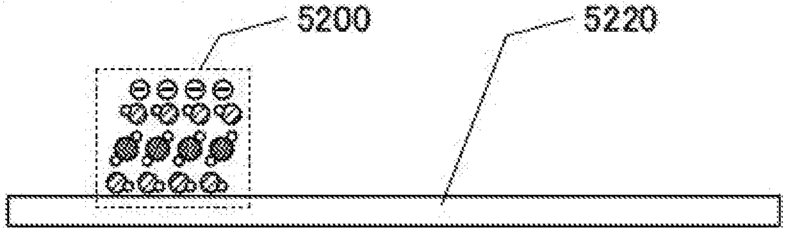


FIG. 16B

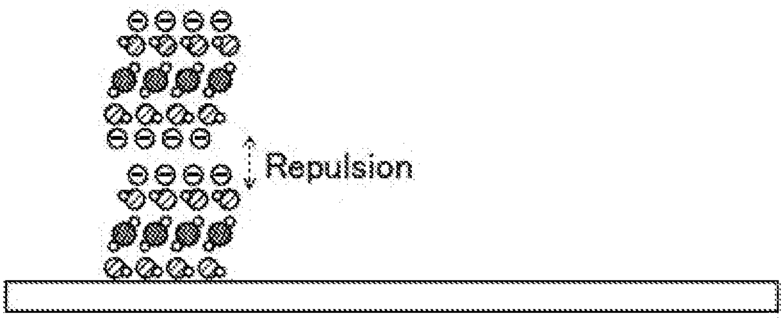


FIG. 16C

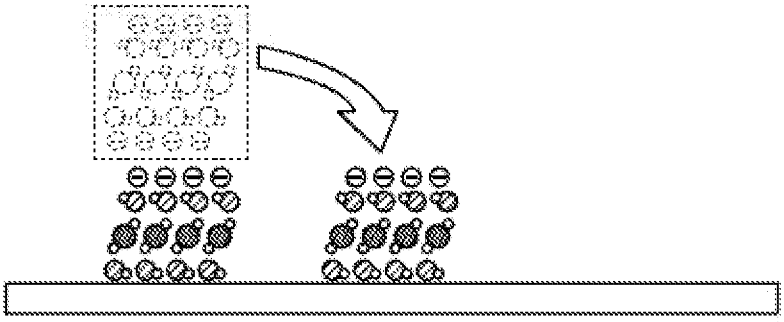


FIG. 16D

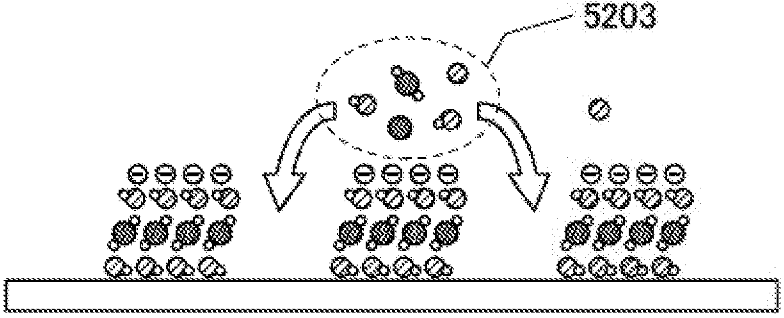


FIG. 16E

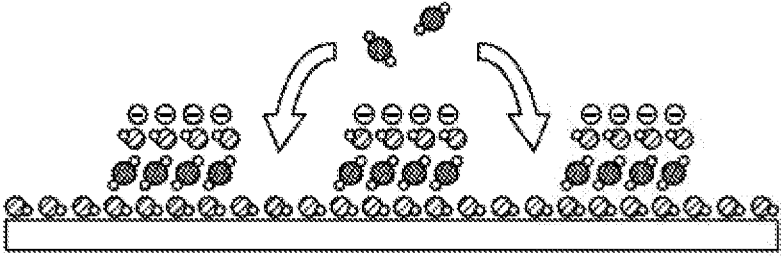


FIG. 17A

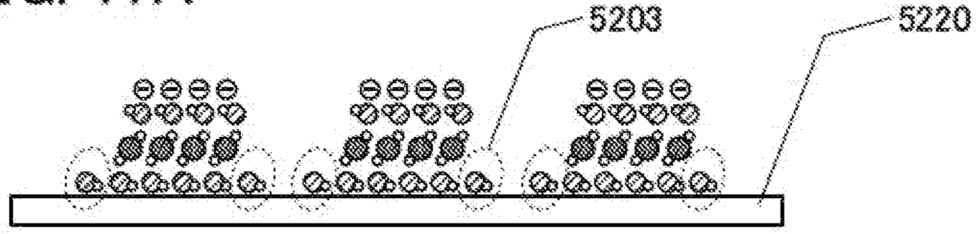


FIG. 17B

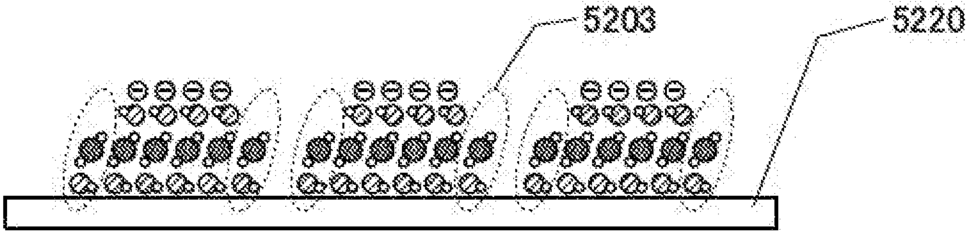


FIG. 17C

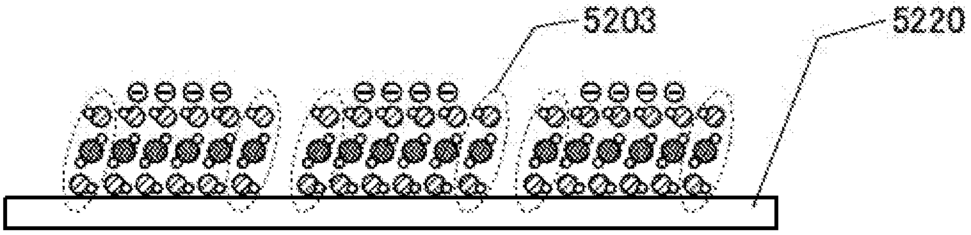


FIG. 18

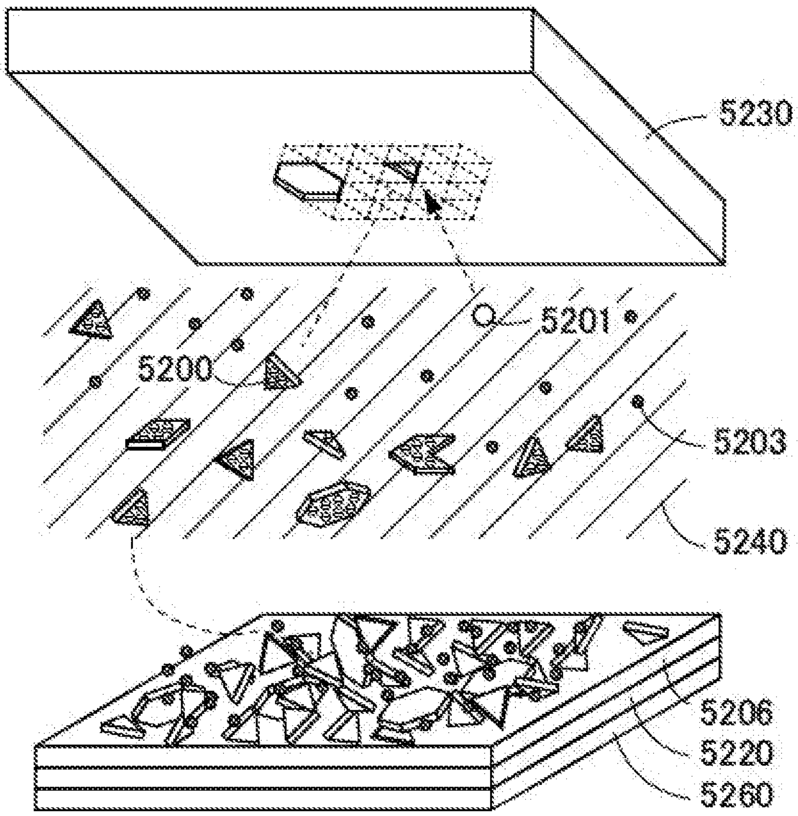


FIG. 19A

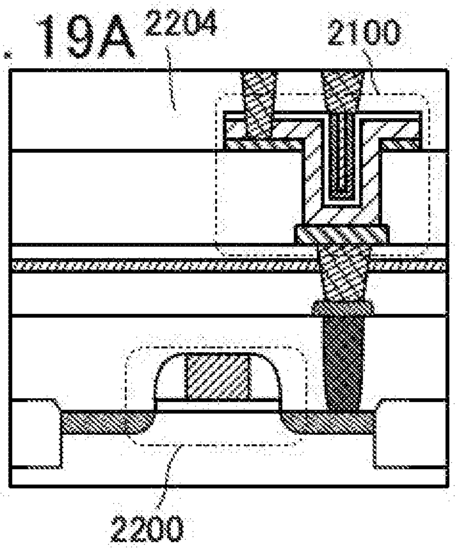


FIG. 19B

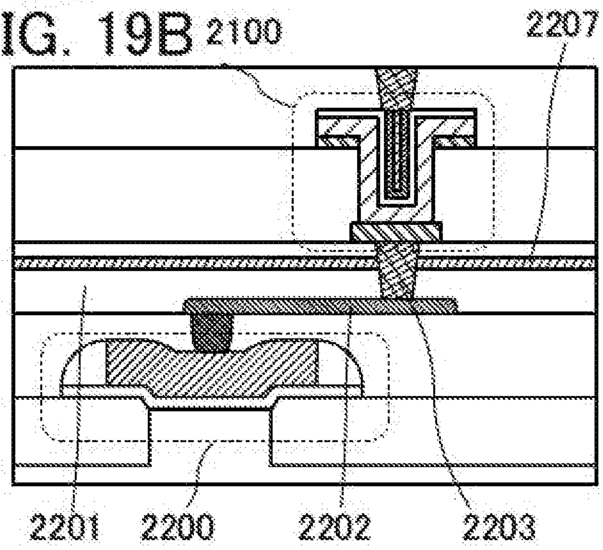


FIG. 19C

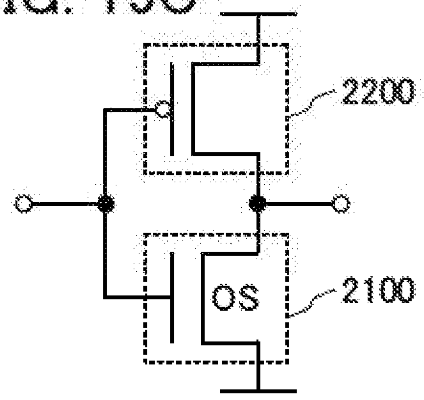


FIG. 19D

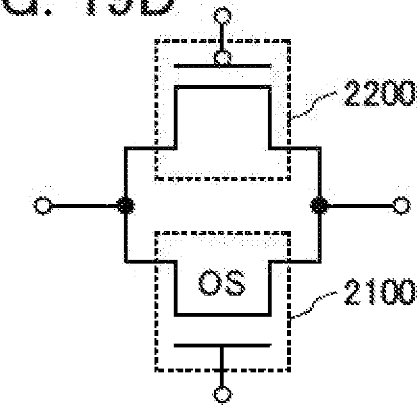


FIG. 19E

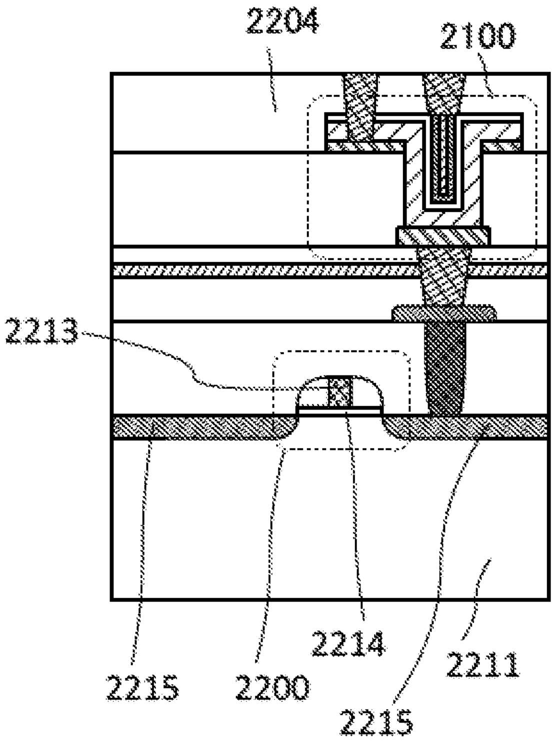


FIG. 19F

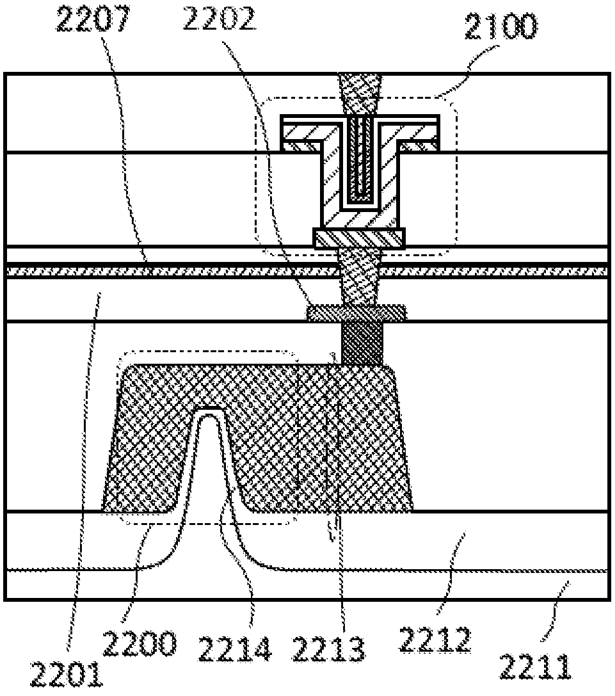


FIG. 20

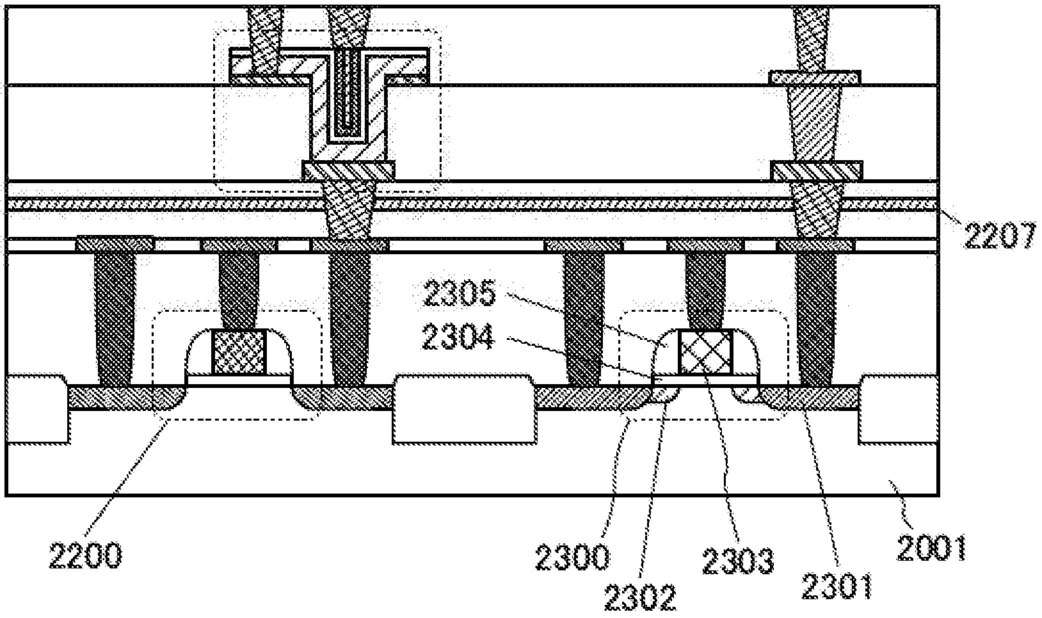


FIG. 21A

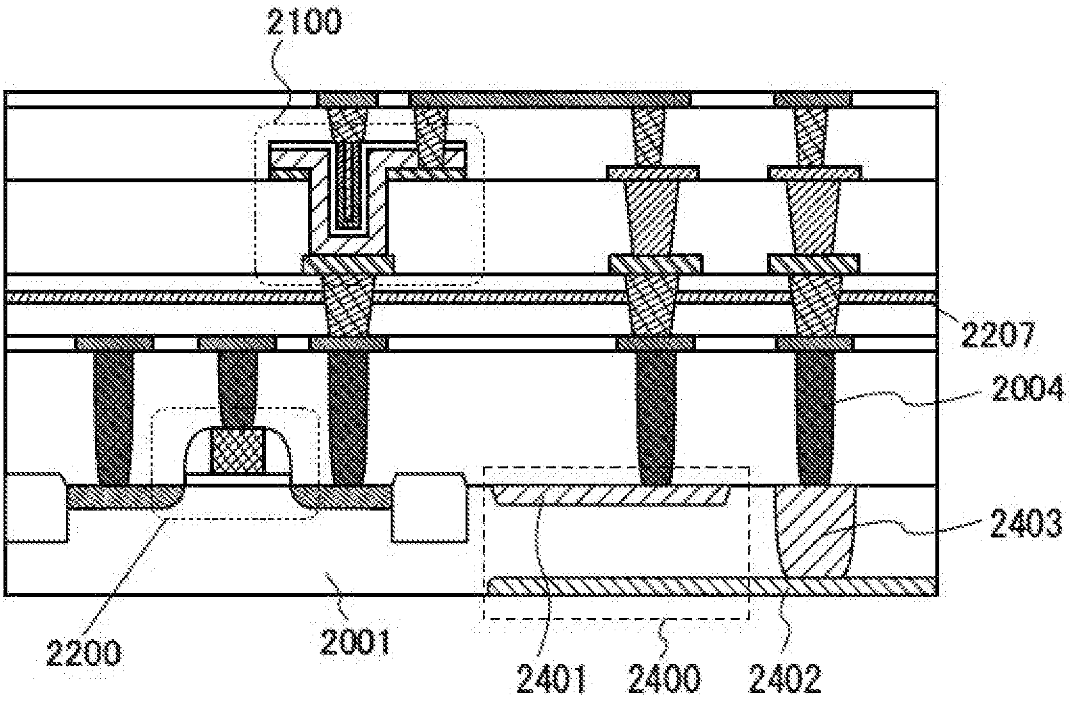


FIG. 21B

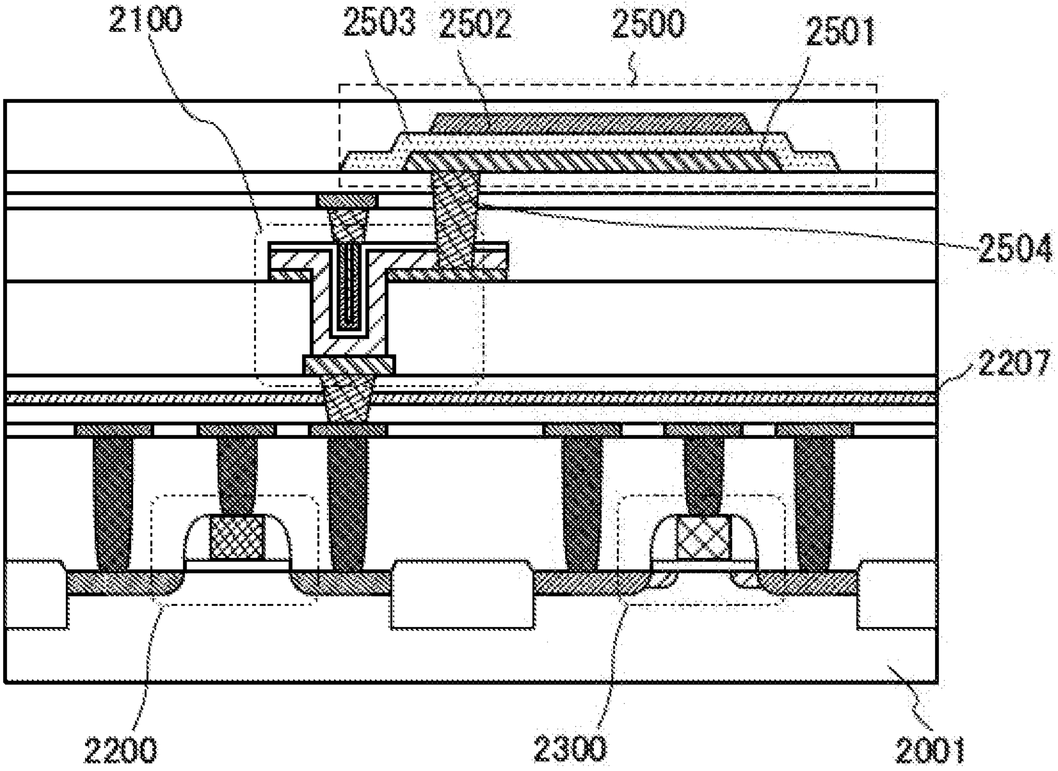


FIG. 22A

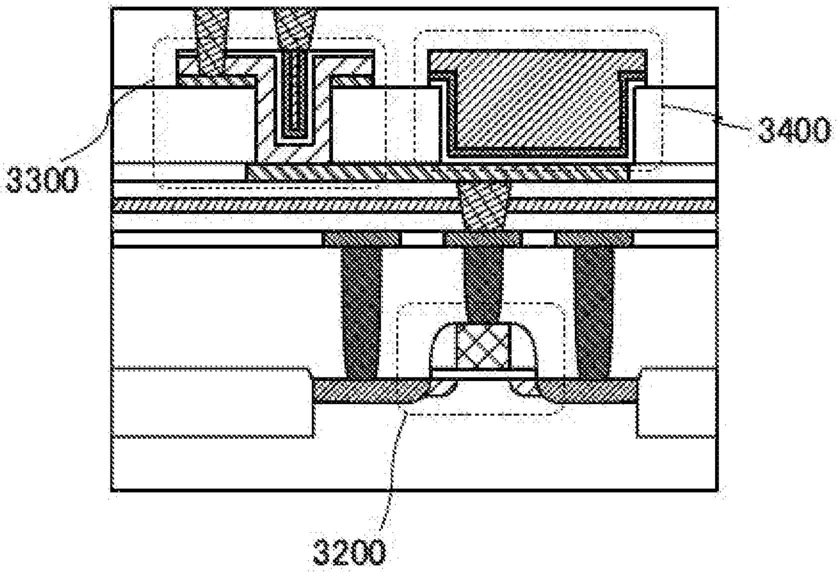


FIG. 22B

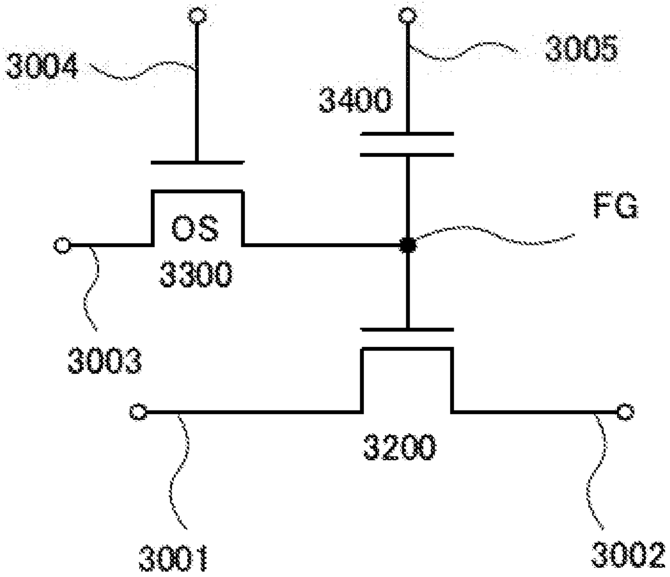


FIG. 22C

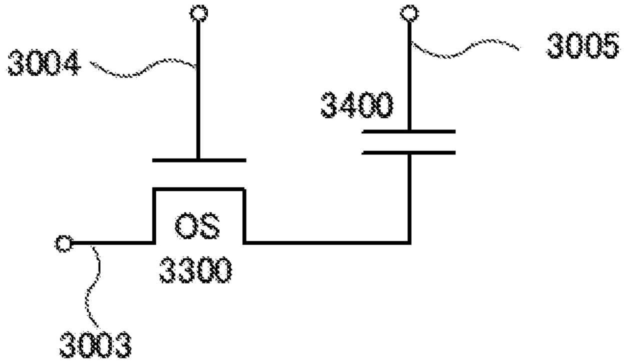


FIG. 23

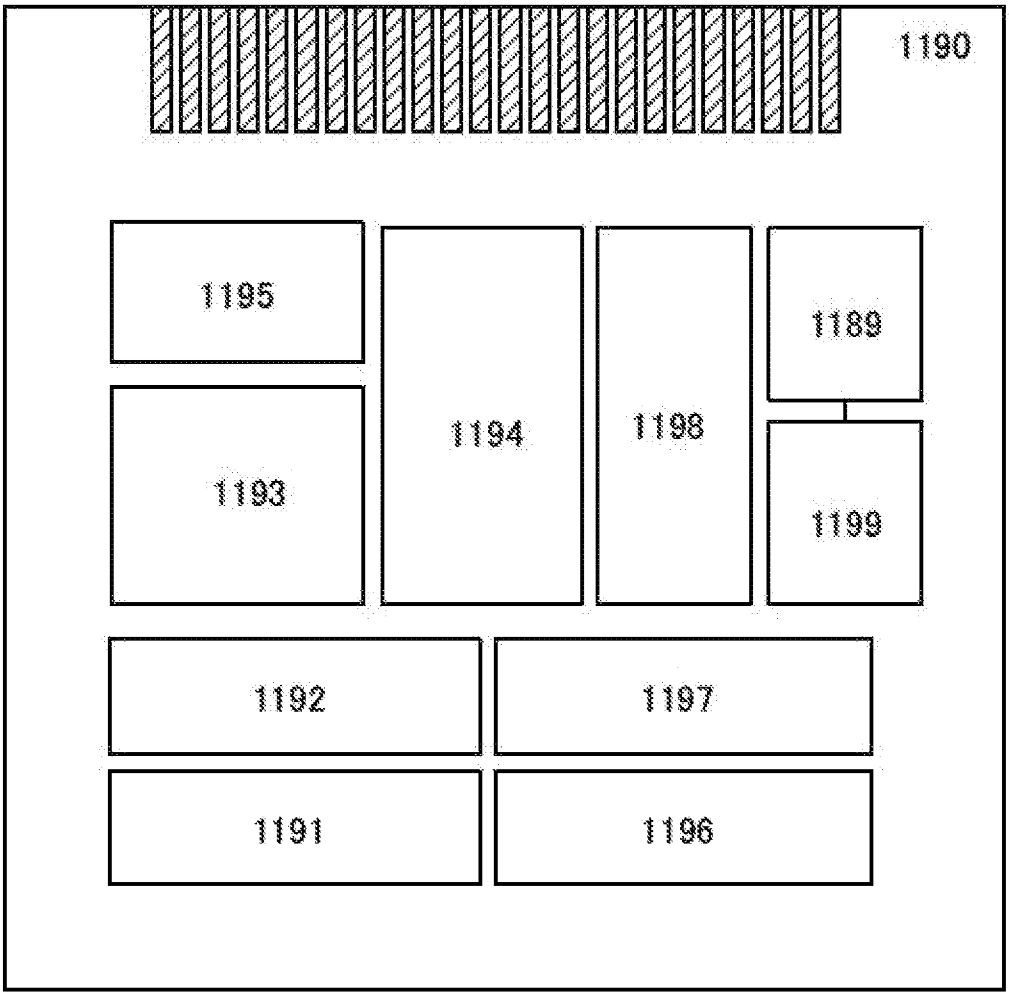


FIG. 24

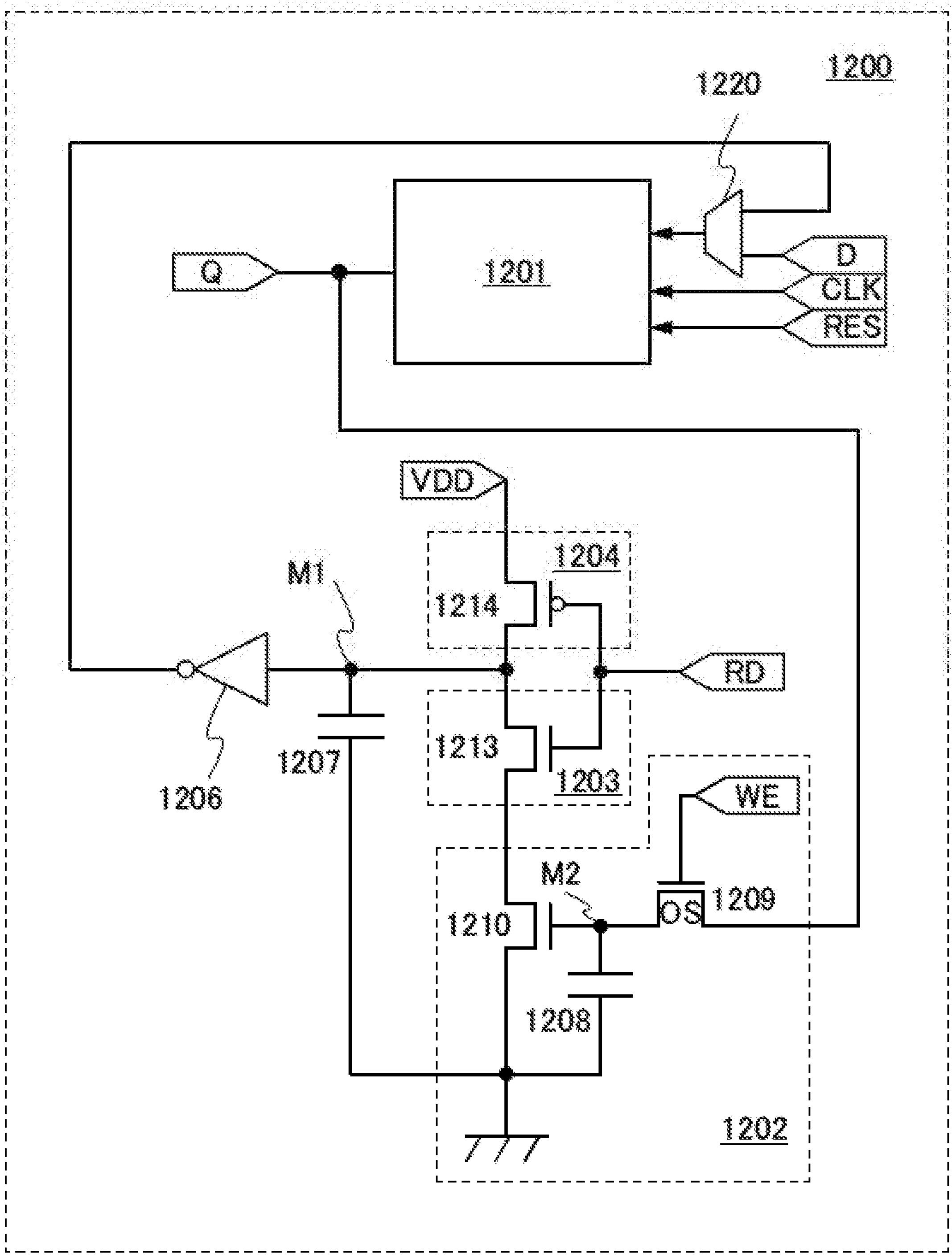

1220
1200
Q
1201
D
CLK
RES
VDD
1204
M1
1214
RD
1213
1207
1203
1206
WE
M2
1209
OS
1210
1208
1202

FIG. 25A

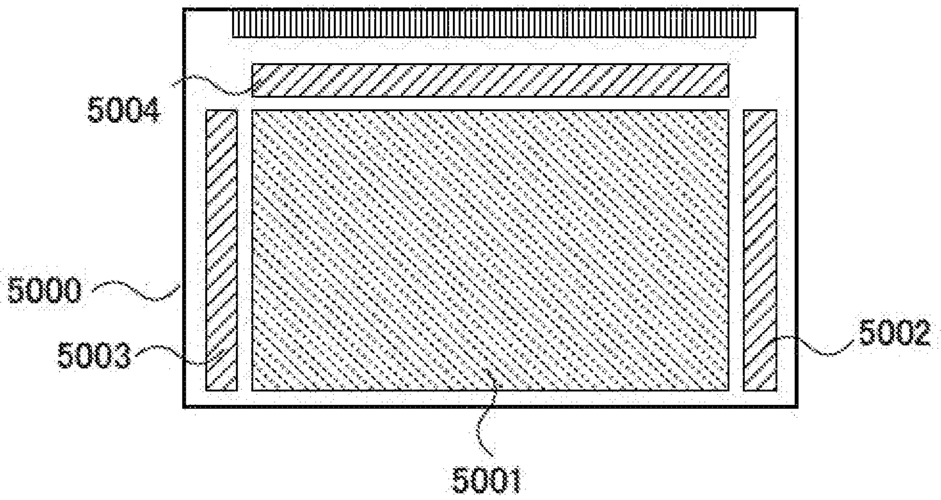


FIG. 25B

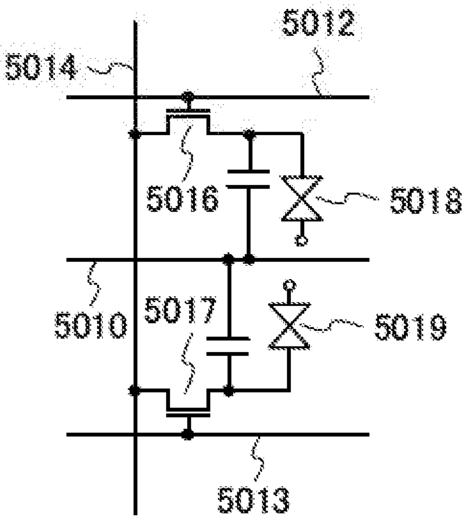


FIG. 25C

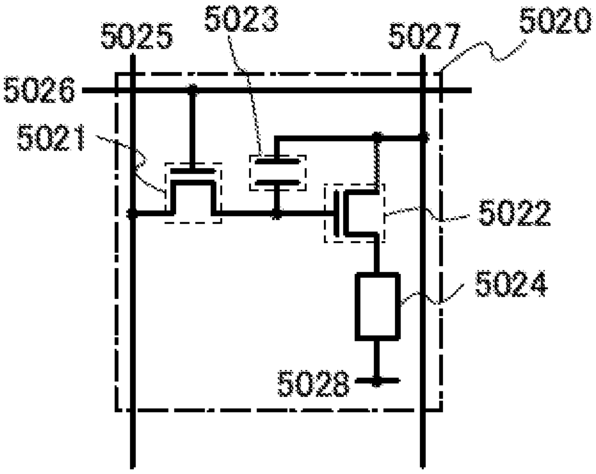


FIG. 26A

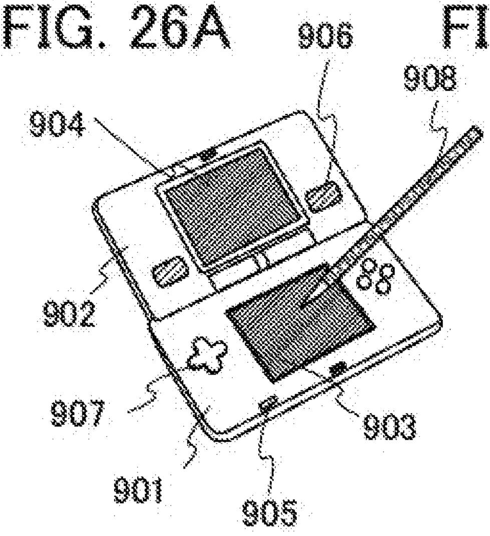


FIG. 26B

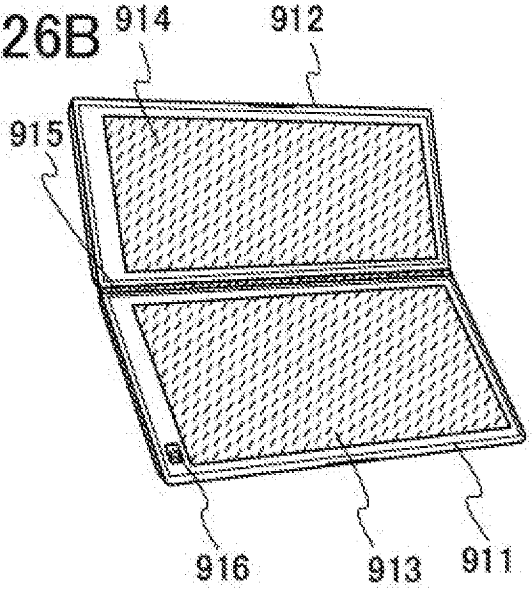


FIG. 26C

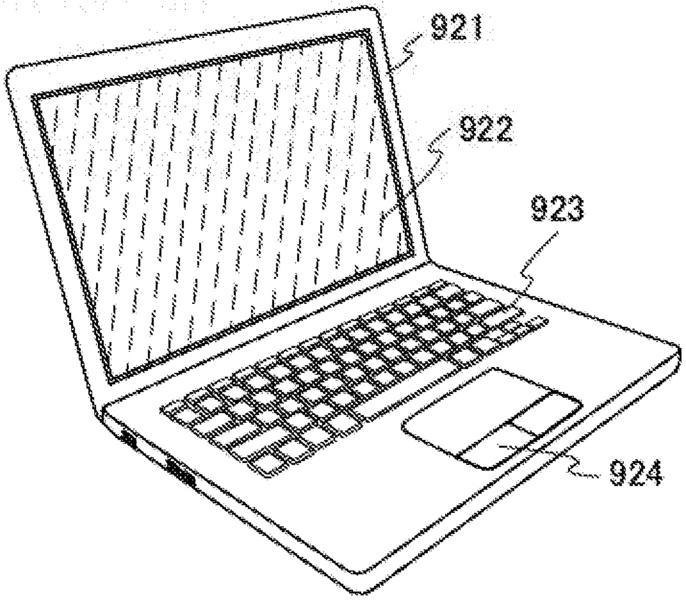


FIG. 26D

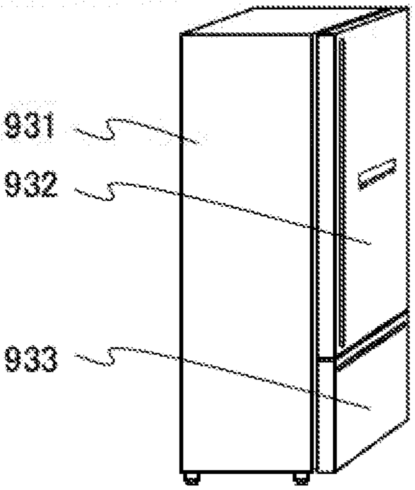


FIG. 26E

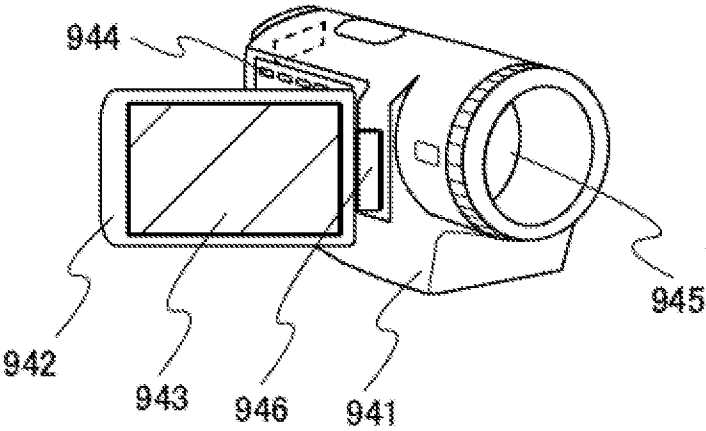
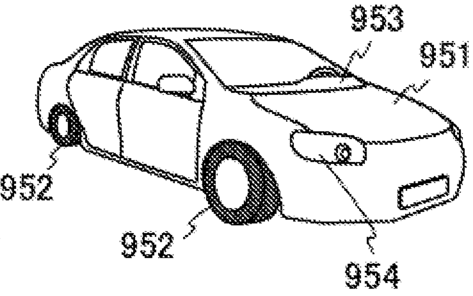


FIG. 26F



INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2016/050533

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, H01L21/336, H01L21/8234, H01L21/8242, H01L21/8247, H01L27/088, H01L27/108, H01L27/115, H01L29/788, H01L29/792

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2016
Registered utility model specifications of Japan 1996-2016
Published registered utility model applications of Japan 1994-2016

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011/0241004 A1 (Tatsuya ISHII) 2011.10.06, pars. [0048]-[0061], figs. 4-7 & JP 2011-221072 A	1-6
A	JP 2012-174836 A (FUJITSU LIMITED) 2012.09.10, pars. [0013]-[0057], figs. 1-9 (No Family)	1-6
A	WO 2011/062041 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2011.05.26, pars. [0022]-[0043], fig. 1 & JP 2011-129898 A & US 2011/0121284 A1 & TW 201138106 A1 & KR 10-2012-0092667 A	1-6

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search 11.05.2016	Date of mailing of the international search report 24.05.2016
Name and mailing address of the ISA/JP **Japan Patent Office** 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Authorized officer 5F 4054 Yasuhiro TAKEGUCHI Telephone No. +81-3-3581-1101 Ext. 3516

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2007/086237 A1 (RICOH COMPANY, LTD.) 2007.08.02, pp. 13-20, fig. 1 & JP 2008-60522 A & US 2010/0164918 A1 & KR 10-2008-0087014 A & CN 101361191 A	1-6
A	WO 2004/055920 A2 (PLASTIC LOGIC LIMITED) 2004.07.01, pp. 12-15, fig. 6 & JP 2006-510210 A & US 2006/0148167 A1 & CN 1745487 A & KR 10-2005-0089826 A	1-6

INTERNATIONAL SEARCH REPORT

International application No.
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CLASSIFICATION OF SUBJECT MATTER
H01L29/786(2006.01)i, H01L21/336(2006.01)i, H01L21/8234(2006.01)i, H01L21/8242(2006.01)i, H01L21/8247(2006.01)i, H01L27/088(2006.01)i, H01L27/108(2006.01)i, H01L27/115(2006.01)i, H01L29/788(2006.01)i, H01L29/792(2006.01)i