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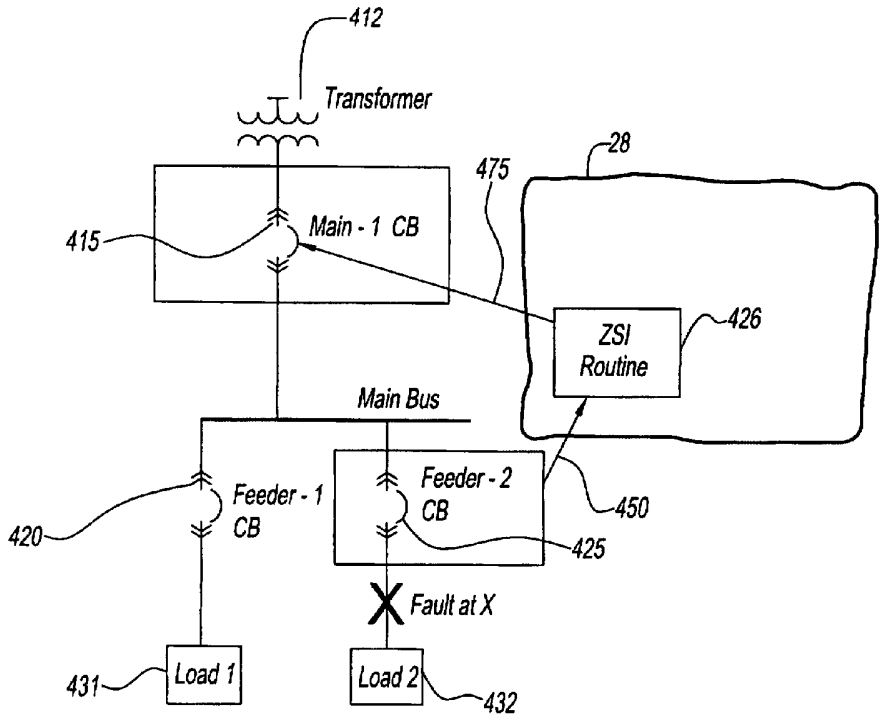

(57) Abstract: A circuit protection system (28) is provided that provides a dynamic delay time to an upstream circuit breaker (415) if a fault is detected in a circuit where the dynamic delay time can be based upon the location of the fault, such as the nearest downstream circuit breaker (420).

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CIRCUIT PROTECTION SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] This invention relates generally to power distribution systems and more particularly, to a method and apparatus for a circuit protection system providing dynamic delay times for circuit breakers throughout the system.

2. Description of the Prior Art

[0002] In power distribution systems, power is distributed to various loads and is typically divided into branch circuits, which supply power to specified loads. The branch circuits also can be connected to various other power distribution equipment, such as, transformers that step down the supply voltage for use by a specific piece of electrical equipment.

[0003] Due to the concern of an abnormal power condition in the system, i.e., a fault, it is known to provide circuit protective devices, e.g., circuit breakers to protect the various loads, as well as the power distribution equipment. The circuit breakers seek to prevent or minimize damage and typically function automatically. The circuit breakers also seek to minimize the extent and duration of electrical service interruption in the event of a fault.

[0004] It is further known to utilize upstream circuit breakers having pre-programmed time delays so that the downstream circuit breakers are provided with an opportunity to clear the fault before the upstream circuit breaker opens or trips. In a known zone selective interlock system, a downstream circuit breaker can be in direct communication with an upstream circuit breaker through wiring such that the downstream circuit breaker sends a signal to the upstream circuit breaker placing the

upstream circuit breaker in a restrained mode. In the restrained mode, the circuit breaker temporarily restrains from opening or tripping until after a pre-determined time delay has timed out. The circuit breakers each have pre-programmed time delay settings incorporated therein. This type of system provides for time delays based upon pre-set, invariable time periods associated with the upstream circuit breaker. Thus, the upstream circuit breaker will delay tripping by a pre-set period of time regardless of the location of the fault in the power distribution system.

[0005] The circuit breakers, can be arranged in a hierarchy or tree configuration having a plurality of layers or levels with the upstream circuit breakers closer to the power source and the downstream circuit breakers closer to the loads. In order to minimize service interruption, the circuit breaker nearest the fault will first attempt to interrupt the fault current. If this first circuit breaker does not timely clear the fault, then the next upstream circuit breaker will attempt to do so. However, this can result in the problem of a circuit breaker multiple levels upstream from a fault being tripped when the fault is detected, which causes power loss to the multiple levels of loads downstream that should otherwise be unaffected.

[0006] Such a system does not delay the upstream circuit breakers based upon an optimal time period to provide the downstream circuit breaker with the opportunity to clear the fault. Where a circuit has downstream circuit branches and circuit breakers having differing temporal properties, such as, for example, clearing time or pre-set delay time of the circuit breakers, such a system fails to account for these differences. This increases the risk of damage to the system where an upstream circuit breaker has a pre-set time delay that is too long based on the location of the fault. This also decreases the efficiency of the system where an upstream circuit breaker has a pre-set time delay that is too short based on the location of the fault and opens before the downstream circuit breaker has a full opportunity to clear the fault. This system also suffers from the drawback of the need to hardwire the upstream circuit breakers with each of the downstream circuit breakers. In a multi-tiered and multi-source system, this can require a complex and costly wiring scheme.

[0007] Accordingly, there is a need for circuit protection systems incorporated into power distribution systems that decrease the risk of damage and increase efficiency of the power distribution system. There is a further need for protection systems that can vary the zones of protection and the time delays of protection as the power distribution system changes and provide optimized protection without sacrificing selectivity.

SUMMARY OF THE INVENTION

[0008] In one aspect, a method of protecting a circuit having a first circuit breaker and a second circuit breaker downstream of the first circuit breaker is provided. The method comprises detecting a fault in the circuit with the fault being downstream of the second circuit breaker, determining a dynamic delay time for opening the first circuit breaker, and opening the first circuit breaker after the dynamic delay time has elapsed.

[0009] In another aspect, a method of protecting a circuit having a first circuit breaker arranged upstream of a plurality of second circuit breakers is provided. The method comprises detecting a fault in the circuit, determining a location of the fault, determining a dynamic delay time for opening the first circuit breaker based at least in part upon the location of the fault, and delaying opening the first circuit breaker until after the dynamic delay time has elapsed.

[0010] In yet another aspect, a protection system coupled to a circuit having a first circuit breaker arranged upstream of a plurality of second circuit breakers is provided. The system comprises a network and at least one control processing unit operatively controlling the first circuit breaker and the plurality of second circuit breakers. The network is communicatively coupled to the circuit, the first circuit breaker, the plurality of second circuit breakers and the control processing unit. The control processing unit determines a dynamic delay time for opening the first circuit breaker if a fault is detected in the circuit. The control processing unit delays opening the first circuit breaker until after the dynamic delay time has elapsed.

[0011] In a further aspect, a power distribution system is provided which comprises a circuit having a plurality of circuit breakers, at least one power source and at least one load. The plurality of circuit breakers are arranged with at least one first circuit breaker upstream of a plurality of second circuit breakers. The system further comprises a network and at least one control processing unit operatively controlling the plurality of circuit breakers. The network is communicatively coupled to the control processing unit and the circuit. The control processing unit determines a dynamic delay time for opening the first circuit breaker if a fault is detected in the circuit. The control processing unit delays opening the first circuit breaker until after the dynamic delay time has elapsed.

[0012] The above-described and other features and advantages of the present disclosure will be appreciated and understood by those skilled in the art from the following detailed description, drawings, and appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figure 1 is a schematic illustration of a power distribution system;

[0014] Figure 2 is a schematic illustration of a module of the power distribution system of FIG. 1;

[0015] Figure 3 is a response time for the protection system of FIG. 1;

[0016] Figure 4 is a schematic illustration of a multiple source power distribution system;

[0017] Figure 5 is a schematic illustration of a portion of the system of FIG. 4 with a fault occurring downstream of Feeder Circuit Breaker 1;

[0018] Figure 6 is a schematic illustration of the portion of the system of FIG. 4 with a fault occurring downstream of Feeder Circuit Breaker 2;

[0019] Figure 7 is a schematic illustration of the portion of the system of FIG. 4 with a fault occurring downstream of Main Circuit Breaker 1;

[0020] Figure 8 is a schematic illustration of a portion of the system of FIG. 4 with a Tie Circuit Breaker in an open or tripped state; and

[0021] Figure 9 is a schematic illustration of the portion of the system of FIG. 8 with a Main Circuit Breaker 2 in an open or tripped state.

DETAILED DESCRIPTION OF THE INVENTION

[0022] Referring now to the drawings and in particular to FIG. 1, an exemplary embodiment of a power distribution system generally referred to by reference numeral 10 is illustrated. System 10 distributes power from at least one power bus 12 through a number or plurality of circuit breakers 14 to branch circuits 16.

[0023] Power bus 12 is illustrated by way of example as a three-phase power system having a first phase 18, a second phase 20, and a third phase 22. Power bus 12 can also include a neutral phase (not shown). System 10 is illustrated for purposes of clarity distributing power from power bus 12 to four circuits 16 by four breakers 14. Of course, it is contemplated by the present disclosure for power bus 12 to have any desired number of phases and/or for system 10 to have any desired number of circuit breakers 14.

[0024] Each circuit breaker 14 has a set of separable contacts 24 (illustrated schematically). Contacts 24 selectively place power bus 12 in communication with at least one load (also illustrated schematically) on circuit 16. The load can include

devices, such as, but not limited to, motors, welding machinery, computers, heaters, lighting, and/or other electrical equipment.

[0025] Power distribution system 10 is illustrated in FIG. 1 with an exemplary embodiment of a centrally controlled and fully integrated protection, monitoring, and control system 26 (hereinafter "system"). System 26 is configured to control and monitor power distribution system 10 from a central control processing unit 28 (hereinafter "CCPU"). CCPU 28 communicates with a number or plurality of data sample and transmission modules 30 (hereinafter "module") over a data network 32. Network 32 communicates all of the information from all of the modules 30 substantially simultaneously to CCPU 28.

[0026] Thus, system 26 can include protection and control schemes that consider the value of electrical signals, such as current magnitude and phase, at one or all circuit breakers 14. Further, system 26 integrates the protection, control, and monitoring functions of the individual breakers 14 of power distribution system 10 in a single, centralized control processor (e.g., CCPU 28). System 26 provides CCPU 28 with all of a synchronized set of information available through digital communication with modules 30 and circuit breakers 14 on network 32 and provides the CCPU with the ability to operate these devices based on this complete set of data.

[0027] Specifically, CCPU 28 performs all primary power distribution functions for power distribution system 10. Namely, CCPU 28 performs all instantaneous overcurrent protection (IOC), short time overcurrent, longtime overcurrent, relay protection, and logic control as well as digital signal processing functions of system 26. Thus, system 26 enables settings to be changed and data to be logged in single, central location, i.e., CCPU 28. CCPU 28 is described herein by way of example as a central processing unit. Of course, it is contemplated by the present disclosure for CCPU 28 to include any programmable circuit, such as, but not limited to, computers, processors, microcontrollers, microcomputers, programmable logic controllers, application specific integrated circuits, and other programmable circuits.

[0028] As shown in FIG. 1, each module 30 is in communication with one of the circuit breakers 14. Each module 30 is also in communication with at least one sensor 34 sensing a condition or electrical parameter of the power in each phase (e.g., first phase 18, second phase 20, third phase 22, and neutral) of bus 12 and/or circuit 16. Sensors 34 can include current transformers (CTs), potential transformers (PTs), and any combination thereof. Sensors 34 monitor a condition or electrical parameter of the incoming power in circuits 16 and provide a first or parameter signal 36 representative of the condition of the power to module 30. For example, sensors 34 can be current transformers that generate a secondary current proportional to the current in circuit 16 so that first signals 36 are the secondary current.

[0029] Module 30 sends and receives one or more second signals 38 to and/or from circuit breaker 14. Second signals 38 can be representative of one or more conditions of breaker 14, such as, but not limited to, a position or state of separable contacts 24, a spring charge switch status, a lockout state or condition, and others. In addition, module 30 is configured to operate or actuate circuit breaker 14 by sending one or more third signals 40 to the breaker to open/close separable contacts 24 as desired, such as open/close commands or signals. In a first embodiment, circuit breakers 14 cannot open separable contacts 24 unless instructed to do so by system 26.

[0030] System 26 utilizes data network 32 for data acquisition from modules 30 and data communication to the modules. Accordingly, network 32 is configured to provide a desired level of communication capacity and traffic management between CCPU 28 and modules 30. In an exemplary embodiment, network 32 can be configured to not enable communication between modules 30 (i.e., no module-to-module communication).

[0031] In addition, system 26 can be configured to provide a consistent fault response time. As used herein, the fault response time of system 26 is defined as the time between when a fault condition occurs and the time module 30 issues an trip

command to its associated breaker 14. In an exemplary embodiment, system 26 has a fault response time that is less than a single cycle of the 60 Hz (hertz) waveform. For example, system 26 can have a maximum fault response time of about three milliseconds.

[0032] The configuration and operational protocols of network 32 are configured to provide the aforementioned communication capacity and response time. For example, network 32 can be an Ethernet network having a star topology as illustrated in FIG. 1. In this embodiment, network 32 is a full duplex network having the collision-detection multiple-access (CSMA/CD) protocols typically employed by Ethernet networks removed and/or disabled. Rather, network 32 is a switched Ethernet for managing collision domains.

[0033] In this configuration, network 32 provides a data transfer rate of at least about 100 Mbps (megabits per second). For example, the data transfer rate can be about 1 Gbps (gigabits per second). Additionally, communication between CCPU 28 and modules 30 across network 32 can be managed to optimize the use of network 32. For example, network 32 can be optimized by adjusting one or more of a message size, a message frequency, a message content, and/or a network speed.

[0034] Accordingly, network 32 provides for a response time that includes scheduled communications, a fixed message length, full-duplex operating mode, and a switch to prevent collisions so that all messages are moved to memory in CCPU 28 before the next set of messages is scheduled to arrive. Thus, system 26 can perform the desired control, monitoring, and protection functions in a central location and manner.

[0035] It should be recognized that data network 32 is described above by way of example only as an Ethernet network having a particular configuration, topography, and data transmission protocols. Of course, the present disclosure contemplates the use of any data transmission network that ensures the desired data capacity and consistent fault response time necessary to perform the desired range of

functionality. The exemplary embodiment achieves sub-cycle transmission times between CCPU 28 and modules 30 and full sample data to perform all power distribution functions for multiple modules with the accuracy and speed associated with traditional devices.

[0036] CCPU 28 can perform branch circuit protection, zone protection, and relay protection interdependently because all of the system information is in one central location, namely at the CCPU. In addition, CCPU 28 can perform one or more monitoring functions on the centrally located system information. Accordingly, system 26 provides a coherent and integrated protection, control, and monitoring methodology not considered by prior systems. For example, system 26 integrates and coordinates load management, feed management, system monitoring, and other system protection functions in a low cost and easy to install system.

[0037] An exemplary embodiment of module 30 is illustrated in FIG. 2. Module 30 has a microprocessor 42, a data bus 44, a network interface 46, a power supply 48, and one or more memory devices 50.

[0038] Power supply 48 is configured to receive power from a first source 52 and/or a second source 54. First source 52 can be one or more of an uninterruptible power supply (not shown), a plurality of batteries (not shown), a power bus (not shown), and other sources. In the illustrated embodiment, second source 54 is the secondary current available from sensors 34.

[0039] Power supply 48 is configured to provide power 56 to module 30 from first and second sources 52, 54. For example, power supply 48 can provide power 56 to microprocessor 42, data bus 42, network interface 44, and memory devices 50. Power supply 48 is also configured to provide a fourth signal 58 to microprocessor 42. Fourth signal 58 is indicative of what sources are supplying power to power supply 48. For example, fourth signal 58 can indicate whether power supply 48 is receiving power from first source 52, second source 54, or both of the first and second sources.

[0040] Network interface 46 and memory devices 50 communicate with microprocessor 42 over data bus 44. Network interface 46 can be connected to network 32 so that microprocessor 42 is in communication with CCPU 28.

[0041] Microprocessor 42 receives digital representations of first signals 36 and second signals 38. First signals 36 are continuous analog data collected by sensors 34, while second signals 38 are discrete analog data from breaker 14. Thus, the data sent from modules 30 to CCPU 28 is a digital representation of the actual voltages, currents, and device status. For example, first signals 36 can be analog signals indicative of the current and/or voltage in circuit 16.

[0042] Accordingly, system 26 provides the actual raw parametric or discrete electrical data (i.e., first signals 36) and device physical status (i.e., second signal 38) to CCPU 28 via network 32, rather than processed summary information sampled, created, and stored by devices such as trip units, meters, or relays. As a result, CCPU 28 has complete, raw system-wide data with which to make decisions and can therefore operate any or all breakers 14 on network 32 based on information derived from as many modules 30 as the control and protection algorithms resident in CCPU 28 require.

[0043] Module 30 has a signal conditioner 60 and an analog-digital converter 62. First signals 36 are conditioned by signal conditioner 60 and converted to digital signals 64 by A/D converter 62. Thus, module 30 collects first signals 36 and presents digital signals 64, representative of the raw data in the first signals, to microprocessor 42. For example, signal conditioner 60 can includes a filtering circuit (not shown) to improve a signal-to-noise ratio first signal 36, a gain circuit (not shown) to amplify the first signal, a level adjustment circuit (not shown) to shift the first signal to a pre-determined range, an impedance match circuit (not shown) to facilitate transfer of the first signal to A/D converter 62, and any combination thereof. Further, A/D converter 62 can be a sample-and-hold converter with external

conversion start signal 66 from microprocessor 42 or a clock circuit 68 controlled by microprocessor 42 to facilitate synchronization of digital signals 64.

[0044] It is desired for digital signals 64 from all of the modules 30 in system 26 to be collected at substantially the same time. Specifically, it is desired for digital signals 64 from all of the modules 30 in system 26 to be representative of substantially the same time instance of the power in power distribution system 10.

[0045] Modules 30 sample digital signals 64 based, at least in part, upon a synchronization signal or instruction 70 as illustrated in FIG. 1. Synchronization instruction 70 can be generated from a synchronizing clock 72 that is internal or external to CCPU 28. Synchronization instruction 70 is simultaneously communicated from CCPU 28 to modules 30 over network 32. Synchronizing clock 72 sends synchronization instructions 70 at regular intervals to CCPU 28, which forwards the instructions to all modules 30 on network 32.

[0046] Modules 30 use synchronization instruction 70 to modify a resident sampling protocol. For example, each module 30 can have a synchronization algorithm resident on microprocessor 42. The synchronization algorithm resident on microprocessor 42 can be a software phase-lock-loop algorithm. The software phase-lock-loop algorithm adjusts the sample period of module 30 based, in part, on synchronization instructions 70 from CCPU 28. Thus, CCPU 28 and modules 30 work together in system 26 to ensure that the sampling (i.e., digital signals 64) from all of the modules in the system are synchronized.

[0047] Accordingly, system 26 is configured to collect digital signals 64 from modules 30 based in part on synchronization instruction 70 so that the digital signals are representative of the same time instance, such as being within a predetermined time-window from one another. Thus, CCPU 28 can have a set of accurate data representative of the state of each monitored location (e.g., modules 30) within the power distribution system 10. The predetermined time-window can be less than about

ten microseconds. For example, the predetermined time-window can be about five microseconds.

[0048] The predetermined time-window of system 26 can be affected by the port-to port variability of network 32. In an exemplary embodiment, network 32 has a port-to-port variability of in a range of about 24 nanoseconds to about 720 nanoseconds. In an alternate exemplary embodiment, network 32 has a maximum port-to-port variability of about 2 microseconds.

[0049] It has been determined that control of all of modules 30 to this predetermined time-window by system 26 enables a desired level of accuracy in the metering and vector functions across the modules, system waveform capture with coordinated data, accurate event logs, and other features. In an exemplary embodiment, the desired level of accuracy is equal to the accuracy and speed of traditional devices. For example, the predetermined time-window of about ten microseconds provides an accuracy of about 99% in metering and vector functions.

[0050] Second signals 38 from each circuit breaker 14 to each module 30 are indicative of one or more conditions of the circuit breaker. Second signals 38 are provided to a discrete I/O circuit 74 of module 30. Circuit 74 is in communication with circuit breaker 14 and microprocessor 42. Circuit 74 is configured to ensure that second signals 38 from circuit breaker 14 are provided to microprocessor 42 at a desired voltage and without jitter. For example, circuit 74 can include de-bounce circuitry and a plurality of comparators.

[0051] Microprocessor 42 samples first and second signals 36, 38 as synchronized by CCPU 28. Then, converter 62 converts the first and second signals 36, 38 to digital signals 64, which is packaged into a first message 76 having a desired configuration by microprocessor 42. First message 76 can include an indicator that indicates which synchronization signal 70 the first message was in response to. Thus, the indicator of which synchronization signal 70 first message 76 is responding to is returned to CCPU 28 for sample time identification.

[0052] CCPU 28 receives first message 76 from each of the modules 30 over network 32 and executes one or more protection and/or monitoring algorithms on the data sent in all of the first messages. Based on first message 76 from one or more modules 30, CCPU 28 can control the operation of one or more circuit breakers 14. For example, when CCPU 28 detects a fault from one or more of first messages 76, the CCPU sends a second message 78 to one or more modules 30 via network 32, such as open or close commands or signals, or circuit breaker actuation or de-actuation commands or signals.

[0053] In response to second message 78, microprocessor 42 causes third signal 40 to operate or actuate (e.g., open contacts 24) circuit breaker 14. Circuit breaker 14 can include more than one operation or actuation mechanism. For example, circuit breaker 14 can have a shunt trip 80 and a magnetically held solenoid 82. Microprocessor 42 is configured to send a first output 84 to operate shunt trip 80 and/or a second output 86 to operate solenoid 82. First output 84 instructs a power control module 88 to provide third signal 40 (i.e., power) to shunt trip 80, which can separate contacts 24. Second output 86 instructs a gating circuit 90 to provide third signal 40 to solenoid 82 (i.e., flux shifter) to separate contacts 24. It should be noted that shunt trip 80 requires first source 52 to be present, while solenoid 82 can be operated when only second source 54 is present. In this manner, microprocessor 42 can operate circuit breaker 14 in response to second message 78 regardless of the state of first and second sources 52, 54. Additionally, a lockout device can be provided that is operably connected to circuit breaker 14.

[0054] In addition to operating circuit breaker 14, module 30 can communicate to one or more local input and/or output devices 94. For example, local output device 94 can be a module status indicator, such as a visual or audible indicator. In one embodiment, device 94 is a light emitting diode (LED) configured to communicate a status of module 30. In another embodiment, local input device 94 can be a status-modifying button for manually operating one or more portions of

module 30. In yet another embodiment, local input device 94 is a module interface for locally communicating with module 30.

[0055] Accordingly, modules 30 are adapted to sample first signals 36 from sensors 34 as synchronized by the CCPU. Modules 30 then package the digital representations (i.e., digital signals 64) of first and second signals 36, 38, as well as other information, as required into first message 76. First message 76 from all modules 30 are sent to CCPU 28 via network 32. CCPU 28 processes first message 76 and generates and stores instructions to control the operation of each circuit breaker 14 in second message 78. CCPU 28 sends second message 78 to all of the modules 30. In an exemplary embodiment, CCPU 28 sends second message 78 to all of the modules 30 in response to synchronization instruction 70.

[0056] Accordingly, system 26 can control each circuit breaker 14 based on the information from that breaker alone, or in combination with the information from one or more of the other breakers in the system 26. Under normal operating conditions, system 26 performs all monitoring, protection, and control decisions at CCPU 28.

[0057] Since the protection and monitoring algorithms of system 26 are resident in CCPU 28, these algorithms can be enabled without requiring hardware or software changes in circuit breaker 14 or module 30. For example, system 26 can include a data entry device 92, such as a human-machine-interface (HMI), in communication with CCPU 28. In this embodiment, one or more attributes and functions of the protection and monitoring algorithms resident on CCPU 28 can easily be modified from data entry device 92. Thus, circuit breaker 14 and module 30 can be more standardized than was possible with the circuit breakers/trip units of prior systems. For example, over one hundred separate circuit breakers/trip units have been needed to provide a full range of sizes normally required for protection of a power distribution system. However, the generic nature of circuit breaker 14 and module 30 enabled by system 26 can reduce this number by over sixty percent. Thus, system 26

can resolve the inventory issues, retrofittability issues, design delay issues, installation delay issues, and cost issues of prior power distribution systems.

[0058] It should be recognized that system 26 is described above as having one CCPU 28 communication with modules 30 by way of a single network 32. However, it is contemplated by the present disclosure for system 26 to have redundant CCPUs 26 and networks 32 as illustrated in phantom in FIG. 1. For example, module 30 is illustrated in FIG. 2 having two network interfaces 46. Each interface 46 is configured to operatively connect module 30 to a separate CCPU 28 via a separate data network 32. In this manner, system 26 would remain operative even in case of a failure in one of the redundant systems.

[0059] Modules 30 can further include one or more backup systems for controlling breakers 14 independent of CCPU 28. For example, system 26 may be unable to protect circuit 16 in case of a power outage in first source 52, during the initial startup of CCPU 28, in case of a failure of network 32, and other reasons. Under these failure conditions, each module 30 includes one or more backup systems to ensure that at least some protection is provided to circuit breaker 14. The backup system can include one or more of an analog circuit driven by second source 54, a separate microprocessor driven by second source 54, and others.

[0060] Referring now to FIG. 3, an exemplary embodiment of a response time 95 for system 26 is illustrated with the system operating stably (e.g., not functioning in a start-up mode). Response time 95 is shown starting at T0 and ending at T1. Response time 95 is the sum of a sample time 96, a receive/validate time 97, a process time 98, a transmit time 99, and a decode/execute time 100.

[0061] In this example, system 26 includes twenty-four modules 30 each connected to a different circuit breaker 14. Each module 30 is scheduled by the phase-lock-loop algorithm and synchronization instruction 70 to sample its first signals 36 at a prescribed rate of 128 samples per cycle. Sample time 96 includes four

sample intervals 101 of about 0.13 milliseconds (ms) each. Thus, sample time 96 is about 0.27 ms for data sampling and packaging into first message 76.

[0062] Receive/validate time 97 is initiated at the receipt of synchronization instruction 70. In an exemplary embodiment, receive/validate time 97 is a fixed time that is, for example, the time required to receive all first messages 76 as determined from the latency of data network 32. For example, receive/validate time 97 can be about 0.25 ms where each first message 76 has a size of about 1000 bits, system 26 includes twenty-four modules 30 (i.e., 24,000 bits), and network 32 is operating at about 100 Mbps. Accordingly, CCPU 28 manages the communications and moving of first messages 76 to the CCPU during receive/validate time 97.

[0063] The protection processes (i.e., process time 98) starts at the end of the fixed receive/validate time 97 regardless of the receipt of first messages 76. If any modules 30 are not sending first messages 76, CCPU 28 flags this error and performs all functions that have valid data. Since system 26 is responsible for protection and control of multiple modules 30, CCPU 28 is configured to not stop the entire system due to the loss of data (i.e., first message 76) from a single module 30. In an exemplary embodiment, process time 98 is about 0.52 ms.

[0064] CCPU 28 generates second message 78 during process time 98. Second message 78 can be twenty-four second messages (i.e., one per module 30) each having a size of about 64 bits per module. Alternately, it is contemplated by the present disclosure for second message 78 to be a single, multi-cast or broadcast message. In this embodiment, second message 78 includes instructions for each module 30 and has a size of about 1600 bits.

[0065] Transmit time 99 is the time necessary to transmit second message 78 across network 32. In the example where network 32 is operating at about 100 Mbps and second message 78 is about 1600 bits, transmit time 99 is about 0.016 ms.

[0066] It is also contemplated for second message 78 to include a portion of synchronization instruction 70. For example, CCPU 28 can be configured to send second message 78 upon receipt of the next synchronization instruction 70 from clock 72. In this example, the interval between consecutive second messages 76 can be measured by module 30 and the synchronization information in the second message, if any, can be used by the synchronization algorithm resident on microprocessor 42.

[0067] Once modules 30 receive second message 78, each module decodes the message and executes its instructions (i.e., send third signals 40), if any, in decode/execute time 100. For example, decode/execute time 100 can be about 0.05 ms.

[0068] In this example, response time 95 is about 1.11 ms. Of course, it should be recognized that system response time 95 can be accelerated or decelerated based upon the needs of system 26. For example, system response time 95 can be adjusted by changing one or more of the sample period, the number of samples per transmission, the number of modules 30, the message size, the message frequency, the message content, and/or the network speed.

[0069] It is contemplated by the present disclosure for system 26 to have response time 95 of up to about 3 milliseconds. Thus, system 26 is configured to open any of its circuit breakers within about 3 milliseconds from the time sensors 34 sense conditions outside of the set parameters.

[0070] Referring to FIG. 4, an exemplary embodiment of a multi-source, multi-tier power distribution system generally referred to by reference numeral 105 is illustrated with features similar to the features of FIG. 1 being referred to by the same reference numerals. System 105 functions as described above with respect to the embodiment of FIGS. 1 through 3, and can include the same features but in a multi-source, multi-layer configuration. System 105 distributes power from at least one power feed 112, in this embodiment a first and second power feed, through a power distribution bus 150 to a number or plurality of circuit breakers 14 and to a number or

plurality of loads 130. CCPU 28 can include a data transmission device 140, such as, for example, a CD-ROM drive or floppy disk drive, for reading data or instructions from a medium 145, such as, for example, a CD-ROM or floppy disk.

[0071] Circuit breakers 14 are arranged in a layered, multi-leveled or multi-tiered configuration with a first level 110 of circuit breakers and a second level 120 of circuit breakers. Of course, any number of levels or configuration of circuit breakers 14 can be used with system 105. The layered configuration of circuit breakers 14 provides for circuit breakers in first level 110 which are upstream of circuit breakers in second level 120. In the event of an abnormal condition of power in system 105, i.e., a fault, protection system 26 seeks to coordinate the system by attempting to clear the fault with the nearest circuit breaker 14 upstream of the fault. Circuit breakers 14 upstream of the nearest circuit breaker to the fault remain closed unless the downstream circuit breaker is unable to clear the fault. Protection system 26 can be implemented for any abnormal condition or parameter of power in system 105, such as, for example, long time, short time or instantaneous overcurrents, or excessive ground currents.

[0072] In order to provide the circuit breaker 14 nearest the fault with sufficient time to attempt to clear the fault before the upstream circuit breaker is opened, the upstream circuit breaker is provided with an open command at an adjusted or dynamic delay time. The upstream circuit breaker 14 is provided with an open command at a modified dynamic delay time that elapses before the circuit breaker is opened. In an exemplary embodiment, the modified dynamic delay time for the opening of the upstream circuit breaker 14 is based upon the location of the fault in system 105. Preferably, the modified dynamic delay time for the opening of the upstream circuit breaker 14 is based upon the location of the fault with respect to the circuit breakers and/or other devices and topology of system 105. CCPU 28 of protection system 26 can provide open commands at modified dynamic delay times for upstream circuit breakers 14 throughout power distribution system 105 depending upon where the fault has been detected in the power flow hierarchy and the modified dynamic delay times for the opening of each of these circuit breakers can preferably

be over an infinite range. Protection system 26 reduces the clearing time of faults because CCPU 28 provides open commands at modified dynamic delay times for the upstream circuit breakers 14 which are optimum time periods based upon the location of the fault. It has been found that the clearing time of faults has been reduced by approximately 50% with the use of protection system 26, as compared to the use of contemporary systems.

[0073] Referring to FIG. 5, an exemplary embodiment of a portion of power distribution system 105 having a two-tier circuit with a main-1 circuit breaker (CB) 415 upstream of feeder 1 CB 420 and feeder 2 CB 425, which are in parallel. Power flow is from transformer 412 through main-1 CB 415, feeder 1 CB 420 and feeder 2 CB 425, to loads 431, 432. In the event of a fault X occurring between feeder 1 CB 420 and load 431, the existence of the fault and the location of the fault is determined by CCPU 28 in the manner as described above and as schematically represented by reference numeral 450. The nearest circuit breaker upstream of the fault X, i.e., feeder 1 CB 420, is placed into "pickup mode" by CCPU 28 and waits a pre-defined delay time before being opened. The modified dynamic delay time for the opening of main-1 CB 415 (the next nearest circuit breaker that is upstream of fault X) is then determined by zone selective interlock (ZSI) routine 426. In an exemplary embodiment, ZSI routine 426 is an algorithm, or the like, performed by CCPU 28. CCPU 28 determines the dynamic delay times for the opening of any number of upstream circuit breakers 14 and provides open or actuation commands to open the circuit breakers at the dynamic delay times.

[0074] In an exemplary embodiment, the modified dynamic delay time for main-1 CB 415 is determined from the sum of the pre-defined delay time and the clearing time of feeder 1 CB 420. The pre-defined delay time is set to best service load 431. The clearing time of a circuit breaker, such as feeder 1 CB 420, is dependent on the type of circuit breaker. The delay time for opening of main-1 CB 415 is then modified based upon the value determined by CCPU 28, as schematically represented by reference numeral 475. This allows feeder 1 CB 420 the optimal time for feeder 1 CB 420 to clear the fault X before main-1 CB 415 opens. The modified

dynamic delay time determined by ZSI routine 426 reduces potential damage to system 105. The modified dynamic delay time also increases the efficiency of system 105 by delaying the opening of main-1 CB 415 for the optimal time period to provide the downstream circuit breaker, feeder 1 CB 420, with the full opportunity to clear the fault X so that other loads, i.e., load 432, can still receive power.

[0075] Referring to FIG. 6, the portion of power distribution system 105 having a two-tier circuit is shown with a fault X occurring between feeder 2 CB 425 and load 432. In the manner described above, the existence and location of fault X is determined, as represented by reference numeral 450. ZSI routine 426 determines the dynamic delay time for opening of main-1 CB 415, as represented by reference numeral 475. Where feeder 2 CB 425 has a different pre-defined delay time set to best service load 432 and/or a different clearing time than feeder 1 CB 420, ZSI routine 426 will determine a different dynamic delay time for the opening of main-1 CB 415. The difference in the two modified dynamic delay times for the opening of main-1 CB 415 (FIGS. 5 and 6) is based upon the location of fault X in system 105 with respect to feeder 1 CB 420 and feeder 2 CB 425.

[0076] Referring to FIG. 7, the portion of power distribution system 105 having a two-tier circuit is shown with a fault X occurring between main-1 CB 415 and either feeder 1 CB 420 or feeder 2 CB 425. In the manner described above, the existence and location of fault X is determined, as represented schematically by reference numeral 480. Since only main-1 CB 415 is available to clear fault X, ZSI routine 426 does not modify the dynamic delay time of the opening of main-1 CB and the main-1 CB will open in its pre-defined delay, which is typically much less than the dynamic time delay in the previous two examples.

[0077] Referring to FIGS. 4 through 7, CCPU 28 coordinates protection system 26 by causing the circuit breaker 14 nearest to the fault to clear the fault. Protection system 26 variably adjusts the dynamic delay time for opening of the upstream circuit breakers 14 to provide backup protection for the downstream circuit breaker nearest the fault. In the event that the downstream circuit breaker 14 nearest

the fault is unable to clear the fault, the next upstream circuit breaker will attempt to clear the fault with minimal additional delay based upon its modified dynamic delay time. As shown in FIG. 7, when a fault occurs between a main circuit breaker and a feeder circuit breaker, e.g., main-1 CB 415 and feeder 1 CB 420, the minimal delay of the main-1 CB opening reduces the let-thru energy. This reduces system stress, damage and potential arc energy exposure of operating and service personnel while maintaining selectivity. In an exemplary embodiment, protection system 26 and CCPU 28 allow the implementation of ZSI routine 426 to modify the dynamic delay times for opening of any circuit breakers 14 throughout system 105 without the need for additional wiring coupling each of the circuit breakers to one another. CCPU 28 provides an open command to the upstream circuit breakers 14 for opening at dynamic delay times as determined by ZSI routine 426.

[0078] In an exemplary embodiment, ZSI routine 426 is performed at CCPU 28 and interacts with the individual protection functions for each module 30, which are also determined at the CCPU. ZSI routine 426 could also use pre-set clearing times for circuit breakers 14 or the clearing times for the circuit breakers could be determined by CCPU 28 based on the physical hardware, which is known by the CCPU. The CCPU 28 effectively knows the topology of power distribution system 105, which allows the CCPU to open the circuit breakers 14 at an infinite range of times.

[0079] Referring to FIG. 8, the portion of power distribution system 105 having a first two-tier circuit branch 490 and a second two-tier circuit branch 790 coupled by a tie CB 700 is shown. In this circuit, the opening of tie CB 700 has created two separate zones of protection in circuit branch 490 and circuit branch 790, which has a transformer 712. In the event of a fault, protection system 26 implements ZSI routine 426, as described above with respect to the two-tier circuit branch of FIGS. 5 through 7, independently for each of the circuit branches 490, 790.

[0080] Referring to FIG. 9, the portion of power distribution system 105 is shown when main-2 CB 715 is open and tie CB 700 is closed. The opening of main-2

CB 715 and the closing of tie CB 700 has created a new single three-tiered zone of protection with feeder 3 CB 720 and feeder 4 CB 725 in the third tier or level of circuit breakers. The status of all of the circuit breakers, including main-2 CB 715 and tie CB 700, is known by CCPU 28, as represented schematically by reference numerals 450. In the event of a fault (not shown) in first circuit branch 490 downstream of the feeder 1 CB 420 or the feeder 2 CB 425, the ZSI routine 426 would modify the dynamic delay time for the opening of main-1 CB 415, as described above with respect to FIG. 5 or FIG. 6.

[0081] In the event of a fault (not shown) in second circuit branch 790 downstream of the feeder 3 CB 720 (or the feeder 4 CB 725), the ZSI routine 426 would modify the dynamic delay time for opening of both the tie CB 700 and the main-1 CB 415. In an exemplary embodiment, the modified dynamic delay time for the opening of tie CB 700 is determined from the sum of the pre-defined delay time and the clearing time of feeder 3 CB 720 (or feeder 4 CB 725). The dynamic delay time for opening of tie CB 700 is then modified based upon the value determined by CCPU 28, as schematically represented by reference numeral 500. This provides feeder 3 CB 720 (or feeder 4 CB 725) with an optimal time to clear the fault before tie CB 700 is opened. Furthermore, the modified dynamic delay time for the opening of main-1 CB 415 is then determined from the sum of the modified dynamic delay time and the clearing time of tie CB 700. The dynamic delay time for opening of main-1 CB 415 is then modified based upon the value determined by CCPU 28, as schematically represented by reference numeral 475. This provides tie CB 700 with an optimal time to clear the fault before main-1 CB 415 is opened by the open command from CCPU 28.

[0082] In the event of a fault between tie CB 700 and feeder 3 CB 720 (or feeder 4 CB 725), the dynamic delay time for opening of main-1 CB 415 is modified from the sum of the pre-defined delay and the clearing time of tie CB 700. The delay for opening of tie CB 700 would not be modified since it is the nearest circuit breaker upstream of the fault for clearing the fault.

[0083] In an exemplary embodiment, the protection functions performed at CCPU 28, including ZSI routine 426, are based on state information or status of circuit breakers 14, as well as current. Through the use of protection system 26, the state information is known by CCPU 28. The state information is synchronized with the current and the voltage in power distribution system 105. CCPU 28 effectively knows the topology of the power distribution system 105 and uses the state information to track topology changes in the system. CCPU 28 and ZSI routine 426 utilizes the topology information of power distribution system 105 to optimize service and protection.

[0084] Of course, it is contemplated by the present disclosure for power distribution system 105 to have any number of tiers or levels and any configuration of branch circuits. The dynamic delay time for opening of any number of circuit breakers 14 upstream of the fault could be modified as described above based upon the location of the fault in the power flow hierarchy. Additionally, the zones of protection and the dynamic delay times can change as the power distribution system 105 changes. In an alternate embodiment, ZSI routine 426 can modify the dynamic delay time for opening of the upstream circuit breakers 14 based upon other factors using different algorithms. Protection system 26 allows for the dynamic changing of the delay times for opening of circuit breakers 14 throughout the power distribution system 105 based upon any number of factors, including the location of the fault. Protection system 26 also allows for the upstream circuit breaker 14 to enter the pickup mode as a function of the downstream circuit breaker 14 fault current and pickup settings as opposed to its own current and pickup settings.

[0085] The embodiments of FIGS. 1 through 9 describe the implementation of ZSI routine 426 at CCPU 28. However, it is contemplated by the present disclosure that the use of dynamic delay times for opening of circuit breakers 14 and/or the use of ZSI routine 426 can be implemented in other ways such as, for example, in a distributed control system with supervision by CCPU 28 or a distributed control system with peer to peer communications. In such distributed control systems, the delay time for opening of the upstream circuit breaker 14 will be modified to a

dynamic delay time and/or based at least in part on the location of the fault in the power flow hierarchy. The dynamic delay times for the upstream circuit breakers 14 can also be determined and communicated to the upstream circuit breakers and/or circuit breaker actuators operably connected to the breakers.

[0086] In an exemplary embodiment, protection system 26 using CCPU 28 and ZSI routine 426 replaces the traditional time-current and fixed-delay protection while achieving both selectivity and tight backup protection. The feeder breakers (load-side) are set best to serve their loads reliably, but the main breakers and tie breakers (line-side) dynamically set their delay and current settings to best fit each feeder when that feeder circuit experiences a fault. The determination of a fault can be based on the feeder's settings and the sensors. In a traditional system, the sensing of a fault at the tie or main breaker is based on the settings at those trips and the current flowing through the respective circuit breakers. If the current magnitude is not sufficient to be recognized as a fault the trip units will not initiate a trip and hence provide no back-up function. There are no additional margins of safety or unnecessary time delays needed to allow the protection system 26 to operate selectively and provide protection to the mechanical limits of the devices used. Protect system 26 also applies within the short-circuit ranges of the devices in power distribution system 105. When the CCPU 28 senses a fault within the short-circuit range of any load-side device, the next line-side device is ready to operate immediately if the CCPU senses that the load-side device is not clearing the fault, even if the fault may not be in the instantaneous range assigned to the line-side device. This form of backup protection could save many cycles of fault current when a feeder breaker fails to open or if the fault occurs in the switchgear, without sacrificing selectivity.

[0087] While the instant disclosure has been described with reference to one or more exemplary embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope thereof. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the disclosure

without departing from the scope thereof. Therefore, it is intended that the disclosure not be limited to the particular embodiment(s) disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A method of protecting a circuit having a first circuit breaker and a second circuit breaker downstream of said first circuit breaker, the method comprising:

detecting a fault in said circuit, said fault being downstream of said second circuit breaker;

determining a dynamic delay time for opening said first circuit breaker; and

opening said first circuit breaker after said dynamic delay time has elapsed.

2. The method of claim 1, wherein determining said dynamic delay time comprises monitoring electrical parameters of said circuit and communicating said electrical parameters over a network to a microprocessor, said microprocessor being configured to operate said first and second circuit breakers.

3. The method of claim 2, further comprising generating an open command by said microprocessor in response to said electrical parameters, communicating said open command from said microprocessor to a circuit breaker actuator operably connected to said second circuit breaker, and opening said second circuit breaker in response to said open command.

4. The method of claim 2, further comprising generating an open command by said microprocessor in response to said electrical parameters, communicating said open command from said microprocessor to a circuit breaker actuator operably connected to said first circuit breaker, and opening said first circuit breaker in response to said open command after said dynamic delay time has elapsed.

5. The method of claim 2, further comprising sensing said electrical parameters with a sensor, communicating signals representative of said electrical parameters to a data sample and transmission module and communicating said signals to said microprocessor, wherein said module, said sensor and said microprocessor are communicatively coupled.

6. The method of claim 3, further comprising detecting if said fault is cleared.

7. The method of claim 6, wherein detecting if said fault is cleared comprises monitoring said electrical parameters and communicating said electrical parameters over said network to said microprocessor.

8. The method of claim 7, further comprising opening said first circuit breaker after said dynamic delay time has elapsed if said fault is not cleared in response to opening said second circuit breaker.

9. A method of protecting a circuit having a first circuit breaker arranged upstream of a plurality of second circuit breakers, the method comprising:

detecting a fault in said circuit;

determining a location of said fault;

determining a dynamic delay time for opening said first circuit breaker based at least in part upon said location of said fault; and

delaying opening said first circuit breaker until after said dynamic delay time has elapsed.

10. The method of claim 9, wherein determining said location of said fault comprises determining a nearest breaker upstream to said fault of said plurality of second circuit breakers, said nearest breaker being nearest to said fault and upstream of said fault.

11. The method of claim 9, wherein said dynamic delay time is determined by at least one control processing unit, said at least one control processing unit being in communication with said first circuit breaker and said plurality of second circuit breakers over a network, said at least one control processing unit being configured to open and close said first circuit breaker and said plurality of second circuit breakers.

12. The method of claim 11, wherein detecting said fault and detecting said location of said fault comprise monitoring electrical parameters of said circuit and communicating said electrical parameters over said network to said at least one control processing unit.

13. The method of claim 12, further comprising opening said first circuit breaker in response to said electrical parameters communicated to said at least one control processing unit.

14. The method of claim 12, further comprising sensing said electrical parameters with a plurality of sensors, communicating said electrical parameters to a plurality of data sample and transmission modules and communicating signals representative of said electrical parameters to said at least one control processing unit, wherein each of said modules is in communication with at least one of said first circuit breaker or said plurality of second circuit breakers, at least one of said plurality of sensors, and said at least one control processing unit.

15. The method of claim 10, wherein said dynamic delay time is the sum of a pre-defined time delay and a clearing time of said nearest breaker.

16. The method of claim 10, further comprising determining dynamic delay times for opening each of a plurality of third circuit breakers based at least in part on said nearest breaker, said plurality of third circuit breakers being upstream of said nearest breaker, and opening each of said plurality of third circuit breakers after said dynamic delay times have elapsed.

17. The method of claim 16 further comprising:

determining a state for each of said first circuit breaker, said plurality of second circuit breakers and said plurality of third circuit breakers, said state being either open or closed; and

opening at least one of said plurality of third circuit breakers based at least in part on said state for each of said first circuit breaker, said plurality of second circuit breakers and said plurality of third circuit breakers.

18. The method of claim 16, further comprising:

determining a state for each of said first circuit breaker, said plurality of second circuit breakers and said plurality of third circuit breakers, said state being either open or closed;

determining a topology of said circuit based upon said state for each of said first circuit breaker, said plurality of second circuit breakers and said plurality of third circuit breakers; and

opening at least one of said first circuit breaker or said plurality of third circuit breakers based on said topology.

19. The method of claim 18, further comprising:

determining a change in said state for each of said first circuit breaker, said plurality of second circuit breakers and said plurality of third circuit breakers; and

monitoring a change in said topology based upon said change in said state for each of said first circuit breaker, said plurality of second circuit breakers and said plurality of third circuit breakers

20. A protection system coupled to a circuit having a first circuit breaker arranged upstream of a plurality of second circuit breakers, the system comprising:

a network and at least one control processing unit operatively controlling said first circuit breaker and said plurality of second circuit breakers, said network being communicatively coupled to said circuit, said first circuit breaker, said plurality of second circuit breakers and said at least one control processing unit, wherein said at least one control processing unit determines a dynamic delay time for opening said first circuit breaker if a fault is detected in said circuit, and wherein said at least one control processing unit delays opening said first circuit breaker until after said dynamic delay time has elapsed.

21. The system of claim 20, wherein said at least one control processing unit receives parameter signals representative of electrical parameters of said circuit, and wherein said at least one control processing unit opens at least one of said second circuit breakers in response to said parameter signals if said fault is detected in said circuit.

22. The system of claim 21, further comprising a plurality of data sample and transmission modules and a plurality of sensors, each of said modules being in communication with at least one of said first circuit breaker or said plurality of second circuit breakers, at least one of said plurality of sensors and said at least one control processing unit, wherein said plurality of sensors sense said electrical parameters and communicate said parameter signals to said plurality of modules, and wherein said plurality of modules communicate said parameter signals to said at least one control processing unit.

23. The system of claim 21, further comprising a circuit breaker actuator in communication with said at least one control processing unit, wherein said circuit breaker actuator receives an actuation signal from said at least one control processing unit, said actuation signal causing said circuit breaker actuator to open said first circuit breaker after said dynamic delay time has elapsed.

24. The system of claim 23, wherein said at least one control processing unit determines a nearest breaker upstream to said fault of said plurality of second circuit breakers, said nearest breaker having a pre-defined delay time and a clearing time, and wherein said at least one control processing unit determines said dynamic delay time based on said pre-defined delay time and said clearing time.

25. The system of claim 24, wherein said at least one control processing unit selectively generates a de-actuation signal, and wherein said de-actuation signal causes said circuit breaker actuator to close said nearest breaker.

26. A power distribution system comprising:

a circuit having a plurality of circuit breakers, at least one power source and at least one load, said plurality of circuit breakers being arranged with at least one first circuit breaker upstream of a plurality of second circuit breakers;

a network; and

at least one control processing unit operatively controlling said plurality of circuit breakers, said network being communicatively coupled to said at least one control processing unit and said circuit,

wherein said at least one control processing unit determines a dynamic delay time for opening said at least one first circuit breaker if a fault is detected in said circuit, and wherein said at least one control processing unit delays opening said at least one first circuit breaker until after said dynamic delay time has elapsed.

27. The system of claim 26, wherein said at least one control processing unit receives parameter signals representative of electrical parameters of said circuit, and wherein said dynamic delay time is selectively generated by said at least one control processing unit in response to said parameter signals if said fault is detected in said circuit.

28. The system of claim 27, further comprising a plurality of data sample and transmission modules and a plurality of sensors, each of said modules being in communication with at least one of said plurality of circuit breakers, at least one of said plurality of sensors and said at least one control processing unit, wherein said plurality of sensors sense said electrical parameters and communicate said parameter signals to said plurality of modules, and wherein said plurality of modules communicate said parameter signals to said at least one control processing unit.

29. The system of claim 27, further comprising a circuit breaker actuator in communication with said at least one control processing unit, wherein said circuit breaker actuator receives an actuation signal from said at least one control processing unit and opens said at least one first circuit breaker after said dynamic delay time has elapsed in response to said actuation signal.

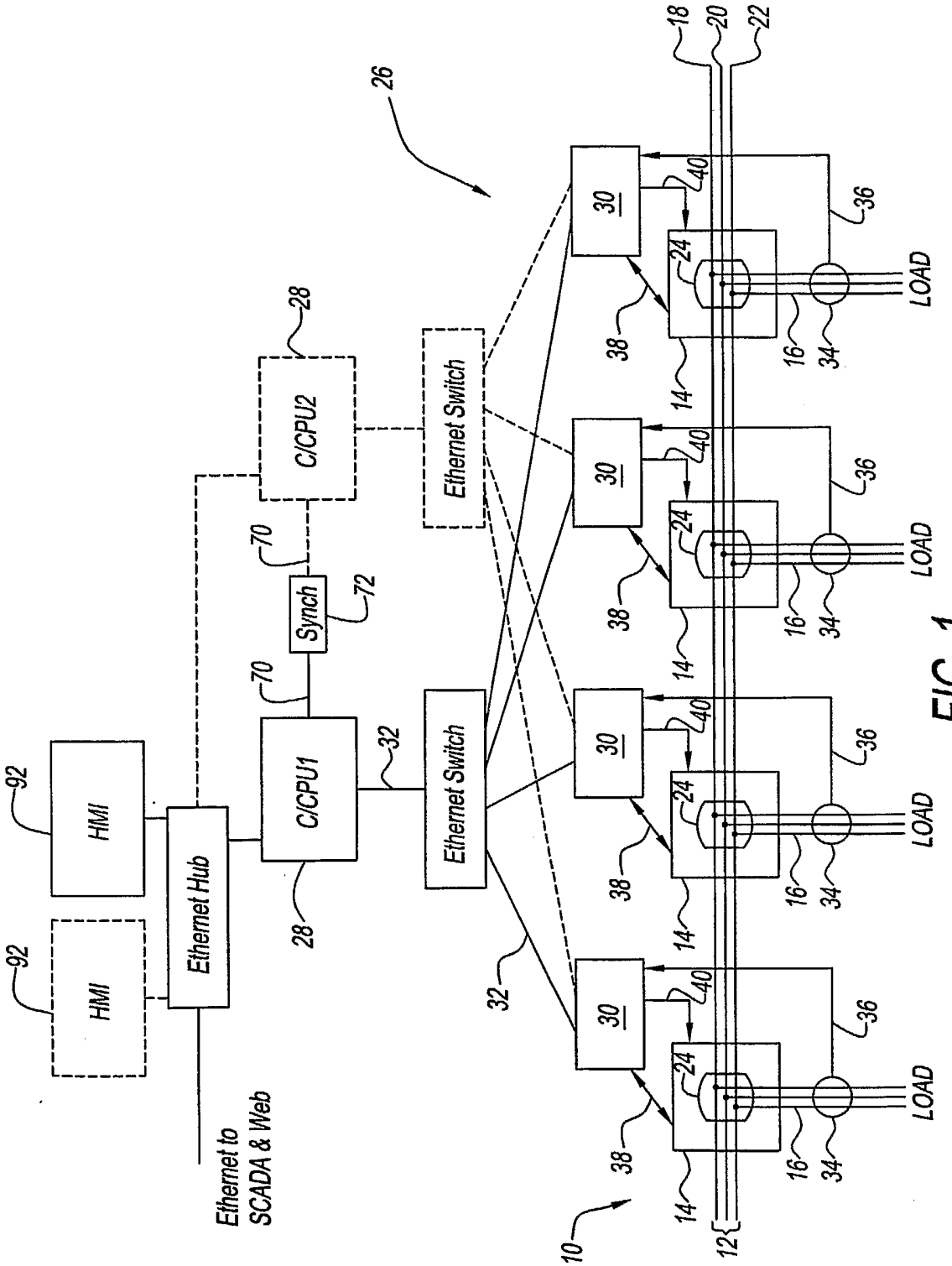
30. The system of claim 27, wherein each of said plurality of circuit breakers has a circuit breaker actuator, wherein said at least one control processing unit determines a nearest breaker upstream to said fault of said plurality of second circuit breakers, wherein said at least one control processing unit selectively generates an actuation signal in response to said parameter signals if said fault is detected in said circuit and communicates said actuation signal to said circuit breaker actuator of said nearest breaker, and wherein said actuation signal causes said circuit breaker actuator of said nearest breaker to open said nearest breaker.

31. The system of claim 30, wherein said at least one control processing unit selectively generates a de-actuation signal and communicates said de-actuation signal to said circuit breaker actuator of said nearest breaker, and wherein said de-actuation signal causes said circuit breaker actuator of said nearest breaker to close said nearest breaker.

32. The system of claim 30, wherein said nearest breaker has a pre-defined delay time and a clearing time, and wherein said dynamic delay time is based at least in part upon said pre-defined delay time and said clearing time.

33. The system of claim 32, wherein said plurality of circuit breakers further comprises a plurality of third circuit breakers upstream of said at least one first circuit breaker and said nearest circuit breaker, and wherein said at least one control processing unit determines dynamic delay times for opening each of said plurality of third circuit breakers, said dynamic delay times being based at least in part on said pre-defined delay time and said clearing time of said nearest breaker.

34. The system of claim 33, wherein said at least one control processing unit determines a state for each of said plurality of circuit breakers, said state being either open or closed, wherein said at least one control processing unit determines a topology of said circuit based upon said state of each of said plurality of circuit breakers, and wherein said at least one control processing unit opens at least one of said plurality of third circuit breakers based on said topology.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18
20
22
30
40
36
24
LOAD
38
16
34
14
28
C/CPU2
Ethernet Switch
70
Synch
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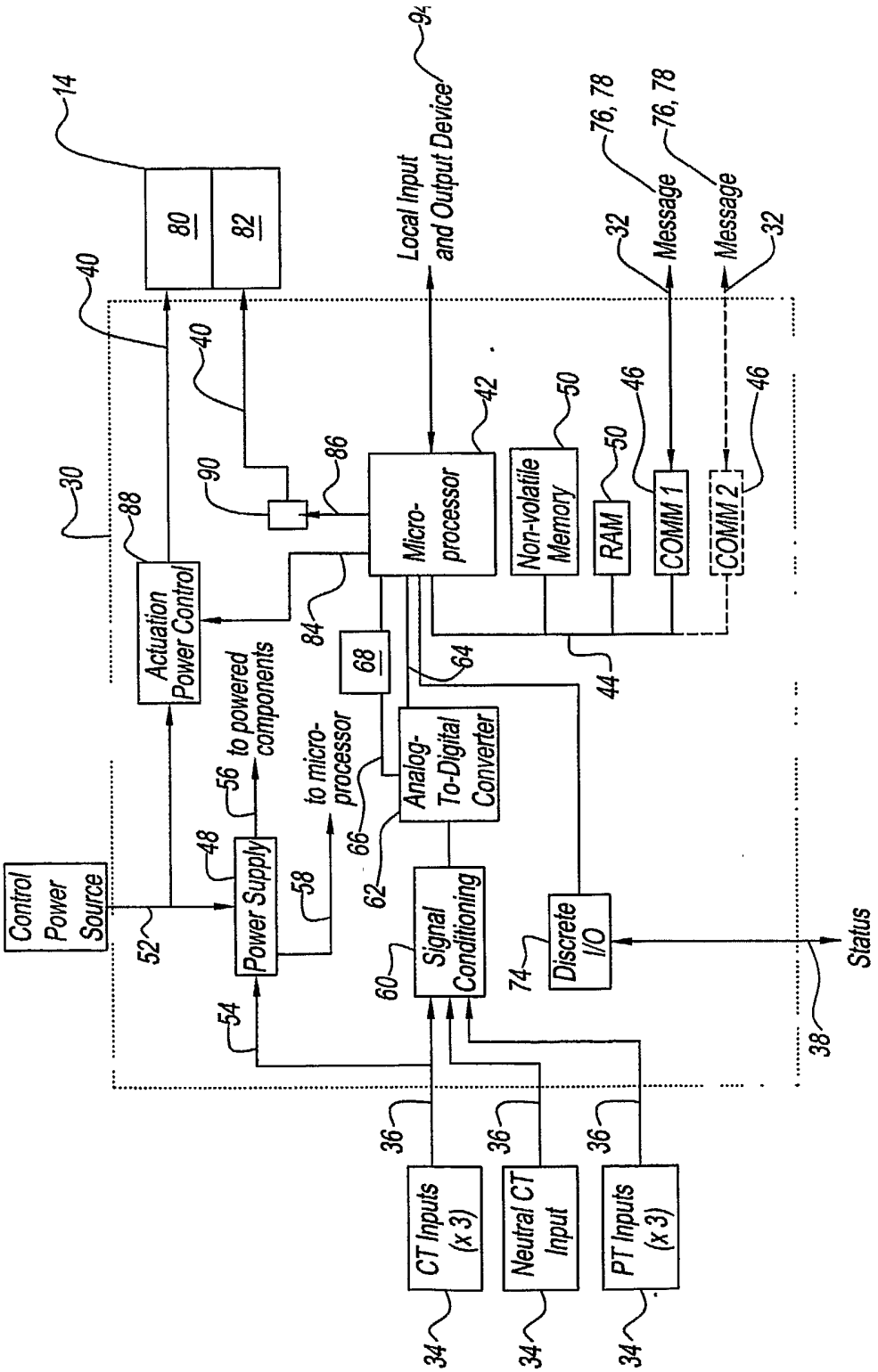
C/CPU1
32
Ethernet Switch
HMI
92
Ethernet Hub
Ethernet to SCADA & Web
10
12

FIG. 1


14
80
82
40
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30
88
Actuation Power Control
90
86
Micro-processor
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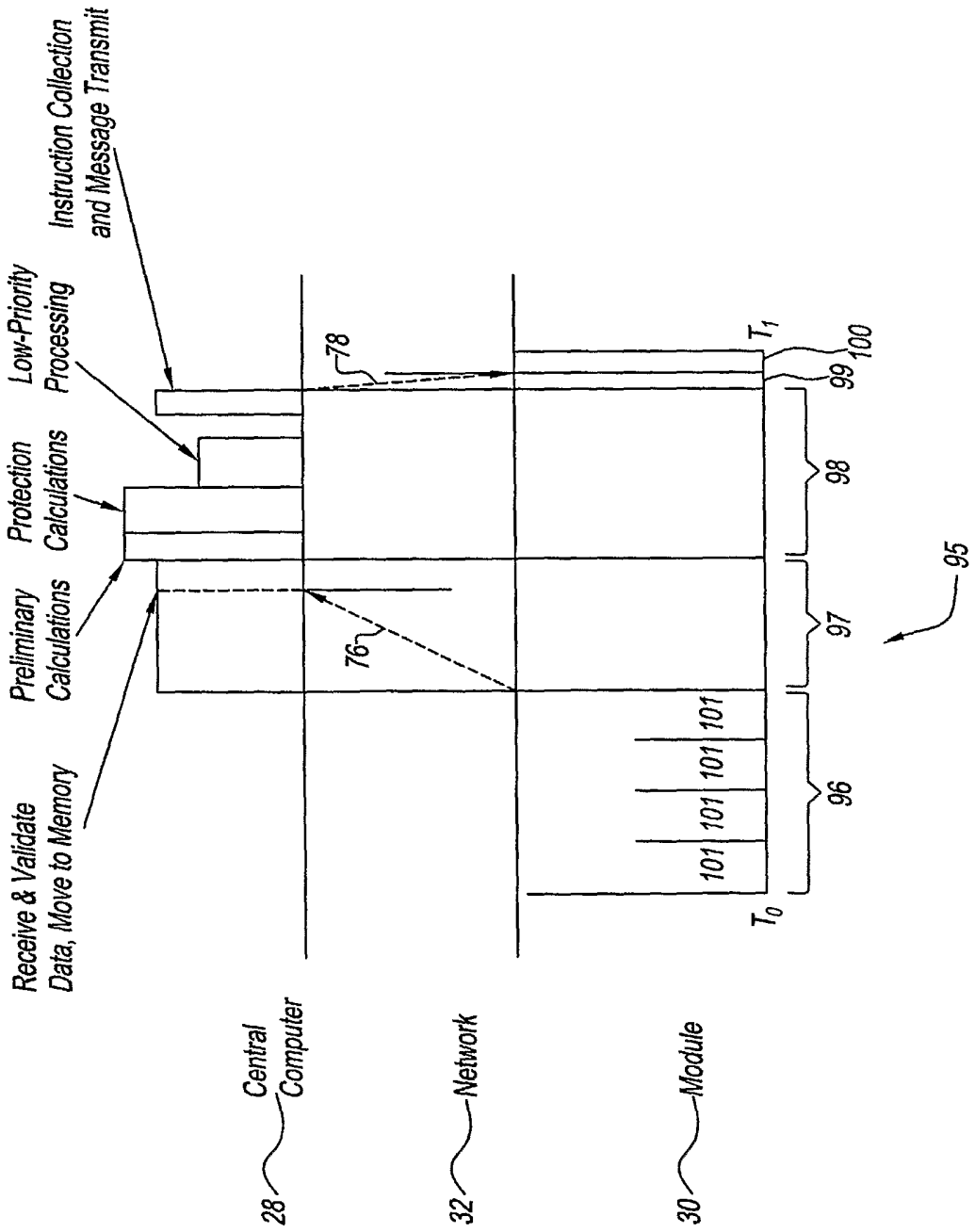
Local Input and Output Device
94
76, 78
Message
32
76, 78
Message
32
Non-volatile Memory
50
RAM
50
COMM 1
46
COMM 2
46
84
68
64
44
to powered components
56
to micro-processor
66
Analog-To-Digital Converter
62
Control Power Source
52
48
Power Supply
58
54
Signal Conditioning
60
Discrete I/O
74
Status
38
36
36
36
CT Inputs (x 3)
Neutral CT Input
PT Inputs (x 3)
34
34
34

FIG. 2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Low-Priority Processing
Protection Calculations
Preliminary Calculations
Receive & Validate Data, Move to Memory
78
76
T_1
T_0
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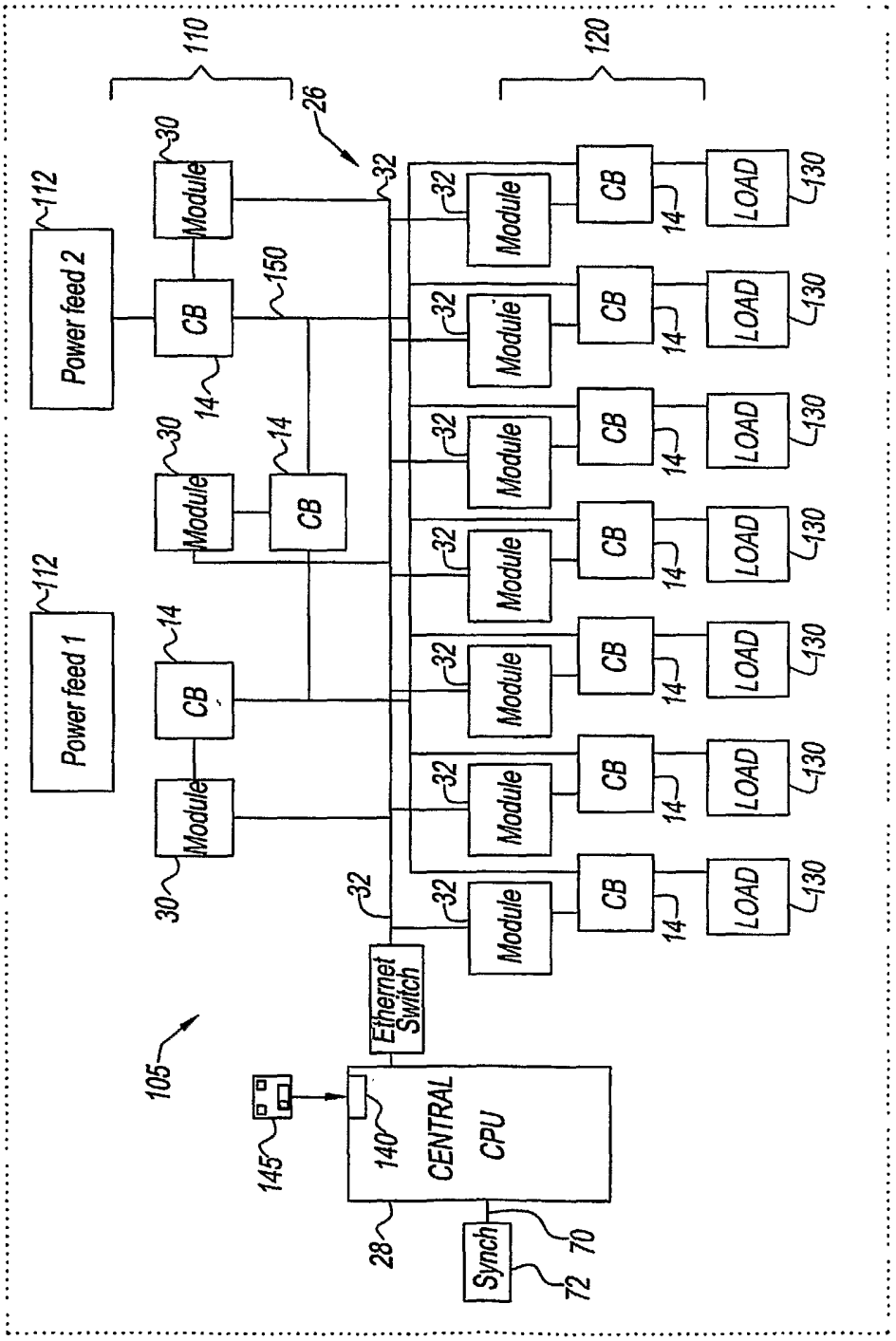
100
98
97
96
95
101
101
101
101
Central Computer
Network
Module
28
32
30

FIG. 3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120
26
Power feed 2
Power feed 1
112
Module
CB
LOAD
Ethernet Switch
CENTRAL CPU
Synch
105
140
145
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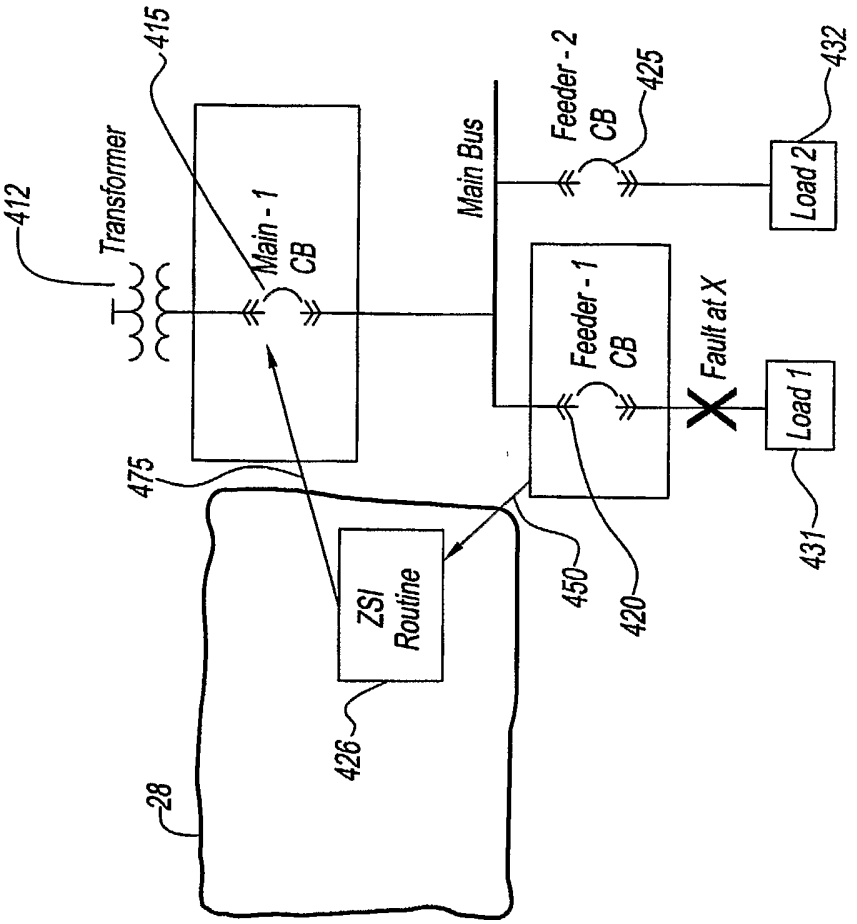
72
150
14
30
32
130

FIG. 4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Transformer
415
Main - 1
CB
Main Bus
Feeder - 2
CB
425
Load 2
432
Feeder - 1
CB
Fault at X
Load 1
431
475
450
420
ZSI
Routine
426
28

FIG. 5

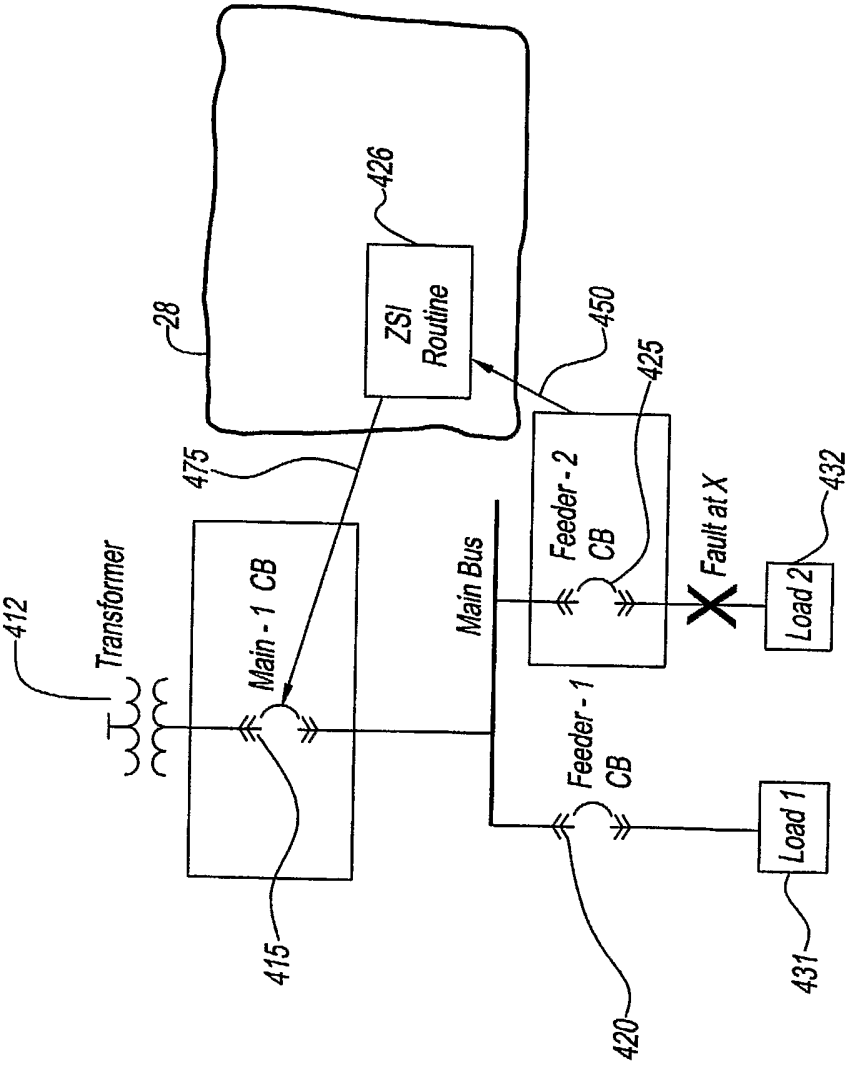
28
426
ZSI Routine
450
425
475
Feeder - 2 CB
Fault at X
432
Load 2
412
Transformer
Main - 1 CB
Main Bus
Feeder - 1 CB
Load 1
415
420
431

FIG. 6

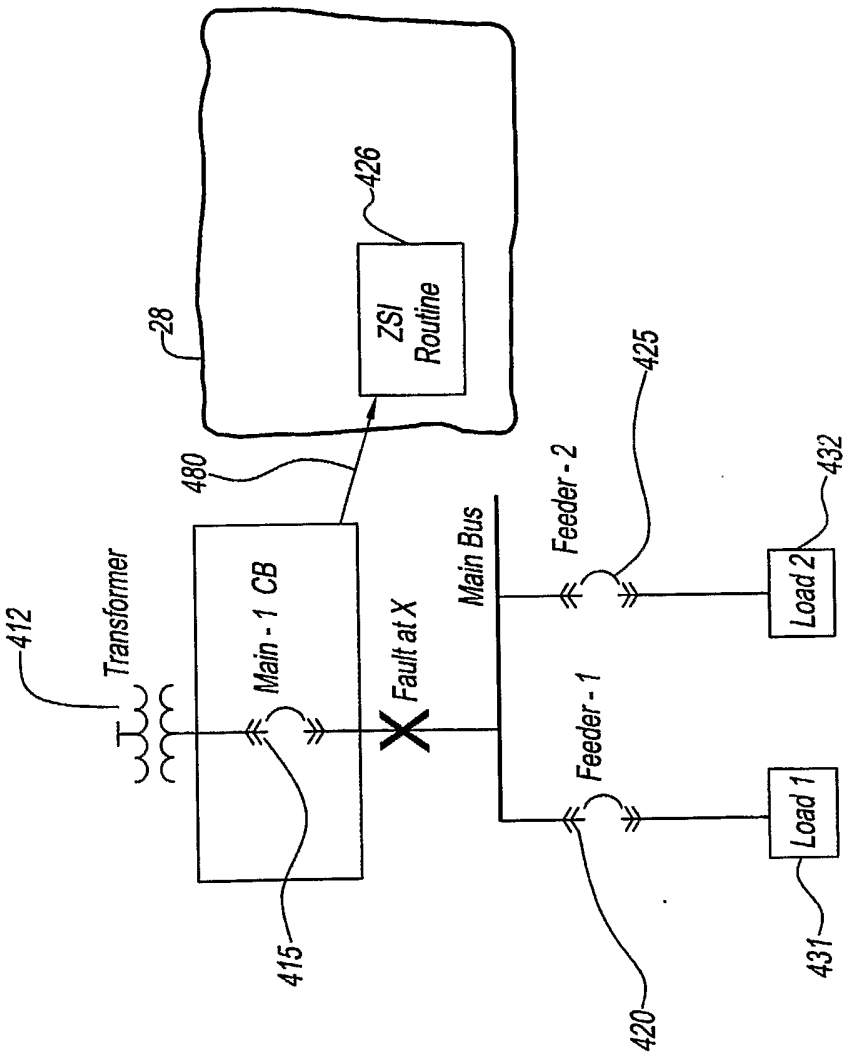
412
Transformer
Main - 1 CB
415
Fault at X
Main Bus
Feeder - 1
420
Feeder - 2
425
Load 1
431
Load 2
432
480
28
ZSI Routine
426

FIG. 7

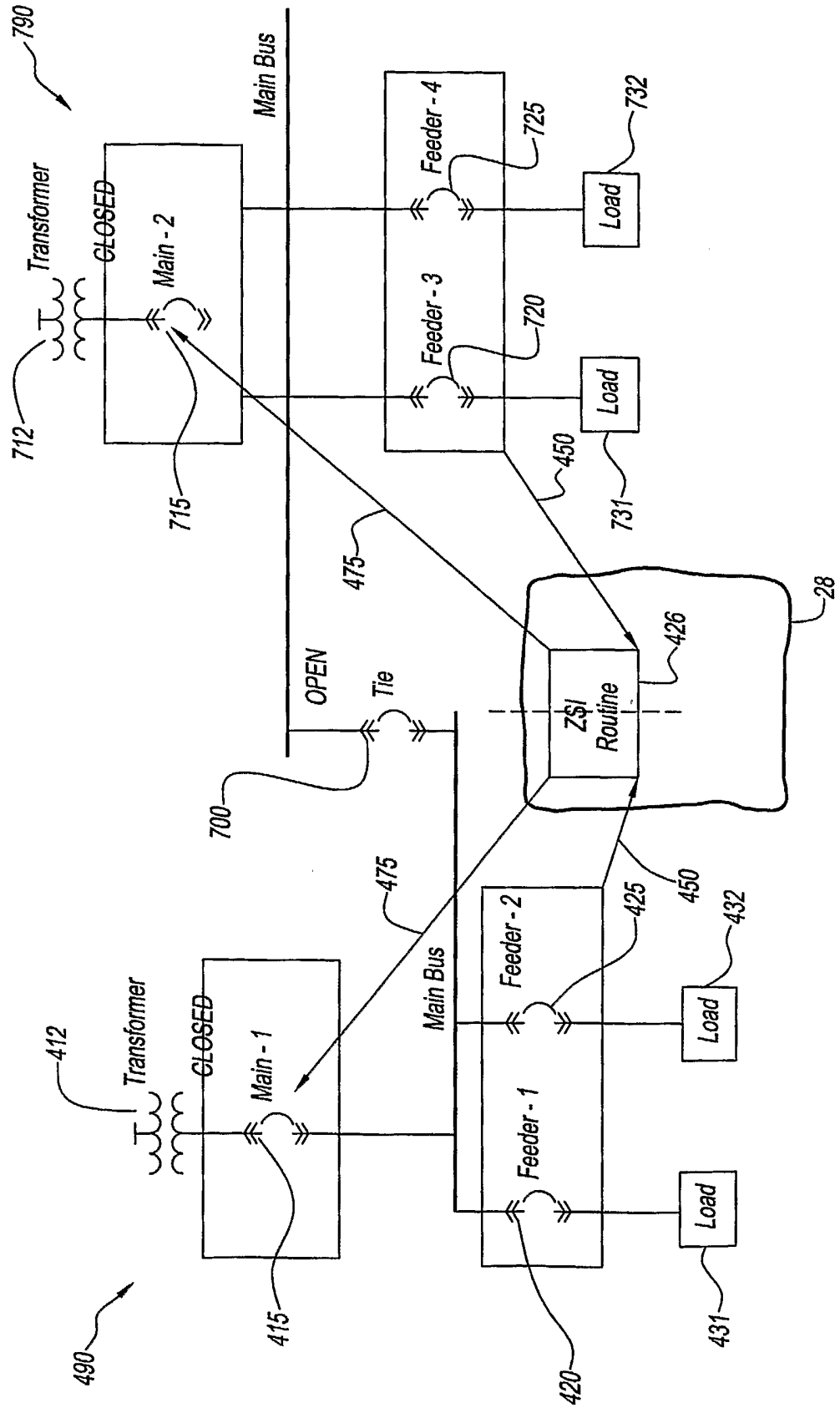
790
Transformer
712
CLOSED
Main - 2
715
Main Bus
Feeder - 4
725
732
Load
Feeder - 3
720
Load
731
450
475
OPEN
Tie
700
ZSI
Routine
426
28
475
450
425
Feeder - 2
432
Load
Main Bus
412
Transformer
CLOSED
Main - 1
415
Feeder - 1
Load
431
490
420

FIG. 8

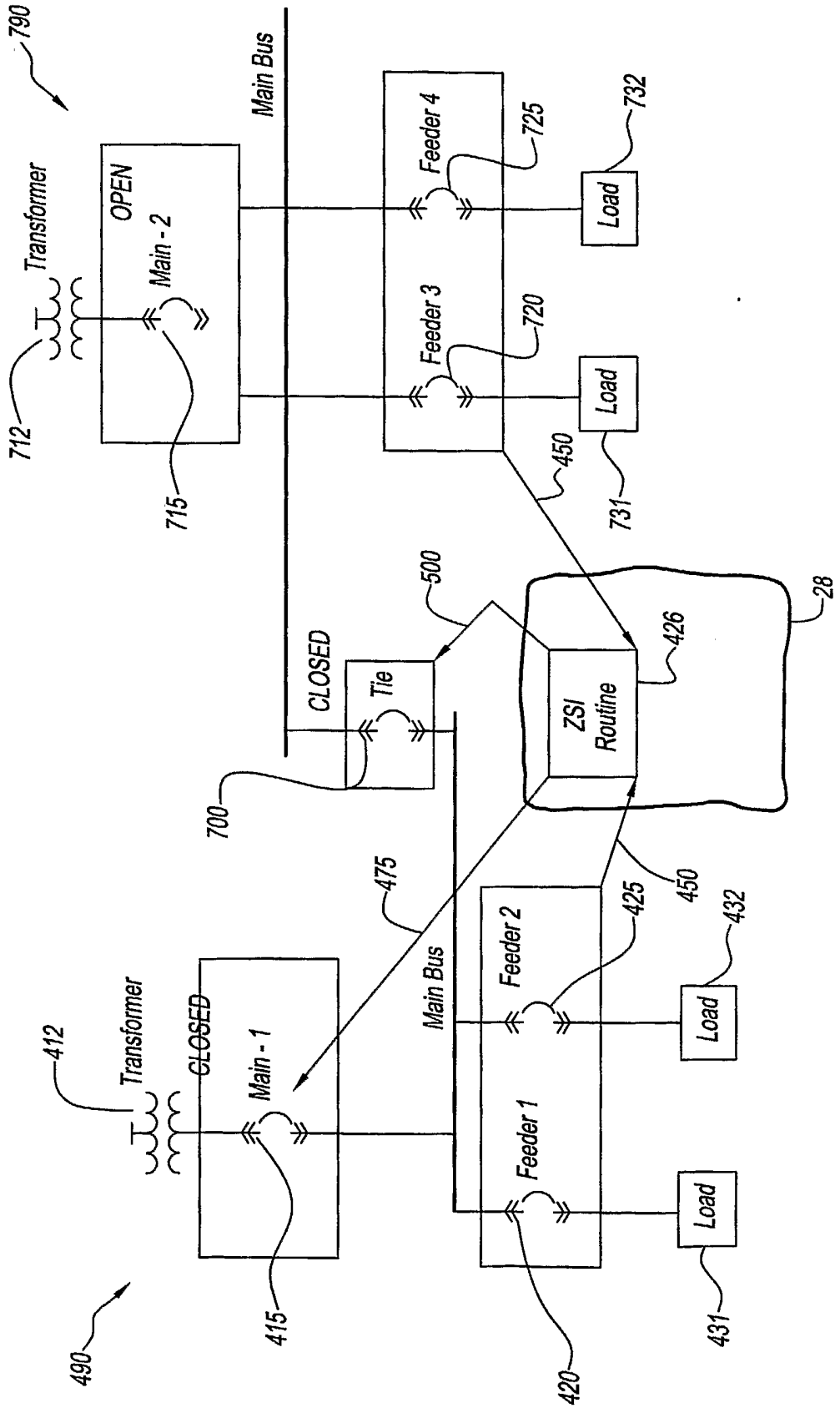
790
Transformer
712
OPEN
Main - 2
715
Main Bus
Feeder 4
725
732
Load
Feeder 3
720
Load
450
731
500
CLOSED
Tie
700
ZSI
Routine
426
28
475
Main Bus
Feeder 2
425
450
432
Load
412
Transformer
CLOSED
Main - 1
415
Feeder 1
420
Load
431
490

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/05625

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H02H 9/02, 3/00
US CL : 361/93.2, 97

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 361/93.2, 97, 94, 96, 68

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPAT, US-PGPUB, EPO, JPO, DERWENT

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 4,996,646A (Farington) 26 February 1991 (31.03.1998), Fig. 8,9, col.6, lines 29 - 68, col. 7, lines 1 - 43, col. 60, lines 55 -68	1 - 9, 11 - 15, 20 - 23, 26 - 29 --- 10, 16, 24, 25, 30 - 34
Y	US 6,297,939 B1 (Bilacet al.) 2 October 2001(05.11.1999), Fig.1, 2, 5, col. 3, lines 19 - 67,col. 4, lines 1 - 32, col. 5, lines 15 - 67, col. 6, lines 1 - 26.	10, 16, 24, 25, 30 - 34
A	US 6,167,329 A(Engelet et al.) 26 December 2000 (6.04.1998)	1 - 34
A	US 5,905,616 A (Lyke) 18 May 1999 (01.06.1998)	1 - 34
A	US 5,440,441 A (Ahuja) 8 August 1995 (18.10.1993)	1 - 34

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
27 June 2003 (27.06.2003)	29 JUL 2003
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703)305-3230	Authorized officer Brian Sircus Telephone No. (703) 308-0269

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Form PCT/ISA/210 (second sheet) (July 1998)