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12/776,323 7 May 2010 (07.05.2010) US(71) Applicant (for all designated States except US): **CY-
PRESS SEMICONDUCTOR CORPORATION**
[US/US]; 198 Champion Circle, San Jose, California
95134 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **SULLAM, Bert**
[US/US]; 12527 NE 32nd Street, Bellevue, Washington
98005 (US). **KUTZ, Harold** [US/US]; 18802 92nd Ave
W, Edmonds, Washington 98020 (US). **WILLIAMS,
Timothy** [US/US]; 13455 SE 24th St, Bellevue, Wash-
ington 98005 (US). **SHUTT, James** [US/US]; 2033 2nd
Ave #2204, Seattle, Washington 98121 (US). **BYR-
KETT, Bruce** [US/US]; 198 Champion Court, San Jose,
California 95134 (US). **RICHMOND, Melany** [US/US];
P.O. Box 816 Ellensburg, Wa, Washington 98926 (US).**KOHAGEN, Nathan** [US/US]; 10720 Sand Point Way
NE, Seattle, Washington 98125 (US). **HASTINGS,
Mark** [US/US]; 9728 50th PL W, Mukilteo, Washington
98275 (US). **THIAGARAJAN, Eashwar** [IN/US];
20225 Bothell-Everett Hwy, #728, Bothell, Washington
98012 (US). **SNYDER, Warren** [CA/US]; 6405 158th
Street SE, Snohomish, Washington 98296 (US).(74) Agent: **SAKO, Bradley**; Cypress Semiconductor Corpo-
ration, Attn: Penny Jackson, 198 Champion Court, San
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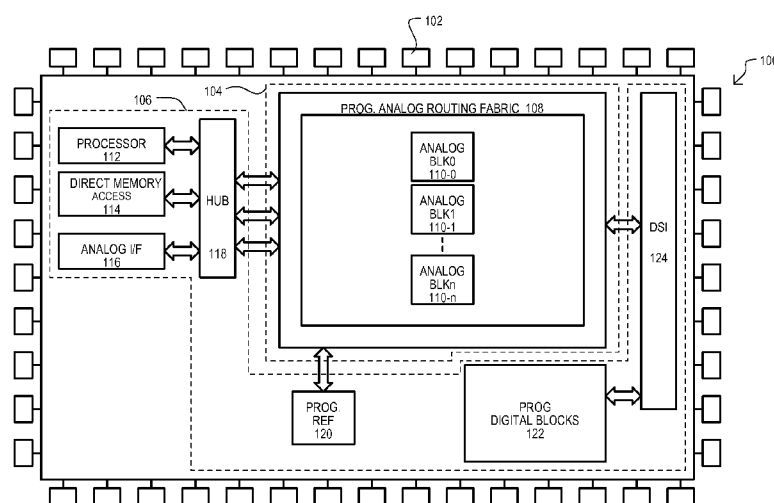
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CHIP

FIG. 1

(57) Abstract: An integrated circuit device may include a reconfigurable analog signal switching fabric comprising a plurality of global buses that are selectively connected to external pins by pin connection circuits in response to changeable analog routing data, and a plurality of local buses that are selectively connected to analog blocks and/or global buses by routing connection circuits in response to the analog routing data; and at least one processor circuit that executes predetermined operations in response to instruction data.



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DYNAMICALLY RECONFIGURABLE ANALOG ROUTING CIRCUITS AND METHODS FOR SYSTEM ON A CHIP

TECHNICAL FIELD

5 The present disclosure relates to integrated circuit devices, and more particularly to reconfigurable integrated circuit devices having digital and analog circuit blocks.

DISCLOSURE OF INVENTION

10 The disclosure includes an integrated circuit device, comprising: a dynamically or statically reconfigurable analog signal switching fabric comprising a plurality of global buses that are selectively connected to external pins by pin connection circuits in response to analog routing data, and a plurality of local buses that are selectively connected to analog blocks and/or global buses by
15 routing connection circuits in response to the analog routing data; and at least one processor circuit that executes predetermined operations in response to instruction data

 The disclosure also includes an integrated circuit, comprising: at least one processor circuit; a plurality of analog circuit blocks; and a dynamically or statically
20 reconfigurable analog routing fabric that selectively interconnects the analog circuit blocks and input/output (I/O) pins in response to analog routing data from at least one routing data source in addition to the at least one processor circuit.

 The disclosure further includes a method, comprising: in response to routing data, configuring a reconfigurable analog routing fabric on an integrated
25 circuit to selectively enable connections between a plurality of input/output (I/O) pins and at least one of a plurality of global buses, and to selectively enable connections between at least one global bus and at least one of a plurality of analog circuit blocks of the integrated circuit; wherein the routing data is dynamically or statically provided from digital circuits of the integrated circuit.

30

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows an integrated circuit device according to an embodiment.

FIG. 2 shows an integrated circuit device according to another

embodiment.

FIG. 3 is a representation of an integrated circuit device architecture according to an embodiment.

FIG. 4 is a representation of an integrated circuit device architecture
5 according to another embodiment.

FIG. 5 shows input/output (I/O) connection circuits according to an embodiment.

FIG. 6 shows I/O connection circuits according to a further embodiment.

FIG. 7 shows a general purpose I/O configuration circuit according to one
10 embodiment.

FIG. 8 shows a programmable analog routing fabric according to an embodiment.

FIGS. 9A to 9H show various analog block connection arrangements according to particular embodiments.

FIGS. 10A to 10D show various signal path connections that may be
15 created with an analog routing fabric according to various embodiments.

FIG. 11 is a schematic diagram showing global I/O connections to buses of an analog routing fabric according to one embodiment.

20 MODE(S) FOR CARRYING OUT THE EMBODIMENTS

Various embodiments will now be described that show devices and methods of an integrated circuit device having a reconfigurable analog routing fabric for connecting input/outputs (I/Os) to one or more analog circuit blocks with multiple buses and connection circuits.

25 In the following description, like items are referred to by the same reference characters, but with the first digit(s) corresponding to the corresponding figure number.

Referring now to FIG. 1, an integrated circuit device according to a first embodiment is shown in a block diagram and designated by the general reference
30 character **100**. In some embodiments, a device **100** may be a "system-on-chip" that provides both programmable analog functions as well as programmable digital functions.

As shown in FIG. 1, a device **100** may include a number of external

connection pins (one shown as **102**), an analog section **104**, and a digital section **106**. Pins (e.g., **102**) may provide a physical signal connection to device **100**, and may be input pins, output pins, or pins serving as both an input and an output.

Such pins (e.g., **102**) will be referred to herein as input/output (I/O) pins, it being understood such pins serve as (or may be configured to serve as) an input, output
5 or both. In some embodiments, pins (e.g., **102**) may be configured as either analog pins (i.e., input or output analog signals) or digital pins (i.e., input or output binary logic signals). Further, in some embodiments, pins (e.g., **102**) may be dedicated pins (e.g., only digital input and/or output pins).

10 An analog section **104** may include a programmable analog routing fabric **108** and a number of analog blocks **110-0** to **-n**.

Analog routing fabric **108** may be configured (and reconfigured) to provide signal paths between I/O pins (e.g., **102**) configured as analog I/Os and any of analog blocks (**110-0** to **-n**). As but a few examples, an analog routing fabric **108**
15 may provide pin-to-pin paths via one or several buses, enable several pins to be connected to a single bus, enable several buses to be connected to a single pin, and/or enable any analog I/O pin to be connected to any analog block (**110-0** to **-n**).

An analog routing fabric **108** may be programmed (and reprogrammed) according to analog routing data. As will be described below, in contrast to
20 conventional approaches, such analog routing data may be provided from any of a number of different sources, rather than only from an on-board processor. In a particular embodiment, an analog routing fabric **108** may include multiple buses that may be connected to one another by connection circuits based on analog
25 routing data.

Analog blocks (**110-0** to **-n**) may include analog circuits that execute analog circuit functions. Analog blocks (**110-0** to **-n**) may be connected to I/O pins (e.g., **102**) and/or to one another by analog routing fabric **108**. Selected or all of analog blocks (**110-0** to **-n**) may also receive and/or output digital data to digital section
30 **106**. Analog blocks (**110-0** to **-n**) may include various analog circuits, including but not limited to capacitance sense circuits, comparators, analog-to-digital-converters (ADCs) (including "sigma-delta" types and/or successive approximation types), filters (including low pass filters), switched capacitor type circuits, and/or

digital-to-analog converters (DACs) (including both current and/or voltage DACs).

It is understood that all or a portion of analog routing fabric **108** may be configured dynamically (changed during the operation of a device **100**) or statically (maintained substantially the same throughout the operation of device **100**).

In the embodiment shown, a digital section **106** may include a processor section **112**, a direct memory access (DMA) circuit **114**, an analog interface I/F circuit **116**, a data transfer hub circuit **118**, a programmable reference generator **120**, programmable digital section **122**, and a digital system interconnect (DSI) **124**. A processor section **112** may include one or more processors that may execute predetermined instructions. A processor section **112** may one source for providing analog routing data for configuring analog routing fabric **108**.

A DMA circuit **114** may enable transfers of data between device **100** and other devices without direct control of processor section **112**. A DMA **114** may also be a source of analog routing data for configuring analog routing fabric **108**. This is in sharp contrast to conventional approaches that limit programmability of a routing fabric to data issued from a processor, or the like. While the embodiment of FIG. 1 shows a DMA circuit **114**, other embodiments may include different types of data transfer circuits that may serve as a source of analog routing data independent of a processor section **112**.

An analog I/F circuit **116** may receive analog signals, and convert them to a digital domain. An analog I/F circuit **116** may be a further source of analog routing data for configuring analog routing fabric **108**.

A data transfer hub circuit **118** may provide a data transfer path between a processor section **112** and devices external to device **100**, as well as locations within device **100**. As but a few of the many possible examples, a data transfer hub **118** may enable data transfers to one or more interfaces for communicating with external devices, including one or more external memory interfaces, one or more serial data transfer interfaces, and/or one or more I/Os (e.g., **102**). Data transfer hub **118** may also transfer data between on board (i.e., circuits of the same device) sections, including internal memory circuits, interrupt control circuits, power management circuits, timing circuits, analog interface circuit **116**, programmable digital section **122** and/or DSI **124**.

A programmable reference generator **120** may generate reference currents and/or voltages that may be used in analog section **104**. Such programmed currents/voltages may also be provided as output values from device **100**.

5 A programmable digital section **120** may provide programmable logic circuits that may be configured into various digital functions based on digital configuration data. In very particular embodiments, a programmable digital section **120** may include programmable logic device blocks with programmable functions, and programmable interconnections. Programmable digital section **120** may be yet another source of analog routing data for configuring analog routing
10 fabric **108**.

A DSI **124** may enable interconnections between various parts of the digital section **106**, and in addition may provide digital connections to analog section **104**. More particularly, DSI **124** may provide analog routing data, or signals generated from such routing data, to dynamically configure analog routing fabric
15 **108**. In very particular embodiments, a DSI **124** may enable analog routing fabric **108** to be configured from any of: processor section **112**, direct access circuit **114**, analog I/F circuit **116** and/or programmable digital section **122**. Though not shown in FIG. 1, a DSI **124** may also provide connections to fixed digital function blocks.

20 In this way, an integrated circuit may include analog circuit blocks connected to I/O pins with an analog routing fabric reconfigurable according to analog routing data from various sources in addition to a processor.

Referring now to FIG. 2, an integrated circuit device according to a further embodiment is shown in a block diagram and designated by the general reference
25 character **200**. The device of FIG. 2 may be one implementation of that shown in FIG. 1.

In the embodiment of FIG. 2, pins may include general purpose I/O (GPIO) pins (one set shown as **202-0**), special I/O pins (SIO) (one set shown as **202-1**), and direct connection pins (three sets shown as **202-2/3/4**).

30 GPIO pins **202-0** may be connected to corresponding GPIO configuration circuits (one shown as **226**). GPIO configuration circuits (e.g., **226**) may enable a GPIO pin to be connected to an analog interconnect **230** and/or a DSI **224**. Accordingly, when connected to analog interconnect **230**, a GPIO pin (e.g., **202-0**)

may serve as an analog input and/or output. Conversely, when connected to DSI **224**, a GPIO pin (e.g., **202-0**) may serve as a digital input and/or output. A GPIO configuration circuit (e.g., **226**) may also provide different types of connections to analog interconnect **230**. In particular, a GPIO pin may be connected one or more
5 different buses of an analog interconnect **230**.

SIO pins (e.g., **202-1**) may be connected to SIO configuration circuits (e.g., **226**). SIO configuration circuits (e.g., **228**) may enable an SIO pin to be connected to DSI **224**. Accordingly, SIO pins (e.g., **202-1**) may be programmable as a digital input and/or output. However, such pins (e.g., **202-1**) may not serve
10 as an analog I/O.

Direct connection pins (e.g., **202-2/3/4**) may have a direct connection to particular circuit sections of device **200**. Set **202-2** may only provide connections to one particular interface circuit. In contrast, set **202-3** may provide a direct connection to a digital circuit, as well as a GPIO configuration circuit (e.g., **226**),
15 while set **202-4** may provide a direct connection to an analog circuit block, as well as a GPIO configuration circuit (e.g., **226**).

Referring still to FIG. 2, an analog block group **210** in combination with GPIO configuration circuits (e.g., **226**) and analog interconnect **230** may form an analog routing fabric. Analog block groups **210** may include a number of analog
20 blocks (ALOG BLK0 to n) which may be connected to GPIOs through analog interconnect **230** and GPIO configuration circuits (e.g., **226**), and to one another through analog interconnect **230**. Analog blocks (ALOG BLK0 to n) may take the form of those shown as **110-0** to -n, or equivalents.

Analog interconnect **230** may include a number of buses and connection
25 circuits to enable reconfigurable interconnection between GPIO configuration circuits (e.g., **226**) and analog block group **210**. In a particular embodiment, analog interconnect **230** may include: global buses that may enable signal paths to be created between GPIOs and any or all of analog blocks (ALOG BLK0 to n), local buses that may enable signal paths to be created between any or all of
30 analog blocks (ALOG BLK0 to n), and multiplexer buses that may enable one bus to connect multiple GPIOs to any or all of analog blocks (ALOG BLK0 to n).

In FIG. 2, a digital section **206** may include a memory system **232**, a processor system **234**, a program and test system **236**, and a digital system **238**.

A memory system **232** may include a memory I/F **242** and one or more memories (MEM0 to -i). A memory I/F **242** may enable external access to memory devices by device **100**. Memories (MEM0 to -i) may include various types of memories, including but not limited to a static random access memory (SRAM), nonvolatile memory (including EEPROMs, and flash EEPROM). Such memories (MEM0 to -i) may be directly accessible by processor system **234**.

A processor system **234** may include a processor **212** as well as peripheral access system **240**. A processor **212** may include one or more processors as well as corresponding circuits such as memory controller (including cache controllers) and an interrupt control circuit. A peripheral access system **240** may include circuits such as a direct access circuit, like that shown as **114** in FIG. 1 and/or a data transfer hub circuit, like that shown as **118**, or equivalents.

A program and test system **236** may include circuits that enable data to be loaded into memory system **232** (program data for execution by processor system **234**), as well as test circuits for providing test data to and test result data from a device **200**.

Memory system **232** and processor system **234** may be connected to a system bus **244**. A system bus **244** may also be connected to analog block group **210**.

A digital system **238** may include programmable digital section **222** as well as a number of fixed function digital blocks (FIXED BLK0 to -j). Programmable digital section **222** may be like that shown as **122** in FIG. 1, or an equivalent. Fixed function digital blocks (FIXED BLK0 to -j) may provide predetermined digital functions for device. Fixed function digital blocks (FIXED BLK0 to -j) may include any suitable digital circuit, including but not limited to timer circuits, counter circuits, digital modulation circuits, serial interface circuits, and/or network interface circuits. In the particular embodiment shown, digital system **238** may be connected to a fixed interface circuit **246**, which may be a physical layer (PHY) interface circuit.

A DSI **224** may provide digital connection between various sections of the digital system **238** and/or connections to suitably configured GPIO pins (e.g., **202-0**) or SIO pins (e.g., **202-1**).

In the particular embodiment shown, a device may also include system

resources **248**. System resources **248** may include a clock system **250** and a power management system **250**. A clock system **250** may provide timing signals to various portions of a device **200** based on one or more clock generation circuits and/or one or more received timing signals. A power management system **250**
5 may provide power supply voltages and regulation to various portions of device **200**. A power management **250** may selectively disable portions of the device for low power (i.e., sleep) modes of operation.

In this way, an integrated circuit may include I/Os programmable to connect to one or more buses of an analog interconnect to enable connections between
10 I/Os and/or to analog blocks.

Referring now to FIG. 3, an integrated circuit device configuration architecture according to an embodiment is shown in a block schematic diagram and designated by the general reference character **300**.

Architecture **300** shows programmable digital section **322**, fixed function
15 digital blocks **354-0/1**, processor system **334** and peripheral access system **340** connected to a DSI **324**. A DSI **324** may provide digital signal paths between various circuits connected to it. In one very particular embodiment, such a connection may be configurable through programmable digital section **322**.

DSI **324** may also be connected to analog route configuration circuit **356**.
20 Analog route configuration circuit **356** may provide configuration values to analog routing fabric **308** to enable reconfigurable connections between GPIOs **302-0** and analog blocks **310-0/1**. In one embodiment, analog route configuration circuit **356** may be accessible via any of the other circuit blocks connected to DSI **324**, enabling analog routing configuration via multiple sources. In a very particular
25 embodiment, analog route configuration circuit **356** may include, or be the output of, configuration registers that may be written to contain analog routing data. Such analog routing data may be updated to dynamically change an analog routing configuration.

In the particular embodiment of FIG. 3, analog routing fabric **308** is
30 represented by various connection elements **360** controlled by analog route configuration circuit **356**. Connection elements **360** may provide connections between buses (not shown), GPIOs **302-0**, and analog blocks **310-0/1**. In particular embodiments, connection circuit elements **360** may be controlled in

groups as connection circuits. Such connection circuits may have a switch configuration, allowing any number of connection elements of a group to be enabled in response to analog routing data. Alternatively, connection circuits may have a multiplexer (MUX) configuration, allowing only one connection element to be enabled in the group at one time. It is understood that FIG. 3 shows but two analog blocks **310-0/1** and two GPIOs **302-0** for illustration purposes. A device **300** may include additional blocks and connections as shown in the other embodiments described herein, and equivalents.

FIG. 3 also shows a GPIO configuration circuit **326** and SIO configuration circuit **328**. A GPIO configuration circuit **326** may provide a digital input and/or output path to DSI **324**, as well as one or more connections (only one shown) as part of the analog routing fabric **308**. In contrast, SIO configuration circuit **328** may provide only a digital connection to DSI **324**.

In this way, an integrated circuit device may include an analog routing fabric controlled by an analog route configuration circuit connected to any one of a number of digital blocks by a configurable digital system interconnect.

Referring now to FIG. 4, an integrated circuit device configuration architecture according to a further embodiment is shown in a block schematic diagram and designated by the general reference character **400**. FIG. 4 includes many of the same items as FIG. 3, thus a description of such items will be omitted.

FIG. 4 differs from FIG. 3 in that switch voltage generator circuits **460-0** to $-i$ may be included to generate switch voltages V_{sw0} to V_{swi} that may be outside of a power supply voltage received by an integrated circuit **400**. For example, a switch voltage (V_{sw0} and/or V_{swi}) may be higher than a high power supply voltage or lower than a low power supply voltage. Switch voltage generator circuits (**460-0** to $-i$) may receive configuration values from DSI **324**. Consequently, switch voltage generator circuits (**460-0** to $-i$) may be configured (and reconfigured) in substantially the same manner as analog routing fabric **308** (e.g., multiple sources). In one particular embodiment, voltage generator circuits **460-0** to $-i$ may be charge pump circuits.

In the embodiment shown, a switch voltage (V_{sw0} and/or V_{swi}) may be applied to connection elements **360** by switch activation circuits **458-0/1** according

to configuration values received from analog route configuration circuit **356**.

In this way, an integrated circuit device may include a programmable analog routing fabric having connection elements operated by voltages levels outside the range of received power supply voltages.

5 As noted above, in some embodiments, I/O pins may be selectively connected to one or more buses of an analog routing fabric to enable analog signal paths between such I/O pins and one or more analog blocks. Particular I/O connection circuits according to one embodiment will now be described with reference to FIG. 5.

10 Referring to FIG. 5, I/O connection circuits according to an embodiment are shown in a block schematic diagram and designated by the general reference character **500**. I/O connection circuits **500** may form part of a programmable analog routing fabric of embodiments shown herein.

I/O connection circuits **500** may include a number of I/O pins **502-0** to **-k**,
15 I/O connection circuits **562-0** to **-k**, analog MUX buses (AMXBUS0/1) **564-0/1**, a number of global buses **566-0** to **-h**, an analog block connection circuit **568**, an analog block **510**, and an analog routing signal source **572**.

I/O connection circuits (**562-0** to **-k**) may receive first analog routing data **574-0** and second routing data **574-1**, and in response, connect a corresponding
20 I/O pin (**502-0** to **-k**) to AMXBUS0 **564-0** and/or a corresponding global bus (**566-0** to **-h**). I/O connection circuits (**562-0** to **-k**) may operate in a switch or MUX like fashion as noted above. It is understood that each I/O connection circuit (**562-0** to **-k**) may connect its corresponding I/O pin (**502-0** to **-k**) to other global buses not shown.

25 Referring still to FIG. 5, an analog block connection circuit **568** may connect any of AMXBUS0/1 **564-0/1** to analog block **510** based on third analog routing data **574-2**.

A routing value source **572** may provide routing data to dynamically reconfigure connections between I/Os and buses. In the particular embodiment of
30 FIG. 5, a routing value source **572** may include any of: a programmable digital section **522**, a direct access circuit **514**, or a processor section **512** that provide routing data by way of a DSI **524**. It is understood that routing data **574-0/1/2** may be dynamic, changing over time according to operations of a device.

In this way, any of multiple I/O pins may be selectively connected to global buses and/or an analog MUX bus, where the analog MUX bus provides a path to one or more analog blocks.

Referring to FIG. 6, I/O connection circuits according to another
5 embodiment are shown in a block schematic diagram and designated by the general reference character **600**. I/O connection circuits **600** may form part of a programmable analog routing fabric of embodiments shown herein, and may be used in combination with those shown in FIG. 5. FIG. 6 includes many of the same items as FIG. 5, thus a description of such items will be omitted.

10 FIG. 6 may differ from FIG. 5 in that a global bus connection circuit **676** may connect any of global buses (**566-0** to **-h**) to analog block **510** based on fourth analog routing data **574-2**.

In this way, I/O pins may be connected to global buses, any of which may be selectively connected to one or more analog blocks.

15 As noted in embodiments above, a GPIO pin may serve as an analog I/O or a digital I/O. One very particular GPIO configuration circuit such a function is shown in FIG. 7.

Referring to FIG. 7, a GPIO configuration circuit according to one embodiment is shown in a block schematic diagram, and designated by the
20 general reference character **700**. A GPIO configuration circuit **700** may be one example of that shown as **226** in FIG. 2.

A GPIO configuration circuit **700** may include a digital input path **778**, a digital output path **780**, an analog path **782**, and an auxiliary function path **784**. A digital path **778** may include an input driver **786** having an input coupled to GPIO
25 pin **702** and an output that provides a digital system input signal. In one embodiment, such a digital input signal may be provided to a DSI (not shown). Input driver **786** may be controlled by digital control signals (DIG. CTRL). An output of input driver **786** may also be connected to interrupt logic **788** which may generate interrupts (INTRUPTS) for other circuits of the device.

30 A digital output path **780** may include an output driver **790** having an input that receives a digital system output signal. Such a digital output signal may be provided from a DSI. Output driver **790** may drive GPIO pin **702** in response to such a digital output signal. An output driver **790** may control a drive strength

and/or slew of an output signal in response to digital output control signal (DIG_OUT_CTRL). In response to a bi-directional control signal (BI-DIR_CTRL), digital output path **780** may be disabled (and digital input path **778** enabled).

An analog path **782** may include an I/O connection circuit **762** that may
5 selectively connect GPIO pin **702** to a global bus **766** and/or an analog MUX bus **764** in response to routing data **774** and output data from global control logic **792**. Global and analog MUX buses may take the form of any of those shown in other embodiments herein, and equivalents.

In the very particular embodiment shown, an auxiliary function path **784**
10 may drive a GPIO **702** with a generated bias voltage VBIAS based on a digital output signal. In a very particular embodiment, an auxiliary function path **784** may be a liquid crystal display (LCD) bus, for driving LCD elements.

Having described various embodiments with programmable analog routing fabrics, an analog routing fabric according to one very particular embodiment is
15 shown in a block schematic diagram in FIG. 8, and designated by the general reference character **808**.

FIG. 8 shows a routing fabric **808** that may connect GPIO pins (one shown as **802**) to any of analog blocks (**810-00** to **810-1n**) by way of analog MUX (AMUX) buses **864-0/1**, global buses **866-0/1** and/or local buses **896-0/1**. Routing
20 fabric **808** may be conceptualized as having a left and right side, with a left side including one left AMUX bus **864-0**, eight left global buses (0-7) **866-0**, and four left local buses (**896-0**). A right side may include one right AMUX bus **864-1**, eight right global buses (0-7) **866-1**, and four right local buses (**896-1**).

Programmable connections between the various buses, GPIO pins, and
25 analog blocks are shown by circles (one shown as **885**). Each programmable connection may be dynamically enabled or disabled in response to analog routing data to configure a routing fabric for desired analog functions. In some embodiments, programmable connections may vary in impedance, with some having a lower on impedance than others. In particular, connections to
30 impedance sensitive analog blocks may have a lower impedance value than other connections.

Connections surrounded by dashed lines may denote a connection group. A connection group may operate in a switch mode (any of the connections can be

enabled) and/or MUX mode (only one connection enabled), as noted above.

Connection groups may take various forms including but not limited to: I/O connection groups (one shown as **894**) that may connect a corresponding GPIO pin to global buses and/or an AMUX bus; reference connection groups (one
5 shown as **898**), that may connect reference voltages and currents to one or more buses or analog blocks, power supply connection groups (one shown as **891**) that may connect power supply voltages to one or more buses; block connection groups (one shown as **887**) that may connect an analog block to any of multiple buses. It is noted that the embodiment of FIG. 8 shows connection blocks with
10 connections to substantially all available buses. As will be shown below, in particular embodiments, connection may be provided to only selected buses.

Programmable connections may also include any of: individual reference connections (one shown as **897**) that may provide a single reference voltage (or current) to a bus or analog block; AMUX joining connections (one shown as **895**)
15 that may connect one AMUX bus to another; global joining connections (one shown as **893**) that may connect a left hand side global bus to a corresponding right hand side global bus; and local joining connections (one shown as **889**) that may a left hand side local bus to a corresponding right hand side local bus.

Referring still to FIG. 8, AMUX buses **864-0/1** may enable any of GPIO pins
20 (e.g., **802**) to be connected to any of analog blocks (**810-00** to **-1n**). Global buses **866-0/1** may connect selected GPIOs to analog blocks (**810-00** to **-1n**). Local buses **896-0/1** may enable analog blocks (**810-00** to **-1n**) to be connected to one another.

In some embodiments, selected or all buses **864-0/1**, **866-0/1**, **896-0/1** may
25 be shielded, to limit signal coupling between buses (and other signal lines). Shielding may include forming a shielding conductor adjacent to such bus lines, a maintaining the shielding conductor at a potential that limits signal coupling, or any other suitable shielding techniques. In a very particular embodiment, local buses **896-0/1** and global buses **866-0/1** may be shielded.

In this way, an analog routing fabric may include: analog MUX buses that
30 may dynamically connect multiple GPIOs to one or more analog blocks, unified global buses that may connect selected GPIOs to analog blocks, and local buses that may connect analog blocks to one another.

Having described embodiments with analog blocks connected to buses of a switching fabric, very particular examples of analog block connections will now be described.

Referring to FIG. 9A, an example of an analog block connection is shown in a block schematic diagram and designated by the general reference character **985-A**. An analog block **910-A** may be a filter block having two filters, one filter may have an input (in0) connectable to a left AMUX bus **964-0** and/or left global bus 0 by a connection group **987-A**. A corresponding output (out0) may be connected to a local bus 0. A second filter may have similar connections to corresponding right hand side buses.

Referring to FIG. 9B, another example of an analog block connection is shown in a block schematic diagram and designated by the general reference character **985-B**. An analog block **910-B** may be a comparator block having four comparators, each having a "+" input and a "-" input. Such inputs may be connected to selected buses and/or reference voltages by connection groups (one shown as **987-B**). In the embodiment shown, comparator block **910-B** may provide comparator results (cmp_results) as digital data. In a particular embodiment, a digital data may be provided to a DSI (not shown).

Referring to FIG. 9C, another example of an analog block connection is shown in a block schematic diagram and designated by the general reference character **985-C**. An analog block **910-C** may be a capacitance sense block having two sense circuits, each having an output (out), an reference input (ref), and a signal input (in). In the embodiment shown, outputs (out) may have a "hard" (i.e., nonprogrammable) connection **985** to AMUX buses **964-0/1**. In addition, another analog block (in this example a DAC block **910-x**), may selectively provide a reference value to a reference input through connection group **987-C**.

FIG. 9D shows an analog block connection for a switched capacitor / continuous time analog circuit block **985-D**. Connections are understood from the above descriptions.

FIG. 9E shows an analog block connection for a voltage or current DAC (VIDAC) block **985-E**. VIDAC block **985-E** shows an arrangement in which outputs (v0, v1) from the analog block **910-E** may be provided as inputs to other analog blocks (**910-z0/1**). A VIDAC block **985-E** may receive input digital values

(DIG_IN) for conversion. In particular embodiments, such digital values may be received from a DSI. FIG. 9E also shows an arrangement in which GPIOs (one shown as **902**) may be connected to an analog block **910-E** by an I/O connection **981**, rather than by buses. Further in the embodiment shown, VIDAC **985-E** may
5 only have connections to left side buses.

FIG. 9F shows an analog block connection for a delta-signal modulation ADC (DSM) block **985-F**. Connections are understood from the above descriptions. A DSM block **985-F** may output digital data (VALUE) reflecting conversion results. In a particular embodiment, a digital conversion results may
10 be provided to a DSI (not shown).

FIG. 9G shows an analog block connection for an operational amplifier (op amp) block **985-G**. Connections are understood from the above descriptions. FIG. 9G shows an arrangement in which analog block **985-G** may have inputs (+,-) connected to lines of local buses **964-0**, lines of global buses **966-0**, or a
15 reference value (V0). However, in addition, such inputs may also be connected to GPIO pins (one shown as **902-0G**) by I/O connection (one shown as **981**). Further, a negative feedback path between an (-) input and an output of each op amp may be enabled by a circuit connection (one shown as **979**). Still further, op amp outputs may also have a direct connection to certain GPIO pins (one shown
20 as **902-1G**).

FIG. 9H shows an analog block connection for a successive approximation (SAR) ADC block **985-H**. Connections and digital output values are understood from the above descriptions.

Having described programmable analog routing fabrics and analog block
25 connections to such fabrics, methods of providing connection paths according to very particular embodiments will now be described. In the below figures, solid circles designate enabled connections to buses.

Referring to FIG. 10A, two of numerous signal routes that may be formed in analog routing fabric **808** of FIG. 8 are shown by bold lines. Route **1077-0** shows
30 how different GPIO pins **1002-2** and **1002-3** may be connected to one another by a single bus, which in the example shown is left AMUX bus **864-0**. Route **1077-1** shows how different GPIO pins **1002-0** and **1002-1** may be connected to one another by a multiple different buses, which in the example shown, includes right

global bus "7", left global bus "7", and left global bus "3".

Referring to FIG. 10B, more signal routes that may be formed in analog routing fabric **808** of FIG. 8 are shown by bold lines. Routes **1077-2** to **-4** shows how different GPIO pins **1002-4**, **-5**, **-6** may be connected to a same bus, which in the example is right global bus "7". FIG. 10B also shows how a single GPIO pin **1002-7** may be connected to multiple buses, which in this example are left global buses 4-7.

Referring to FIG. 10C, additional examples of possible signal routes in an analog routing fabric **808'** like that of FIG. 8 are shown by bold lines. FIG. 10C shows how GPIO pins **1002-8** to **-10** may all be connected to a same analog block **810-00** at different signal points. In particular, GPIO pin **1002-8** may be connected by right and left AMUX buses **864-0/1**, GPIO pin **1002-10** may be connected by left global bus "0", and GPIO pin **1002-9** may be connected by right global bus "6" and left global bus "6".

FIG. 10C also shows how local buses may be utilized to connect analog blocks together. In the particular embodiment shown, analog blocks **810-1n** and **810-10** may be connected together by right local bus "2", and analog block **810-10** and **810-0n** may be connected together by left local bus "3" and right local bus "3".

Referring now to FIG. 10D, still further examples of possible signal routes in an analog routing fabric **808** like that of FIG. 8 are shown by bold lines. FIG. 10D shows how multiple GPIO pins **1002-11** to **-14** may each be connected to different analog blocks. In particular, GPIO pins **1002-11** to **-14** may be connected to analog blocks **810-00**, **-0n**, **-10** and **-1n**, respectively.

FIG. 10D also shows how multiple GPIO pins **1002-15** to **-17** may each be connected to a same analog block input or output. In particular, GPIO pins **1002-15** to **-17** may all be connected to a same I/O of analog blocks **810-00**.

As noted above, according to some embodiments, GPIO pins may have particular connections to buses. GPIO bus connections according to one particular embodiment are shown in FIG. 11.

Referring to FIG. 11, a portion of an analog routing fabric like that of FIG. 8 is shown in schematic diagram and designated by the reference character **808**". FIG. 11 shows various GPIO pins **1102-0** to **-11** and possible connections to buses. In particular, FIG. 11 shows how all GPIO pins **1102-0** to **-11** may have a

connection to a same analog MUX bus **864-1**, and have connections to only selected global buses.

It should be appreciated that in the foregoing description of exemplary embodiments. Various features are sometimes grouped together in a single
5 embodiment, figure, or description thereof for the purpose of streamlining the disclosure aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less
10 than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description, with each claim standing on its own as a separate embodiment.

It is also understood that the embodiments of the invention may be
15 practiced in the absence of an element and/or step not specifically disclosed. That is, a feature of the invention may be elimination of an element.

Accordingly, while the various aspects of the particular embodiments set forth herein have been described in detail, the present invention could be subject to various changes, substitutions, and alterations without departing from the spirit
20 and scope of the invention.

IN THE CLAIMS

What is claimed is:

1. An integrated circuit device, comprising:
a dynamically or statically reconfigurable analog signal switching fabric
comprising
a plurality of global buses that are selectively connected to external pins by
pin connection circuits in response to analog routing data, and
a plurality of local buses that are selectively connected to analog blocks
and/or global buses by routing connection circuits in response to the analog routing
data; and
at least one processor circuit that executes predetermined operations in
response to instruction data.
2. The integrated circuit device of claim 1, wherein:
the pin connection circuits comprise switch circuits that selectively connect
one external pin to any of a plurality of global buses in response to the analog
routing data.
3. The integrated circuit device of claim 1, wherein:
the pin connection circuits comprise multiplexer circuits that selectively
connect one external pin to any one of a plurality of global buses in response to the
analog routing data.
4. The integrated circuit of claim 1, wherein:
the routing connection circuits comprise switch circuits that selectively
connect at least one analog block to any of the local buses and/or global buses in
response to the analog routing data.
5. The integrated circuit of claim 1, wherein:
the routing connection circuits include
first routing connection circuits that provide connections having a first
impedance, and

second routing connection circuits that provide connections having a second impedance less than the first impedance.

6. The integrated circuit of claim 1, wherein:
the local buses and global buses are shielded to reduce signal coupling therebetween.
7. The integrated circuit device of claim 1, wherein:
the reconfigurable analog signal switching fabric further includes
at least one multiplexer (MUX) bus selectively connected to any of the pins by the pin connection circuits and to at least one global and/or local bus by the routing connection circuits.
8. The integrated circuit device of claim 1, further including:
a programmable logic section comprising a plurality of digital programmable blocks; and
a digital system interconnect that provides the analog routing data from at least the programmable logic section or the at least one processor circuit.
9. The integrated circuit of claim 8, further including:
a direct access circuit coupled to transfer data between the integrated circuit and a source external to the integrated circuit; and
the digital system interconnect also provides the analog routing data from the direct access circuit.
10. An integrated circuit, comprising:
at least one processor circuit;
a plurality of analog circuit blocks; and
a dynamically or statically reconfigurable analog routing fabric that selectively interconnects the analog circuit blocks and input/output (I/O) pins in response to analog routing data from at least one routing data source in addition to the at least one processor circuit.

11. The integrated circuit device of claim 10, wherein:

the at least one other routing data source is selected from: a programmable digital logic section formed in the integrated circuit, and a direct access circuit that transfers data between the integrated circuit and a source external to the integrated circuit.

12. The integrated circuit device of claim 10, wherein:

the reconfigurable analog routing fabric includes connection circuits selected from: switch circuits that provide connections between single fabric points and any of multiple other fabric points, and multiplexer circuits that provide a single connection between a single fabric point and one of multiple other fabric points.

13. The integrated circuit device of claim 12, wherein:

at least one voltage generation circuit that generate at least one switch voltage outside a range of power supply voltages received by the integrated circuit, and provides the at least one switch voltage to at least one connection circuit.

14. The integrated circuit of claim 10, wherein:

the reconfigurable analog routing fabric includes
input/output (I/O) connection circuits corresponding to each of a plurality of I/O pins, each I/O connection circuit selectively connecting its I/O pin to at least one multiplexer (MUX) bus and/or at least one of a plurality of global buses; wherein
the global buses are connectable to the analog circuit blocks through the analog routing fabric.

15. The integrated circuit of claim 10, wherein:

the reconfigurable analog routing fabric includes
routing connection circuits, each corresponding to an analog circuit block, that selectively connects its analog circuit block to any of a plurality of local buses;
wherein
the local buses are connectable to input/output (I/O) pins through the analog routing fabric.

16. The integrated circuit of claim 10, wherein:

the analog circuit blocks include two selected from: an analog signal filter, a comparator, a capacitance sensing circuit, a switched capacitor circuit, an digital-to-analog converter, an analog-to-digital converter, and an operational amplifier.

17. A method, comprising:

in response to routing data, configuring a reconfigurable analog routing fabric on an integrated circuit to selectively enable connections between a plurality of input/output (I/O) pins and at least one of a plurality of global buses, and to selectively enable connections between at least one global bus and at least one of a plurality of analog circuit blocks of the integrated circuit; wherein

the routing data is dynamically or statically provided from digital circuits of the integrated circuit.

18. The method of claim 17, wherein:

the configuring further includes

selectively enabling connections between the plurality of I/O pins and a same multiplexer bus, and

selectively enabling connections between the multiplexer bus and at least one of the analog circuit blocks.

19. The method of claim 17, wherein:

the routing data may be provided from a processor of the integrated circuit and either of: programmable digital circuits of the integrated circuit, and a direct access circuit of the integrated circuit that transfers data between the integrated circuit and a location external to the integrated circuit.

20. The method of claim 17, wherein:

the configuring further includes

selectively enabling connections between a plurality of local buses and the analog circuit blocks to chain at least two analog circuit blocks together.

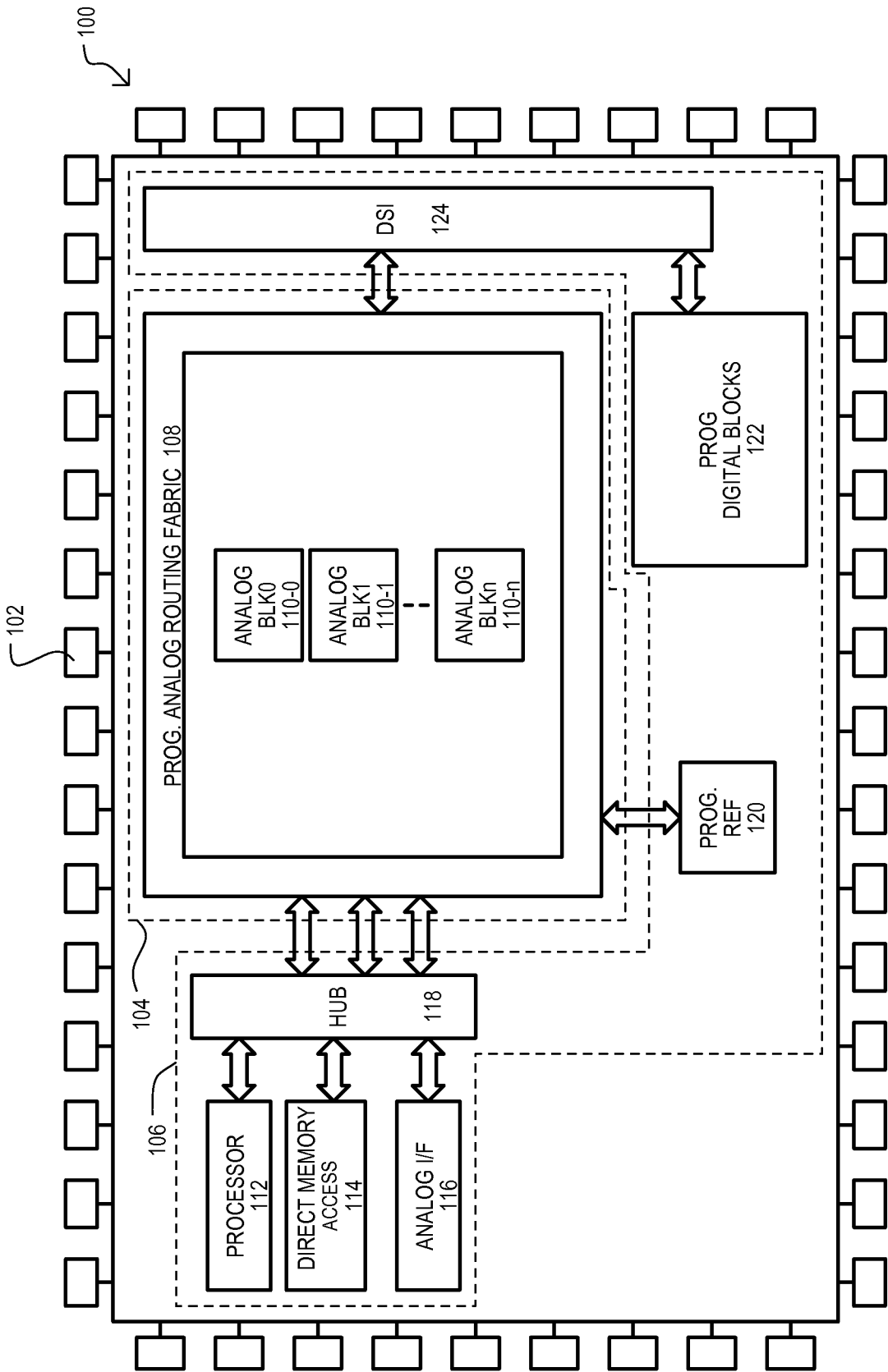


FIG. 1

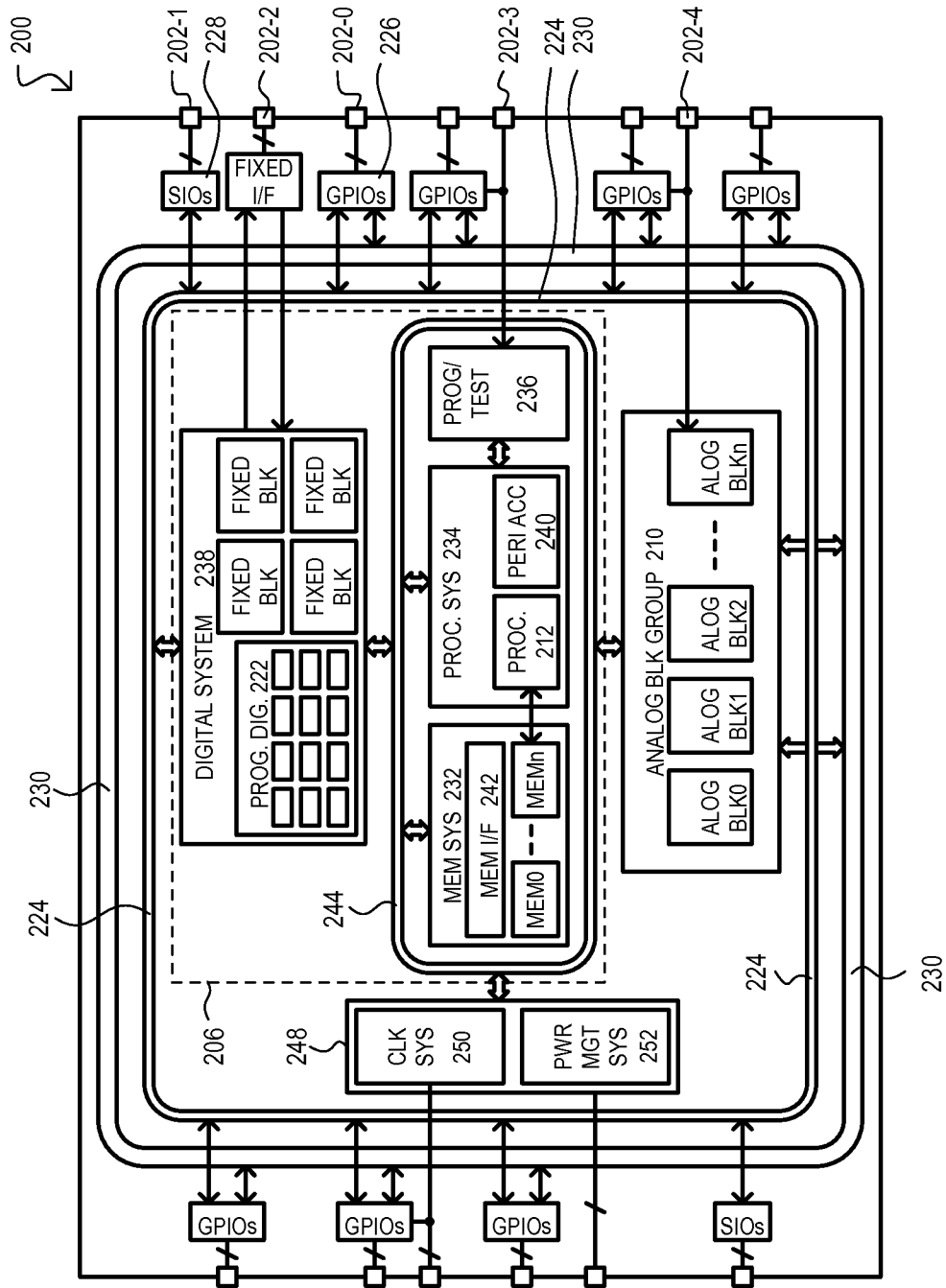


FIG. 2

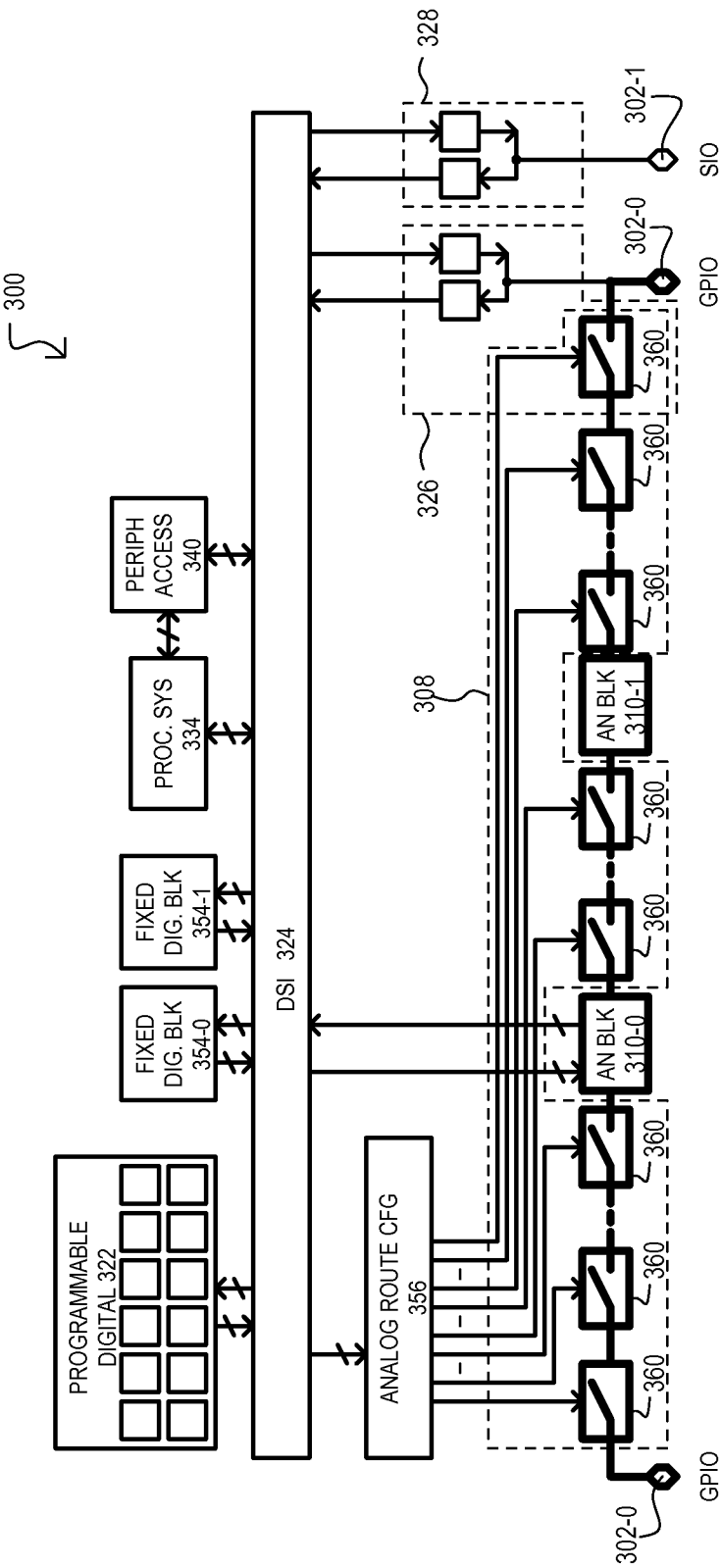


FIG. 3

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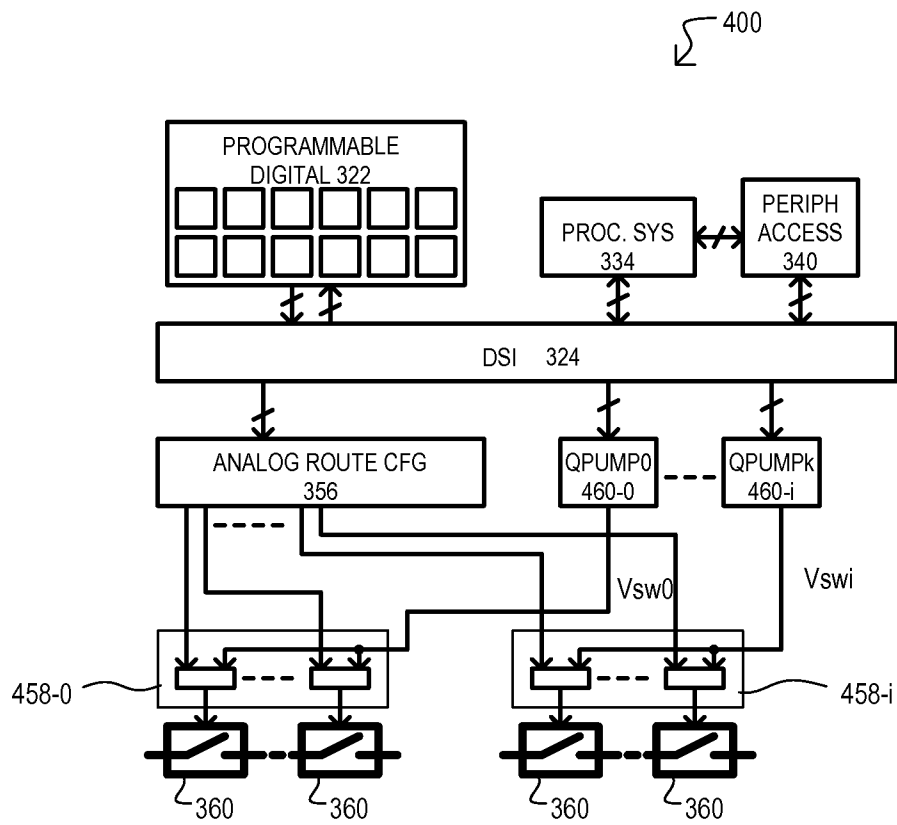


FIG. 4

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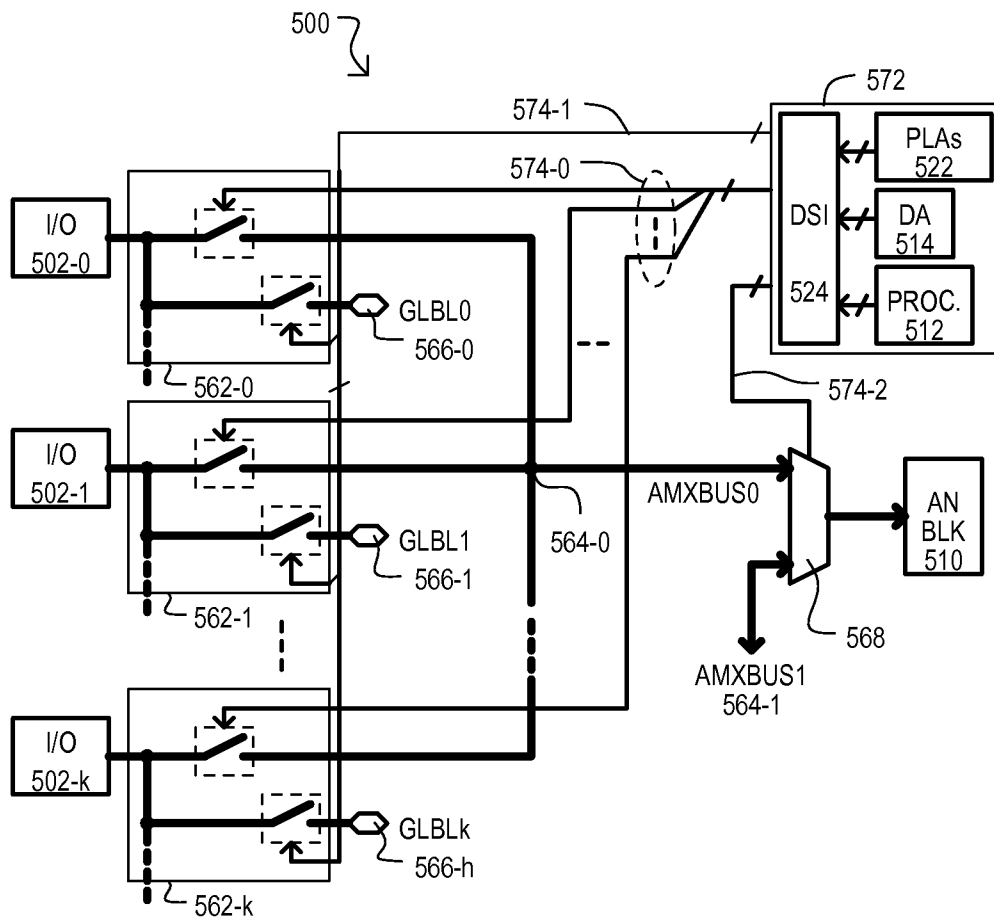


FIG. 5

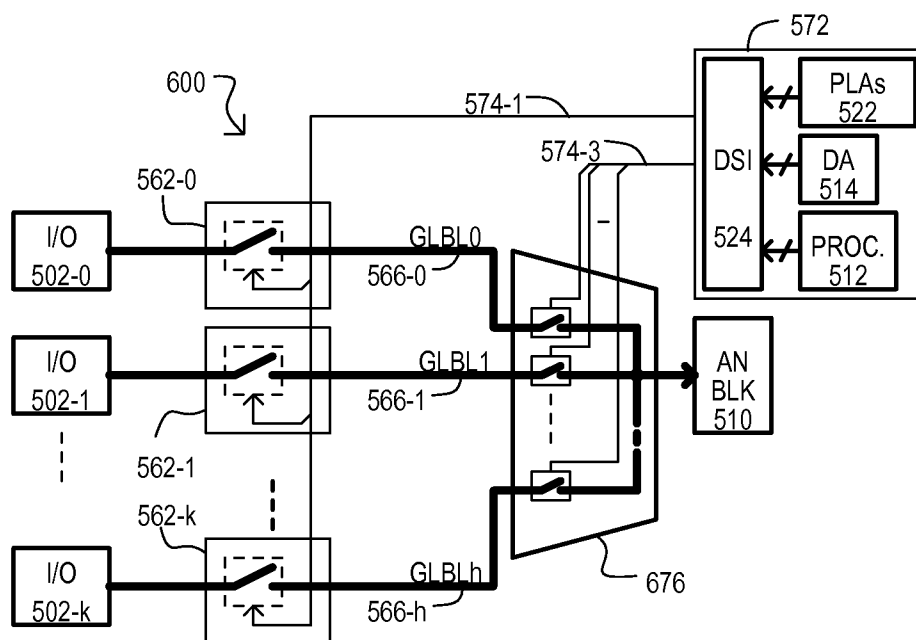


FIG. 6

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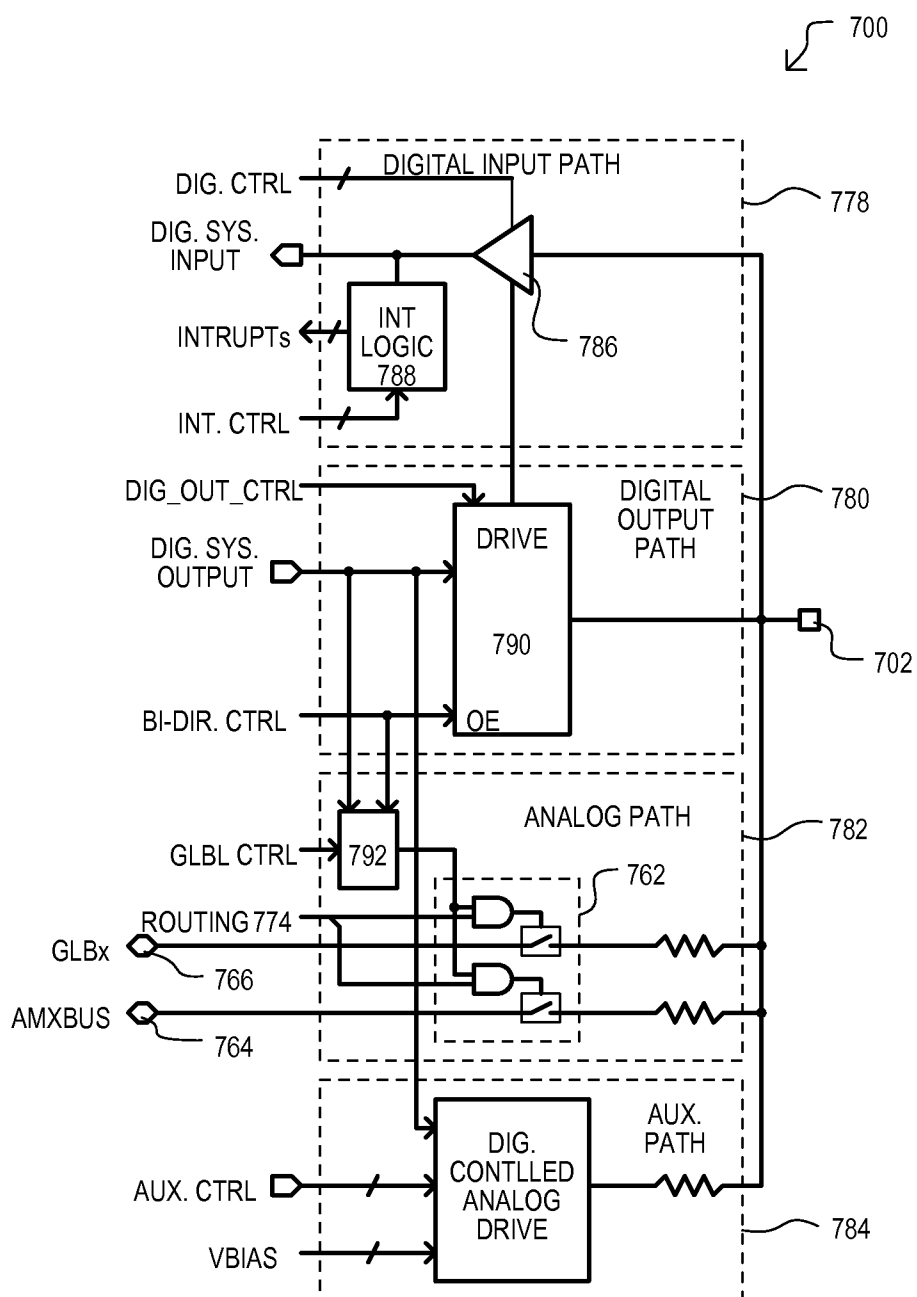


FIG. 7

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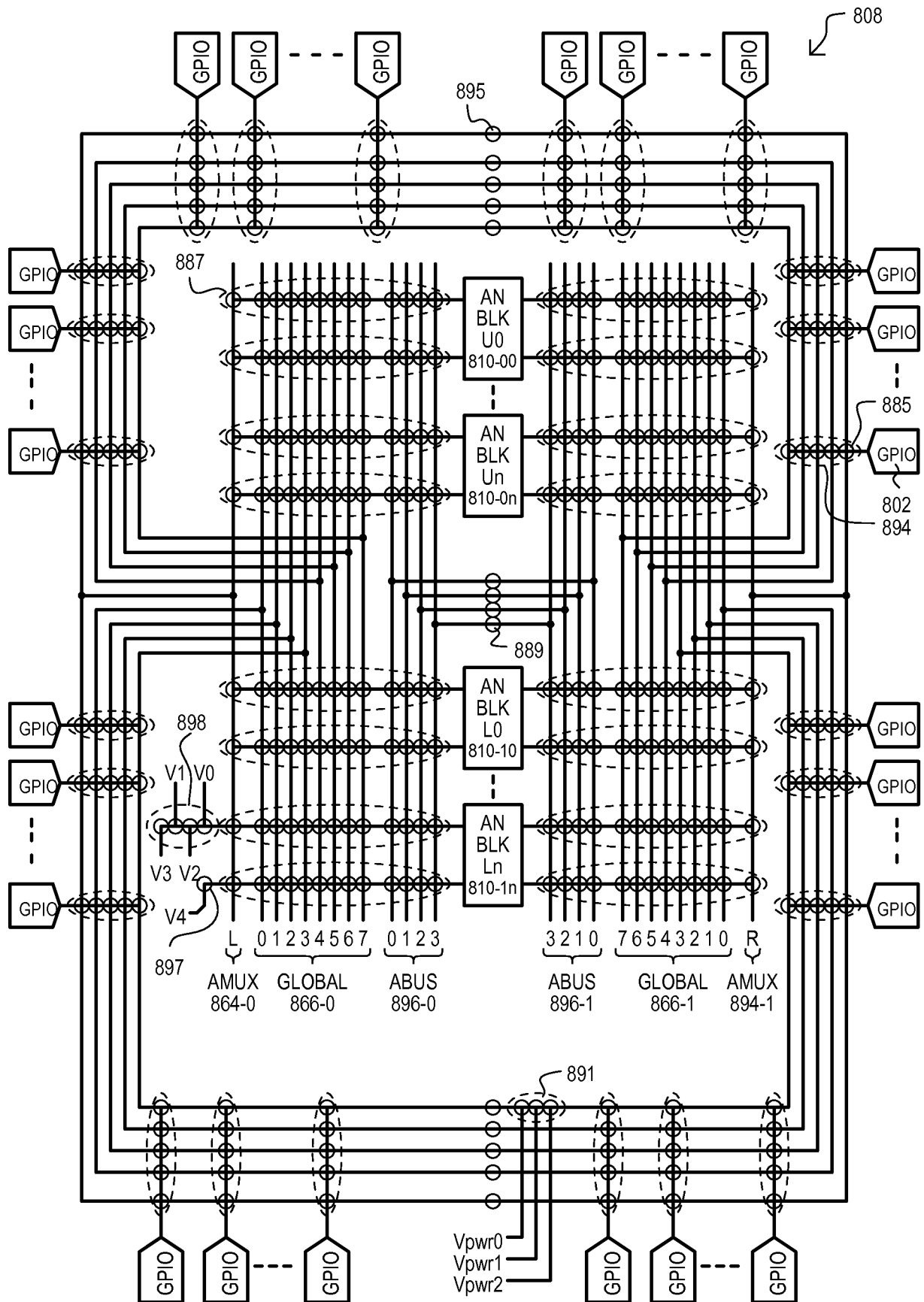


FIG. 8

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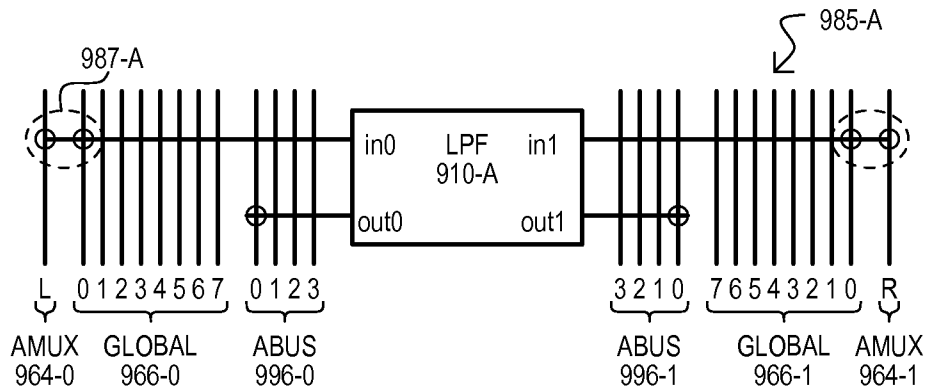


FIG. 9A

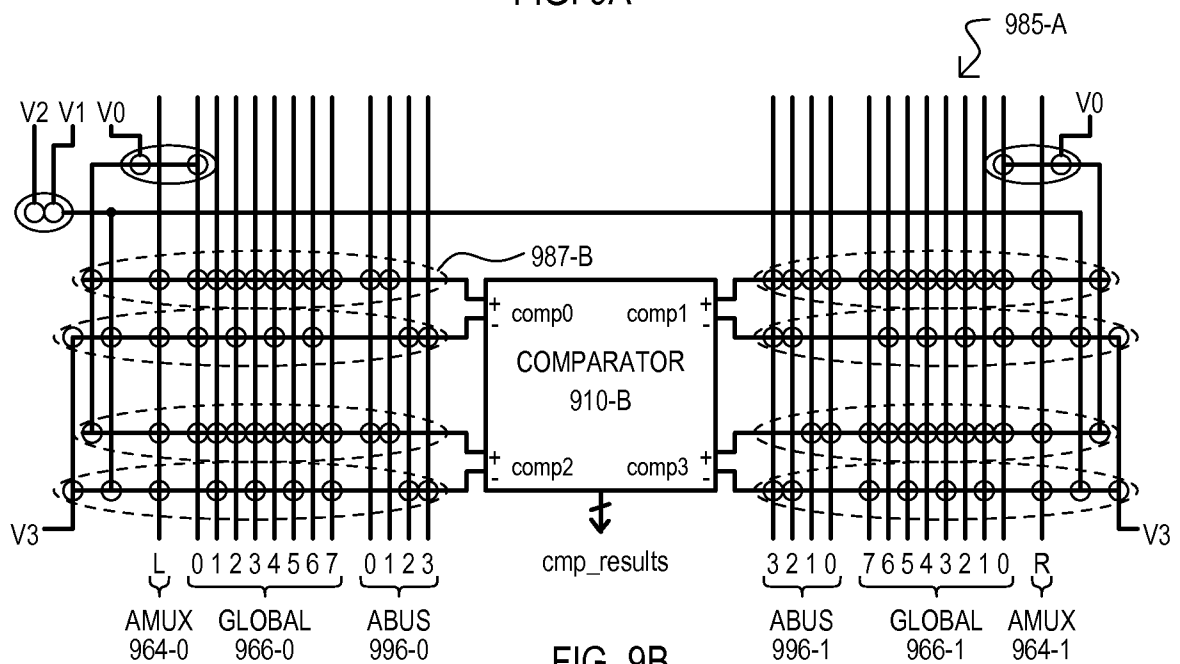


FIG. 9B

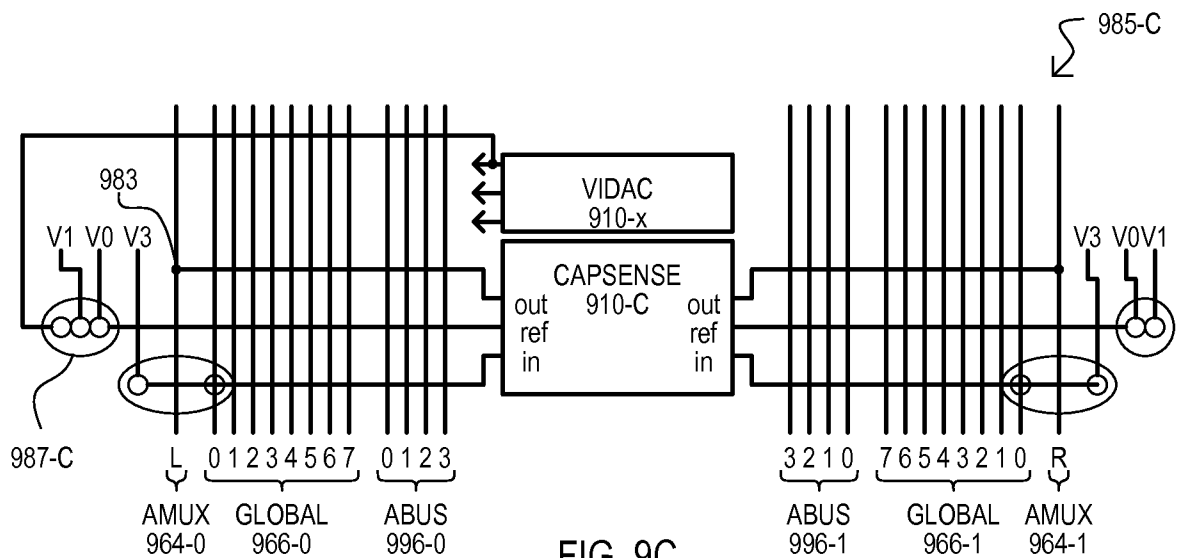
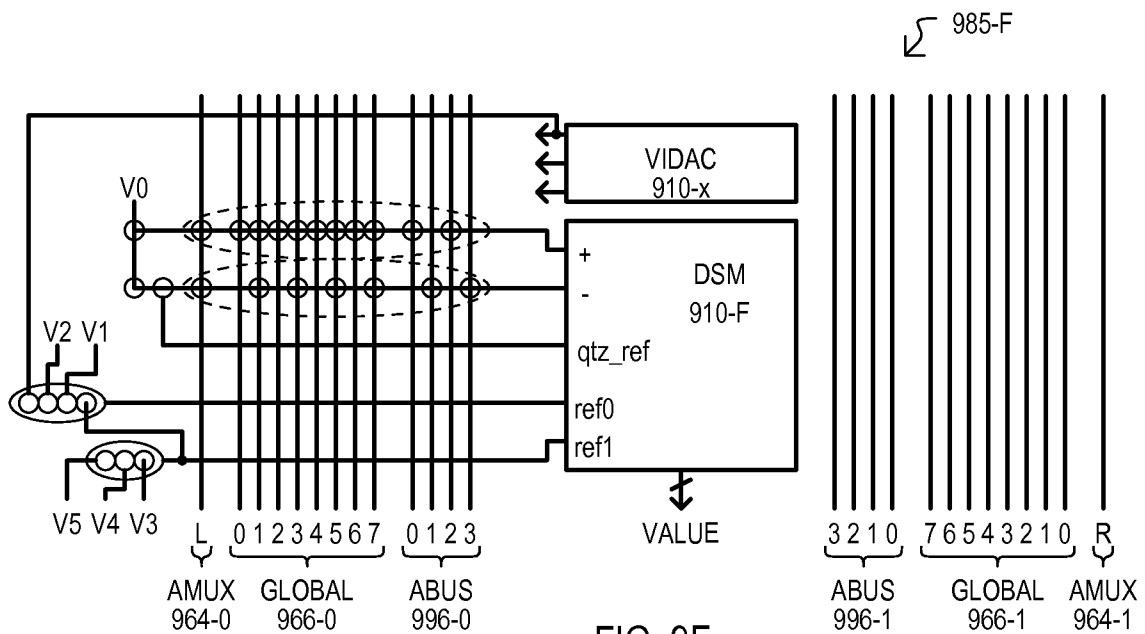
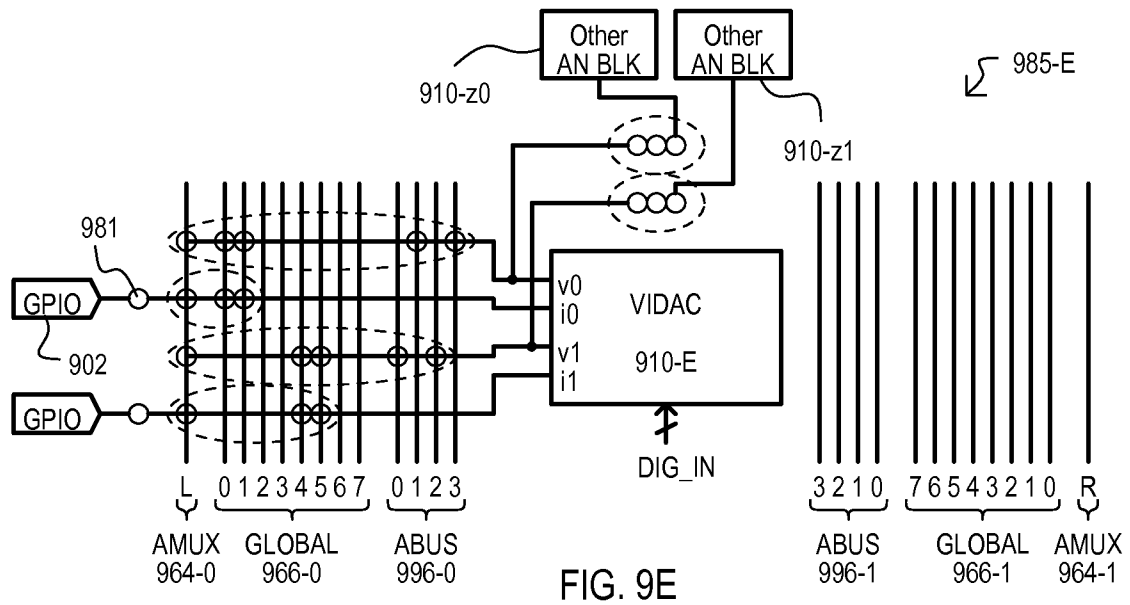
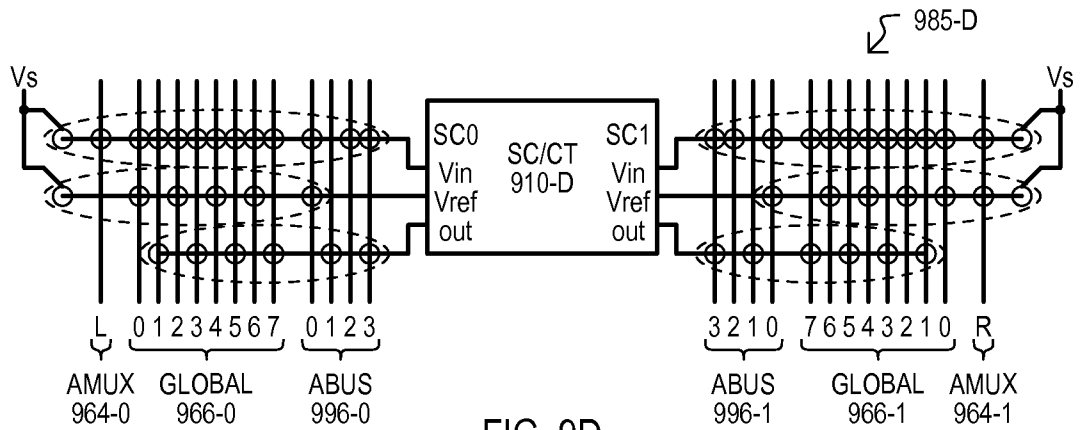


FIG. 9C

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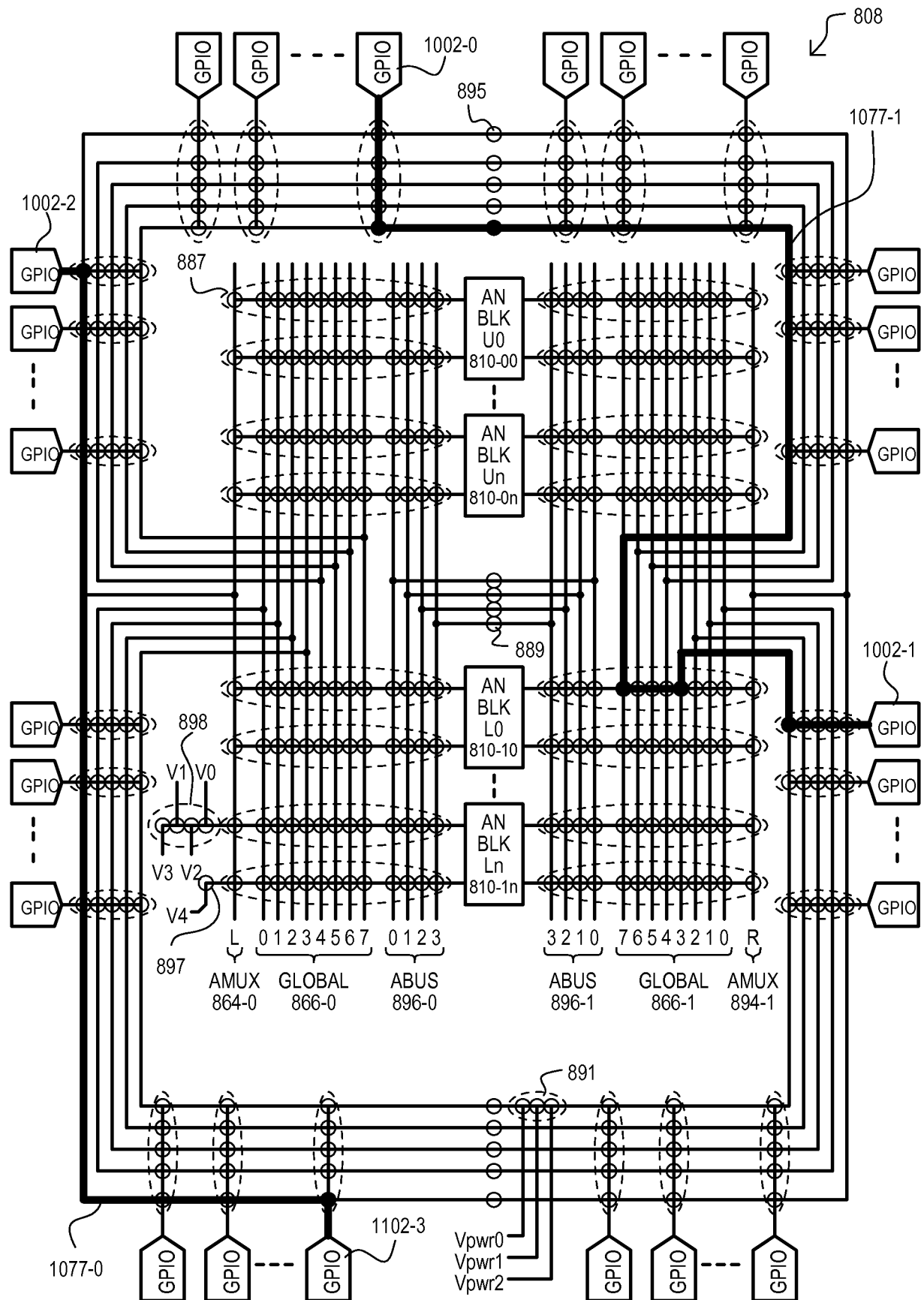


FIG. 10A

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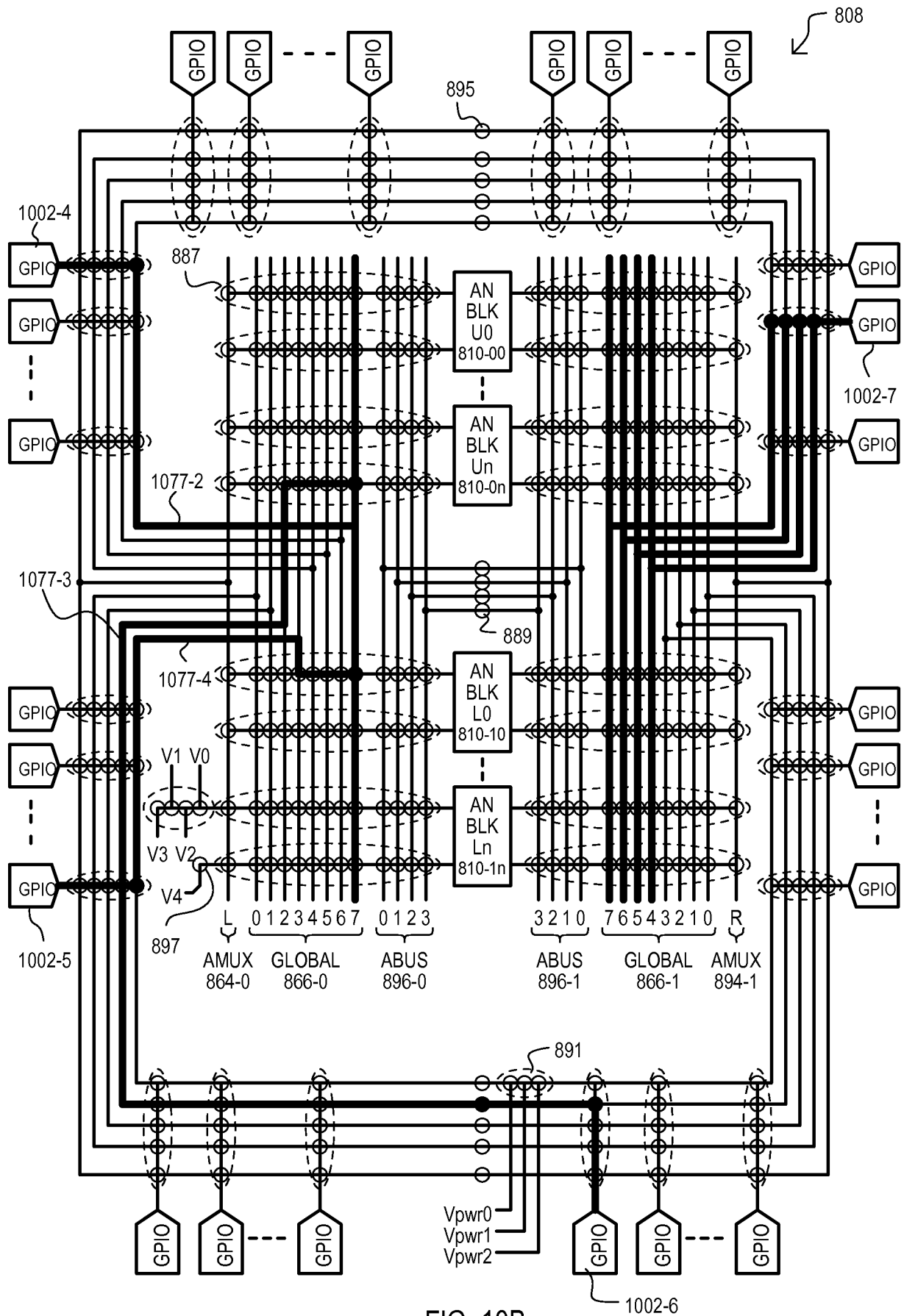


FIG. 10B

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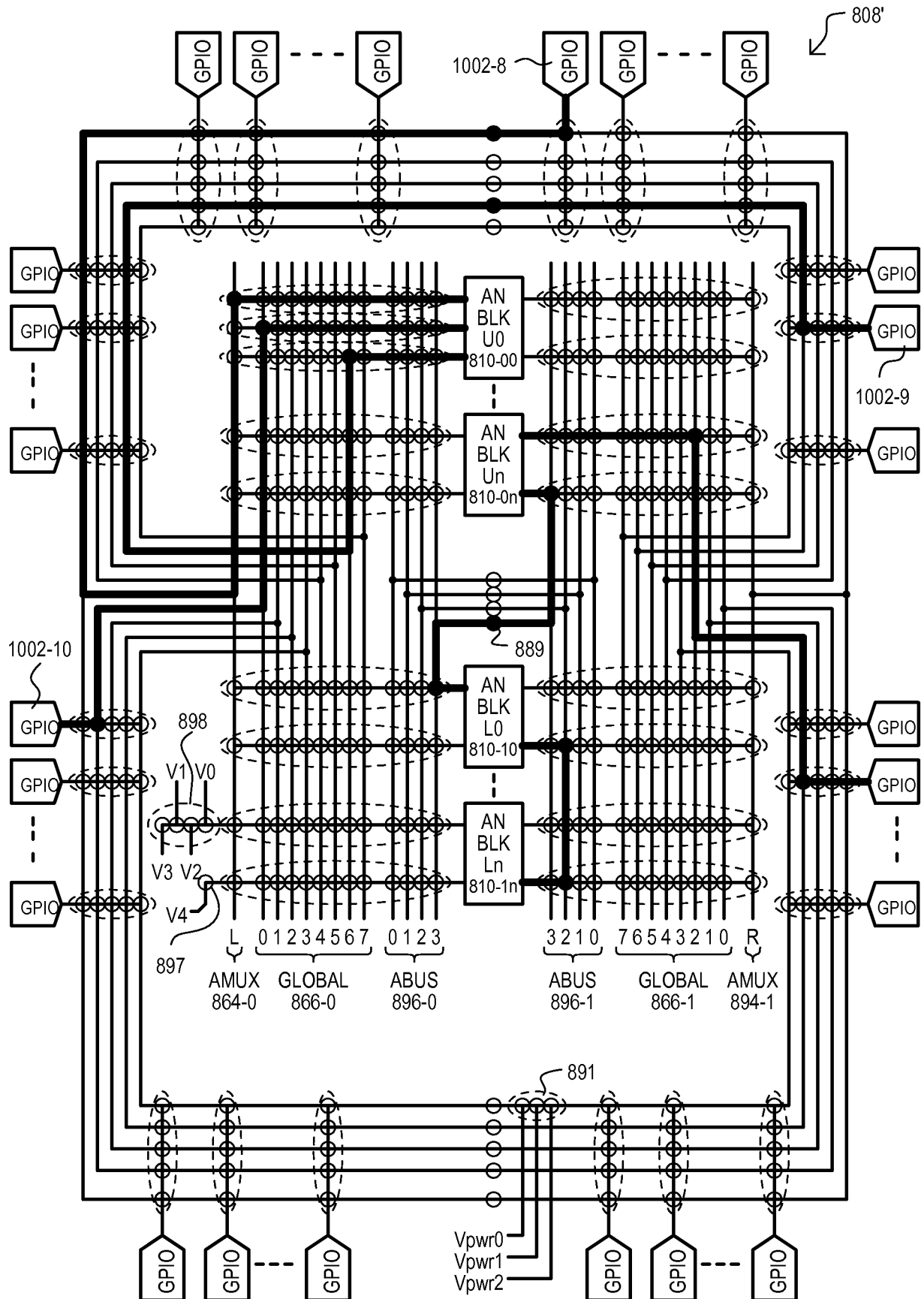
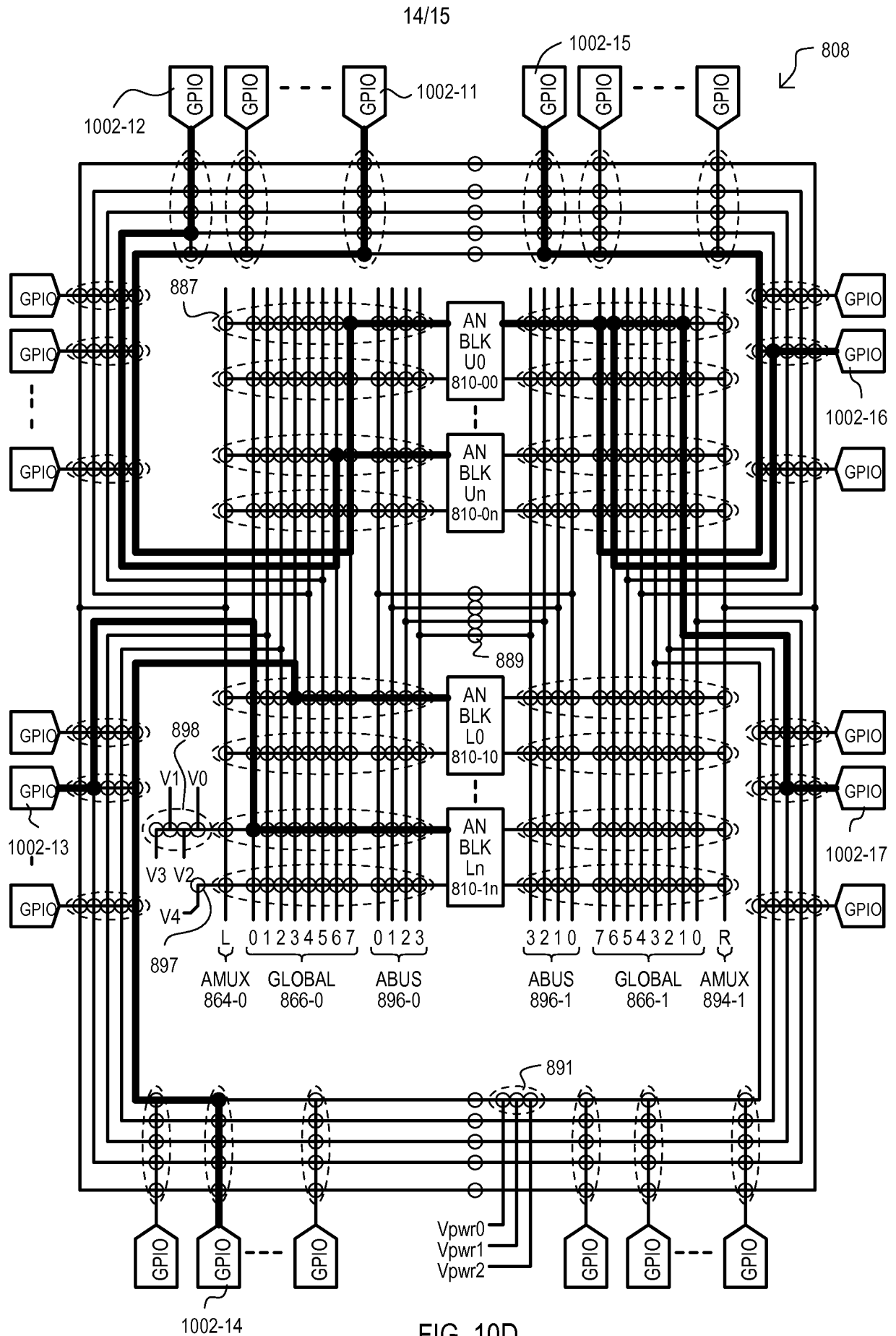


FIG. 10C



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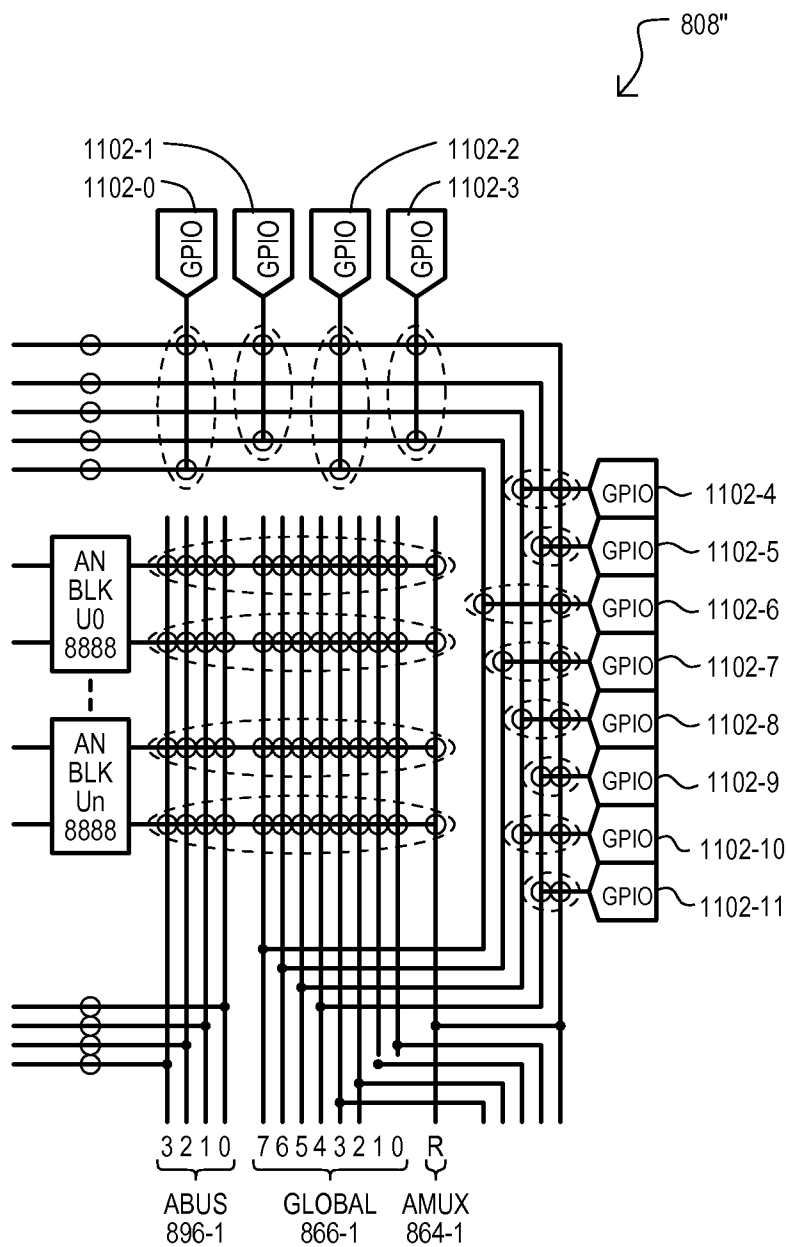


FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2010/034185

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G06F 13/00 (2010.01)

USPC - 370/351

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - G06F 13/00; H03K 19/00, 19/173, 19/177 (2010.01)

USPC - 326/37, 38, 39; 370/351

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Patbase, Micropatent

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,778,439 A (TRIMBERGER et al) 07 July 1998 (07.07.1998) entire document	1-20
Y	US 6,701,340 B1 (GORECKI et al) 02 March 2004 (02.03.2004) entire document	1-20
Y	US 5,079,451 A (GRUDGER et al) 7 January 1992 (07.01.1992) entire document	1-20
Y	US 5,598,408 A (NICKOLLS et al) 28 January 1997 (28.01.1997) entire document	5
A	US 2003/0067919 A1 (QIAO et al) 10 April 2003 (10.03.2003) entire document	1-20

☐ Further documents are listed in the continuation of Box C.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 August 2010

Date of mailing of the international search report

07 SEP 2010

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Blaine R. Copenheaver

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