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(54) Title: SEMICONDUCTOR MODULE AND METHOD FOR MANUFACTURING IT

Fig. 2A

(57) Abstract: A semiconductor module (2) is disclosed. The semiconductor module (2) comprises a shaped metal body (20) fixed to an upper surface of a semiconductor (26) having a lower surface that is connected by sintering onto a top layer (8') of a substrate (4). The shaped metal body (20) comprises a top surface (30) provided with surface structuring (32) that increases the surface area of the top surface (30). The semiconductor module (2) enables an improved cooling solution and thus makes it possible to improve the volumetric power density.

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Semiconductor Module and Method for Manufacturing it

Field of invention

The present invention relates to a semiconductor module comprising a shaped metal body fixed to an upper surface of a semiconductor having a lower surface that is sintered onto a top layer of a substrate. The invention also relates to a method for manufacturing a semiconductor module.

Prior art

Modern power electronics applies solid-state electronics to control and convert electric power with semiconductor switching devices such as diodes, thyristors and transistors. In contrast to electronic systems that are configured to transmit and process signals and data, in power electronics substantial amounts of electrical energy are processed.

More and more applications are adopting power electronics technologies to improve energy efficiency, reliability, and control. Semiconductor components are essential for power semiconductors and, since such components are sensitive to high temperatures, to avoid device failure due to thermal runaway, effective cooling is required.

Moreover, the increasing demand for enhanced functionality, smaller form factor, higher reliability and lower cost in electronic devices has initiated development of large-scale integrations and miniaturizations. These miniaturizations and large-scale integrations in turn are responsible for a steady increase in the power dissipated by the electronic chips and other components. Accordingly, effective cooling technologies have attracted the attention of producers and researchers.

In general, air-cooling provides a simple, low cost, effective, and reliable cooling solution. However, with the increase of heat flux dissipation, the prior air

cooling technology may not be sufficient.

It is an object to provide a semiconductor module that enables an improved, effective, and reliable air-cooling solution.

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Summary of the invention

The object of the present invention can be achieved by a semiconductor module as defined in claim 1 and by a method as defined in claim 12. Preferred embodiments are defined in the dependent subclaims, explained in the following description and illustrated in the accompanying drawings.

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The semiconductor module according to the invention is a semiconductor module comprising a shaped metal body fixed to an upper surface of a semiconductor having a lower surface that is sintered onto a top layer of a substrate, wherein the shaped metal body comprises a top surface provided with surface structuring that increases the surface area of the top surface.

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Hereby, it is possible to provide a semiconductor module that enables an improved, effective, and reliable cooling solution. Accordingly, it is possible to increase the volumetric power density.

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In a preferred embodiment of the invention, the shaped metal body is attached to the upper surface of the semiconductor by means of a sintering layer.

25

The sintering technology of the invention may use a silver-based paste to connect the respective elements. Silver is thermally very stable, suffering from virtually no creep effects in power module service temperatures. This provides a considerable advantage over the standard solder technology using low-melting temperature metals for connecting chips to substrates or other elements. The temperatures in power modules are in the range of creep

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effects for solder alloys, meaning that they can crack and/or deform easily in service. Moreover, in terms of process flow, a soldering process requires a subsequent process step to clean the surface from unwanted chemicals. This is not required in a sintering process.

The surface structuring may be of any suitable type as long as it increases the surface area of the top surface. The increased surface area of the top surface increases the cooling capacity of the top surface. Accordingly, it is an advantage to have a surface structuring that increases the surface area of the top surface to a large extent.

In one embodiment, the surface structuring increases the surface area of that portion of the top surface at which the surface structuring is provided, with at least 10 %.

In one embodiment, the surface structuring increases the surface area of that portion of the top surface at which the surface structuring is provided, with at least 25 %.

In one embodiment, the surface structuring increases the surface area of that portion of the top surface at which the surface structuring is provided, with at least 40 %.

In one embodiment, the surface structuring increases the surface area of that portion of the top surface at which the surface structuring is provided, with at least 50 %.

In one embodiment, the surface structuring increases the surface area of that portion of the top surface at which the surface structuring is provided, with more than 50 %.

In one embodiment, the semiconductor module may be a power module for automotive, solar, wind or industrial applications.

The shaped metal body may be a plate-shaped metal body. In one embodi-
5 ment, the shaped metal body is made of copper.

In one embodiment, the shaped metal body is a copper foil.

In a preferred embodiment, the semiconductor module is a power module.
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In one embodiment, the shaped metal body is fixed to an upper surface of the semiconductor, the semiconductor having a lower surface being sintered onto a top layer of the substrate.

15 In one embodiment, the semiconductor module comprises an encapsulation that is brought into thermal contact with the surface structuring, wherein the encapsulation covers at least a portion the surface structuring and is electrically insulating and thermally conductive.

20 By applying a thermally conductive encapsulation, it is possible to increase the heat transfer coefficient of the media (encapsulation) covering the surface structuring and thus enhance the cooling capacity of the surface structuring. Accordingly, it advantageous to apply an encapsulation having a thermal conductance that is higher than a predefined level such as more than 0.1 W/mK.
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In one embodiment, the electrically insulating and thermally conductive encapsulation has a thermal conductance in the range 0.1-15 W/mK.

In one embodiment, the electrically insulating and thermally conductive en-
30 capsulation has a thermal conductance in the range 0.15-10 W/mK.

In one embodiment, the electrically insulating and thermally conductive encapsulation is made of epoxy, preferably epoxy having a thermal conductance in the range 1 to 10 W/mK.

5 In one embodiment, the electrically insulating and thermally conductive encapsulation is made of, preferably silicone having a thermal conductance in the range 0.17 W/mK up to 3 W/mK.

In one embodiment, the electrically insulating and thermally conductive en-
10 capsulation is made of cement, preferably cement having a thermal conductance in the range with 2-10 W/mK.

In one embodiment, the electrically insulating and thermally conductive encapsulation is a cement-ceramic encapsulation material comprising a calcium
15 aluminate cement matrix. In one embodiment, the cement-ceramic encapsulation material may comprise alumina fillers.

In one embodiment, the encapsulation covers the entire surface structuring. Hereby, it is possible to increase the cooling capacity of the surface structuring
20 to a very high level.

In one embodiment, the thermal conductance of the encapsulation is in the range 0.17-10 W/mK.

25 In one embodiment, the encapsulation has a dielectric strength of at least 10 kV/mm.

It may be an advantage that the height of the encapsulation is more than two times larger than the height of the surface structuring.

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In one embodiment, the height of the encapsulation is more than four times

larger than the height of the surface structuring. Hereby, it is possible to provide a semiconductor, wherein the cooling capacity of the surface structuring is enhanced.

In one embodiment, one or more wire bonds or ribbon bonds are attached to the shaped metal body. By this way it is possible to increase the surface area of the shaped metal body and thus enhance the cooling capacity by simple means.

In one embodiment, one or more wire bonds or ribbon bonds are electrically connected to a structure being electrically insulated from the top layer of the substrate. Thus, the wire bonds or ribbon bonds are used as connectors providing electrical connection. The use of wire bonds or ribbon bonds having a large cross-sectional area makes it possible to reduce the electrical resistance and hereby the heat generation.

In one embodiment, the surface structuring comprises wires or ribbons attached to the top surface of the shaped metal body. This type of surface structuring can be provided using the same bonding machine utilised for other bonds in the module, and thus no additional steps or tools are required in the production process, leading to an efficient and cost-effective means of providing efficient cooling. Furthermore, it is possible to provide a very large surface area of the surface structuring.

In one embodiment, the surface structuring comprises a plurality of structures made by a laser structuring process applied to the top surface of the shaped metal body. Hereby, it is possible to increase the surface structuring without adding any structures.

It may be advantageous that the structures made by the laser structuring process are protruding structures and/or groove-shaped structures.

According to the invention, the ratio between height and distance of the structures is in the range from 1:2 up to 30:1. In an inventive pattern, the height of the structures is below 3 mm, preferably below 2 mm, more preferably below 1,5 mm, and in a small-scale pattern in the range of 0.5 to 1,0 mm, wherein the distance between the individual structures is below 6 mm, preferably below 4 mm, more preferably below 3 mm, and in a small-scale pattern in the range of 1.5 to 2.0 mm. The smallest size is achieved using laser structuring and may be down to 20nm in form of pores or protrusions.

In one embodiment, the laser structuring process is combined with another surface structuring process. Thus, it is possible to increase the surface area of the top surface of the shaped metal body even further.

In one embodiment, the surface structuring comprises structures made by a stamping process applied to the top surface of the shaped metal body. Hereby, it is possible to provide protruding structures and groove structures arranged in an alternating manner.

It may be an advantage that the surface structuring comprises protruding pins attached to the top surface of the shaped metal body. The protruding pins may comprise a cylindrical portion. The protruding pins may comprise a conical portion, e.g. a pointed distal portion.

In one embodiment, the surface structuring comprises protruding pins attached to the top surface of the shaped metal body, wherein the protruding pins extend basically perpendicular to the top surface of the shaped metal body.

It may be advantageous that the shaped metal body comprises a lateral portion without surface structuring. Hereby, it is possible to establish a good

electrical connection (providing a large contact area) between a connector (e.g. a wire bond) and the shaped metal body in the lateral portion.

In one embodiment, the shaped metal body comprises a central portion without surface structuring. Hereby, it is possible to provide a good electrical connection between a connector such as a wire bond and the shaped metal body in the central portion.

It may be an advantage that the substrate is attached to a base plate, preferably by means of a sintering process. Hereby, a firm attachment between the substrate and the base plate can be provided.

In one embodiment, the shaped metal body is sintered to the upper surface of the semiconductor. Accordingly, it is possible to provide a strong and reliable attachment between the shaped metal body and the semiconductor.

In one embodiment, the substrate is a direct bonded copper (DBC) substrate. Hereby, it is possible to achieve a very good thermal conductivity. The use of other substrates is also possible, such as ceramic (or ceramic-metal) substrates in general, and/or active metal brazed (AMB) substrates.

The method according to the invention is a method for manufacturing a semiconductor module, wherein the method comprises the step of:

a) placing a shaped metal body on an upper surface of a semiconductor;
b) placing the semiconductor on a substrate;
c) fixing the shaped metal body onto the upper surface of the semiconductor and fixing the semiconductor onto the top layer of the substrate,

wherein the method comprises the step of providing to the top surface of the shaped metal body a surface structuring that increases the surface area of the top surface.

Hereby, it is possible to manufacture a semiconductor module having a high volumetric power density due to the improved cooling properties caused by the increased surface area.

5 In one embodiment, the method comprises the step of connecting the shaped metal body and one additional component using wire bonds or ribbon bonds.

In one embodiment, the stamped structures are provided to the shaped metal body prior to attaching the shaped metal body to the upper surface of the 10 semiconductor.

In one embodiment, lasered structures are provided to the shaped metal body prior to or after attaching the shaped metal body to the upper surface of the semiconductor. Hereby, it is possible to increases the surface area of the top 15 surface without adding structures to the shaped metal body.

It may be an advantage that the shaped metal body is fixed onto the upper surface of the semiconductor by using a sintering process.

20 In one embodiment, the semiconductor is fixed onto the top layer of the substrate by using a sintering process.

It may be advantageous that the substrate is a DBC substrate.

25 **Description of the Drawings**

The invention will become more fully understood from the detailed description given herein below. The accompanying drawings are given by way of illustration only, and thus, they are not limitative of the present invention. In the accompanying drawings:

30 Fig. 1A shows a cross-sectional view of a prior art semiconductor module;

Fig. 1B shows a close-up view of the prior art semiconductor module shown in Fig. 1A;

Fig. 2A shows a cross-sectional view of a semiconductor module according to the invention;

5 Fig. 2B shows a cross-sectional view of a portion of a semiconductor module according to the invention;

Fig. 2C shows a cross-sectional view of a portion of another semiconductor module according to the invention;

Fig. 2D shows a cross-sectional view of a portion of a further semiconductor module according to the invention;

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Fig. 2E shows a top view of the semiconductor module shown in Fig. 2C;

Fig. 2F shows a top view of the semiconductor module shown in Fig. 2D;

Fig. 3A shows a top view of a shaped metal body comprising a top surface provided with surface structuring;

15 Fig. 3B shows a top view of another shaped metal body comprising a top surface provided with surface structuring;

Fig. 3C shows a close-up view of the surface structuring shown in Fig. 3B;

Fig. 3D shows a cross-sectional view of a shaped metal body comprising a top surface provided with surface structuring according to the invention;

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Fig. 3E shows a cross-sectional view of another shaped metal body comprising a top surface provided with surface structuring according to the invention;

25 Fig. 4A shows a cross-sectional view of a shaped metal body comprising a top surface provided with surface structuring according to the invention;

Fig. 4B shows a close-up cross-sectional view of a shaped metal body comprising a top surface provided with surface structuring according to the invention and

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Fig. 4C shows the shaped metal body shown in Fig. 4B in a configuration,

in which an encapsulation is covering the surface structuring.

Detailed description of the invention

Referring now in detail to the drawings for the purpose of illustrating preferred embodiments of the present invention, a semiconductor module 2 of the present invention is illustrated in Fig. 2A.

Fig. 2A is a schematic side view of a semiconductor module 2 according to the invention. The semiconductor module 2 comprises a shaped metal body 20 fixed to an upper surface of a semiconductor 26 having a lower surface that is sintered onto a top layer 8′ of a substrate 4. The shaped metal body 20 comprises a top surface provided with surface structuring 32. Hereby, the surface structuring 32 increases the surface area of the top surface.

The semiconductor module 2 comprises a base plate 6. A sintering layer 12 is provided on the top of the base plate 6 in order to attach (during a sintering process) a copper layer 8 thereto. Other means of attaching the copper layer 8 to the base plate 6 are also possible, such as the use of solder. The copper layer 8 constitutes the bottom part of a direct bonded copper (DBC) substrate 4. The DCB substrate 4 comprises a ceramic substrate 10 sandwiched between the lower copper layer 8 and an upper copper layer 8′. A separate conducting portion 16 of the upper copper layer is also shown here attached to the top portion of the ceramic substrate 10. This may form a separate section of the electrical circuit pattern on the upper surface of the DBC.

A shaped metal body 20 is attached to the semiconductor 26 (of silicon or silicon carbide). The semiconductor 26 is attached to the upper copper layer 8′ by means of a sintering layer 28. The surface structuring 32 is attached to a shaped metal body 20 that is attached to the semiconductor 26 by means of a sintering layer 22.

A wire bond 18 is electrically connected to the shaped metal body 20 and the conducting portion 16. The semiconductor module 2 comprises an encapsulation 34 that is brought into thermal contact with the surface structuring 32. The encapsulation 34 covers the entire surface structuring 32 and is electrically insulating and thermally conductive. It can be seen that the height H_2 of the encapsulation 34 is larger than the height H_1 of the surface structuring 32.

In one embodiment, the shaped metal body 20 is a copper foil. In one embodiment, the wire bond may be replaced by ribbon bond (e.g. made of copper).

Fig. 2B illustrates a cross-sectional view of a portion of a semiconductor module according to the invention comprising a shaped metal body 20 provided with surface structuring 32′. The surface structuring 32′ is attached to a shaped metal body 20 a chip 30. The surface structuring 32′ is made from wire bonds. The surface structuring 32 comprises a central portion attached to the shaped metal body 20 and lateral portions that protrude therefrom. Accordingly, the surface area and thus the cooling capacity of the shaped metal body 20 is increased. The surface structuring 32′ may be attached to the shaped metal body 20 by using the same technique as when attaching a wire bond 18. It can be seen that the surface structuring 32′ comprises a plurality of members made from wire bonds. These members are spaced from each other.

Fig. 2C illustrates a cross-sectional view of a portion of another semiconductor module according to the invention, whereas Fig. 2E illustrates a top view of the semiconductor module shown in Fig. 2C in a configuration, in which no wire bond 18 is attached to the shaped metal body 20. The shaped metal body 20 is provided with a surface structuring 32′′ formed by a plurality of pins protruding from the lower portion of the shaped metal body 20. The shaped

metal body 20 comprises a central portion 36 without surface structuring. The central portion 36 is rectangular, however, it could be shaped differently. In Fig. 2C, a wire bond 18 is attached to the central portion 36.

5 Fig. 2D illustrates a cross-sectional view of a portion of a semiconductor module according to the invention, whereas Fig. 2F illustrates a top view of the semiconductor module shown in Fig. 2D in a configuration, in which no wire bond 18 is attached to the shaped metal body 20.

10 The shaped metal body 20 is provided with a surface structuring 32′′ comprising a plurality of pins protruding from the lower portion of the shaped metal body 20. The shaped metal body 20 comprises a lateral portion 38 having no surface structuring. The lateral portion 38 extends along the periphery of the shaped metal body 20. In Fig. 2D, a wire bond 18 is attached to the lateral 15 portion 38.

Fig. 1A illustrates a cross-sectional view of a prior art semiconductor module 102. The semiconductor module 102 comprises a heatsink 14 attached to the bottom surface of a base plate 6. The prior art semiconductor module 102 20 comprises a metal body 20 fixed to an upper surface of a semiconductor 26 having a lower surface that is sintered onto a top layer 8′ of a substrate 4. The top surface of the metal body 20 is not provided with any surface structuring.

25 A sintering layer 12 is provided on the top of the base plate 6 in order to attach a copper layer 8 thereto. Other means of attaching the copper layer 8 to the base plate 6 are also known, such as the use of solder. The copper layer 8 constitutes the bottom part of a DBC substrate 4 comprising a ceramic substrate 10 sandwiched between the lower copper layer 8 and an upper cop-30 per layer 8′. A conducting portion 16 is attached to the top portion of the ceramic substrate 10 in a distance from the upper copper layer 8′.

The semiconductor 26 is attached to the upper copper layer 8′ by means of a sintering layer 28. The surface structuring 32 is attached to a shaped metal body 20 that is attached to the semiconductor 26 by means of a sintering layer 22.

Fig. 1B illustrates a close-up view of the prior art semiconductor module shown in Fig. 1A.

Fig. 3A illustrates a top view of a shaped metal body 20 comprising a top surface provided with surface structuring 32‴. The surface structuring 32‴ is made by a stamping process applied to the top surface of the shaped metal body 20. Although it is not shown, it is possible to provide both protruding members and groove members. In a preferred embodiment, protruding structures and groove structures are arranged in the top surface of the shaped metal body 20 in an alternating manner.

The shaped metal body 20 comprises a lateral portion 38 without surface structuring. Hereby, it is possible to establish a good electrical connection (having a large contact area) between a connector (e.g. a wire bond) and the shaped metal body 20 in the lateral portion 38. The lateral portion 38 is provided in the right side of the shaped metal body 20.

Fig. 3B illustrates a top view of a shaped metal body 20 having a top surface provided with surface structuring 32⁗. The surface structuring comprises protruding pins attached to the top surface of the shaped metal body 20. The protruding pins have a basically a cylindrical body portion and a conical distal portion.

The shaped metal body 20 comprises a lateral portion 38 without surface structuring. The lateral portion 38 extends along the periphery of the shaped

metal body 20.

Fig. 3C illustrates a close-up view of the surface structuring 32′′′′ shown in Fig. 3B. It can be seen that the pins are evenly distributed and formed as convex bodies protruding from the shaped metal body.

Fig. 3D illustrates a cross-sectional view of a shaped metal body 20 comprises a top surface provided with surface structuring 32′′′′ according to the invention. The shaped metal body 20 is provided with a surface structuring 32′′′′ formed by a plurality of pins protruding from the lower portion of the shaped metal body 20. The shaped metal body 20 comprises a central portion, in which no surface structuring is provided. A wire bond 18 is attached to the central portion. Hereby, it is achieved that a large contact area is provided between the wire bond 18 and the central portion of the shaped metal body 20.

Fig. 3E illustrates a cross-sectional view of a shaped metal body 20 comprising a top surface provided with surface structuring 32′′′′′ according to the invention. The shaped metal body 20 is provided with a surface structuring 32′′′′ formed by a plurality of pins protruding from the lower portion of the shaped metal body 20. The shaped metal body 20 comprises a lateral portion, in which no surface structuring is provided. A wire bond 18 is attached to the lateral portion. Hereby, a large contact area is provided between the wire bond 18 and the lateral portion of the shaped metal body 20.

Fig. 4A illustrates a cross-sectional view of a shaped metal body 20 comprising a top surface provided with surface structuring 32′′′′′ according to the invention. The shaped metal body 20 is provided with a surface structuring 32′′′′′ formed by a plurality of pins protruding from the lower portion of the shaped metal body 20. The surface structuring 32′′′′′ is provided at the entire top surface of the shaped metal body 20.

Accordingly, a wire bond 18 attached to a portion of the shaped metal body 20 is attached to the surface structuring 32′′′′′.

5 Fig. 4B illustrates a close-up cross-sectional view of a shaped metal body 20 which is provided with surface structuring 32′ according to the invention. The surface structuring 32′ is made by a plurality of the wire bonds each being fixed in both ends to the top surface of the shaped metal body 20. Each wire bond is basically U-shaped and protrudes from the top surface of the shaped 10 metal body 20. The wire bonds basically extend perpendicular to the top surface of the shaped metal body 20.

Fig. 4C illustrates the shaped metal body 20 shown in Fig. 4B in a configuration, in which an encapsulation 34 is covering the surface structuring 32′. The 15 thermal flow 42 is indicated with undulating arrows. It can be seen that the thermal flow 42 occurs from the entire outer surface of the encapsulation 34.

The encapsulation 34 entirely encloses the surface structuring 32′ and the portion of the top surface of the shaped metal body 20, onto which the wire 20 bonds are fixed.

Artikel I. List of reference numerals

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2	Semiconductor module (power module)
4	Direct bonded copper (DBC) substrate
6	Base plate
8, 8′	Copper layer
10	Ceramic substrate
12	Sinter layer
14	Heatsink
16	Conductor
18	Wire bond or ribbon bond (e.g. made of copper)
20	Shaped metal body
22	Sinter layer
26	Semiconductor (such as a semiconductor comprising silicon or silicon carbide)
28	Sinter layer
30	Chip
32, 32′, 32′′	Surface structuring
32′′′, 32′′′′, 32′′′′′	Surface structuring
34	Encapsulation
36	Central portion
38	Lateral portion
42	Thermal flow
102	Prior art semiconductor module
H_1, H_2	Height

Claims

1. A semiconductor module (2) comprising a shaped metal body (20) fixed to an upper surface of a semiconductor (26) having a lower surface that is sintered onto a top layer (8′) of a substrate (4), **characterised in** that the shaped metal body (20) comprises a top surface (30) provided with surface structuring (32, 32′, 32″, 32‴, 32⁗, 32′′′′′) that increases the surface area of the top surface (30),

2. A semiconductor module (2) according to claim 1, **characterized in** that the shaped metal body (20) is attached to the upper surface of the semiconductor (26) by means of a sintering layer (22).

3. A semiconductor module (2) according to claim 1 or 2 , **characterised in** that the semiconductor module (2) comprises an encapsulation (34) that is brought into thermal contact with the surface structuring (32, 32′, 32″, 32‴, 32⁗, 32′′′′′), wherein the encapsulation (34) covers at least a portion the surface structuring (32, 32′, 32″, 32‴, 32⁗, 32′′′′′) and is electrically insulating and thermally conductive.

4. A semiconductor module (2) according to claim 3, **characterised in** that the encapsulation (34) has a thermal conductance in the range 0.17-10 W/mK.

5. A semiconductor module (2) according to one of the claims 3-4, **characterised in** that the encapsulation (34) has a dielectric strength of at least 10k V/mm.

6. A semiconductor module (2) according to one of claims 3-5, **characterised in** that the encapsulation (34) is made of cement.

7. A semiconductor module (2) according to one of the preceding claims,

characterised in that one or more wire bonds or ribbon bonds (18) are attached to the shaped metal body (20).

8. A semiconductor module (2) according to one of the preceding claims,
5 **characterised in** that the surface structuring (32, 32′, 32″, 32‴, 32⁗, 32′′′′′) comprises wires (32′) or ribbons attached to the top surface (30) of the shaped metal body (20).

9. A semiconductor module (2) according to one of the preceding claims,
10 **characterised in** that the surface structuring (32, 32′, 32″, 32‴, 32⁗, 32′′′′′) comprises a plurality of structures (32″) made by a laser structuring process applied to the top surface (30) of the shaped metal body (20).

10. A semiconductor module (2) according to one of the preceding claims,
15 **characterised in** that the surface structuring (32, 32′, 32″, 32‴, 32⁗, 32′′′′′) comprises structures (32″) made by a stamping process applied to the top surface (30) of the shaped metal body (20).

11. A semiconductor module (2) according to one of the preceding claims,
20 **characterised in** that the surface structuring (32, 32′, 32″, 32‴, 32⁗, 32′′′′′) comprises protruding pins (32′′′′′) attached to the top surface (30) of the shaped metal body (2T0).

12. A semiconductor module (2) according to one of the preceding claims,
25 **characterised in** that the shaped metal body (20) comprises a lateral portion (38) without surface structuring (32, 32′, 32″, 32‴, 32⁗, 32′′′′′).

13. A semiconductor module (2) according to one of the preceding claims, **characterised in** that the shaped metal body (20) comprises a central por-
30 tion (36) without surface structuring (32, 32′, 32″, 32‴, 32⁗, 32′′′′′).

14. A method for manufacturing a semiconductor module (2), wherein the method comprises the step of:

a) placing a shaped metal body (20) on an upper surface of a semiconductor (26);
5 b) placing the semiconductor (26) on a substrate (4);
c) fixing the shaped metal body (20) onto the upper surface of the semiconductor (26) and fixing the semiconductor (26) onto the top layer (8′) of the substrate (4);

characterised in that the method comprises the step of providing to the top
10 surface (30) of the shaped metal body (20) a surface structuring (32, 32′, 32″, 32‴, 32⁗, 32′′′′′) that increases the surface area of the top surface (30).

15. A method according to claim 14, **characterised in** that the method comprises the step of attaching the shaped metal body (20) to the upper surface of
15 the semiconductor (26) by means of a sintering layer (22).

16. A method according to claim 14 or 15, **characterised in** that the method comprises the step of connecting the shaped metal body (20) and one additional component (16) using wire bonds or ribbon bonds (18).

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17. A method according to any of claims 14-16, **characterised in** that the stamped structures (32‴) are provided to the shaped metal body (20) prior to attaching the shaped metal body (20) to the upper surface of the semiconductor (26).

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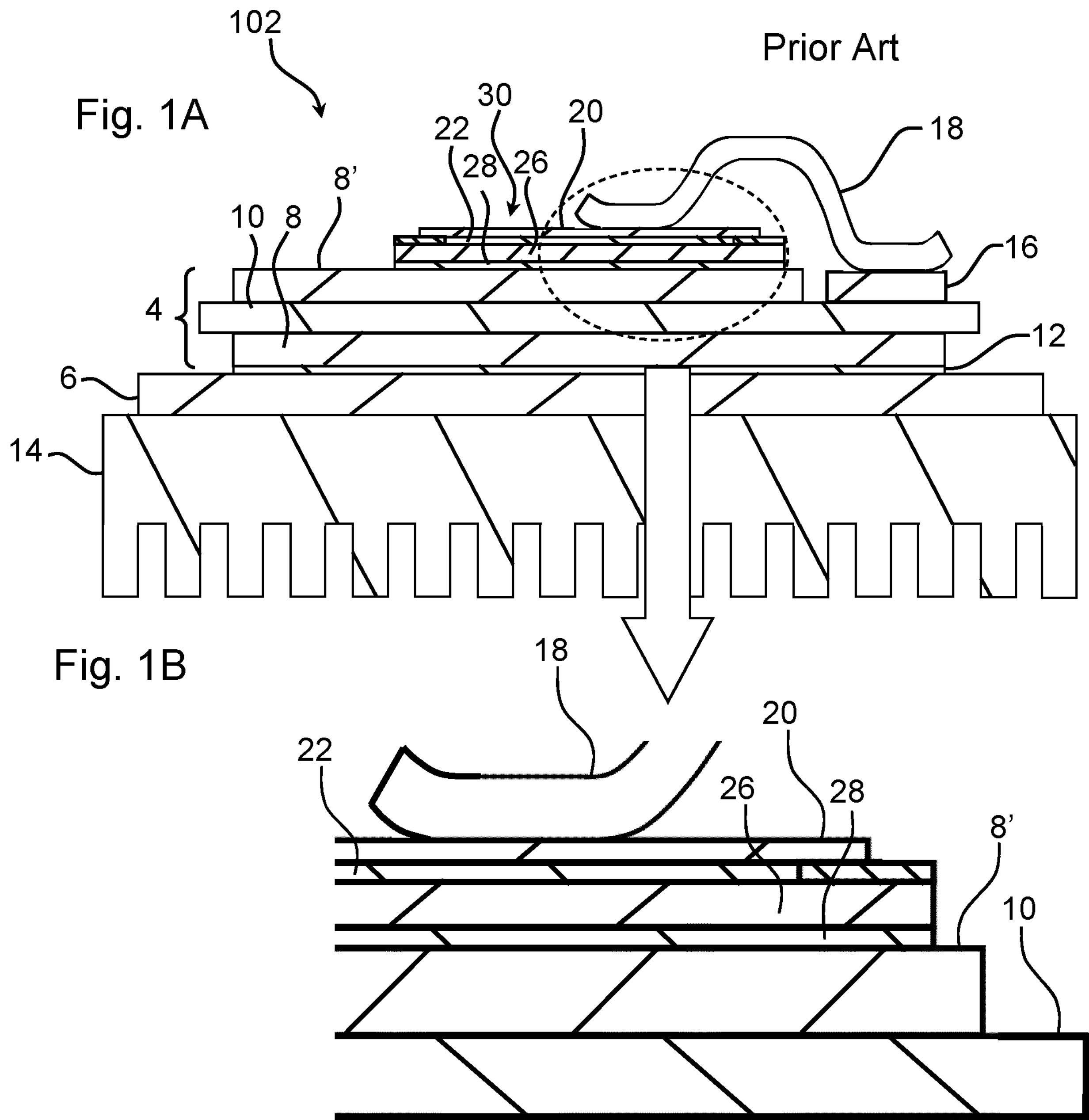

102
Prior Art
Fig. 1A
30
20
22
18
28
26
8'
10
8
16
4
12
6
14
Fig. 1B
18
20
22
26
28
8'
10

Fig. 2A

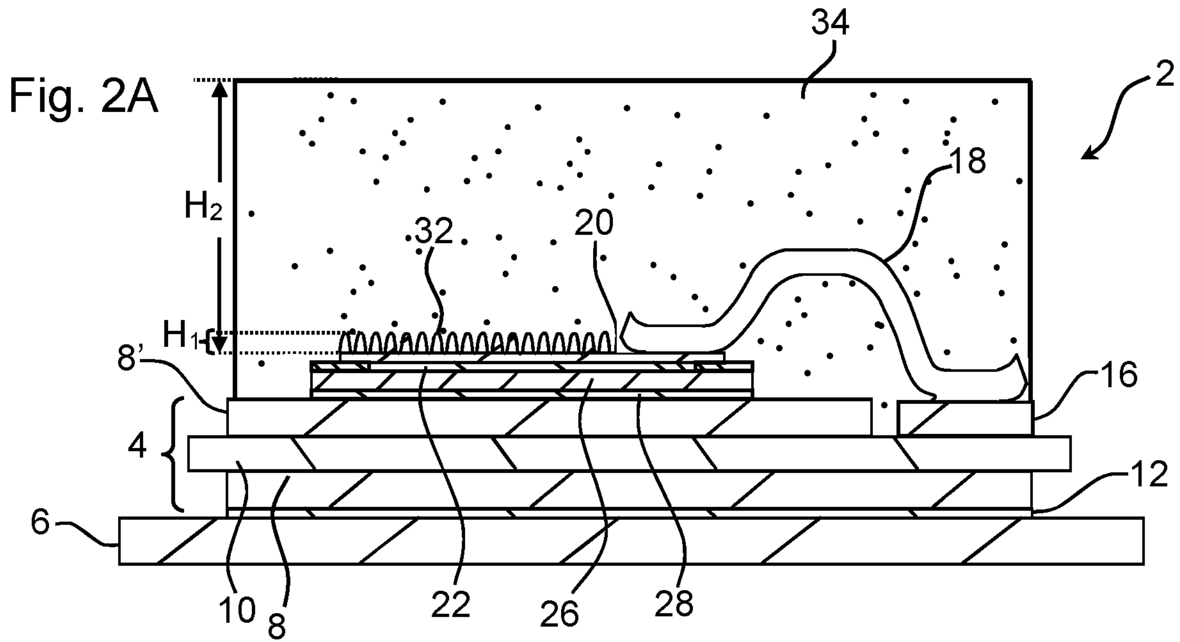


Fig. 2B

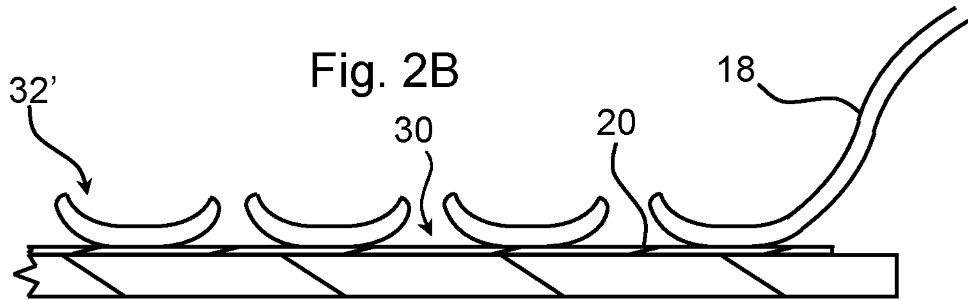


Fig. 2C

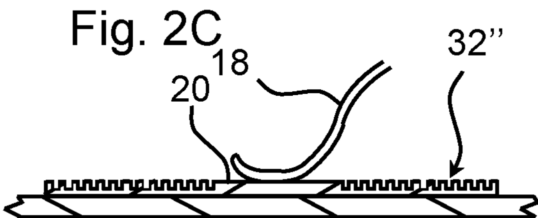
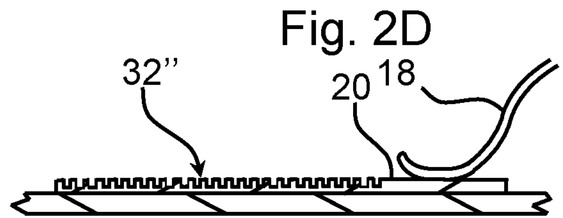
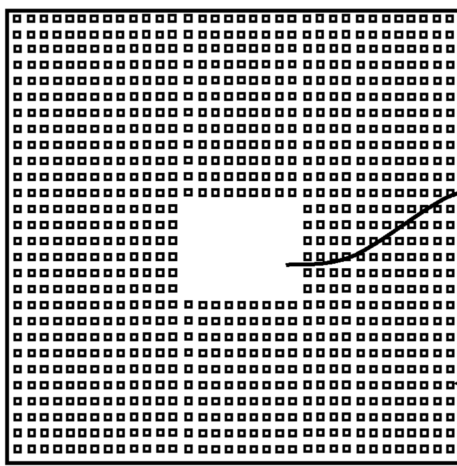


Fig. 2D





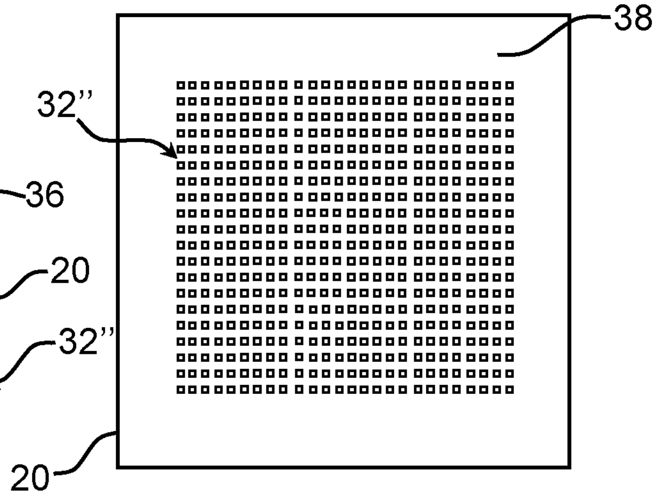


Fig. 2E

Fig. 2F

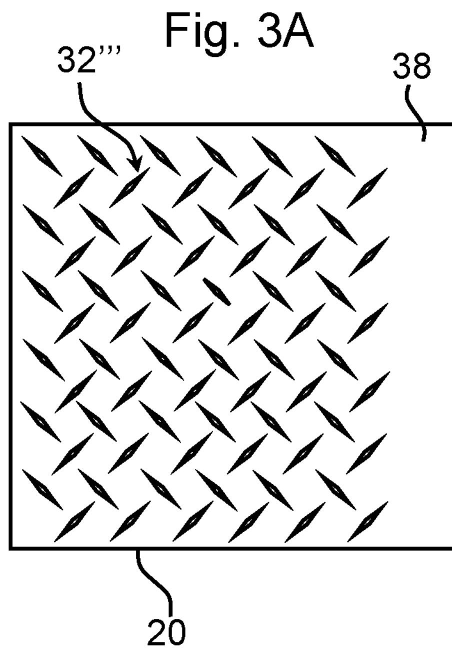


Fig. 3A

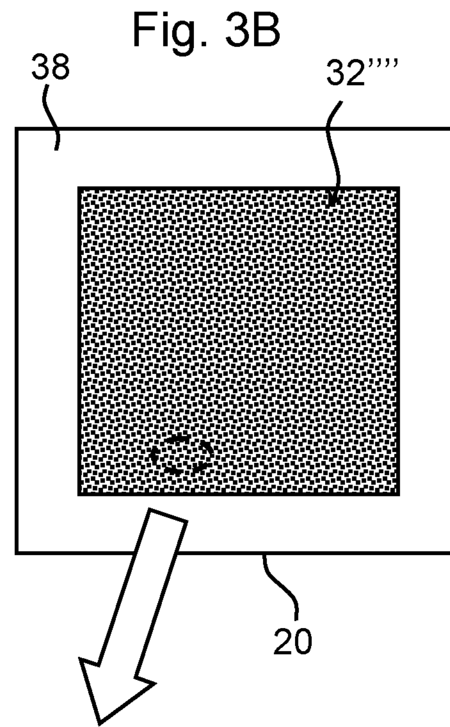


Fig. 3B

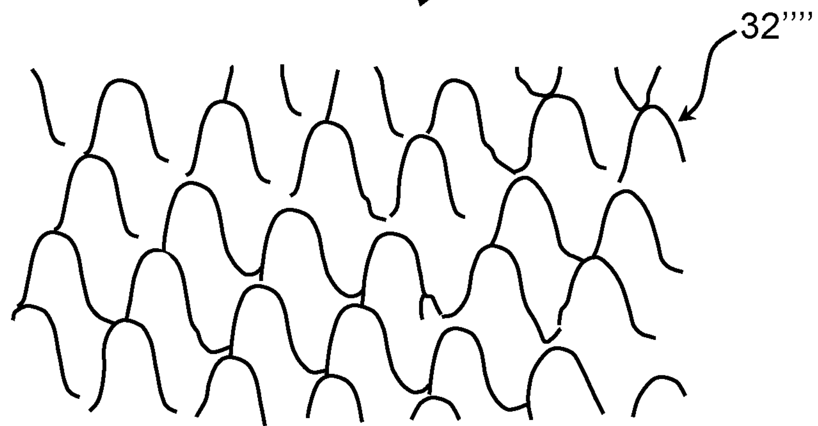


Fig. 3C

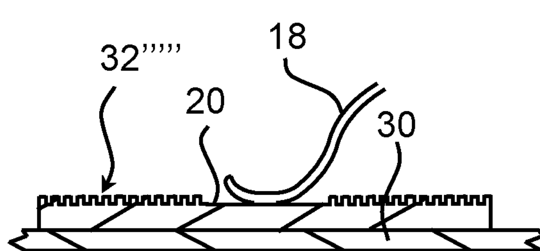


Fig. 3D

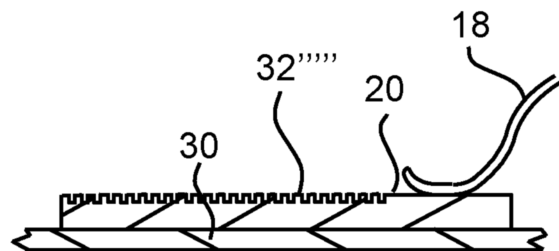


Fig. 3E

Fig. 4A

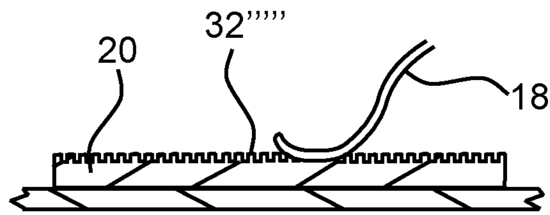


Fig. 4B

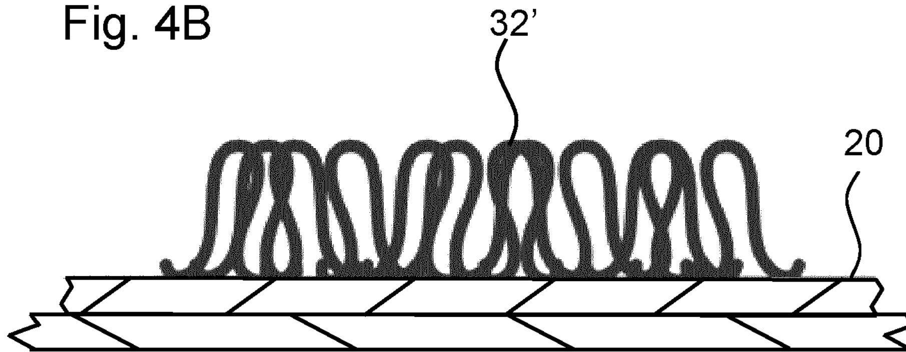
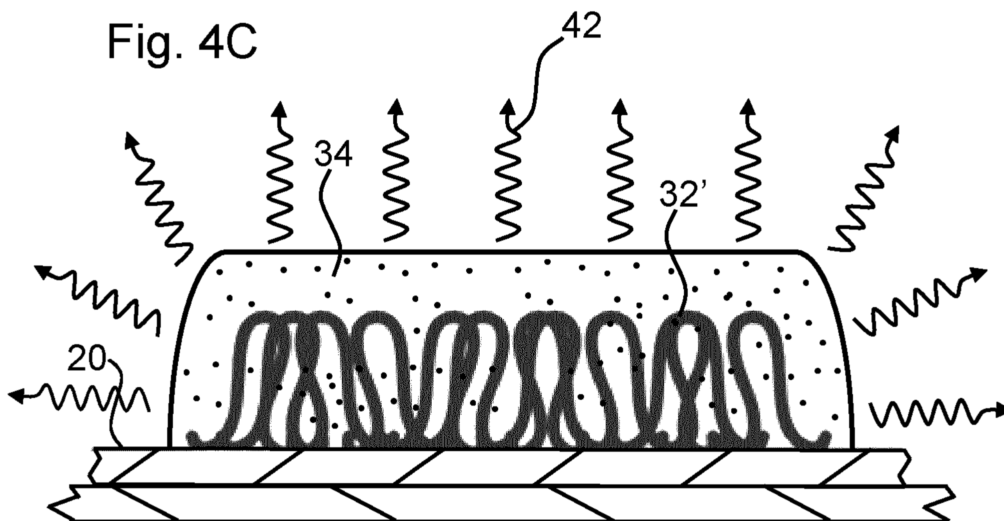


Fig. 4C



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2020/058532

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/36 H01L23/29 H01L21/48
ADD. H01L23/49 H01L21/60

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2006/012847 A1 (INFINEON TECHNOLOGIES AG [DE]; HOSSEINI KHALIL [DE]) 9 February 2006 (2006-02-09)	1-3,7,8, 12-16
Y	page 14, line 23 - page 19, line 2; figures 2,4	4-6
Y	US 2016/260648 A1 (EISELE RONALD [DE]) 8 September 2016 (2016-09-08) paragraphs [0018], [0019], [0037]	4-6
X,P	WO 2019/197304 A1 (ABB SCHWEIZ AG [CH]) 17 October 2019 (2019-10-17) page 8, line 14 - page 11, line 13; figures 3,4,7	1,2,7,8, 14-16

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 June 2020	30/07/2020

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Ahlstedt, Mattias

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2020/058532

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-8, 12-16

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-8, 12-16

directed to that the encapsulation has a thermal conductance in the range 0.17-10 W/mK or that the encapsulation is made of cement.

1.1. claim: 5

directed to that the encapsulation has a dielectric strength of at least 10k V/mm.

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2. claim: 9

directed to that the surface structuring comprises a plurality of structures made by a laser structuring process applied to the top surface of the shaped metal body.

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3. claims: 10, 17

directed to that the surface structuring comprises structures made by a stamping process applied to the top surface of the shaped metal body, as well as to a method wherein the stamped structures are provided to the shaped metal body prior to attaching the shaped metal body to the upper surface of the semiconductor.

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4. claim: 11

directed to the surface structuring comprises protruding pins attached to the top surface of the shaped metal body.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2020/058532

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2006012847 A1	09-02-2006	DE 102004036905 A1	23-03-2006
		WO 2006012847 A1	09-02-2006
US 2016260648 A1	08-09-2016	CN 105706230 A	22-06-2016
		DE 102013112267 A1	07-05-2015
		EP 3066684 A1	14-09-2016
		HU E043748 T2	30-09-2019
		JP 6472458 B2	20-02-2019
		JP 2016535464 A	10-11-2016
		KR 20160083031 A	11-07-2016
		MX 363041 B	06-03-2019
		TW 201535631 A	16-09-2015
		US 2016260648 A1	08-09-2016
		WO 2015067441 A1	14-05-2015
WO 2019197304 A1	17-10-2019	NONE	