## (19) World Intellectual Property Organization International Bureau





(43) International Publication Date 21 May 2004 (21.05.2004)

# T (10) International Publication Number WO 2004/042569 A3

(51) International Patent Classification<sup>7</sup>: G06F 9/445, 15/78, 17/50, 15/80

(21) International Application Number:

PCT/US2003/034556

(22) International Filing Date: 31 October 2003 (31.10.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/422,503	31 October 2002 (31.10.2002)	US
10/683,929	9 October 2003 (09.10.2003)	US
10/683,932	9 October 2003 (09.10.2003)	US
10/684,053	9 October 2003 (09.10.2003)	US
10/684,057	9 October 2003 (09.10.2003)	US
10/684,102	9 October 2003 (09.10.2003)	US

(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier application:

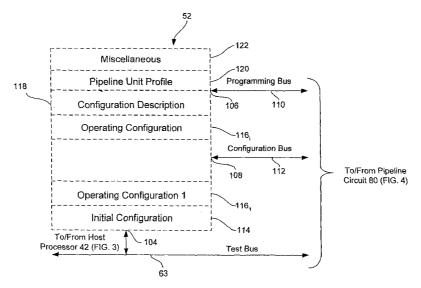
US 60/422,503 (CIP) Filed on 31 October 2002 (31.10.2002)

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- (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (regional): ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE,

[Continued on next page]

(54) Title: PROGRAMMABLE CIRCUIT AND RELATED COMPUTING MACHINE AND METHOD



(57) Abstract: A programmable circuit receives configuration data from an external source, stores the firmware in a memory, and then downloads the firmware from the memory. Such a programmable circuit allows a system, such as a computing machine, to modify the programmable circuit's configuration, thus eliminating the need for manually reprogramming the configuration memory. For example, if the programmable circuit is an FPGA that is part of a pipeline accelerator, a processor coupled to the accelerator can modify the configuration of the FPGA. More specifically, the processor retrieves from a configuration registry firmware that represents the modified configuration, and sends the firmware to the FPGA, which then stores the firmware in a memory such as an electrically erasable and programmable read-only memory (EEPROM). Next, the FPGA downloads the firmware from the memory into its configuration registers, and thus reconfigures itself to have the modified configuration.



## WO 2004/042569 A3



SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(88) Date of publication of the international search report: 27 April 2006

#### Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

#### INTERNATIONAL SEARCH REPORT

International Application No Pc1/US 03/34556

A. CLASSIFICATION OF SUBJECT MATTER G06F9/445 G06F G06F15/78 G06F17/50 G06F15/80 According to International Patent Classification (IPC) or to both national classification and IPC **B. FIELDS SEARCHED** Minimum documentation searched (classification system followed by classification symbols) G06F Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal C. DOCUMENTS CONSIDERED TO BE RELEVANT Relevant to claim No. Category 6 Citation of document, with indication, where appropriate, of the relevant passages US 6 326 806 B1 (FALLSIDE HAMISH T ET AL) 1 - 38χ 4 December 2001 (2001-12-04) the whole document US 5 784 636 A (RUPP ET AL) 1 - 38χ 21 July 1998 (1998-07-21) the whole document 1 - 38LECURIEUX-LAFAYETTE G: "UN SEUL FPGA DOPE X LETRAITEMENT D'IMAGES" ELECTRONIQUE, CEP COMMUNICATION, PARIS, FR, no. 55, January 1996 (1996-01), pages 98,101-103, XP000551946 ISSN: 1157-1152 the whole document -/--Patent family members are listed in annex Further documents are listed in the continuation of box C. X χ ° Special categories of cited documents: "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the "A" document defining the general state of the art which is not considered to be of particular relevance invention earlier document but published on or after the international "X" document of particular relevance; the claimed invention filing date cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such docu-"O" document referring to an oral disclosure, use, exhibition or ments, such combination being obvious to a person skilled document published prior to the international filing date but later than the priority date claimed "&" document member of the same patent family Date of the actual completion of the international search Date of mailing of the international search report 07/03/2006 22 February 2006 **Authorized officer** Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Beyer, 0 Fax: (+31-70) 340-3016

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International Application No
FeT/US 03/34556

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