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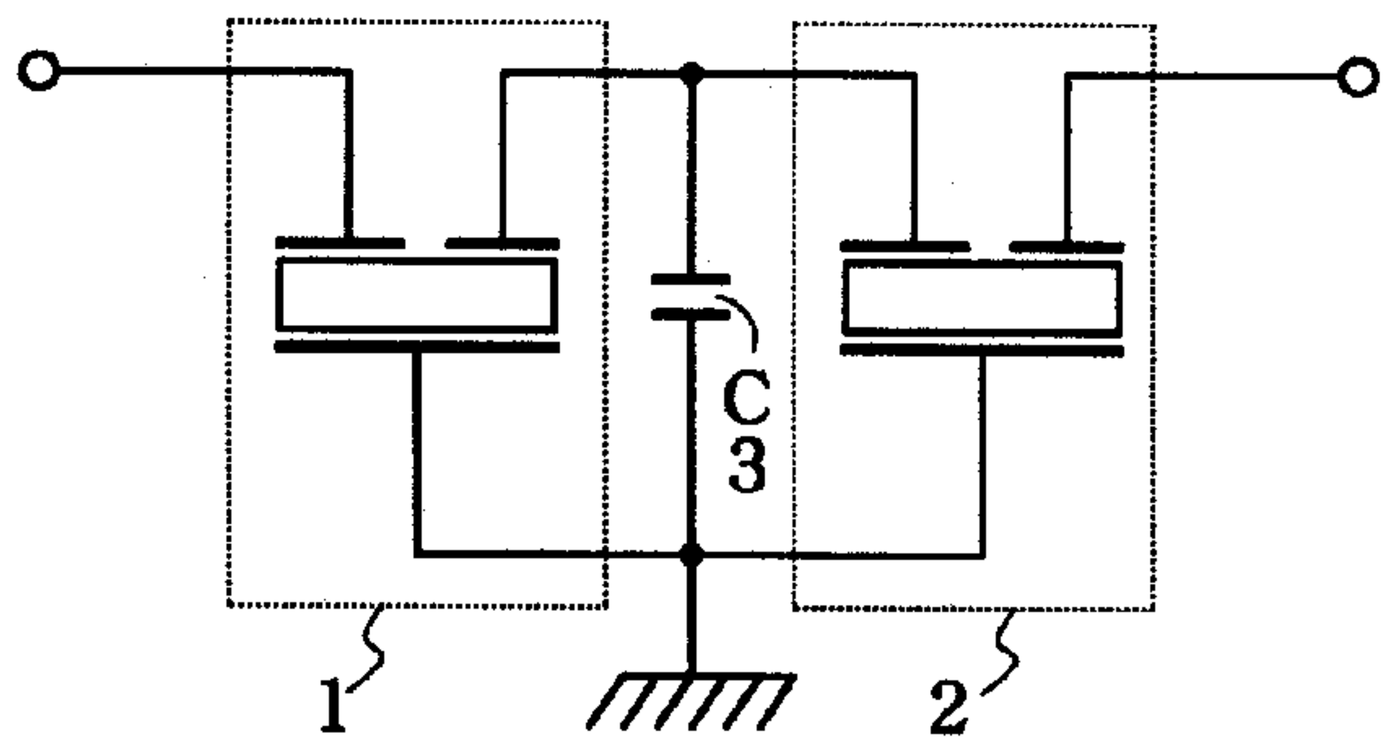
(54) **CIRCUIT DE FILTRES EN CERAMIQUE PIEZOELECTRIQUE, ET FILTRE DE CE TYPE**

(54) **PIEZOELECTRIC CERAMIC FILTER CIRCUIT AND PIEZOELECTRIC CERAMIC FILTER**



(57) Multiple piezoelectric ceramic filter elements have different center frequencies from each other and are cascade connected together. The piezoelectric ceramic filter elements satisfy the condition $0 < |dF_0| / BW_3 < 0.8$; where $|dF_0|$ is the absolute value of the frequency difference dF_0 between the center frequencies, and BW_3 is the band width, wherein the amplitude loss is 3dB or less. Thereby, a low insertion loss and an improvement in the group delay characteristics can be compatible at the same time.

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ABSTRACT

Multiple piezoelectric ceramic filter elements have different center frequencies from each other and are cascade connected together. The piezoelectric ceramic filter elements satisfy the condition $0 < |dF_0| / BW_3 < 0.8$;

where $|dF_0|$ is the absolute value of the frequency difference dF_0 between the center frequencies, and BW_3 is the band width, wherein the amplitude loss is 3dB or less.

Thereby, a low insertion loss and an improvement in the group delay characteristics can be compatible at the same time.

PIEZOELECTRIC CERAMIC FILTER CIRCUIT AND PIEZOELECTRIC CERAMIC FILTER

TECHNICAL FIELD

The present invention relates to a piezoelectric ceramic filter circuit and a piezoelectric ceramic filter.

BACKGROUND ART

Piezoelectric ceramic filters of this type are used, for example, as IF filters in various mobile communication devices and FM sound multiplex receivers. To date, the following types of piezoelectric ceramic filter circuits are well known: multistage type piezoelectric ceramic filter circuits and ceramic filters with trapped energy type multiple mode piezoelectric resonators having approximately the same center frequencies connected in cascade.

Insertion loss and group delay characteristics are important factors in piezoelectric ceramic filter circuits and piezoelectric ceramic filters. The insertion loss must be maintained at a low level in order to hold down signal attenuation through filtering. It is desirable that the group delay characteristics are as flat as possible within the pass band so that transmission time difference depending on frequency will not be created in the signal transmission within the pass band. Since piezoelectric ceramic filters are minimum phase shift devices, it is not possible to control the amplitude characteristics and the group delay characteristics independently. Previous attempts, therefore, to improve the group delay characteristics have been limited to keeping the mechanical quality factor Q of the piezoelectric resonator as low as possible.

However, with the prior art, wherein the group delay characteristics are improved by keeping the mechanical quality factor Q of the piezoelectric resonator low, the amplitude characteristics degrade and the insertion loss becomes extremely large, resulting in lowered filter transmission efficiency. In order to lower the insertion loss, Q must be high, thereby degrading the group delay characteristics. In other words, with the prior art, it has been difficult to improve the insertion loss and the group delay characteristics at the same time.

DISCLOSURE OF THE INVENTION

It is the object of the present invention to provide a piezoelectric ceramic filter circuit and a piezoelectric ceramic filter, wherein lowered insertion loss and improved group delay characteristics can be realized at the same time.

In order to achieve the afore-mentioned object, the piezoelectric ceramic filter circuit according to the present invention comprises a plurality of piezoelectric ceramic filter elements connected in cascade with each other, of which at least two piezoelectric ceramic filter elements have different center frequencies and satisfy the condition $0 < |dF_0| / BW_3 < 0.8$.

Here $|dF_0|$ is the absolute value of the frequency difference dF_0 between the center frequencies of said piezoelectric ceramic filter elements, and BW_3 is the pass band width in which the amplitude loss is 3dB or less.

Also, the piezoelectric ceramic filter according to the present invention has a plurality of trapped energy type filter elements on the same piezoelectric ceramic substrate. At least two of these trapped energy type filter elements have different center frequencies, are connected in cascade and satisfy the condition

$$0 < |dF_0| / BW_3 < 0.8.$$

Here $|dF_0|$ is the absolute value of the frequency difference dF_0 between the center frequencies of said trapped energy type ceramic filter elements, and BW_3 is the passband width in which the amplitude loss is 3dB or less.

Since at least two of the piezoelectric ceramic filter elements have different center frequencies and since they are connected in cascade with each other, it is possible, depending upon the selected center frequencies, to synthesize the group delay characteristics of the multi-type piezoelectric ceramic filter circuit and to obtain total stage group delay characteristics which are flat within the pass band.

Especially with a piezoelectric ceramic filter circuit that satisfies the condition $0 < |dF_0| / BW_3 < 0.8$, where $|dF_0|$ is the absolute value of the frequency difference dF_0 between the center frequencies of said piezoelectric ceramic filter elements, and BW_3 is the pass band width in which the amplitude loss is 3dB or less, the total stage group delay characteristics are largely flattened in the pass band.

In addition, unlike the method of the prior art to control the group delay characteristics by keeping the mechanical quality factor Q low, the piezoelectric ceramic filter circuit of the present invention does not increase the insertion loss.

When the above-mentioned concept of the present invention is applied to a piezoelectric ceramic filter that has trapped energy type filter elements on the same piezoelectric substrate, it is possible to make the filter more compact than a piezoelectric ceramic filter circuit that uses separate piezoelectric ceramic filters.

Moreover, it becomes possible to obtain a piezoelectric ceramic filter wherein the total stage group delay characteristics are very flat within the pass band without increasing the insertion loss.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention and many of the attendant advantages thereof become better understood when refering to the following detailed describtion of the accompanied drawings, wherein:

FIG. 1 is a schematic electrical diagram of the piezoelectric ceramic filter circuit of the present invention.

FIG. 2 is a graph showing the relationship between the frequency and the group delay time, and the relationship between the frequency and the amplitude loss in the piezoelectric ceramic filter circuit.

FIG. 3 is a graph showing the relationships between piezoelectric ceramic filter circuit frequencies, the group delay characteristics (with frequency difference dF_0 used as a parameter) and the amplitude loss.

FIG. 4 is a plan view of the trapped energy type piezoelectric ceramic filter of the present invention.

FIG. 5 is the bottom view of the piezoelectric ceramic filter shown in FIG. 4.

FIG. 6 is a plan view of a different embodiment of the piezoelectric ceramic filter of the present invention.

FIG. 7 is a plan view of yet another embodiment of the piezoelectric ceramic filter of the present invention.

FIG. 8 is a cross sectional view of yet another embodiment of the piezoelectric ceramic filter of the present invention.

BEST MODE OF CARRYING OUT OF THE INVENTION

FIG. 1 shows the piezoelectric ceramic filter circuit comprising two piezoelectric ceramic filter elements (1) and (2) which are cascade connected via a coupling capacitor (3). Piezoelectric ceramic filter elements (1) and (2) have different center frequencies F_{01} and F_{02} respectively, and satisfy the condition

$$0 < |dF_0| / BW_3 < 0.8.$$

Here $|dF_0|$ is the absolute value of the center frequency difference dF_0 between center frequencies F_{01} and F_{02}, is $|dF_0| = |F_{02} - F_{01}|$, and BW_3 is the pass band width wherein the amplitude loss is 3dB or less.

As mentioned above, since piezoelectric ceramic filter elements (1) and (2) have different center frequencies, F_{01} and F_{02}, respectively, and since they are cascade connected to each other, it is possible to flatten the total stage group delay characteristics of the piezoelectric ceramic filter circuit within the pass band, as shown in FIG. 2, by selecting the center frequencies.

Specifically, when the absolute value $|dF_0|$ of the frequency difference dF_0 between the center frequencies is represented by $0 < |dF_0|/BW_3 < 0.8$, the group delay characteristics of piezoelectric ceramic filter elements (1) and (2), that are cascade connected and are combined together, result in extremely flat total stage group delay characteristics within the pass band width.

Moreover, unlike the conventional method of the prior art to control the group delay characteristics by keeping the mechanical quality factor Q low, the technology of the present invention does not increase the insertion loss.

FIG. 2 illustrates that the total stage group delay characteristics of the piezoelectric ceramic filter circuit become flat when a particular center frequency difference is selected. In the FIG., the horizontal axis represents frequency (MHz), the left vertical axis represents amplitude (dB) and the right vertical axis represents the G.D.T. (Group Delay Time) (μs).

As shown, the group delay characteristics GDT_1 of a piezoelectric ceramic filter element in which the center frequency is F_{01} and the group delay characteristics GDT_2 of a piezoelectric ceramic filter element in which the center frequency is F_{02}, are combined so that their wave forms interfere. Because of this, the flat group delay characteristics GDT can be obtained. BW_3 refers to the frequency band width which is within 3dB of the maximum value of amplitude loss characteristics (A) of the piezoelectric ceramic filter circuit. Below, further explanation is given by citing actual measured data.

FIG. 3 shows the frequency-amplitude relationship and the group delay characteristics when the center frequency difference dF_0 between center frequencies F_{01} and F_{02} of piezoelectric ceramic filter elements (1) and (2) respectively, is set at 0, 20, 40, 60, 80 and 100 (kHz). The horizontal axis represents frequency (MHz), the left vertical axis represents amplitude (dB) and the right vertical axis represents G.D.T. (Group Delay Time)(μs).

As can be seen, when the center frequency difference dF_0 is 60 kHz ($|dF_0|/BW_3 = 0.33$), the total stage group delay characteristics GDT are more flattened than when the center frequency difference dF_0 is 0 kHz ($|dF_0|/BW_3 = 0$).

Furthermore, when the center frequency difference dF_0 is 100 (kHz) ($|dF_0|/BW_3 = 0.55$) the total stage group delay characteristics are even more flattened than when center frequency difference is dF_0 is 60 kHz. Unlike the conventional method to control the group delay characteristics that keeps the mechanical quality factor Q low, insertion loss with the present invention does not increase.

FIG. 4 shows a plan view of a trapped energy type piezoelectric ceramic filter which comprises a pair of piezoelectric ceramic filter elements formed on the same piezoelectric substrate.

FIG. 5 shows a bottom view of the piezoelectric ceramic filter shown in FIG. 4. In these FIGS., (10) indicates a piezoelectric ceramic substrate. (11) indicates a sheathing made of insulating resin. (20) and (30) indicate filter elements. (21) and (31) indicate connecting electrodes. (22) and (32), and (23) and (33) indicate drive electrodes. (24) and (34) indicate common electrodes. (25) indicates a capacitor electrode. (26) indicates a ground electrode and (40), (41) and (42) indicate lead terminals.

Filter elements (20) and (30) have different center frequencies F_{01} and F_{02} respectively, are cascade connected to each other and satisfy the condition $0 < |dF_0| / BW_3 < 0.8$.

Here, $|dF_0|$ is the absolute value of the frequency difference dF_0 between the center frequencies, and BW_3 is the band width wherein the amplitude loss is 3dB or less.

When the above-mentioned concept of the present invention is applied to a piezoelectric ceramic filter that has trapped energy type filter elements on the same piezoelectric substrate, it is possible to make the filter more compact than a piezoelectric ceramic filter circuit that uses separate piezoelectric ceramic filters. Moreover, the total stage group delay characteristics can be very flat within the pass band without increasing the insertion loss.

FIG. 6 shows the piezoelectric ceramic filter in which one of the filter elements is coated with an insulating substance. The same reference numerals as in FIGS. 4 and 5 indicate the components in common. Reference numeral (100) is an insulating substance.

As shown, an filter element (20) that is coated with the insulating substance (100), has a lowered center frequency F_{01} due to the mass load. Therefore, the center frequency difference dF_0 will be generated between center frequency F_{01} of filter element (20) and center frequency F_{02} of another filter element (30) which unlike filter element (20), is not coated with the insulating substance. Therefore, by selecting the center frequency difference dF_0, based on the difference of mass loads, the total stage group delay characteristics GDT are flattened.

FIG. 7 shows a 2-element type piezoelectric ceramic filter in which a mass load is applied by creating a difference in electrode film thickness between the filter elements.

As can be seen, filter element (20) with drive electrodes (22) and (23) which have thicker films, is subject to a larger mass load than filter element (30) with drive electrodes (32) and (33) which have thinner films, resulting in a lower center frequency F_{01}. Therefore, the center frequency difference dF_0 is generated between filter element (20) with drive electrodes (22) and (23) which have thicker films, and filter element (30) with drive electrodes (32) and (33) which have thinner films. By selecting the center frequency difference dF_0, the total stage group delay characteristics GDT can be flattened.

FIG. 8 shows a piezoelectric ceramic filter in which the thickness of the piezoelectric ceramic substrate is different at the two filter elements. As the resonant frequency of the piezoelectric ceramic substrate is in reverse proportion to its thickness, the center frequency difference dF_0 is generated between center frequency F_{01} of filter element (20) where the piezoelectric ceramic substrate is thin, and center frequency F_{02} of filter element (30) where the piezoelectric ceramic substrate is thick. Depending upon the selected center frequency difference dF_0 based upon this difference in thickness, the total stage group delay characteristics GDT is flattened.

INDUSTRIAL APPLICABILITY

As has been described above, the following effects can be obtained with the present invention:

(a) Unlike the conventional methods for controlling the group delay characteristics that require the mechanical quality factor Q to be kept low, the present invention can provide a piezoelectric ceramic filter circuit wherein the group delay characteristics can be flattened within the pass band without increasing the insertion loss.

(b) The present invention can provide a more compact piezoelectric ceramic filter than that of the prior art in which a piezoelectric ceramic filter circuit is structured by using separate piezoelectric ceramic filters.

CLAIMS

1. (Amended) A piezoelectric ceramic filter circuit comprising a plurality of piezoelectric ceramic filter elements, wherein at least two of said piezoelectric ceramic filter elements have center frequencies different from each other, and are connected in cascade with each other, and satisfy the condition

$$0 < |dF_0| / BW_3 < 0.8;$$

where $|dF_0|$ is the absolute value of the frequency difference dF_0 between the center frequencies of said piezoelectric ceramic filter elements, and BW_3 is the pass band width in which the amplitude loss of each of said piezoelectric ceramic filter elements is 3dB or less.

2. The piezoelectric ceramic filter circuit according to claim 1, wherein said piezoelectric ceramic filter elements are formed on the same piezoelectric ceramic substrate.

3. (Amended) A piezoelectric ceramic filter comprising a plurality of trapped energy type ceramic filter elements on the same piezoelectric ceramic substrate, wherein at least two of said trapped energy type ceramic filter elements have different center frequencies and are connected in cascade with each other, and satisfy the condition

$$0 < |dF_0| / BW_3 < 0.8;$$

where $|dF_0|$ is the absolute value of the frequency difference dF_0 between the center frequencies of said trapped energy type ceramic filter elements, and BW_3 is the pass band width in which the amplitude loss of each of said piezoelectric ceramic filter elements is 3dB or less.

4. The piezoelectric ceramic filter according to claim 3, wherein said trapped energy type ceramic filter elements have different mass loads from each other.

5. The piezoelectric ceramic filter according to claim 4, wherein said mass loads on said trapped energy type ceramic filter elements comprise a coating of insulating substance.

6. The piezoelectric ceramic filter according to claim 4, wherein said mass loads on said trapped energy type ceramic filter elements are effectuated by a difference in film thickness of the electrodes.

7. The piezoelectric ceramic filter according to claim 3, wherein the thickness of the piezoelectric ceramic substrate for each of said trapped energy type ceramic filter elements is different.

FIG. 1

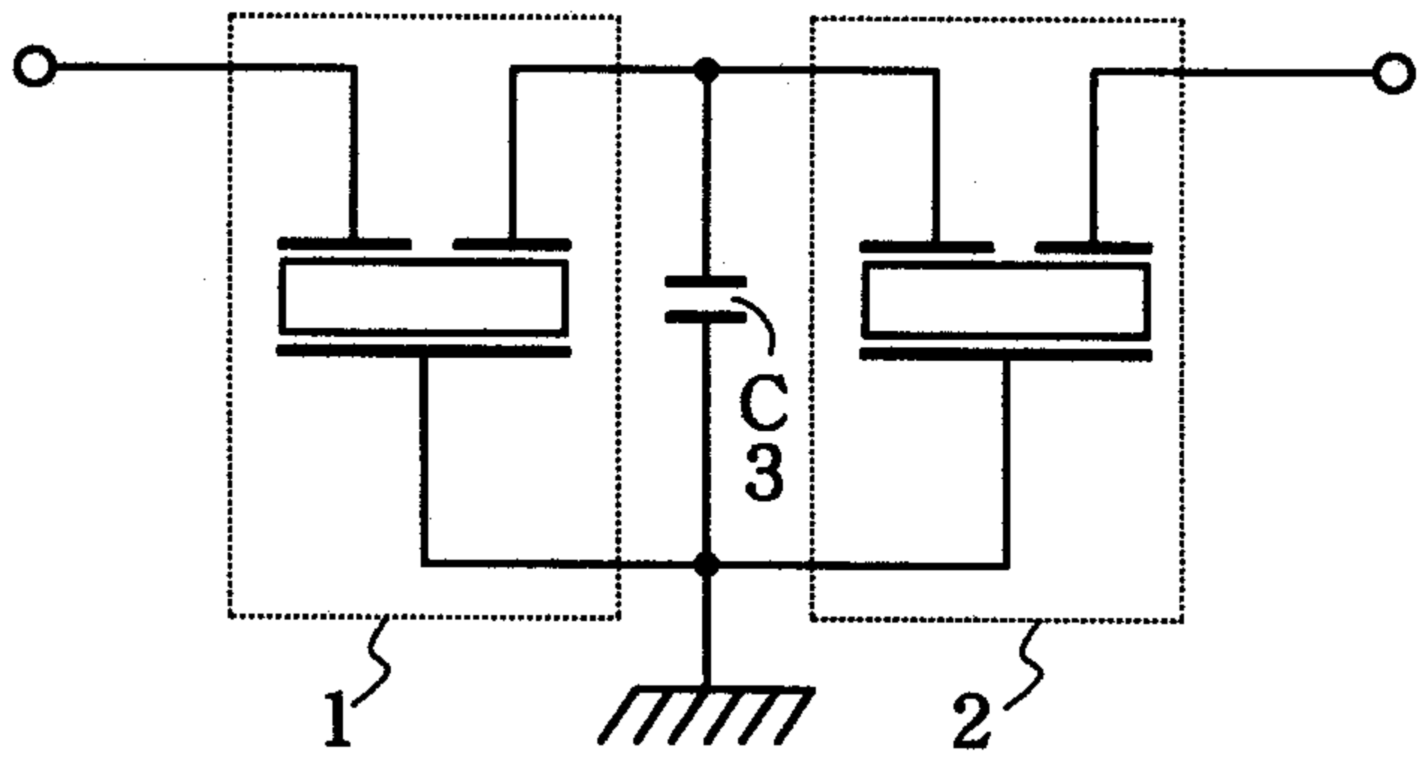
C
3
1
2

FIG. 2

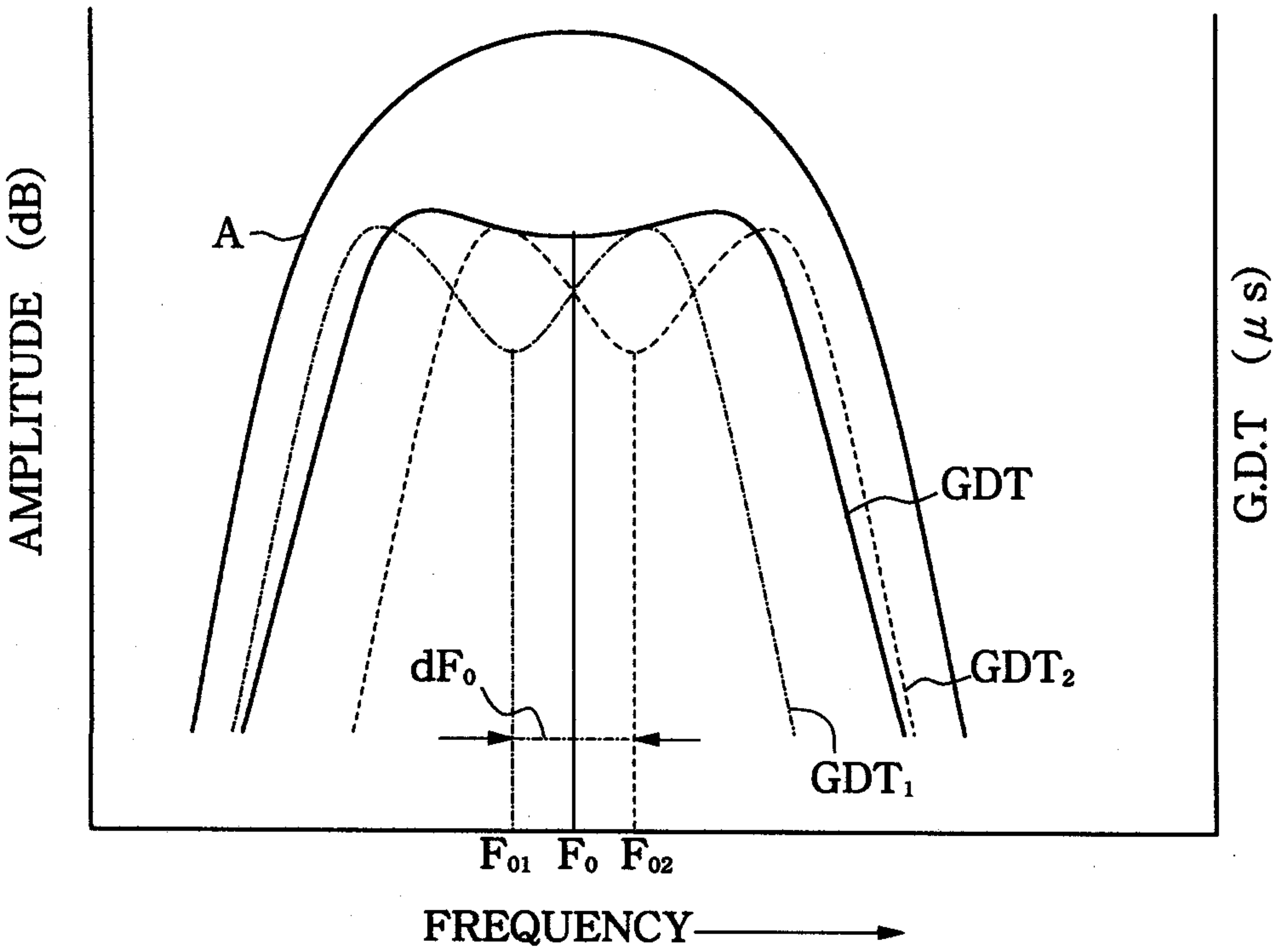
AMPLITUDE (dB)
G.D.T (μs)
A
GDT
GDT2
GDT1
dF0
F01 F0 F02
FREQUENCY

FIG. 3

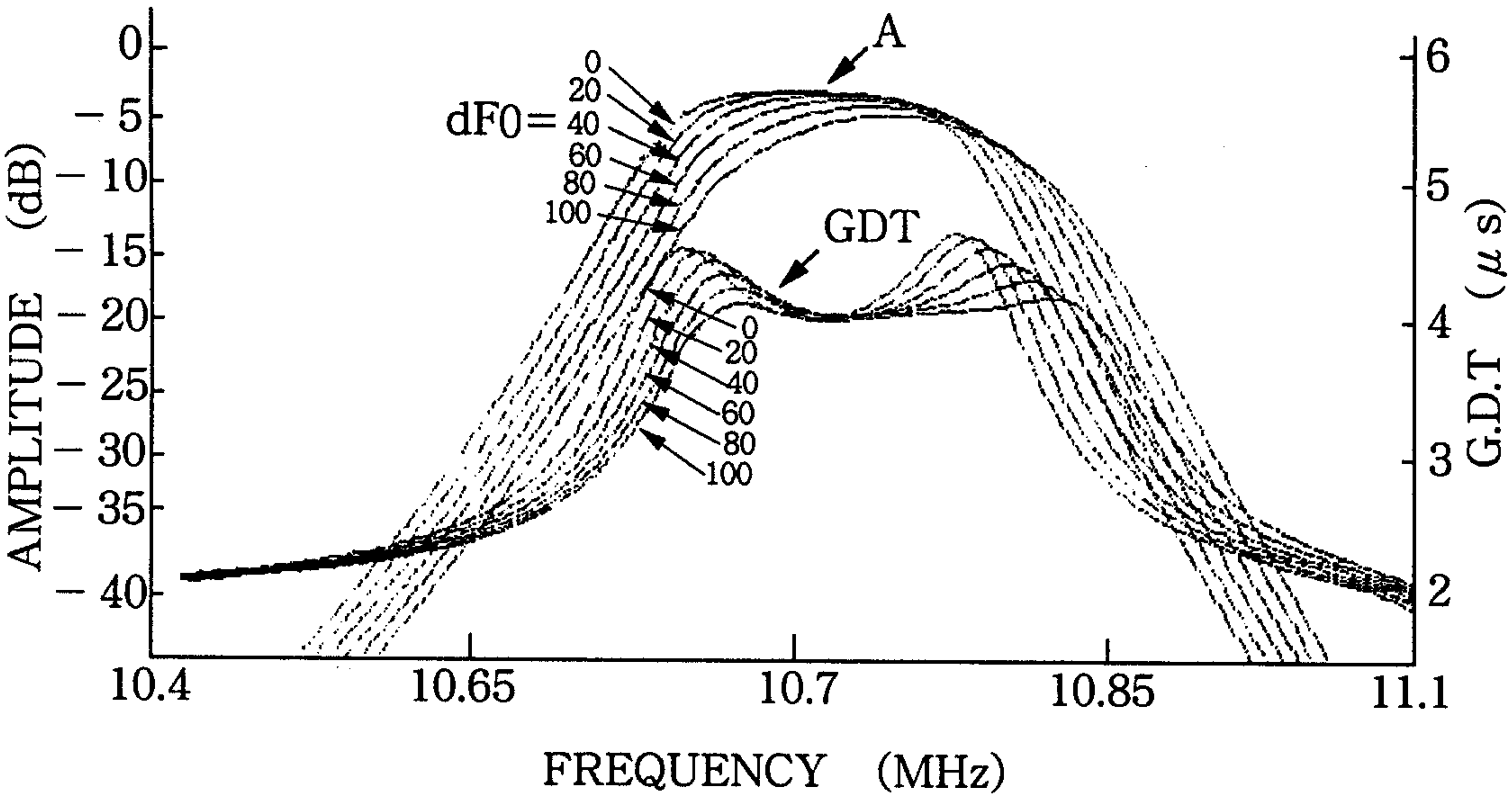
A
dF0=
0
20
40
60
80
100
GDT
0
20
40
60
80
100
AMPLITUDE (dB)
0
- 5
- 10
- 15
- 20
- 25
- 30
- 35
- 40
6
5
4
3
2
G.D.T (μ s)
10.4
10.65
10.7
10.85
11.1
FREQUENCY (MHz)

FIG. 4

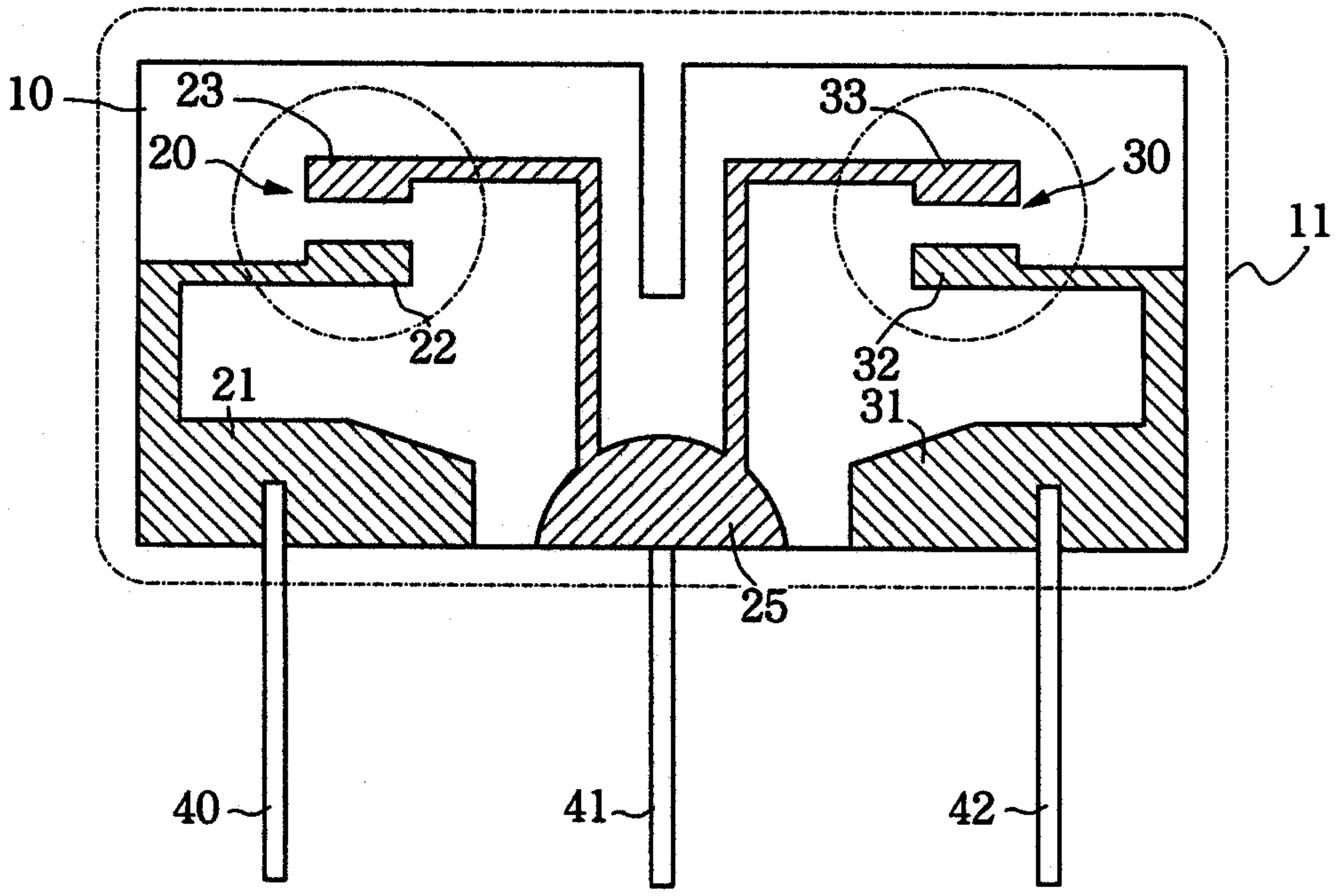

FIG. 5

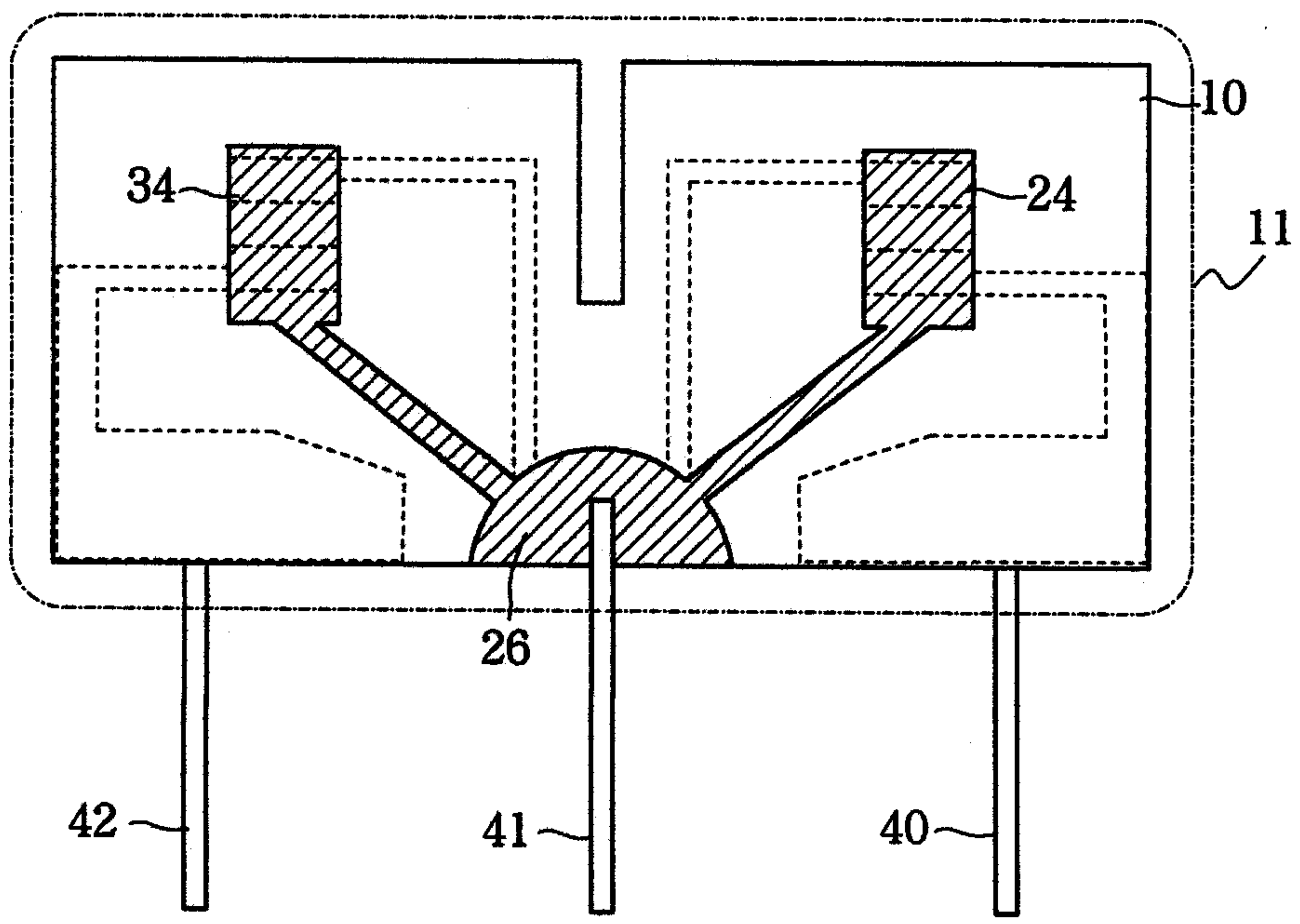

FIG. 6

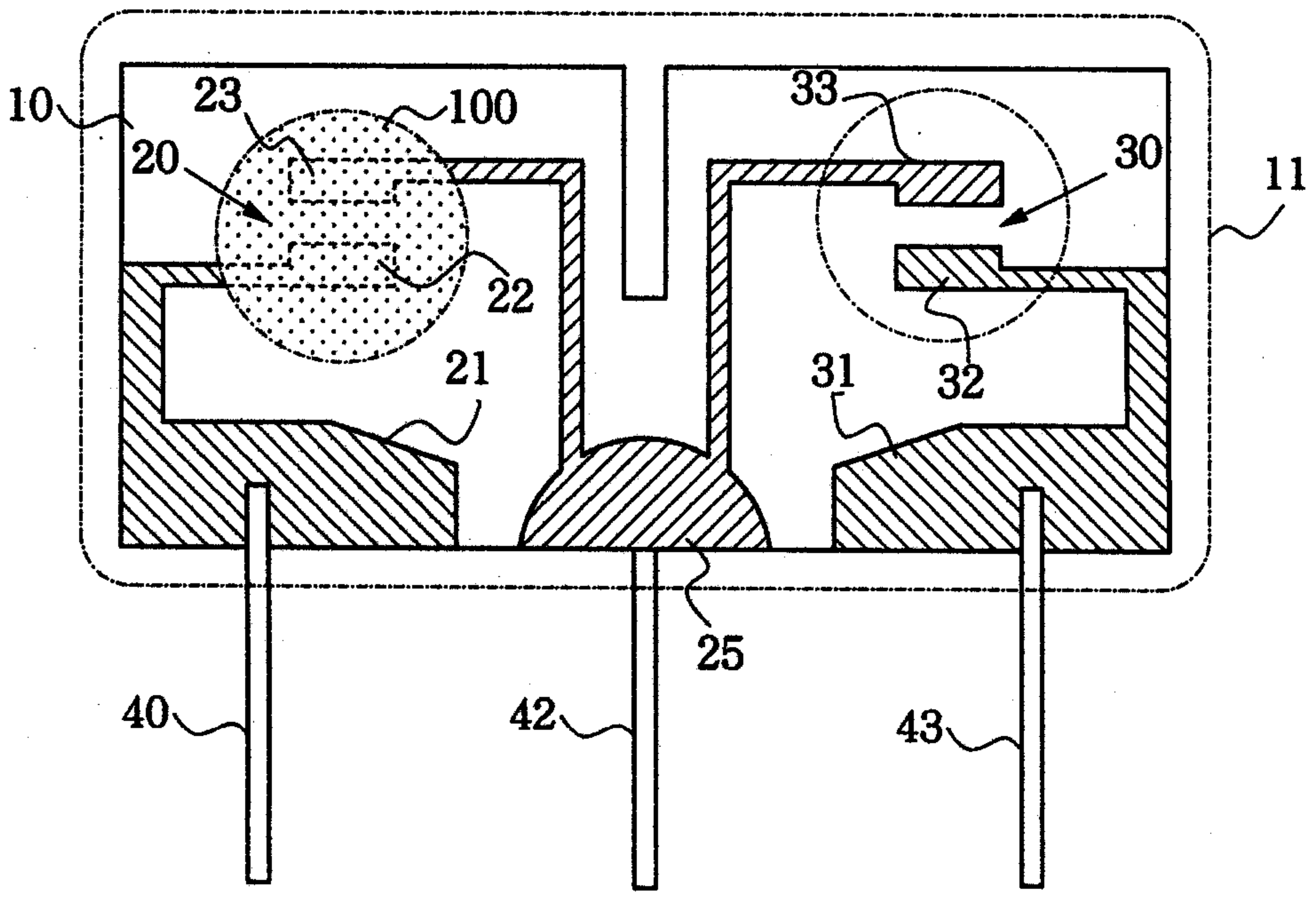
10
23
100
33
30
20
11
22
21
31
32
25
40
42
43

FIG. 7

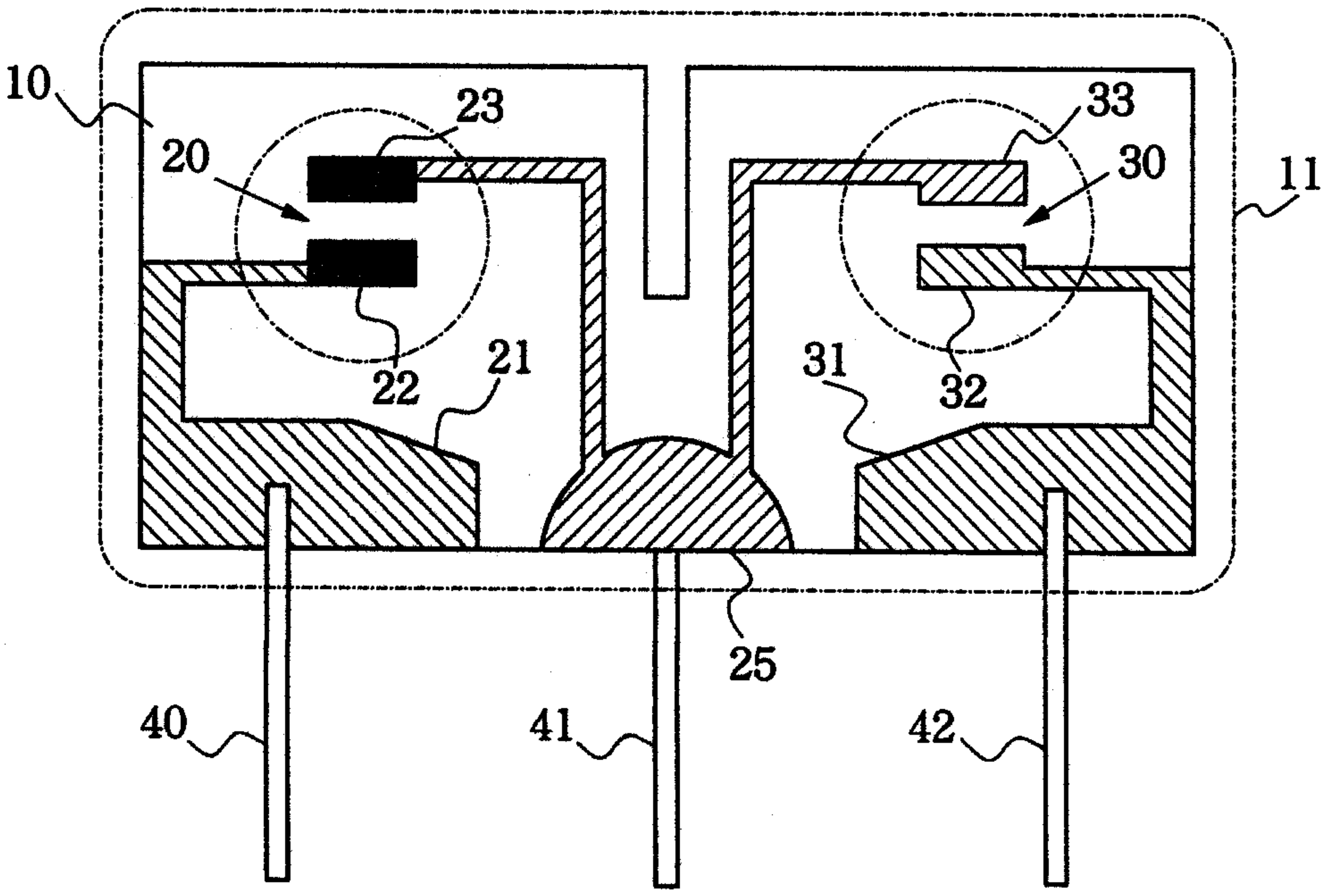
10
23
33
20
30
11
21
31
22
32
25
40
41
42

FIG. 8