



- (51) **International Patent Classification:**
H02M 1/42 (2007.01) *H05B 33/00* (2006.01)
- (21) **International Application Number:**
PCT/US2015/039651
- (22) **International Filing Date:**
9 July 2015 (09.07.2015)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
201410352820.7 23 July 2014 (23.07.2014) CN
- (71) **Applicant:** **GE LIGHTING SOLUTIONS, LLC**
[US/US]; 1975 Noble Road, Bldg. 338, Nela Park, East
Cleveland, OH 44112 (US).
- (72) **Inventors:** **WEI, Hongbin**; 1800 Cai Lun Road Zhangji-
ang Hi-Tech Park, Shanghai, Shanghai, 201203 (CN).
ZHANG, Youmin; 1800 Cai Lun Road Zhangjiang Hi-
Tech Park, Shanghai, Shanghai, 201203 (CN). **NI, Qian**;
1800 Cai Lun Road Zhangjiang Hi-Tech Park, Shanghai,
Shanghai, 201203 (CN). **YAO, Gang**; 1975 Noble Road,
East Cleveland, OH 44112 (US).
- (74) **Agents:** **DIMAURO, Peter, T.** et al.; GENERAL ELEC-
TRIC COMPANY, Global Patent Operation, 3135 Easton
Turnpike, Fairfield, CT 06828 (US).

(81) **Designated States** (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,
MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,
PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,
SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ,
TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,
TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,
DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a
patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the
earlier application (Rule 4.17(iii))

[Continued on next page]

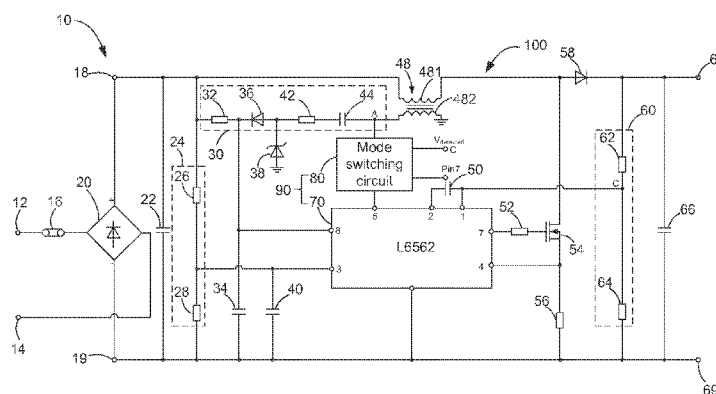
(54) Title: POWER FACTOR CORRECTION APPARATUS

FIG. 1

(57) **Abstract:** A circuit is provided. The circuit includes a DC/DC converter 100 and a power factor correction apparatus. The DC/DC converter 100 is for converting a rectified line power into an output power. The DC/DC converter 100 includes a first inductor and a converting switch. The power factor correction apparatus includes a mode switching circuit and a switch controller. The mode switching circuit is for comparing a detected signal of the output power with a threshold signal and outputting a ZCD signal. The switch controller coupled with the mode switching circuit for driving the converting switch based on the ZCD signal. When the detected signal is beyond the threshold signal, first switch signal is generated. When the detected signal is not beyond the threshold signal, a second switch signal is generated.

Published:

— *with international search report (Art. 21(3))*

POWER FACTOR CORRECTION APPARATUS

BACKGROUND

[0001] Embodiments of the invention relate generally to power factor correction in voltage applications, and more particularly to circuits and methods to apply a power factor correction apparatus to wide range applications.

[0002] Power factor (PF) is the ratio of the actual output power and the apparent power drawn from the power source, so that PF of one is desirable. Power factor correction (PFC) pre-regulators are used in various voltage/power applications so that a quasi-sinusoidal current is drawn in-phase with the line voltage, thereby achieving a power factor (PF) of very close to one. A common technique for achieving PFC in low power applications such as lamp ballasts and low-end monitors is the transition mode (TM) control. TM control is used in many different PFC integrated circuit (IC) products such as STL6561, FAN7527B, TDA4862, TDA4863, MC33260, MC33262, UC3852, SG6561, and the like.

[0003] However, since boost circuit is widely used in the dimming circuit, the boost circuit is controlled to be operated at the TM with peak current control in order to save cost and have a high PF and a low Total Harmonic Distortion (THD). When the boost circuit is operated at a high line input and the load is operated at a deep dimming mode when a lower output power is needed, the current flowing through the boost circuit is small. Furthermore, the DC capacitor stores much energy in the high line input can't be fully discharged in this case especially when the input AC current passes through zero due to a short ON time of the switch signal generated at the TM. This will cause poor PF and THD.

[0004] Usually, the IC can achieve good PF and THD for one fixed load with wide input voltage. For example, a boost circuit IC STL6561 can achieve $PF > 0.9$ and $THD < 20\%$. However, the problem is that the PF and THD will get worse when the load is

also changed for a wide range. For example, from full power load to 3% of the full power load.

[0005] Therefore, there is a need for providing a new circuit or method to solve at least one of the above problems.

BRIEF DESCRIPTION

[0006] In accordance with an embodiment of the invention, a circuit is provided. The circuit includes a DC/DC converter and a power factor correction apparatus. The DC/DC converter is for converting a rectified line power at input terminals into an output power at output terminals. The DC/DC converter includes a first inductor and a converting switch. The first inductor is electrically coupled with one of the input terminals and the converting switch. The power factor correction apparatus includes a mode switching circuit and a switch controller. The mode switching circuit is for comparing a detected signal of the output power with a threshold signal and outputting a ZCD signal. The switch controller is coupled with the mode switching circuit for driving the converting switch based on the ZCD signal. When the detected signal is beyond the threshold signal, the switch controller is for generating a first switch signal provided to the converting switch and ON time of the first switch signal of each cycle is fixed. When the detected signal is not beyond the threshold signal, the switch controller is for generating a second switch signal provided to the converting switch and OFF time of the second switch signal of each cycle is fixed.

[0007] In accordance with another embodiment of the invention, a power factor correction apparatus is provided. The power factor correction apparatus includes a mode switching circuit and a switch controller. The mode switching circuit is for comparing a detected signal of an output power of a DC/DC converter with a threshold signal and outputting a ZCD signal. The switch controller is coupled with the mode switching circuit for driving a converting switch of the DC/DC converter based on the ZCD signal. When the detected signal is beyond the threshold signal, the switch controller is for

generating a first switch signal provided to the converting switch and ON time of the first switch signal of each cycle is fixed. When the detected signal is not beyond the threshold signal, the switch controller is for generating a second switch signal provided to the converting switch and OFF time of the second switch signal of each cycle is fixed.

[0008] In accordance with another embodiment of the invention, a method is provided. The method includes detecting an output power of a DC/DC converter to generate a detected signal thereof. The method includes comparing the detected signal with a threshold signal. The method includes driving a converting switch of the DC/DC converter in at least two conditions. When the detected signal is beyond the threshold signal, providing a first switch signal to the converting switch, ON time of the first switch signal of each cycle is fixed. When the detected signal is not beyond the threshold signal, providing a second switch signal to the converting switch, OFF time of the second switch signal of each cycle is fixed.

DRAWINGS

[0009] These and other features, aspects, and advantages of the present invention will become better understood when the following detailed description is read with reference to the accompanying drawings in which like characters represent like parts throughout the drawings, wherein:

[0010] FIG. 1 is a schematic diagram of a circuit in accordance with one exemplary embodiment;

[0011] FIG. 2 is a schematic diagram of a mode switching circuit of the circuit of FIG. 1 in accordance with one exemplary embodiment;

[0012] FIG. 3 is a schematic diagram of the circuit of FIG. 1 including a first external unit of FIG. 2 in accordance with one exemplary embodiment;

[0013] FIG. 4 is a waveform view of a first switch signal in accordance with one exemplary embodiment;

[0014] FIG. 5 is a schematic diagram of the circuit of FIG. 1 including a second external unit of FIG. 2 in accordance with one exemplary embodiment;

[0015] FIG. 6 is a waveform view of a second switch signal in accordance with one exemplary embodiment;

[0016] FIG. 7 is a waveform view of an input AC current of the circuit of FIG. 1 having a lower output power in accordance with one exemplary embodiment;

[0017] FIG. 8 is a waveform view of an input AC current of the circuit of FIG. 1 having a higher output power in accordance with one exemplary embodiment; and

[0018] FIG. 9 is a flowchart of a method for operating a circuit in accordance with one exemplary embodiment.

DETAILED DESCRIPTION

[0019] Unless defined otherwise, technical and scientific terms used herein have the same meaning as is commonly understood by one of ordinary skill in the art to which this invention belongs. The terms “first”, “second”, and the like, as used herein do not denote any order, quantity, or importance, but rather are used to distinguish one element from another. Also, the terms “a” and “an” do not denote a limitation of quantity, but rather denote the presence of at least one of the referenced items, unless otherwise noted, are merely used for convenience of description, and are not limited to any one position or spatial orientation.

[0020] Referring to FIG. 1, a schematic view of a circuit 10 in accordance with one exemplary embodiment is shown. The circuit 10 includes a DC/DC converter 100, for example, a boost converter. In another embodiment, the DC/DC converter 100 includes a buck converter, a cuk converter and the like.

[0021] The circuit 10 further includes a bridge circuit 20 for delivering a rectified line power to input terminals 18 and 19 of the DC/DC converter 100. The DC/DC converter 100 is configured to convert the rectified line power into an output power at output terminals 68 and 69 for providing to a load. The DC/DC converter 100 includes a first inductor 481 (in this case, a primary winding of a transformer 48), a diode 58, a converting switch 54 and an output capacitor 66. The first inductor 481 is electrically coupled with an input terminal 18 and the converting switch 54. The converting switch 54 is coupled with the output terminals 68 and 69. The converting switch 54 includes a MOSFET, an IGBT or the like.

[0022] The circuit 10 further includes a power factor correction (PFC) apparatus 90. The purpose of the PFC apparatus 90 is to shape an input sinusoidal current at terminals 12 and 14 to be in-phase with an input sinusoidal voltage as well as regulate the output voltage. The PFC apparatus 90 includes a mode switching circuit 80 and a switch controller 70.

[0023] In the illustrated embodiment, the switch controller 70 includes an integrated circuit (IC). As an example, a product number L6562 is used as the switch controller 70. In other embodiments, other products L6561, MC34262 and the like can be employed as the switch controller 70. The switch controller 70 is configured to receive a plurality of electrical signals from the DC/DC converter 100 and for generate a switch signal to the converting switch 54.

[0024] The input sinusoidal voltage at the terminals 12 and 14 is applied across the bridge circuit 20 through a fuse 16. The rectified line power from the bridge circuit 20 at the input terminals 18 and 19 is filtered by a capacitor 22 and applied across a voltage divider 30 having a resistor 32, a diode 36, a resistor 42, a capacitor 44, and a second inductor 482 (in this case, a secondary winding of the transformer 48) coupled in series. The second inductor 482 is electromagnetically coupled with the first inductor 481 for allowing a second inductor voltage thereof to be induced by the first inductor 481.

[0025] The voltage in the voltage divider 30 between the resistor 32 and the diode 36 is applied to Vcc pin 8 of the switch controller 70, and a Vcc input signal is used to power the switch controller 70. A capacitor 34 is coupled to Vcc pin 8 for filtering.

[0026] The converting switch 54 (e.g., a MOSFET) along with a resistor 56 forms a controlled power switch path coupled between the first inductor 481 and ground for charging or discharging the first inductor 481. The gate of the converting switch 54 is controlled by an output GD pin 7 of the switch controller 70 as a function of various input signals at multiple input pins of the switch controller 70. These pins include a ZCD pin 5, a COMP pin 2, an INV pin 1, and a MULT pin 3.

[0027] The ZCD pin 5 is coupled to the second inductor 482 via the mode switching circuit 80 for the purpose of zero current detection and triggering a turn on and a turn off of the converting switch 54. Initially, the switch controller 70 generates a start-up signal at the output GD pin 7 which switches on the converting switch 54. Thereafter, the switch controller 70 generates a switch signal at the output GD pin 7 to switch on the converting switch 54 based on the external circuits coupled with the switch controller 70.

[0028] The COMP pin 2 and the INV pin 1 are coupled to an intermediate node between resistors 62 and 64 in a voltage divider 60 coupled with the output terminals 68 and 69. The switch controller 70 compares a sensed signal of the output voltage at the terminals 68 and 69 with an internal reference voltage to maintain the output voltage constant by turning on and turning off the converting switch 54. A feedback capacitor 50 is coupled between the pins 1 and 2 for frequency compensation. A voltage across the resistor 56 is applied to the CS pin 4 to determine a time when the converting switch 54 is switched off.

[0029] The MULT pin 3 is coupled to an intermediate node between the resistors 26 and 28 in a voltage divider 24 for receiving a portion of the rectified line power. A MULT input signal at the MULT pin 3 is configured to set a peak current of the

converting switch 54. Typically, the MULT input signal is shaped like a rectified sinusoid. A capacitor 40 is coupled to the MULT pin 3 for filtering.

[0030] The mode switching circuit 80 is coupled with the switch controller 70 and works together with the switch controller 70 to keep the circuit 10 have a high PF and a low THD. More specifically, the mode switching circuit 80 is coupled with the second inductor 482, the gate of the converting switch 54 and the ZCD pin 5 of the switch controller 70 for receiving a detected signal V_{detected} of the output power. The mode switching circuit 80 is configured to compare the detected signal V_{detected} with a threshold signal $V_{\text{threshold}}$ and output a zero current detection (ZCD) signal to the ZCD pin 5. The switch controller 70 is for driving the converting switch 54 based on the ZCD signal.

[0031] Referring to FIG. 2, a schematic diagram of the mode switching circuit 80 of the circuit 10 of FIG. 1 in accordance with one exemplary embodiment is shown. The mode switching circuit 80 includes a mode decision unit 800, a first external unit 810 and a second external unit 820. The mode decision unit 800 is configured to determine one of the first external unit 810 and the second external unit 820 to generate the ZCD signal.

[0032] The mode decision unit 800 receives the detected signal V_{detected} . The detected signal V_{detected} is proportional to the output power. Since the output voltage of the output power is maintained constant, the output power is proportional to an output current or the current flowed through the first inductor 481 or the second inductor 482. Therefore, in one embodiment, a power sensor (e.g., a power detection circuit) can be used to detect the output power directly and output the detected signal V_{detected} . In another embodiment, a current sensor (e.g., a diode) coupled with the first inductor 481 or the second inductor 482 can also be used to output the detected signal V_{detected} .

[0033] The mode decision unit 800 delivers the detected signal V_{detected} to a threshold device 804. The threshold device 804 is configured to determine the threshold signal. As an example, the detected signal V_{detected} is delivered to a cathode of a Zener diode 804, and an anode of the Zener diode 804 is coupled to a gate of an external switch 806 (e.g., a

MOSFET). A reverse breakdown voltage of Zener diode 804 is configured to determine the threshold signal.

[0034] A resistor 801 and a resistor 803 are used as a voltage divider and limit a current flowed through the Zener diode 804 so as to protect the Zener diode 804 from being damaged. A capacitor 802 is coupled with an intermediate node between the resistor 801 and the Zener diode 804, the ground for filtering.

[0035] When the detected signal V_{detected} is beyond the threshold signal $V_{\text{threshold}}$, a voltage across the Zener diode 804 is kept at a constant value (e.g., 6V). Under this circumstance, a current flowing through the Zener diode 804 is injected into the external switch 806 and a voltage is added to the external switch 806, then the external switch 806 is switched on. An anode of a diode 826 of the second external unit 820 is coupled with a drain of the external switch 806. When the external switch 806 is switched on, a voltage level at the anode of the diode 826 is zero. As a result, the second external unit 820 is blocked and no electrical signal from the gate of the converting switch 54 (the pin 7 of the switch controller 70) flows into the ZCD pin 5. The first external unit 810 is configured to deliver the second inductor voltage from the point A to the ZCD pin 5 as the ZCD signal. In this case, the first external unit 810 is configured to provide the ZCD signal and the switch controller 70 is configured to generate a first switch signal to the converting switch 54 and ON time of the first switch signal of each cycle is fixed. How the first switch signal is generated will be illustrated in FIG. 3 and FIG. 4.

[0036] When the detected signal V_{detected} is not beyond the threshold signal $V_{\text{threshold}}$, the Zener diode 804 is blocked and the external switch 806 is switched off. The resistor 805 and the external switch 806 or the Zener diode 804, the resistor 803 and the external switch 806 can form a circuit path for dissipating the power in the external switch 806. The first external unit 810 is blocked and no electrical signal from the point A flows into the ZCD pin 5. The second external unit 820 is configured to deliver a driving voltage from the gate of the converting switch 54 to the ZCD pin 5 as the ZCD signal. In this case, the second external unit 820 is configured to provide the ZCD signal and the switch

controller 70 is configured to generate a second switch signal to the converting switch 54 and OFF time of the second switch signal of each cycle is fixed. How the second switch signal is generated will be illustrated in FIG. 5 and FIG. 6.

[0037] Wherein the detected signal V_{detected} is proportional to the output power P_{output} at the two terminals 68 and 70, the threshold signal $V_{\text{threshold}}$ represents a critical value of the load power. At the critical value of the load power, the switch signal provided to the converting switch 54 is switched from the first switch signal to the second switch signal or switched from the second switch signal to the first switch signal. In the illustrated embodiment, the detected signal $V_{\text{threshold}}$ represents 20% of the full load power P_{full} . In the illustrated embodiment, when $V_{\text{detected}} > V_{\text{threshold}}$ ($P_{\text{output}} > 20\%P_{\text{full}}$), the switch controller 70 is configured to generate the first switch signal which can ensure a high PF and THD based on the ZCD signal generated by the first external unit 810. When $V_{\text{detected}} \leq V_{\text{threshold}}$ ($P_{\text{output}} \leq 20\%P_{\text{full}}$), the switch controller 70 is configured to generate the second switch signal which can ensure a high PF and THD based on the ZCD signal generated by the second external unit 820.

[0038] Referring to FIG. 3, a schematic diagram of the circuit of FIG. 1 including the first external unit 810 of FIG. 2 in accordance with one exemplary embodiment is shown. When $V_{\text{detected}} > V_{\text{threshold}}$, the first external unit 810 for generating the ZCD signal is illustrated above. Therefore, the mode decision unit 800 and the second external unit 820 are not shown in this embodiment when describing how the first external unit 810 is employed to generate the first switch signal. In the illustrated embodiment, the first external unit 810 includes a resistor.

[0039] An error amplifier (VA) 701 of the switch controller 70 compares the sensed signal V_{output} of the output voltage with a reference V_{REF} and generates an error signal V_c proportional to a difference thereof. V_{REF} is proportional to a desirable output voltage of the load (e.g., the LED). Usually, V_{REF} can be generated by an external switch knob.

[0040] A sensed voltage V_{MULT} of the input voltage is detected and provided to the MULT pin 3 of the switch controller 70. The sensed voltage V_{MULT} and the error signal V_c are delivered into inputs of a multiplier 703 and a rectified sinusoid signal V_{CSREF} represents a sinusoidal reference for PWM modulation is generated. The amplitude of the rectified sinusoid signal V_{CSREF} is proportional to that of the sensed voltage V_{MULT} and the error signal V_c . The rectified sinusoid signal V_{CSREF} represents a peak current of the converting switch 54 as shown in FIG. 4.

[0041] The rectified sinusoid signal V_{CSREF} is delivered into an inverting input of a comparator 705 and a non-inverting input of the comparator 705 receives a voltage V_{cs} on the resistor 56. The voltage V_{cs} is proportional to a current flowing through the converting switch 54 and the first inductor 481 during the ON time of the converting switch 54. The comparator 705 compares the voltage V_{cs} with the rectified sinusoid signal V_{CSREF} and outputs a high voltage signal to a reset terminal R of a flip-flop 707 when the voltage V_{cs} reaches the rectified sinusoid signal V_{CSREF} . Accordingly, the flip-flop 707 outputs an OFF signal as shown in FIG. 4 at an output terminal Q to switch off the converting switch 54. A driver 713 is coupled with the gate of the converting switch 54 and the driver 713 receives the OFF signal from the flip-flop 707 to switch off the converting switch 54. Then, the current of the first inductor 481 gradually decreases.

[0042] The current of the first inductor 481 or the converting switch 54 is sensed by the second inductor 482 via the resistor 810, the second inductor voltage of the second inductor 482 is inputted as the ZCD signal V_{ZCD} to a ZCD unit 709 (e.g., a comparator) via the ZCD pin 5. The ZCD unit 709 is configured to compare V_{ZCD} with a reference voltage V_{th} . The reference voltage V_{th} is set at the value of zero. When V_{ZCD} reaches zero, a set terminal S of the flip-flop 707 switches to a high voltage signal. Accordingly, the flip-flop 707 outputs an ON signal as shown in FIG. 4 at the output terminal Q to switch on the converting switch 54.

[0043] The ON time of the first switch signal over each switching cycle is fixed due to the physical characteristic of the first inductor 481. Eventually, the input current

follows the input voltage at the terminals 12 and 14, and the DC/DC converter 100 is operated based on the first switch signal.

[0044] Usually, if the detected signal V_{detected} is beyond the threshold signal $V_{\text{threshold}}$, the ON time in a switching cycle is long enough to discharge the energy stored in the capacitor 22 when the input AC current at the two terminals 12 and 14 passes zero, and a corresponding high PF and THD can be obtained. In the illustrated embodiment, the threshold signal $V_{\text{threshold}}$ represents 20% of the full load power P_{full} . In another embodiment, the threshold signal can be adjusted according to the parameters of the components of the circuit 10 (e.g., 30% of the full load power). That means when the output power is lowered to a critical value when a poor PF and THD could not be accepted, the corresponding detected signal of the output power can be set as the threshold signal.

[0045] Referring to FIG. 5, a schematic diagram of the circuit of FIG. 1 including the second external unit 820 of FIG. 2 in accordance with one exemplary embodiment is shown. When $V_{\text{detected}} \leq V_{\text{threshold}}$, the second external unit 820 for generating the ZCD signal is illustrated above. Therefore, the mode decision unit 800 and the first external unit 810 are not shown to in this embodiment when describing how the first external unit 810 is employed to generate the first switch signal.

[0046] The second external unit 820 includes a first resistor 824 and a first capacitor 825 coupled in parallel with the ZCD unit 709 and ground. The second external unit 820 further includes a first diode 821 having an anode and a cathode coupled with the gate of the converting switch 54 and the first resistor 824 respectively. A second diode 826 is coupled with the ZCD unit 709 and the first resistor 824. The second external unit 820 further includes a second resistor 822 and a second capacitor 823 coupled in parallel with the ZCD unit 709 and the cathode of the first diode 821.

[0047] The driving voltage of the converting switch 54 is configured to determine the ZCD signal V_{ZCD} . The comparator 709 is configured to compare V_{ZCD} with the reference

voltage V_{th} . The reference voltage V_{th} is set at the value of zero. When V_{ZCD} reaches zero, the set terminal S of the flip-flop 707 switches to a high voltage signal. Accordingly, the flip-flop 707 outputs an ON signal as shown in FIG. 6 at the output terminal Q. The driver 713 coupled with the gate of the converting switch 54 receives the ON signal and the converting switch 54 is switched on.

[0048] During the ON time of the converting switch 54, the driving voltage of the converting switch 54 is a high voltage (e.g., 18V), the first diode 821 is forward-biased and the voltage at the ZCD pin 5 is internally clamped at a clamp voltage V_{clamp} (e.g., 5.7V) by a Zener diode (not shown) inside the switch controller 70. The voltage V_{cs} on the resistor 56 is compared with V_{CSREF} and a high voltage signal is provided to the reset terminal R of the flip-flop 707 when the voltage V_{cs} reaches V_{CSREF} . Accordingly, the flip-flop 707 outputs an OFF signal as shown in FIG. 6 at the output terminal Q. The driver 713 receives the OFF signal and the converting switch 54 is switched off.

[0049] During the OFF time of the converting switch 54, the driving voltage of the converting switch 54 is a low voltage, the first diode 821 is reverse-biased and the voltage at the ZCD pin 5 decays with an exponential law:

$$V_{ZCD} = V_{clamp} e^{\frac{-t}{RC}} \quad (1),$$

[0050] Wherein R refers to as a resistance of the first resistor 824 and C refers to as a capacitance of the first capacitor 825. Until V_{ZCD} reaches V_{th} , the ON signal is generated. The period when the ZCD signal is decreased from V_{clamp} to V_{th} defines the duration of the OFF time T_{OFF} :

$$T_{OFF} = RC \ln \frac{V_{clamp}}{V_{th}} \quad (2),$$

[0051] Therefore, T_{OFF} is determined by the first resistor 824 and the first capacitor 825 and T_{OFF} is fixed for a particular application. T_{OFF} can be set by regulating the first resistor 824 and the first capacitor 825. When $V_{detected} \leq V_{threshold}$, the OFF time in a

switching cycle of the second switch signal is set to be a small value and the ON time in the switching cycle of the second switch signal is long enough to discharge the energy stored in the capacitor 22, a corresponding high PF and low THD can be obtained when the input AC current passes zero.

[0052] Referring back to FIG. 5, when working at high rectified line power/light load, the ON time of the converting switch 54 becomes very short and the second resistor 822 alone is no more able to charge the first capacitor 825 to V_{clamp} . The second capacitor 823 is then used in parallel to the second resistor 822. The second capacitor 823 will cause an almost instantaneous charge of the first capacitor 825 up to a voltage level, after that the second resistor 822 will complete the charge up to V_{clamp} .

[0053] Referring to FIG. 7, a waveform view of an input AC current of the circuit of FIG. 1 having a lower output power in accordance with one exemplary embodiment is shown. The output power of the DC/DC converter 100 as shown in FIG. 1 is 7W at the output voltage of 277V. FIG. 7(A) shows a waveform view of an input AC current of a circuit. The circuit includes the first external unit 810, the switch controller 70 and the DC/DC converter 100 and the power factor correction apparatus 90 is not included. The PF of the circuit is 0.5 and the THD is 58.1%. FIG. 7(B) shows a waveform view of an input AC current of the circuit 10. The PF of the circuit 10 is 0.73 and the THD is 17%.

[0054] Referring to FIG. 8, a waveform view of an input AC current of the circuit of FIG. 1 having a higher output power in accordance with one exemplary embodiment is shown. The output power of the DC/DC converter 100 as shown in FIG. 1 is 100W at the output voltage of 277V. FIG. 8(A) shows a waveform view of an input AC current of a circuit. The circuit includes the first external unit 810, the switch controller 70 and the DC/DC converter 100 and the power factor correction apparatus 90 is not included. The PF of the circuit is 0.99 and the THD is 4%. FIG. 8(B) shows a waveform view of an input AC current of the circuit 10. The PF of the circuit 10 is 0.99 and the THD is 4%.

[0055] Therefore, from FIG. 7 and FIG. 8, it can be seen that by using the power factor correction apparatus 90, the circuit 10 can achieve a high PF and a low THD when the load power changes in a wide range, for example, from 7W to 100W.

[0056] Referring to FIG. 9, a flowchart of a method 900 for operating a circuit in accordance with one exemplary embodiment is shown. The method includes the following steps. At block 901, an output power of a DC/DC converter 100 is detected and a detected signal is output. At block 903, the detected signal V_{detected} is compared with a threshold signal $V_{\text{threshold}}$. When the detected signal V_{detected} is beyond the threshold signal $V_{\text{threshold}}$, the method goes to block 905. When the detected signal V_{detected} is not beyond the threshold signal $V_{\text{threshold}}$, the method goes to block 907. At block 905, a first switch signal is provided to the converting switch 54, ON time of the first switch signal of each cycle is fixed. At block 907, a second switch signal is provided to the converting switch 54, OFF time of the first switch signal of each cycle is fixed

[0057] The details of how to operate the factor correction apparatus 90 has been illustrated in above embodiments. Therefore, the detailed description is omitted here.

[0058] It is to be understood that a skilled artisan will recognize the interchangeability of various features from different embodiments and that the various features described, as well as other known equivalents for each feature, may be mixed and matched by one of ordinary skill in this art to construct additional systems and techniques in accordance with principles of this disclosure. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

[0059] Further, as will be understood by those familiar with the art, the present invention may be embodied in other specific forms without depending from the spirit or essential characteristics thereof. Accordingly, the disclosures and descriptions herein are

intended to be illustrative, but not limiting, of the scope of the invention which is set forth in the following claims.

CLAIMS:

1. A circuit, comprising:

a DC/DC converter for converting a rectified line power at input terminals into an output power at output terminals, and comprising a first inductor and a converting switch, the first inductor being electrically coupled with one of the input terminals and the converting switch; and

a power factor correction apparatus comprising:

a mode switching circuit for comparing a detected signal of the output power with a threshold signal and outputting a ZCD signal; and

a switch controller coupled with the mode switching circuit for driving the converting switch based on the ZCD signal, wherein:

when the detected signal is beyond the threshold signal, the switch controller is for generating a first switch signal provided to the converting switch and ON time of the first switch signal of each cycle is fixed; and

when the detected signal is not beyond the threshold signal, the switch controller is for generating a second switch signal provided to the converting switch and OFF time of the second switch signal of each cycle is fixed.

2. The circuit of claim 1, wherein the mode switching circuit comprises a mode decision unit, a first external unit and a second external unit, the mode decision unit is coupled with the first external unit and the second external unit, and the mode decision unit is for comparing the detected signal with the threshold signal to determine one of the first external unit and the second external unit to generate the ZCD signal.

3. The circuit of claim 2, comprising a second inductor electromagnetically coupled with the first inductor for allowing a second inductor voltage thereof to be

induced by the first inductor, wherein the second inductor voltage is for determining the ZCD signal when the first switch signal is generated and a driving voltage of the converting switch is for determining the ZCD signal when the second switch signal is generated.

4. The circuit of claim 3, wherein:

the switch controller comprises a ZCD unit for receiving the ZCD signal;

the first external unit is coupled with the second inductor and the ZCD unit;

the second external unit is coupled with a gate of the converting switch and the ZCD unit; and

the mode decision unit is for receiving the detected signal.

5. The circuit of claim 4, wherein the first external unit comprises a resistor coupled with the second inductor and the ZCD unit.

6. The circuit of claim 4, wherein the second external unit comprises:

a first resistor and a first capacitor coupled in parallel with the ZCD unit and ground;

a first diode comprises an anode and a cathode coupled with the gate of the converting switch and the first resistor respectively; and

a second diode is coupled with the ZCD unit and the first resistor.

7. The circuit of claim 6, wherein the second external unit comprises a second resistor and a second capacitor coupled in parallel with the ZCD unit and the cathode of the first diode.

8. The circuit of claim 2, wherein the mode decision unit comprises a threshold device and an external switch, the threshold device is coupled with a gate of the external switch for determining the threshold signal and a drain of the external switch is coupled with the ZCD unit.

9. The circuit of claim 8, wherein the threshold device comprises a Zener diode and a breakdown voltage thereof is for determining the threshold signal.

10. The circuit of claim 1, wherein the threshold signal represents 20%~30% of a full load power.

11. A power factor correction apparatus, comprising:

a mode switching circuit for comparing a detected signal of an output power of a DC/DC converter with a threshold signal and outputting a ZCD signal; and

a switch controller coupled with the mode switching circuit for driving a converting switch of the DC/DC converter based on the ZCD signal, wherein:

when the detected signal is beyond the threshold signal, the switch controller is for generating a first switch signal provided to the converting switch and ON time of the first switch signal of each cycle is fixed; and

when the detected signal is not beyond the threshold signal, the switch controller is for generating a second switch signal provided to the converting switch and OFF time of the second switch signal of each cycle is fixed.

12. The power factor correction apparatus of claim 11, wherein the mode switching circuit comprises a mode decision unit, a first external unit and a second external unit, the mode decision unit is coupled with the first external unit and the second external unit, and the mode decision unit is for comparing the detected signal with the threshold signal to determine one of the first external unit and the second external unit to generate the ZCD signal.

13. The power factor correction apparatus of claim 12, wherein:
- the switch controller comprises a ZCD unit for receiving the ZCD signal;
 - the first external unit is coupled with the second inductor and the ZCD unit;
 - the second external unit is coupled with a gate of the converting switch and the ZCD unit; and
 - the mode decision unit is for receiving the detected signal.
14. The power factor correction apparatus of claim 13, wherein the second external unit comprises:
- a first resistor and a first capacitor coupled in parallel with the ZCD unit and ground;
 - a first diode comprises an anode and a cathode coupled with the gate of the converting switch and the first resistor respectively;
 - a second resistor and a second capacitor coupled in parallel with the ZCD unit and the cathode of the first diode; and
 - a second diode is coupled with the ZCD unit and the first resistor.
15. The power factor correction apparatus of claim 13, wherein the mode decision unit comprises a threshold device and an external switch, the threshold device is coupled with a gate of the external switch for determining the threshold signal and a drain of the external switch is coupled with the ZCD unit.
16. The power factor correction apparatus of claim 15, wherein the threshold device comprises a Zener diode and a breakdown voltage thereof is for determining the threshold signal.

17. A method, comprising
- detecting an output power of a DC/DC converter to generate a detected signal thereof;
- comparing the detected signal with a threshold signal; and
- driving a converting switch of the DC/DC converter in at least two conditions:
- when the detected signal is beyond the threshold signal, providing a first switch signal to the converting switch, ON time of the first switch signal of each cycle is fixed; and
- when the detected signal is not beyond the threshold signal, providing a second switch signal to the converting switch, OFF time of the second switch signal of each cycle is fixed.
18. The method of claim 17, comprising:
- applying a second inductor voltage of a second inductor electromagnetically coupled with a first inductor of the DC/DC converter to a ZCD unit of a switch controller when the detected signal is beyond the threshold signal; and
- applying a driving voltage of a converting switch of the DC/DC converter to the ZCD unit when the detected signal is not beyond the threshold signal.
19. The method of claim 17, comprising determining the threshold signal by a reverse breakdown voltage of a Zener diode.
20. The method of claim 17, comprising:
- injecting a current to an external switch to allow the switch controller to work together with a first external unit for generating the first switch signal; and

allowing the switch controller to work together with a second external unit for generating the second switch signal.

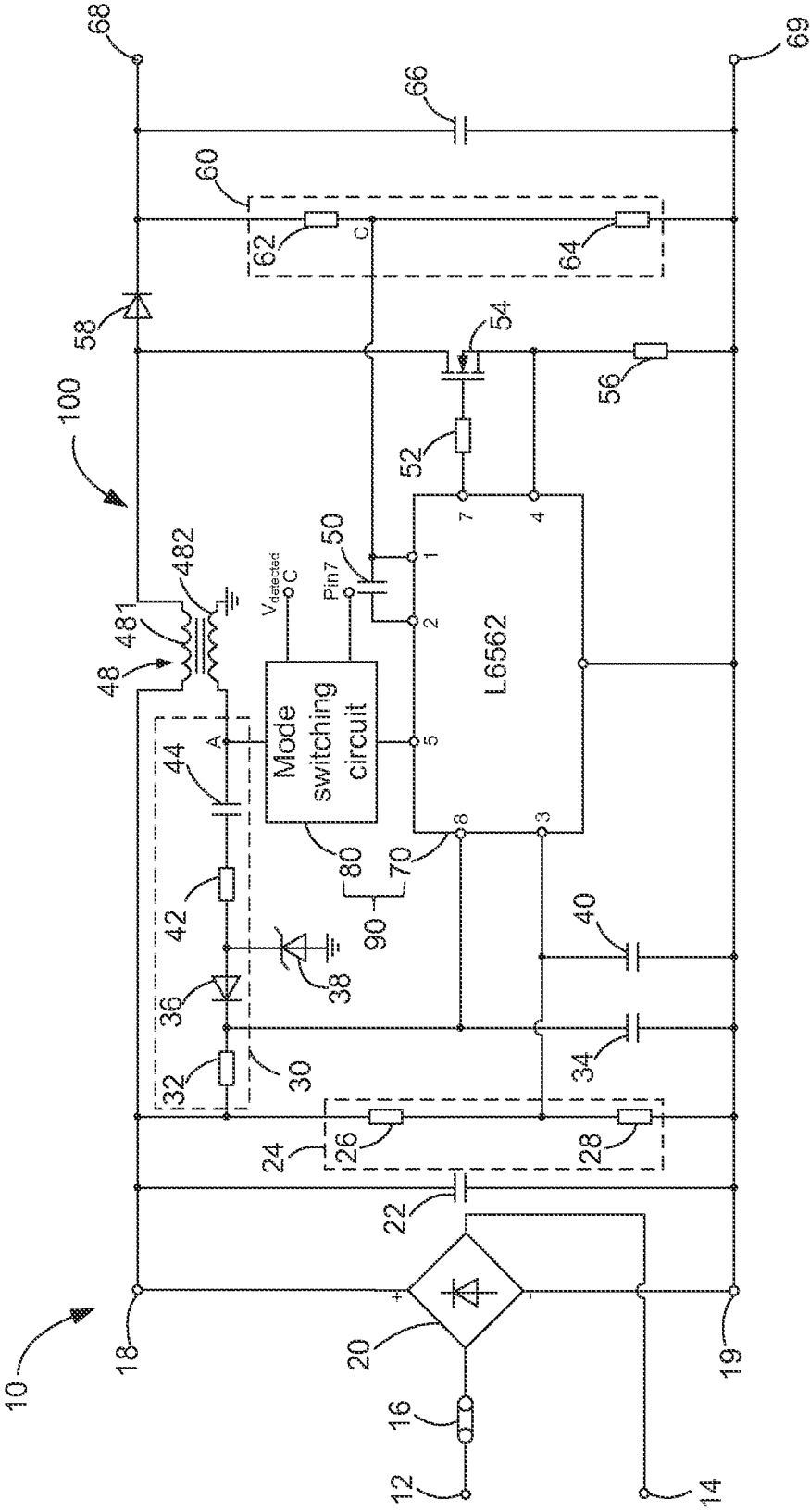


FIG. 1

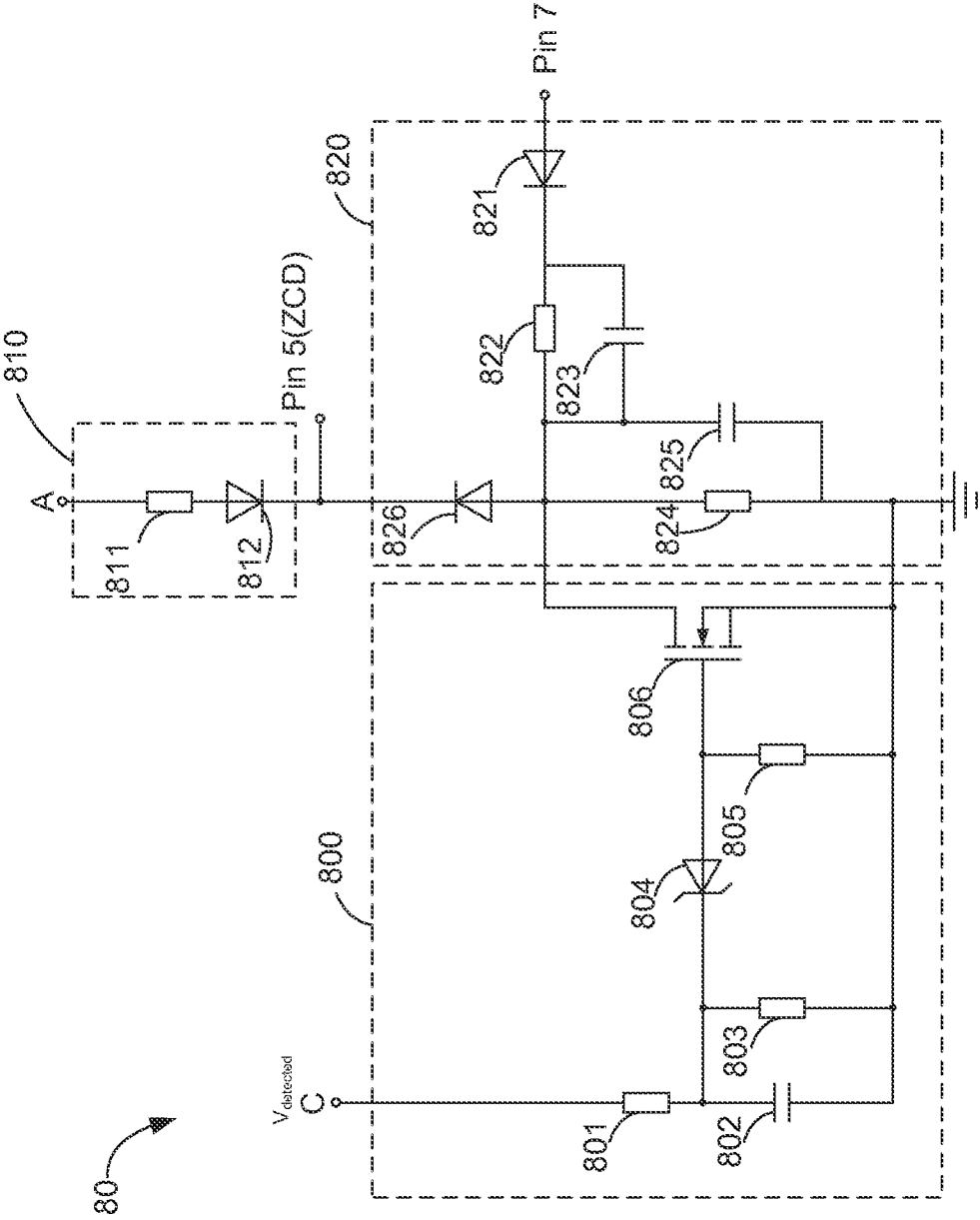


FIG. 2

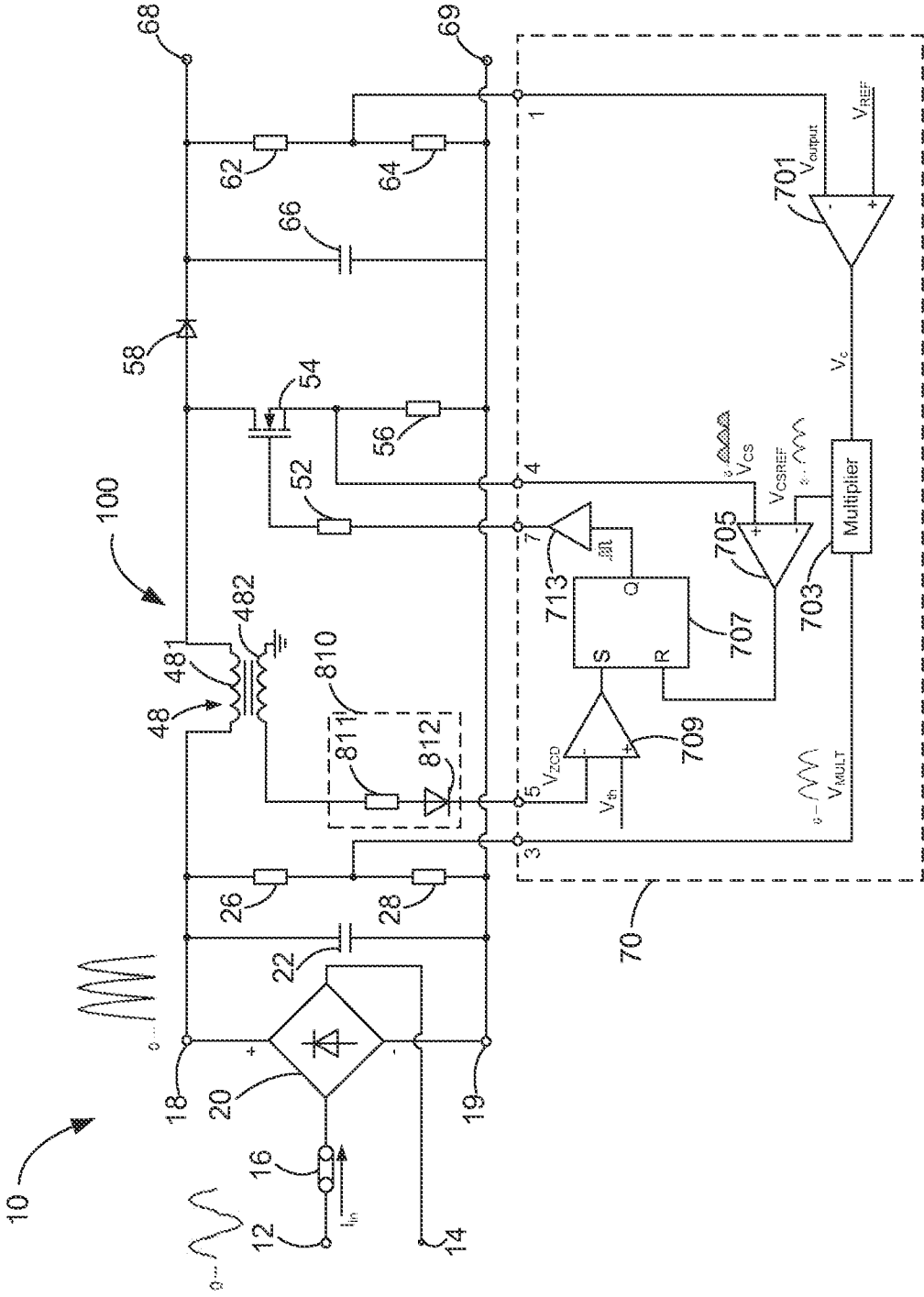


FIG. 3

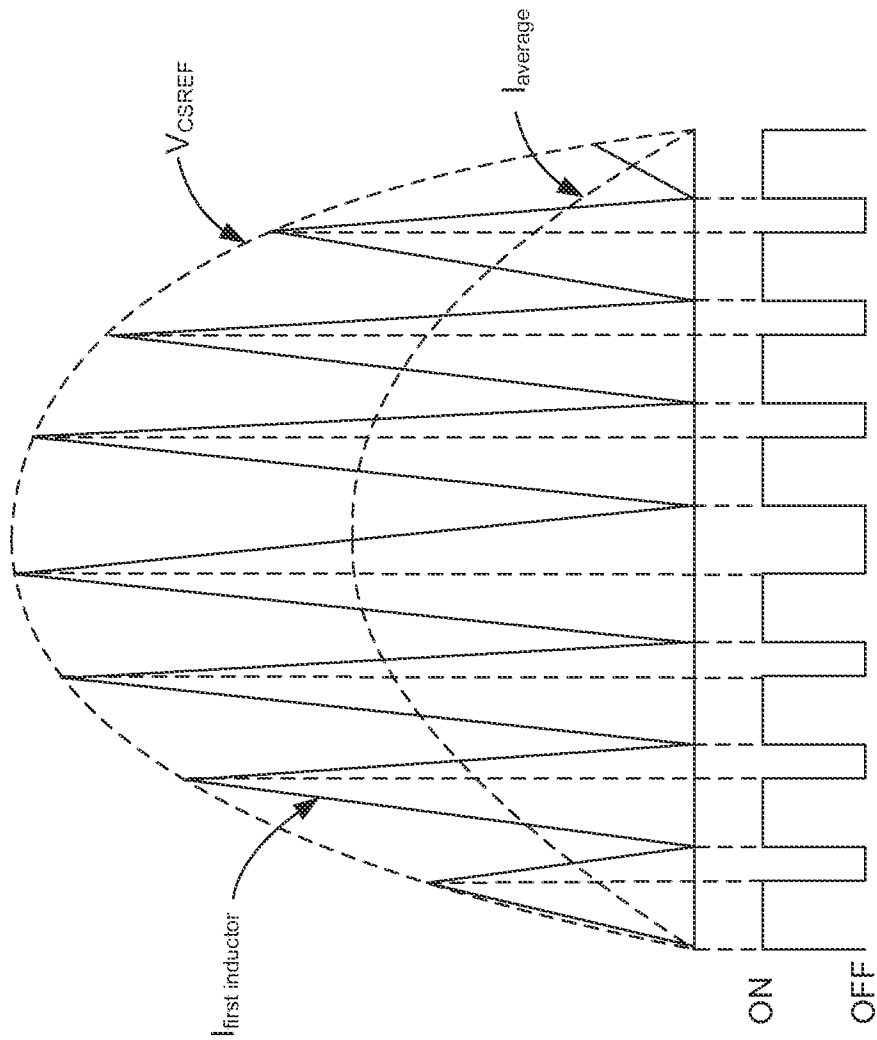


FIG. 4

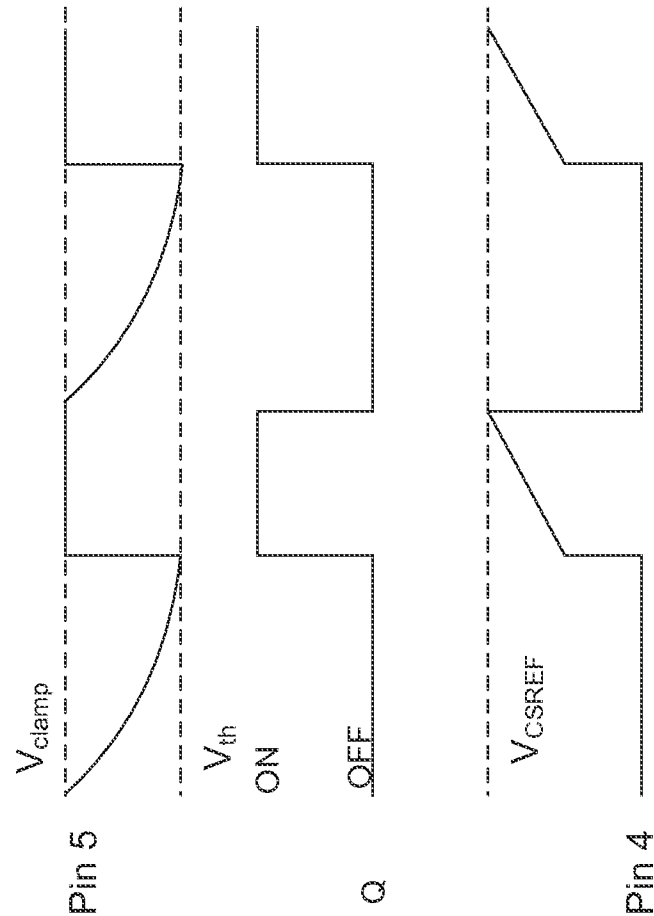
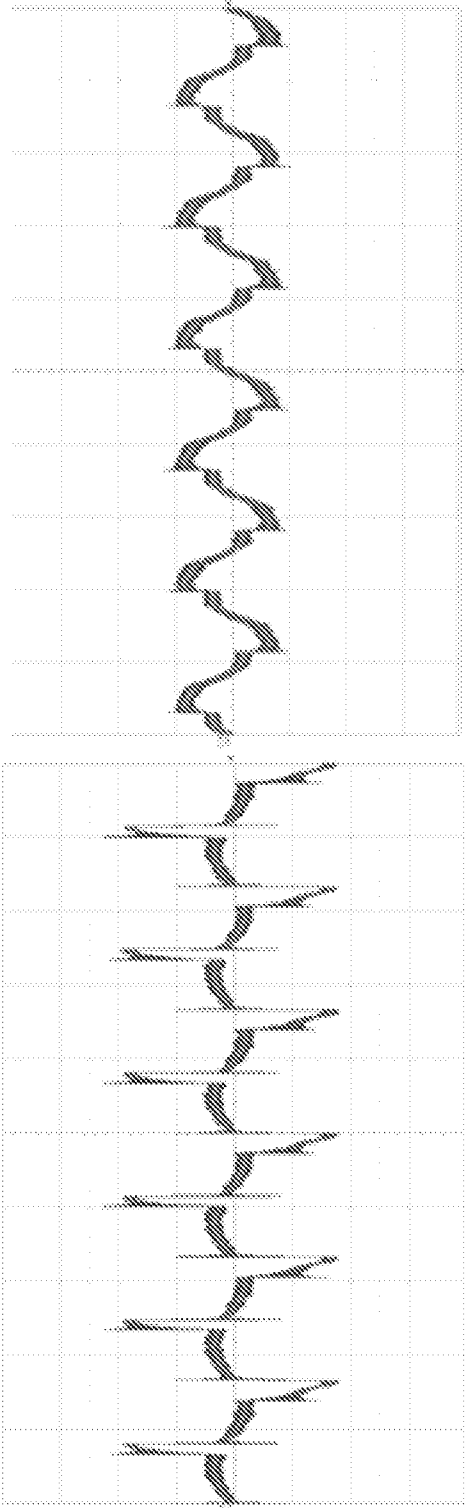


FIG. 6



(A) (B)

FIG. 7

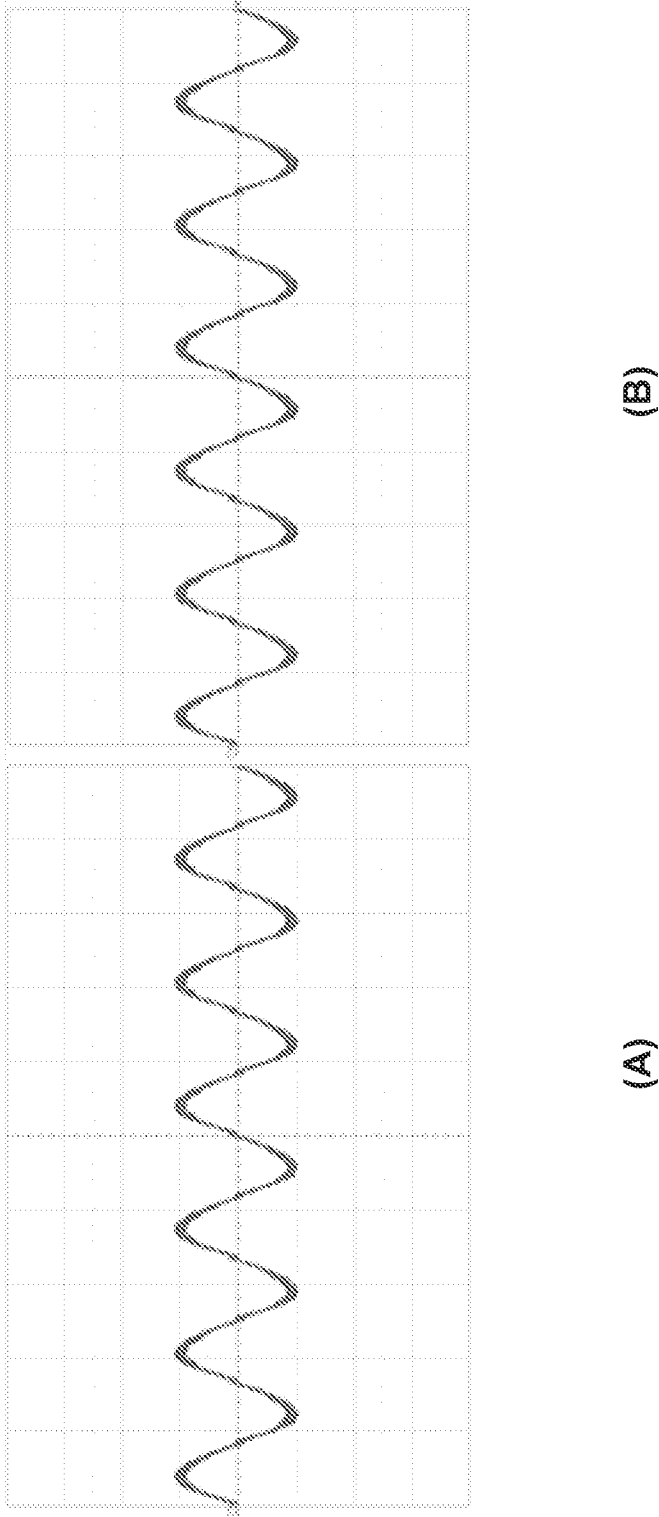


FIG. 8

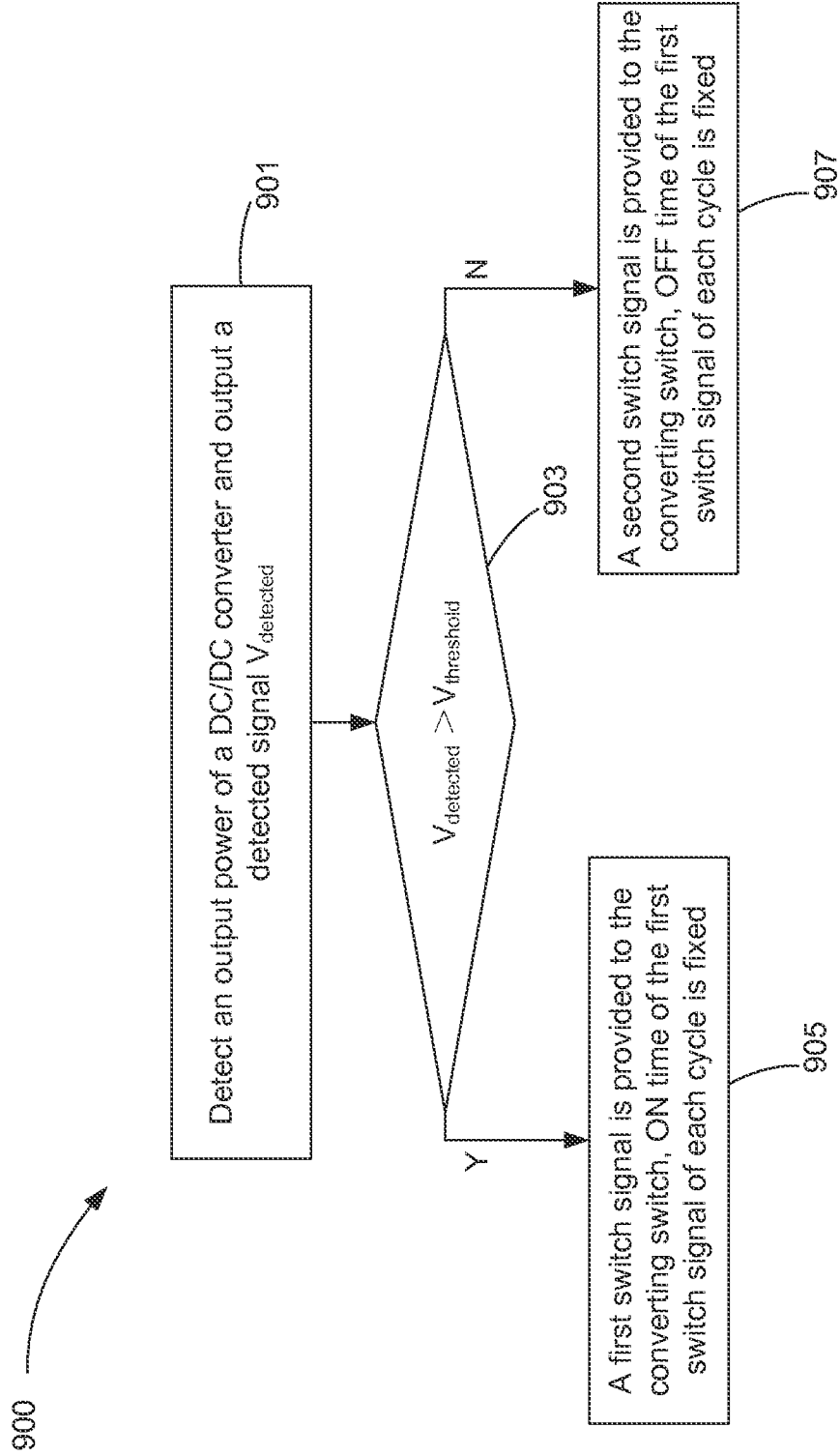


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/039651

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M1/42 H05B33/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/095733 A1 (PARK YOUNG-BAE [KR] ET AL) 28 April 2011 (2011-04-28) paragraphs [0074], [0081], [0085]; figures 1, 3, 6, 7 -----	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 September 2015

Date of mailing of the international search report

01/10/2015

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Taccoen, J

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2015/039651

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011095733	A1	28-04-2011	NONE
