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(54) Title: PULSED PLASMA SYSTEM WITH PULSED REACTION GAS REPLENISH FOR ETCHING SEMICONDUCTOR STRUCTURES

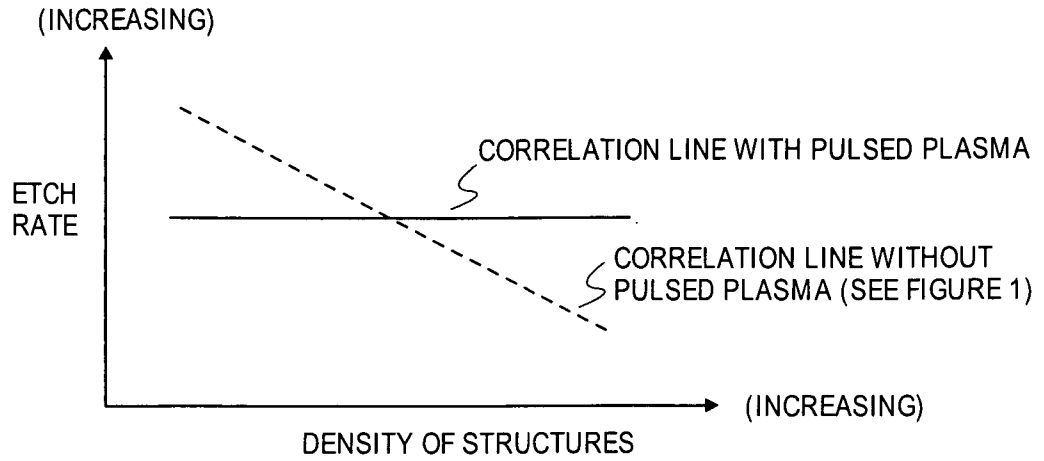

FIG. 3

(57) Abstract: A pulsed plasma system with pulsed reaction gas replenish for etching semiconductor structures is described. In an embodiment, a portion of a sample is removed by applying a pulsed plasma etch process. The pulsed plasma etch process comprises a plurality of duty cycles, wherein each duty cycle represents the combination of an ON state and an OFF state of a plasma. The plasma is generated from a reaction gas, wherein the reaction gas is replenished during the OFF state of the plasma, but not during the ON state. In another embodiment, a first portion of a sample is removed by applying a continuous plasma etch process. The continuous plasma etch process is then terminated and a second portion of the sample is removed by applying a pulsed plasma etch process having pulsed reaction gas replenish.

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Pulsed Plasma System with Pulsed Reaction Gas Replenish for Etching Semiconductor Structures

BACKGROUND OF THE INVENTION

1) FIELD OF THE INVENTION

[0001] The invention is in the fields of Semiconductor Structures and Semiconductor Equipment.

2) DESCRIPTION OF RELATED ART

[0002] For the past several years, the performance and capabilities of integrated circuits (ICs), e.g. logic circuits for computation and memory circuits for information storage, have been greatly enhanced by scaling the features of semiconductor structures to ever smaller dimensions. However, it is seldom the case that the equipment and processes used to fabricate ICs scale without issue. Continued advances in both semiconductor process technologies as well as in the equipment used to carry out such processes has ensured survival of the relentless pursuit of scaling by the Semiconductor Industry.

[0003] In order to pattern semiconductor stacks into meaningful structures, a lithography/etch process is typically employed. State-of-the-art etch processes include etching a semiconductor stack with a system comprising an ionized gas, i.e. a plasma. Plasma etch processing may be particularly useful for etching multiple adjacent structures with fine features. However, as demands on feature size and spacing become more stringent, limitations of the plasma etch process have revealed themselves.

[0004] One potential limitation of plasma etching may be with respect to the fabrication of an IC with variable spacing between various semiconductor structures within a single sample. For example, the etch rate may exhibit a dependence on pattern density, a phenomenon referred to as "micro-loading." At very small dimensions, and particularly in high aspect ratio regimes, the etch rate of a material that has been patterned with a high density (i.e. smaller spacings between features) may be slower than the etch rate of the same material patterned with a low density (i.e. larger spacings between features). Thus an "over-etch" may be required to fully etch all of the various structures within a single sample, i.e. the areas that are first to completely etch continue to be exposed to the etch process while areas that have not completely etched undergo completion of the etch process. In some cases, this over-etch may have a detrimental impact on the resultant semiconductor structures.

[0005] Referring to Figure 1, a plot is provided correlating the etch rate of a particular semiconductor material with the density (i.e. spacings between features) of various semiconductor structures in a single sample in which micro-loading occurs. As indicated by the decreasing slope of the correlation line, the etch rate decreases with increasing density. Referring to Figure 2A, a semiconductor stack 200 comprises a substrate 202, a semiconductor layer 204 and a mask 206. Referring to Figure 2B, the pattern of mask 206 is etched into semiconductor layer 204 with a plasma etch process. Micro-loading can occur during the etch process of semiconductor stack 200, such that semiconductor layer 204 etches faster in low density region 208 than in medium density region 210 and high density region 212, as depicted in Figure 2B. Referring to Figure 2C, the etch process performed on semiconductor stack 200 is completed in low density region 208 prior to completion in medium density region

210 and in high density region 212. Thus, the structures in low density region 208 are exposed to an over-etch while the etch is completed in regions of higher density. Referring to Figure 2D, during the over-etch, some detrimental undercutting 214 may occur on structures in regions of lower density. The undercutting may vary with the density, depending on the extent of over-etch that a particular region experiences, as depicted in Figure 2D.

[0006] Thus, a method for etching semiconductor structures is described herein, along with a system within which the method may be conducted.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figure 1 illustrates a correlation plot of Etch Rate versus Density of Structures, in accordance with the prior art.

[0008] Figures 2A-D illustrate cross-sectional views representing the effects of micro-loading during an etch process conducted on a semiconductor stack, in accordance with the prior art.

[0009] Figure 3 illustrates a correlation plot of Etch Rate versus Density of Structures, in accordance with an embodiment of the present invention.

[0010] Figures 4A-C illustrate cross-sectional views representing the effects of a significant reduction in micro-loading during a pulsed etch process with pulsed reaction gas replenish as conducted on a semiconductor stack, in accordance with an embodiment of the present invention.

[0011] Figure 5A is a flowchart and Figure 5B is a waveform, both representing a series of steps in a pulsed plasma process with pulsed reaction gas replenish, in accordance with an embodiment of the present invention.

[0012] Figures 6A-F illustrate cross-sectional views representing the steps of the flowchart from Figure 5A performed on a semiconductor stack, in accordance with an embodiment of the present invention.

[0013] Figures 7A-C illustrate cross-sectional views representing a continuous/pulsed plasma etch process with pulsed reaction gas replenish performed on a semiconductor stack, in accordance with an embodiment of the present invention.

[0014] Figure 8 is a flowchart representing a series of steps in a pulsed plasma process with pulsed reaction gas replenish, in accordance with an embodiment of the present invention.

[0015] Figures 9A-D illustrate cross-sectional views representing the steps of the flowchart from Figure 8 performed on a semiconductor stack, in accordance with an embodiment of the present invention.

[0016] Figure 10 illustrates a system in which a pulsed plasma process with pulsed reaction gas replenish is conducted, in accordance with an embodiment of the present invention.

[0017] Figures 11A-B illustrate the chamber from the system of Figure 10 in a plasma ON state and a plasma OFF state, respectively, in accordance with an embodiment of the present invention.

[0018] Figures 12A-B illustrate the chamber from the system of Figure 10 in a plasma ON/gas inlet device OFF state and a plasma OFF/gas inlet device ON state, respectively, in accordance with an embodiment of the present invention.

[0019] Figures 13A-D illustrate the chamber from the system of Figure 10 in a plasma ON/bias OFF state, a plasma ON/bias ON state, a plasma OFF/bias ON state

and a plasma OFF/bias OFF state, respectively, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0020] A method and a system for etching semiconductor structures are described. In the following description, numerous specific details are set forth, such as specific dimensions and chemical regimes, in order to provide a thorough understanding of the present invention. It will be apparent to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known processing steps, such as patterning steps or wet chemical cleans, are not described in detail in order to not unnecessarily obscure the present invention. Furthermore, it is understood that the various embodiments shown in the figures are illustrative representations and are not necessarily drawn to scale.

[0021] Disclosed herein are a pulsed plasma method and a corresponding system for etching semiconductor structures. A portion of a sample may be etched by applying a pulsed plasma process. The pulsed plasma process comprises a plurality of duty cycles, wherein each duty cycle represents the combination of an ON state and an OFF state of a plasma. In accordance with an embodiment of the present invention, the plasma is generated from a reaction gas, wherein the reaction gas is replenished during the OFF state of the plasma in a pulsed plasma process, but not during the ON state. In another embodiment, a first portion of a sample is removed by applying a continuous plasma process. The continuous plasma process is then terminated and a second portion of the sample is removed by applying a pulsed plasma process having pulsed reaction gas replenish.

[0022] By repeatedly pulsing a plasma during an etch process, the etch rate dependency on structure density may be mitigated. During an ON state of a plasma (i.e. when the plasma is in the form of an ionized gas), and hence during the primary etching phase of a semiconductor material in a plasma etch process, etch by-products are formed. As the etch process progresses in regions of higher density, these by-products may migrate away from the sample at a rate slower than in lower density regions of the sample. Thus, in a continuous ON state, etch by-products may hinder the etch process lending to micro-loading. In the OFF state, however, these by-products may be removed from all regions without competing with the etch process. The application of a plurality of duty cycles (i.e. cycles of ON/OFF states) may be performed in order to etch a semiconductor material with substantially the same etch rate over an entire sample, regardless of structure density. Figure 3 illustrates a correlation plot of Etch Rate versus Density of Structures in a pulsed plasma etch process, in accordance with an embodiment of the present invention. As indicated by the negligible slope of the correlation line, the etch rate is substantially the same with increasing density. A semiconductor material etched in this manner may suffer less detriment from over-etch because the etch process may be completed in all portions of the sample at substantially the same time.

[0023] Reaction gas species used to generate the plasma may be consumed during the ON state of a duty cycle in a pulsed plasma etch process, potentially lending to plasma modification. In some instances, the plasma modification may be substantial enough to alter the etching characteristics of the plasma. This effect may be detrimental on attempts to conduct a controlled etching process. By replenishing the reaction gas during the etching process, plasma modification may be mitigated.

On the other hand, replenishing the reaction gas during the ON state of a plasma in a pulsed plasma etch process may cause a plasma species gradient to form, lending to inconsistent etching across a sample. A substantially homogeneous plasma may be achieved during the ON state of the duty cycle by replenishing the reaction gas during the OFF state of the duty cycle only. Thus, in accordance with an embodiment of the present invention, a pulsed reaction gas replenish process is conducted in parallel with the pulsed plasma process. That is, the reaction gas replenish is implemented during the OFF state, but not during the ON state, of a duty cycle in a pulsed plasma etch process.

[0024] A semiconductor stack may be etched by a pulsed plasma etch process with pulsed reaction gas replenish. Figures 4A-C illustrate cross-sectional views representing the effects of a significant reduction in micro-loading during a pulsed etch process with pulsed reaction gas replenish conducted on a semiconductor stack, in accordance with an embodiment of the present invention.

[0025] Referring to Figure 4A, a semiconductor stack 400 comprises a substrate 402, an etch layer 404 and a mask 406. Mask 406 is patterned with a low density region 408, a medium density region 410 and a high density region 412. Semiconductor stack 400 may comprise a stack of greater complexity of material layers and/or pattern types, but is depicted in the manner shown herein for illustrative purposes.

[0026] Substrate 402 may comprise any material that can withstand a manufacturing process and upon which semiconductor layers may suitably reside. In an embodiment, substrate 402 is comprised of group IV-based materials such as crystalline silicon, germanium or silicon/germanium. In one embodiment, the atomic

concentration of silicon atoms in substrate 402 is greater than 99%. In another embodiment, substrate 402 is comprised of a III-V material such as, but not limited to, gallium nitride, gallium phosphide, gallium arsenide, indium phosphide, indium antimonide, indium gallium arsenide, aluminum gallium arsenide, indium gallium phosphide or a combination thereof. In an alternative embodiment, substrate 402 is comprised of an epitaxial layer grown atop a distinct crystalline substrate, e.g. a silicon epitaxial layer grown atop a boron-doped bulk silicon mono-crystalline substrate. Substrate 402 may also comprise an insulating layer in between a bulk crystal substrate and an epitaxial layer to form, for example, a silicon-on-insulator substrate. In one embodiment, the insulating layer is comprised of a material selected from the group consisting of silicon dioxide, silicon nitride, silicon oxy-nitride and a high-k dielectric layer. In another embodiment, substrate 402 comprises a top insulating layer, directly adjacent to etch layer 404.

[0027] Substrate 402 may additionally comprise charge-carrier dopant impurity atoms. For example, in accordance with an embodiment of the present invention, substrate 402 is comprised of silicon and/or germanium and the charge-carrier dopant impurity atoms are selected from the group consisting of boron, arsenic, indium, antimony or phosphorus. In another embodiment, substrate 402 is comprised of a III-V material and the charge-carrier dopant impurity atoms are selected from the group consisting of carbon, silicon, germanium, oxygen, sulfur, selenium or tellurium.

[0028] Etch layer 404 may comprise any material that can be suitably patterned into an array of distinctly defined semiconductor structures. In accordance with an embodiment of the present invention, etch layer 404 is comprised of a group IV-based material or a III-V material, such as those discussed above in association

with substrate 402. Additionally, etch layer 404 may comprise any morphology that can suitably be patterned into an array of distinctly defined semiconductor structures. In an embodiment, the morphology of etch layer 404 is selected from the group consisting of amorphous, single-crystalline and poly-crystalline. In one embodiment, etch layer 404 comprises charge-carrier dopant impurity atoms, such as those described above in association with substrate 402.

[0029] The composition of etch layer 404 need not be limited to semiconductor materials, *per se*. In accordance with an alternative embodiment of the present invention, etch layer 404 is comprised of a metal layer such as but not limited to copper, aluminum, tungsten, metal nitrides, metal carbides, metal silicides, hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel or conductive metal oxides, e.g. ruthenium oxide. In yet another embodiment of the present invention, etch layer 404 is comprised of an insulating layer. In one embodiment, etch layer 404 is comprised of an insulating material selected from the group consisting of silicon dioxide, silicon oxy-nitride and silicon nitride. In another embodiment, etch layer 404 is comprised of a high-K dielectric layer selected from the group consisting of hafnium oxide, hafnium silicate, lanthanum oxide, zirconium oxide, zirconium silicate, tantalum oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantalum oxide and lead zinc niobate.

[0030] Mask 406 may be comprised of any material suitable for patterning via a lithography or direct-write process. In one embodiment, mask 406 is comprised of a photo-resist material. In a specific embodiment, the photo-resist material is used in a lithographic process and is selected from the group consisting of a positive photo-

resist and a negative photo-resist. Mask 406 may further comprise a material suitable for blocking a plasma etch process, such as a plasma etch process used to pattern etch layer 404. Thus, in accordance with another embodiment of the present invention, mask 406 also comprises a hard-mask layer, such as a hard-mask layer selected from the group consisting of silicon dioxide, silicon oxy-nitride, silicon nitride and a metal film.

[0031] Referring to Figure 4B, the pattern of mask 406 is etched into etch layer 404 with a pulsed plasma etch process having pulsed reaction gas replenish to form partially patterned etch layer 414. Under the appropriate conditions, and in accordance with an embodiment of the present invention, the etch rate of all density regions 408, 410 and 412 are substantially similar when a pulsed plasma process with pulsed reaction gas replenish is employed, as depicted in Figure 4B. The pulsed plasma process with pulsed reaction gas replenish contains a plurality of duty cycles, wherein each duty cycle represents the combination of an ON state and an OFF state of the etching plasma. A reaction gas replenish step is implemented during the OFF state of the duty cycle, but not during the ON state of the duty cycle. A duty cycle may be comprised of one ON state and one OFF state, wherein the durations of the ON state and OFF state are suitable to transfer the pattern of mask 406 into etch layer 404 at a substantially similar etch rate for density regions 408, 410 and 412. In accordance with an embodiment of the present invention, the portion of each duty cycle comprised of said ON state is in the range of 5 – 95% of the duty cycle. In a specific embodiment, the portion of each duty cycle comprised of said ON state is in the range of 65 – 75% of the duty cycle. In another embodiment, the frequency of a plurality of duty cycles is in the range of 1Hz – 200 kHz, i.e. each duty cycle has a

duration in the range of 5 micro-seconds – 1 second. In a specific embodiment, the frequency of a plurality of duty cycles is 50 kHz and the portion of each duty cycle comprised of said ON state is 70%. In accordance with an embodiment of the present invention, the quantity and duration of the reaction gas replenish implemented during the OFF state of the plasma are such that, as a result of the reaction gas being replenished during the OFF state, the composition of gaseous species of the plasma at the end of a pulsed plasma process is within 1% of the composition of gaseous species of a plasma at the beginning of the pulsed plasma process. In one embodiment, the pressure of the plasma at the end of the pulsed plasma process is within 1 mTorr of the pressure of the plasma at the beginning of the pulsed plasma process.

[0032] The method of generating a plasma for use in the pulsed plasma process with pulsed reaction gas replenish for etching etch layer 404 may comprise any method suitable to strike and maintain the plasma for a duration sufficient to satisfy the duration of the ON state in a duty cycle. For example, in accordance with an embodiment of the present invention, the method of generating the plasma comprises generating a plasma selected from the group consisting of an electron cyclotron resonance (ECS) plasma, a helicon wave plasma, an inductively coupled plasma (ICP) and a surface wave plasma. In a specific embodiment, the method of generating the plasma comprises generating an inductively coupled plasma in an Applied Materials^{TM} AdvantEdge G3 etcher.

[0033] The plasma generated for the pulsed plasma etch process with pulsed reaction gas replenish may be comprised of any reaction gas suitable to generate ions and reactive radicals to remove portions of etch layer 404 without detrimentally impacting the pattern of mask 406. For example, in accordance with an embodiment

of the present invention, the reaction gas is comprised of a halide species and is used to etch a silicon-based material. In a specific embodiment, the reaction gas is comprised of the species HBr, He and a 70%/30% He/O_2 mixture in the approximate ratio of 300:50:12, respectively, and the pulsed plasma is used to etch amorphous silicon, poly-silicon or single-crystal silicon. In another embodiment, the reaction gas is comprised of a fluorocarbon species and is used to etch a dielectric layer. In a specific embodiment, the reaction gas is comprised of the species CF_4 and the pulsed plasma is used to etch silicon dioxide or carbon-doped silicon oxide. The reaction gas may have a pressure suitable to provide a controlled etch rate. In an embodiment, the pressure is in the range of 1 – 100 mTorr. In another embodiment, the pressure is in the range of 3 – 100 mTorr. In a specific embodiment, the reaction gas is comprised of HBr, He and O_2, the pressure of the reaction gas is in the range of 30 - 50 mTorr and the etch rate of poly-silicon is in the range of 500 – 6000 Angstroms/minute.

[0034] Referring to Figure 4C, the pulsed plasma process with pulsed reaction gas replenish described above is continued until partially patterned etch layer 414 becomes patterned etch layer 424. By using the pulsed plasma etch process with pulsed reaction gas replenish described above through to completion of the etching of etch layer 404, the etch process is completed at density regions 408, 410 and 412 at substantially the same time. Thus, only a negligible amount of over-etching may be required in order to form patterned etch layer 424. As such, detrimental undercutting of the various structures of patterned etch layer 424 may be significantly mitigated, as depicted by the lack of undercut in Figure 4C.

[0035] The duration of the ON state and the OFF state in a duty cycle of a pulsed plasma etch process with pulsed reaction gas replenish may be targeted to

correspond with the formation and removal of etch by-products. Figure 5A is a flowchart and Figure B is a waveform, both representing a series of such targeted steps in a pulsed plasma process with pulsed reaction gas replenish, in accordance with an embodiment of the present invention. Figures 6A-D illustrate cross-sectional views representing the steps of the flowchart from Figure 5A as performed on a semiconductor stack.

[0036] Referring to step 502 of flowchart 500 and corresponding Figure 6A, a semiconductor stack 600 comprises a substrate 602, an etch layer 604 and a mask 606 at the start of a pulsed plasma etching process having pulsed reaction gas replenish. Mask 606 is patterned with a low density region 608, a medium density region 610 and a high density region 612. Substrate 602, etch layer 604 and mask 606 may be comprised of any materials described in association with substrate 402, etch layer 404 and mask 406, respectively, from Figure 4A. Semiconductor stack 600 may comprise a stack of greater complexity of material layers and/or pattern types, but is depicted in the manner shown herein for illustrative purposes.

[0037] Referring to step 504 of flowchart 500 and corresponding Figure 6B, the pattern of mask 606 is partially etched into etch layer 604 during the ON state of a duty cycle in a pulsed plasma etch process with pulsed reaction gas replenish to form partially patterned etch layer 614A. Unmasked portions of etch layer 604 are accessible by plasma etching species 620 while masked portions of etch layer 604, covered by mask 606, are protected from plasma etching species 620, as depicted in Figure 6B. Etch by-products 616 are generated within reaction region 618 of semiconductor stack 600.

[0038] Etching species 620 may be comprised of any charged species and reactive neutrals ejected from the plasma used in a pulsed plasma etch process. For example, in accordance with an embodiment of the present invention, etching species 620 are comprised of positively charged ions and radicals. In one embodiment, the reaction gas is comprised of HBr, He and O_2 and the etching species 620 are selected from the group consisting of H^+, Br^+, He^+, O^+, H, Br and O. In another embodiment, the reaction gas is comprised of a fluorocarbon and the etching species 620 are selected from the group consisting of F^+, CF^+, CF_2^+, CF_3^+, F, CF, CF_2 and CF_3. Etch by-products 616 may be comprised of any combination of atoms from etch layer 604 and etching species 620. In a specific embodiment, etching species 620 are comprised of a halide cation X^+ and/or a halide radical X (X = F, Cl, Br), etch layer 604 is comprised of silicon atoms, and etch by-products 620 are comprised of by-products selected from the group consisting of the neutral species SiX_n, where n is 1, 2, 3 or 4.

[0039] The duration of the ON state of a duty cycle may be selected to maximize etch efficiency while maintaining a substantially similar etch rate for all density regions 608, 610 and 612 of partially patterned etch layer 614A. As depicted in Figure 6B, etch by-products 616 are formed and reside, at least for a time, among the partially etched features of partially patterned etch layer 614A, i.e. within reaction region 618. Reaction region 618 is a region adjacent semiconductor stack 600 within which etch by-products 616 that are formed may interfere with plasma etching species 620. That is, as the amount of etch by-products 616 increases within reaction region 618 throughout the lifetime of an ON cycle, plasma etching species 620 may be hindered from accessing unmasked portions of partially patterned etch layer 604. Such hindering of plasma etching species 620 may be more severe in high structure

density regions as compared to low structure density regions, slowing the etch rate in the high density regions as compared with the etch rate of the low density regions. Thus, in accordance with an embodiment of the present invention, the ON state of a duty cycle in a pulsed plasma etch process with pulsed reaction gas replenish is selected to be less than or, at most, correspond with the time at which a sufficient amount of etch by-products are generated to slow the etch rate of a high density region versus the etch rate of a low density region. In one embodiment, the duration of the ON state is selected to substantially match the time at which the etch rate of the partially patterned etch layer 614A becomes dependent on the density of the pattern of mask 606. In another embodiment, the ON state is of a sufficiently short duration to substantially inhibit micro-loading within reaction region 618. In an embodiment, the duration of the ON state is within any of the ranges described for the ON state of the duty cycle discussed in association with Figure 4B. In accordance with an embodiment of the present invention, a reaction gas replenish step is implemented during the OFF state of the duty cycle, but not during the ON state of the duty cycle.

[0040] Referring to step 506 of flowchart 500 and corresponding Figure 6C, the plasma is in an OFF state and, thus, etching species 620 are no longer present in reaction region 618 of semiconductor stack 600. As depicted in Figure 6C, etch by-products 616 are removed from reaction region 618.

[0041] The duration of the OFF state of a duty cycle may be selected to allow a sufficient time for etch by-products 616 to be removed from (i.e. dissipated from or evacuated from) reaction region 618. During the ON state, etch by-products 616 are formed within reaction region 618, as described above. Additionally, during the transition from the ON state to the OFF state of the plasma, negatively charged ions

may be ejected from the plasma gas as it neutralizes, generating a new set of etching species. These new etching species may further contribute to the quantity of etch by-products present in reaction region 618.

[0042] At the initiation of the OFF state of the duty cycle, the concentration of by-products 616 may be substantially greater inside reaction region 618 than outside of reaction region 618. Thus, a natural diffusion gradient may form and etch by-products 616 may diffuse outside of reaction region 618. This process may be enhanced by an additional pressure gradient. That is, along with a build-up in etch by-products 616 during the ON state, the pressure within reaction region 618 may become greater than the pressure outside of reaction region 618, enhancing the extrusion of etch by-products 616. Thus, in accordance with an embodiment of the present invention, the OFF state of a duty cycle in a pulsed plasma etch process with pulsed reaction gas replenish is selected to be of a sufficiently long duration to substantially enable removal of a set of etch by-products 616 from reaction region 618. In another embodiment, the quantity of etch by-products 616 removed is sufficient such that any etch by-products that remain within reaction region 618 do not substantially interfere with etching species during an ON state of a subsequent duty cycle. In one such embodiment, the duration of the OFF state is selected to substantially match the time at which more than 50% of the etch by-products 616 have been removed from reaction region 618. In another embodiment, the duration of the OFF state is selected to substantially match the time at which more than 75% of the etch by-products 616 have been removed from reaction region 618. In an alternative embodiment, the duration of the OFF state is within any of the ranges described for the OFF state of the duty cycle discussed in association with Figure 4B. In an

embodiment, an inert gas such as Ar or He is injected during the OFF state of the plasma to enhance the by-product removal.

[0043] The duration of the OFF state of a duty cycle may further be selected to allow a sufficient reaction gas replenish step to be implemented. Thus, a reaction gas replenish step may be implemented during the OFF state of the duty cycle, without requiring implementation during the ON state of the duty cycle. In accordance with an embodiment of the present invention, the quantity and duration of the reaction gas replenish implemented during the OFF state of the plasma are such that, as a result of the reaction gas being replenished during the OFF state, the composition of gaseous species of the plasma at the end of a pulsed plasma process is within 1% of the composition of gaseous species of a plasma at the beginning of the pulsed plasma process. In one embodiment, the pressure of the plasma at the end of the pulsed plasma process is within 1 mTorr of the pressure of the plasma at the beginning of the pulsed plasma process.

[0044] Referring to step 508 of flowchart 500 and corresponding Figures 6D-E, the pattern of mask 606 is continued to be etched into etch layer 604 during subsequent duty cycles of a pulsed plasma etch process with pulsed reaction gas replenish, forming more extensively etched partially patterned etch layer 614B. The duty cycles (i.e. step 508) may be repeated until a desired amount of etch layer 604 has been etched. Thus, in accordance with an embodiment of the present invention, a portion of etch layer 604 is removed with a pulsed plasma etch process comprising a plurality of duty cycles. A reaction gas replenish step is implemented during the OFF state of the duty cycle, but not during the ON state of the duty cycle. Figure 5B illustrates the timeline of a duty cycle, as represented in a waveform.

[0045] Referring to step 510 of flowchart 500 and corresponding Figure 6F, the pulsed plasma etch process with pulsed reaction gas replenish is terminated following removal of a desired quantity of etch layer 604. By using the pulsed plasma etch process with pulsed reaction gas replenish described above through to completion of the etching of etch layer 604, the etch process is completed at density regions 608, 610 and 612 at substantially the same time. Thus, only a negligible amount of over-etching may be required in order to form patterned etch layer 624. As such, detrimental undercutting of the various structures of patterned etch layer 624 may be significantly mitigated, as depicted by the lack of undercut in Figure 6F. The determination of when to terminate the pulsed plasma process having pulsed reaction gas replenish may be made by any suitable factor. For example, in accordance with an embodiment of the present invention, the termination of the pulsed plasma etch process with pulsed reaction gas replenish is determined by ending the repetition of duty cycles at a predetermined time. In an alternative embodiment, the termination of the pulsed plasma etch process with pulsed reaction gas replenish is determined by detecting a change in etch by-products 612 at the completion of the etching of etch layer 604 and the corresponding exposure of the top surface of substrate 602. In another embodiment, the termination of the pulsed plasma etch process with pulsed reaction gas replenish is determined by measuring the depth of a trench using an interferometric technique.

[0046] A pulsed plasma etch process with pulsed reaction gas replenish may be combined with a continuous plasma etch process. For example, it may be the case that a differential in etch rate for differing density regions of a semiconductor stack may not be significant until a portion of the semiconductor stack has already been

etched, since the etch process may suffer from more severe micro-loading with increased aspect ratio of a pattern. As such, it may be more efficient to apply a continuous plasma for etching the first portion of a semiconductor stack, until a particular depth has been reached, and then to apply a pulsed plasma etch process with pulsed reaction gas replenish to remove a second portion of the semiconductor stack. In accordance with an embodiment of the present invention, a semiconductor stack is etched with a continuous plasma etch process until a desired depth has been reached. The etching of the semiconductor stack is then completed by utilizing a pulsed plasma etch process with pulsed reaction gas replenish. In one embodiment, a continuous/pulsed plasma etch process with pulsed reaction gas replenish is utilized to increase the throughput of wafers in a single-wafer processing tool. This continuous/pulsed plasma etch process with pulsed reaction gas replenish is illustrated in Figures 7A-C, in accordance with an embodiment of the present invention. Etch layer 704 patterned with mask 712 (Figure 7A) is partially patterned with a continuous plasma etch process (Figure 7B). A pulsed plasma etch process with pulsed reaction gas replenish is subsequently employed to complete etching etch layer 704, i.e. until the etch stops on etch-stop layer 706, as depicted in Figure 7C. In an embodiment, the depth at which the plasma etch process is changed from continuous to pulsed is selected as being in the range of 0.5 – 4 times the spacing width of the region of highest structure density. In one embodiment, the depth is selected as being substantially equal to the spacing width of the region of highest structure density, i.e. when an aspect ratio of 1 has been achieved among the highest density structures.

[0047] Figure 8 is a flowchart representing a series of steps combining a continuous plasma etch process with a subsequent pulsed plasma etch process with

pulsed reaction gas replenish, in accordance with an embodiment of the present invention. Figures 9A-D illustrate cross-sectional views representing the steps of the flowchart from Figure 8 as performed on a more complex semiconductor stack.

[0048] Referring to step 802 of flowchart 800 and corresponding Figure 9A, a semiconductor stack 900 comprises a substrate 902, two etch layers 904 and 908, two dielectric layers 906 and 910 and a mask 912 at the start of a continuous/pulsed plasma etching process. Substrate 902, etch layers 904 and 908 and mask 912 may be comprised of any materials described in association with substrate 902, etch layer 904 and mask 912, respectively, from Figure 4A. Semiconductor stack 900 may comprise a stack of greater or lesser complexity of material layers, but is depicted in the manner shown herein for illustrative purposes. In one embodiment, semiconductor stack 900 is comprised of poly-silicon/SiON/poly-silicon/SiO_2, as is found in a typical Flash memory stack.

[0049] Dielectric layers 906 and 910 may be comprised of any material suitable to insulate conductive portions of a semiconductor stack. In one embodiment, dielectric layers 906 and 910 are comprised of an insulating material selected from the group consisting of silicon dioxide, silicon oxy-nitride and silicon nitride. In another embodiment, dielectric layers 906 and 910 are comprised of a high-K dielectric layer selected from the group consisting of hafnium oxide, hafnium silicate, lanthanum oxide, zirconium oxide, zirconium silicate, tantalum oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantalum oxide and lead zinc niobate.

[0050] Referring to step 804 of flowchart 800 and corresponding Figure 9B, the pattern of mask 912 is etched into etch layer 904 with a continuous plasma etch

process to form patterned etch layer 914. A continuous plasma etch process may be sufficient for the etching of etch layer 904 in the case that a differential in etch rate for differing density regions of a first portion of semiconductor stack 900 is not significant. The method of generating a plasma for use in the continuous plasma process to form patterned etch layer 914 may comprise any method suitable to strike and maintain the plasma for a duration sufficient to satisfy the duration of the continuous etch process. For example, in accordance with an embodiment of the present invention, the method of generating the continuous plasma comprises generating a plasma selected from the group consisting of an electron cyclotron resonance (ECS) plasma, a helicon wave plasma, an inductive coupled plasma (ICP) and a surface wave plasma. In a specific embodiment, the method of generating the continuous plasma comprises generating an inductive coupled plasma in an Applied Materials^{TM} AdvantEdge G3 etcher.

[0051] Referring to step 806 of flowchart 800 and corresponding Figure 9B, the determination of when to terminate the continuous plasma process may be made by any suitable factor. For example, in accordance with an embodiment of the present invention, the termination of the continuous plasma etch process is determined by ending at a predetermined time based on characteristics of the material being etched. In an alternative embodiment, the termination of the continuous plasma etch process is determined by detecting a change in etch by-products at the completion of the etching of etch layer 904 and the corresponding exposure of the top surface of dielectric layer 906, i.e. by detecting an end-point. In one embodiment, the termination of the continuous plasma etch process is determined by the real-time composition of a set of chemical species generated during the continuous etch process.

Referring to Figure 9C, the exposed portions of dielectric layer 906 may be removed to form patterned dielectric layer 916 following the patterning of etch layer 904. In accordance with an embodiment of the present invention, exposed portions of dielectric layer 906 are removed by an etch process selected from the group consisting of a wet etch process, a continuous plasma etch process and a pulsed plasma etch process.

[0052] Referring to steps 808, 810 and 812 of flowchart 800 and corresponding Figures 9C-D, the pattern of mask 912 is continued to be etched into semiconductor stack 900. At this point, because a first portion of semiconductor stack 900 has already been etched, a differential in etch rate for differing density regions of etch layer 908 may be significant, requiring the application of a pulsed plasma etch process. Thus, in accordance with an embodiment of the present invention, a pulsed plasma etch process with pulsed reaction gas replenish is utilized to pattern etch layer 908 to form patterned etch layer 918. The duty cycles (i.e. step 812) may be repeated until a desired amount of etch layer 908 has been etched. Thus, in accordance with an embodiment of the present invention, a first portion of semiconductor stack 900 is patterned with a continuous etch plasma process and a second portion of semiconductor stack 900 is patterned with a pulsed plasma etch process comprising a plurality of duty cycles. A reaction gas replenish step is implemented during the OFF state of each duty cycle, but not during the ON state of each duty cycle.

[0053] Referring to step 814 of flowchart 800 and corresponding Figure 9D, the pulsed plasma etch process with pulsed reaction gas replenish is terminated following removal of a desired quantity of etch layer 908. By using the pulsed plasma etch process with pulsed reaction gas replenish described above through to completion

of the etching of etch layer 908, the etch process is completed at various density regions at substantially the same time. Thus, only a negligible amount of over-etching may be required in order to form patterned etch layer 918. As such, detrimental undercutting of the various structures of patterned etch layer 918 may be significantly mitigated, as depicted by the lack of undercut in Figure 9D. The determination of when to terminate the pulsed plasma process with pulsed reaction gas replenish may be made by any suitable factor. For example, in accordance with an embodiment of the present invention, the termination of the pulsed plasma etch process with pulsed reaction gas replenish is determined by ending the repetition of duty cycles at a predetermined time. In an alternative embodiment, the termination of the pulsed plasma etch process with pulsed reaction gas replenish is determined by detecting a change in etch by-products at the completion of the etching of etch layer 908 and the corresponding exposure of the top surface of dielectric layer 910.

[0054] The approach of combining continuous and pulsed plasma etch processes, as described above, may be applied to more complex material stacks by applying cyclic continuous/pulsed plasma etch processes. For example, in accordance with an embodiment of the present invention, a first portion of a semiconductor stack is patterned with a first continuous plasma etch process, a second portion of a semiconductor stack is patterned with a first pulsed plasma etch process having pulsed reaction gas replenish, a third portion of a semiconductor stack is patterned with a second continuous plasma etch process and a fourth portion of a semiconductor stack is patterned with a second pulsed plasma etch process having pulsed reaction gas replenish. In a specific embodiment, etch layer 904 of semiconductor stack 900 is also patterned with a first continuous plasma etch process followed by a first pulsed

plasma etch process having pulsed reaction gas replenish. Etch layer 908 is then patterned with a second continuous plasma etch process followed by a second pulsed plasma etch process having pulsed reaction gas replenish.

[0055] A pulsed plasma etch process with pulsed reaction gas replenish may be conducted in any processing equipment suitable to provide an etch plasma in proximity to a sample for etching. Figure 10 illustrates a system in which a pulsed plasma etch process with pulsed reaction gas replenish is conducted, in accordance with an embodiment of the present invention.

[0056] Referring to Figure 10, a system 1000 for conducting a pulsed plasma etch process comprises a chamber 1002 equipped with a sample holder 1004. An evacuation device 1006, a gas inlet device 1008 and a plasma ignition device 1010 are coupled with chamber 1002. A computing device 1012 is coupled with plasma ignition device 1010 and gas inlet device 1008. System 1000 may additionally include a detector 1016 coupled with chamber 1002 and a voltage source 1014 coupled with sample holder 1004. Computing device 1012 may also be coupled with evacuation device 1006, voltage source 1014 and detector 1016, as depicted in Figure 10.

[0057] Chamber 1002 and sample holder 1004 may be comprised of any reaction chamber and sample positioning device suitable to contain an ionized gas, i.e. a plasma, and bring a sample in proximity to the ionized gas or charged species ejected therefrom. Evacuation device 1006 may be any device suitable to evacuate and de-pressurize chamber 1002. Gas inlet device 1008 may be any device suitable to inject a reaction gas into chamber 1002. Plasma ignition device 1010 may be any device suitable for igniting a plasma derived from the reaction gas injected into

chamber 1002 by gas inlet device 1008. Detection device 1016 may be any device suitable to detect an end-point of a processing step. In one embodiment, system 1000 comprises a chamber 1002, a sample holder 1004, an evacuation device 1006, a gas inlet device 1008, a plasma ignition device 1010 and a detector 1016 similar to, or the same as, those included in an Applied Materials™ AdvantEdge G3 etcher. In another embodiment, multiple gas inlet devices are coupled with chamber 1002 in order to optimize a pulsed reaction gas replenish process.

[0058] Computing device 1012 comprises a processor and a memory. In accordance with an embodiment of the present invention, the memory of computing device 1012 includes a set of instructions for controlling plasma ignition device 1010 to switch between an ON state and an OFF state of a plasma in a pulsed plasma etch process with pulsed reaction gas refresh. In an embodiment, the set of instructions contains machine operable code capable of effecting a plurality of duty cycles, wherein each duty cycle represents the combination of one ON state and one OFF state of the plasma. The memory of computing device 1012 also includes a set of instructions for controlling gas inlet device 1008 to switch between an open state and a closed state. The reaction gas is replenished when gas inlet device 1008 is in the open state and during the OFF state of the plasma, but not during the ON state of the plasma. In a specific embodiment, the set of instructions for controlling plasma ignition device 1010 includes timing instructions for each duty cycle to have an ON state in the range of 5 – 95% of the duration of the duty cycle. In an embodiment, the set of instructions for controlling plasma ignition device 1010 includes timing instructions for each duty cycle to have an ON state in the range of 65 – 75% of the duration of the duty cycle. In another embodiment, the set of instructions for

controlling plasma ignition device 1010 includes timing instructions such that the frequency of a plurality of duty cycles is in the range of 1Hz – 200 kHz, i.e. each duty cycle has a duration in the range of 5 micro-seconds – 1 second. In a specific embodiment, the set of instructions for controlling plasma ignition device 1010 includes timing instructions such that the frequency of a plurality of duty cycles is 50 kHz and the portion of each duty cycle comprised of said ON state is 70%.

[0059] Figures 11A-B illustrate the chamber from the system of Figure 10 in a plasma ON state and a plasma OFF state, respectively, in accordance with an embodiment of the present invention. Referring to Figure 11A, chamber 1002 of system 1000 comprises a plasma 1100 in an ON state and in proximity to a sample 1102 on sample holder 1004. A reaction region 1104 is directly adjacent to sample 1102. During an etch process, etch by-products may be formed and reside, at least for a time, within reaction region 1102. Thus, in accordance with an embodiment of the present invention, the set of instructions for controlling plasma ignition device 1010 includes timing instructions such that the ON state is of a sufficiently short duration to substantially inhibit micro-loading within reaction region 1104. Referring to Figure 11B, chamber 1002 of system 1000 comprises a plasma in an OFF state (i.e. a neutral reaction gas). In accordance with an embodiment of the present invention, the set of instructions for controlling plasma ignition device 1010 includes timing instructions such that the OFF state of a duty cycle in a pulsed plasma etch process is selected to be of a sufficiently long duration to substantially enable removal of a set of etch by-products from reaction region 1104.

[0060] Reaction gas species used to generate the plasma may be consumed during the ON state of a duty cycle in a pulsed plasma etch process, potentially

lending to plasma modification. In some instances, the plasma modification may be substantial enough to alter the etching characteristics of the plasma. This effect may be detrimental on attempts to conduct a controlled etching process. By replenishing the reaction gas during the etching process, plasma modification may be mitigated. On the other hand, replenishing the reaction gas during the ON state of a plasma in a pulsed plasma etch process may cause a plasma species gradient to form, lending to inconsistent etching across a sample.

[0061] Figures 12A-B illustrate the chamber from the system of Figure 10 in a plasma ON/gas inlet device OFF state and a plasma OFF/gas inlet device ON state, respectively, in accordance with an embodiment of the present invention. Referring to Figure 12A, a substantially homogeneous plasma is achieved during the ON state of the duty cycle by replenishing the reaction gas during the OFF state of the duty cycle only. Referring to Figure 12B, the reaction gas on which the plasma from Figure 12A is based is replenished during the OFF state of the plasma. Thus, in accordance with an embodiment of the present invention, a pulsed reaction gas replenish process is conducted in parallel with the pulsed plasma process. That is, the reaction gas replenish is implemented during the OFF state, but not during the ON state, of a duty cycle in a pulsed plasma etch process.

[0062] During the ON state of a duty cycle in a pulsed plasma etch process with pulsed reaction gas replenish, positive charge may be imparted to the sample being etched. In some instances, the positive charge of the sample may be substantial enough to partially deflect the positively charged etch species ejected from a plasma. Such deflection of the etching species may result in detrimental undercut of features being etched into a particular sample. By biasing the sample with a negative charge

during the etching process, the deflection of positively charged particles may be mitigated. On the other hand, during the transition from the ON state to the OFF state of a duty cycle in a pulsed plasma etch process having pulsed reaction gas replenish, the discharge of negatively-charged particles from the plasma may be inhibited if the sample is negatively biased. By zero-biasing the sample during the OFF state of a duty cycle, and thus not repelling negatively-charged particles emitted as the plasma discharges, a reduced time for plasma discharge may be achieved. Additionally, the negatively charged species may contribute to, and thus enhance, the etching process. Thus, in accordance with an embodiment of the present invention, a pulsed sample bias process is conducted in parallel with the pulsed plasma process having pulsed reaction gas replenish. That is, the sample is negatively biased during the ON state and is zero-biased during the OFF state of a duty cycle in a pulsed plasma etch process having pulsed reaction gas replenish.

[0063] Figures 13A-D illustrate chamber 1002 from system 1000 of Figure 10 in a plasma ON/bias OFF state, a plasma ON/bias ON state, a plasma OFF/bias ON state and a plasma OFF/bias OFF state, respectively, in accordance with an embodiment of the present invention. A voltage source 1014 is coupled with sample holder 1004 and is used to bias sample holder 1004, and hence sample 1102, during the ON state of a duty cycle. Referring to Figure 13A, voltage source 1014 is in an OFF state and positively charged etch species ejected from plasma 1100 are partially deflected near the surface of sample 1102. However, referring to Figure 13B, voltage source 1014 is in an ON state (i.e. negatively biasing sample holder 1004) and, thus, positively charged etch species ejected from plasma 1100 are held to an orthogonal trajectory (i.e. anisotropic trajectory) near the surface of sample 1102. In accordance

with an embodiment of the present invention, voltage source 1014 is used to apply a negative bias to sample holder 1004 in the range of 100 – 200 Watts during the ON state of a duty cycle. A pulsed plasma etch process (as compared with a continuous plasma etch process) may reduce the extent of positive charge build-up on sample 1102 during an etch process. However, the additional step of biasing sample holder 1004 with voltage source 1014 may still be utilized as part of the pulsed plasma etch process having pulsed reaction gas replenish in order to optimize the mitigation of undercutting of structures during the etch process. Therefore, in accordance with another embodiment of the present invention, the additional step of biasing sample holder 1004 with voltage source 1014 is used to extend the duration of the ON state of a duty cycle in a pulsed plasma etch process with pulsed reaction gas replenish.

[0064] Referring to Figure 13C, voltage source 1014 is in an ON state and negatively-charged particles ejected during the transition from plasma ON state to plasma OFF state are inhibited from approaching the surface of sample 1102, thus slowing the plasma OFF state step. However, referring to Figure 13D, voltage source 1014 is in an OFF state (i.e. zero-biasing sample holder 1004) and, thus, negatively-charged particles ejected during the transition from plasma ON state to plasma OFF state are inhibited from approaching the surface of sample 1102. In accordance with an embodiment of the present invention, voltage source 1014 is turned off in order to apply a zero bias to sample holder 1004 during the OFF state of a duty cycle. Therefore, in accordance with an embodiment of the present invention, sample holder 1004 is negatively biased with voltage source 1014 to extend the duration of the ON state of a duty cycle in a pulsed plasma etch process with pulsed reaction gas

replenish, while sample holder 1004 is zero-biased with voltage source 1014 to reduce the duration of the OFF state of the duty cycle.

[0065] Thus, a pulsed plasma system with pulsed reaction gas replenish for etching semiconductor structures has been disclosed. In an embodiment, a portion of a sample is removed by applying a pulsed plasma etch process. The pulsed plasma etch process comprises a plurality of duty cycles, wherein each duty cycle represents the combination of an ON state and an OFF state of a plasma. The plasma is generated from a reaction gas, wherein the reaction gas is replenished during the OFF state of the plasma, but not during the ON state. In another embodiment, a first portion of a sample is removed by applying a continuous plasma etch process. The continuous plasma etch process is then terminated and a second portion of the sample is removed by applying a pulsed plasma etch process with pulsed reaction gas replenish. It is to be understood that the pulsed reaction gas replenish process need not be tied to the pulsed plasma process. Thus, in accordance with another embodiment of the present invention, the ON state of the pulsed plasma duty cycle and the OFF state of the pulsed reaction gas replenish are independent from one another. In another embodiment, the OFF state of the pulsed plasma duty cycle and the ON state of the pulsed reaction gas replenish are independent from one another.

CLAIMS

What is claimed is:

1. A method for etching a sample, comprising:

removing a portion of said sample by applying a pulsed plasma process, wherein said pulsed plasma process comprises a plurality of duty cycles, wherein each duty cycle represents the combination of an ON state and an OFF state of a plasma, wherein said plasma is generated from a reaction gas, and wherein said reaction gas is replenished during said OFF state of said plasma but not during said ON state of said plasma.

2. The method of claim 1 wherein, as a result of said reaction gas being replenished during said OFF state of said plasma, the composition of gaseous species of said plasma at the end of said pulsed plasma process is within 1% of the composition of gaseous species of said plasma at the beginning of said pulsed plasma process.

3. The method of claim 2 wherein the pressure of said plasma at the end of said pulsed plasma process is within 1 mTorr of the pressure of said plasma at the beginning of said pulsed plasma process.

4. The method of claim 1 wherein said ON state is of a duration sufficiently short to substantially inhibit micro-loading in a reaction region adjacent to said sample, and wherein said OFF state is of a duration sufficiently long to substantially enable removal of a set of etch by-products from said reaction region adjacent to said sample.

5. The method of claim 1 wherein a negative bias is applied to said sample during said ON state, and wherein a zero bias is applied to said sample during said OFF state.

6. The method of claim 1 wherein the portion of each duty cycle comprised of said ON state is in the range of 5 – 95%.

7. The method of claim 4 wherein the duration of said OFF state of said plasma is selected to substantially match the time at which more than 50% of the etch by-products have been removed from said reaction region.

8. The method of claim 4 wherein an inert gas is used to enhance the removal of said set of etch by-products during said OFF state of said plasma.

9. A method for etching a sample, comprising:

removing a first portion of said sample by applying a continuous plasma process;

terminating said continuous plasma process; and

removing a second portion of said sample by applying a pulsed plasma process,

wherein said pulsed plasma process comprises a plurality of duty cycles, wherein each duty cycle represents the combination of an ON state and an OFF state of a plasma, wherein said plasma is generated from a reaction gas, and wherein said reaction gas is replenished during said OFF state of said plasma but not during said ON state.

10. The method of claim 9 wherein, as a result of said reaction gas being replenished during said OFF state of said plasma, the composition of gaseous species of said plasma at the end of said pulsed plasma process is within 1% of the composition of gaseous species of said plasma at the beginning of said pulsed plasma process.

11. The method of claim 10 wherein the pressure of said plasma at the end of said pulsed plasma process is within 1 mTorr of the pressure of said plasma at the beginning of said pulsed plasma process.

12. The method of claim 9 wherein said ON state is of a duration sufficiently short to substantially inhibit micro-loading in a reaction region adjacent to said sample, and wherein said OFF state is of a duration sufficiently long to substantially enable removal of a set of etch by-products from said reaction region adjacent to said sample.

13. The method of claim 9 wherein a negative bias is applied to said sample during said ON state, and wherein a zero bias is applied to said sample during said OFF state.

14. The method of claim 9 wherein the portion of each duty cycle comprised of said ON state is in the range of 5 – 95%.

15. The method of claim 9 wherein terminating said continuous etch process comprises detecting an end point.

16. The method of claim 15 wherein said end point is determined by the real-time composition of a set of chemical species generated during said continuous etch process.

17. The method of claim 15 wherein said end point is determined by the real-time film thickness measurement by interferometry.

18. The method of claim 9, further comprising:

removing a third portion of said sample by applying a second continuous plasma process;

terminating said second continuous plasma process; and

removing a fourth portion of said sample by applying a second pulsed plasma process, wherein said second pulsed plasma process comprises a second plurality of duty cycles, wherein each duty cycle represents the combination of a second ON state and a second OFF state of a second plasma, wherein said second plasma is generated from a second reaction gas, and wherein said second reaction gas is replenished during said OFF state of said second plasma but not during said ON state.

19. A system for use in etching a sample, wherein the system comprises:

a chamber equipped with a sample holder;

an evacuation device coupled with said chamber, wherein said evacuation device is for de-pressurizing said chamber;

a gas inlet device coupled with said chamber, wherein said gas inlet device is for injecting a reaction gas into said chamber;

a plasma ignition device coupled with said chamber, wherein said plasma ignition device is for igniting a plasma derived from said reaction gas; and

a computing device coupled with said plasma ignition device and with said gas inlet device, wherein said computing device comprises a processor and a memory, wherein said memory includes a set of instructions for controlling said plasma ignition device to switch between an ON state and an OFF state of a plasma in a pulsed plasma process, wherein said pulsed plasma process comprises a plurality of duty cycles, wherein each duty cycle represents the combination of one ON state and one OFF state of said plasma, wherein said memory also includes a set of instructions for controlling said gas inlet device to switch between an open state and a closed state, wherein said plasma is generated from said reaction gas, wherein said reaction gas is replenished when said gas inlet device is in said open state, and wherein said reaction gas is replenished during said OFF state of said plasma but not during said ON state.

20. The system of claim 19, further comprising:

a voltage source coupled with said sample holder, wherein said voltage source is for biasing said sample.

21. The system of claim 19, further comprising:

a detection device coupled with said chamber, wherein said detection device is for detecting an end point of a processing step.

22. The system of claim 19 wherein said ON state is of a duration sufficiently short to substantially inhibit micro-loading in a reaction region adjacent to a sample, and wherein said OFF state is of a duration sufficiently long to substantially enable removal of a set of etch by-products from said reaction region adjacent to said sample.

23. The system of claim 22 wherein the portion of each duty cycle comprised of said ON state is in the range of 5 – 95%.

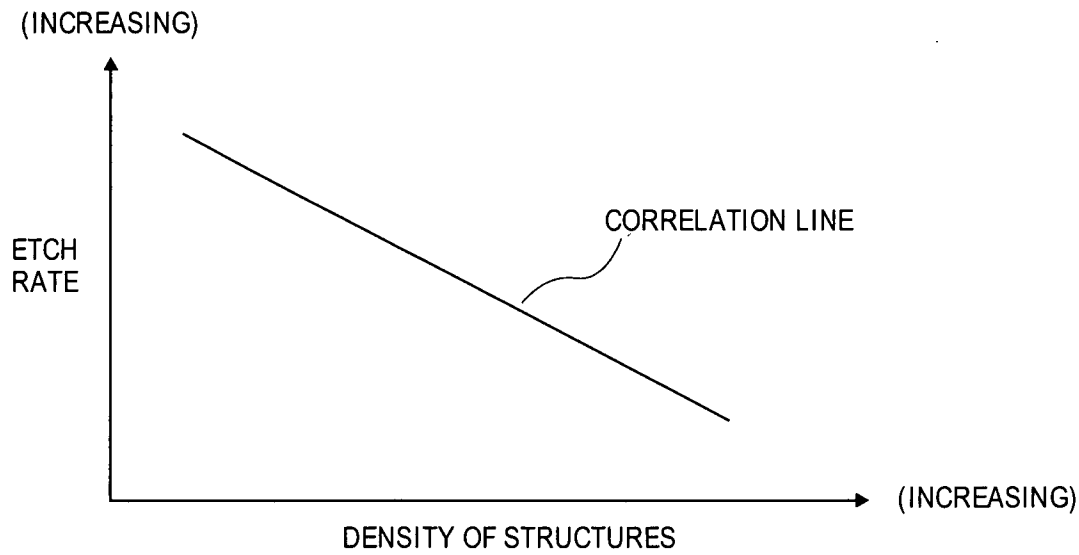
(INCREASING)
ETCH
RATE
CORRELATION LINE
(INCREASING)
DENSITY OF STRUCTURES

FIG. 1

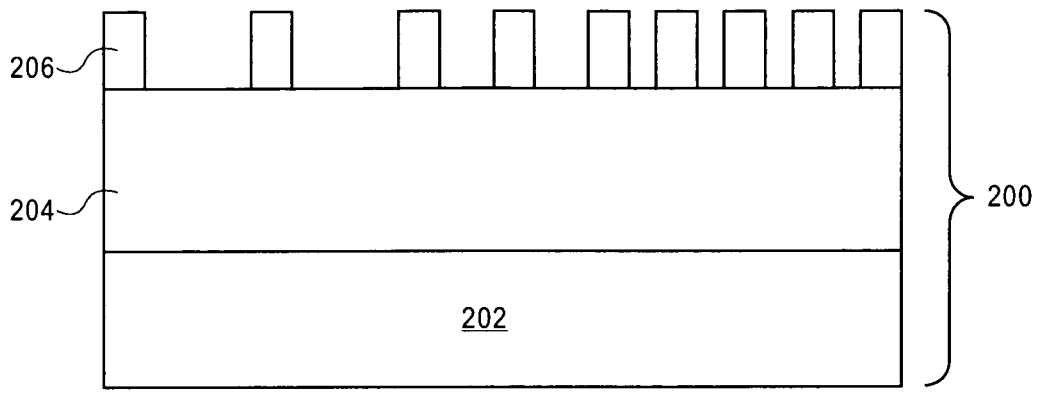

FIG. 2A

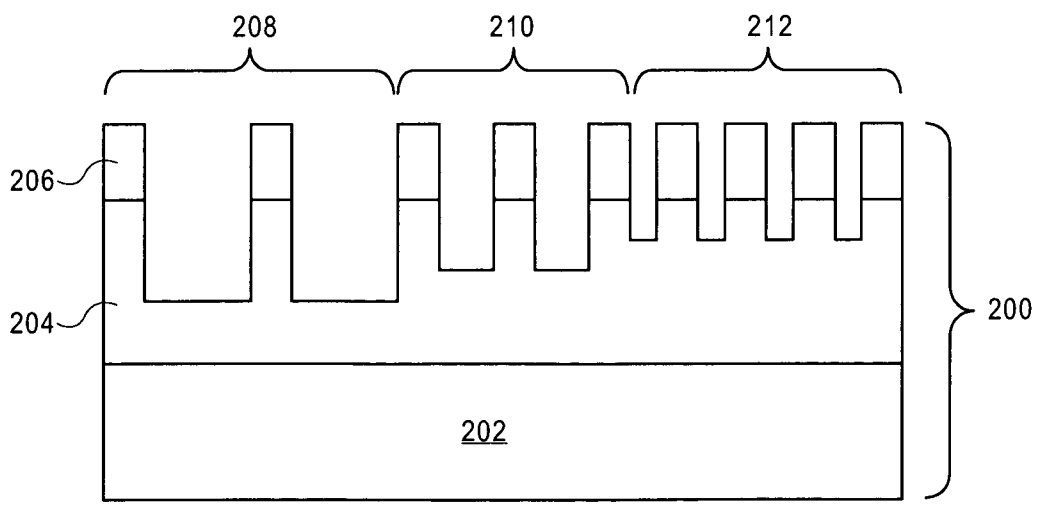

FIG. 2B

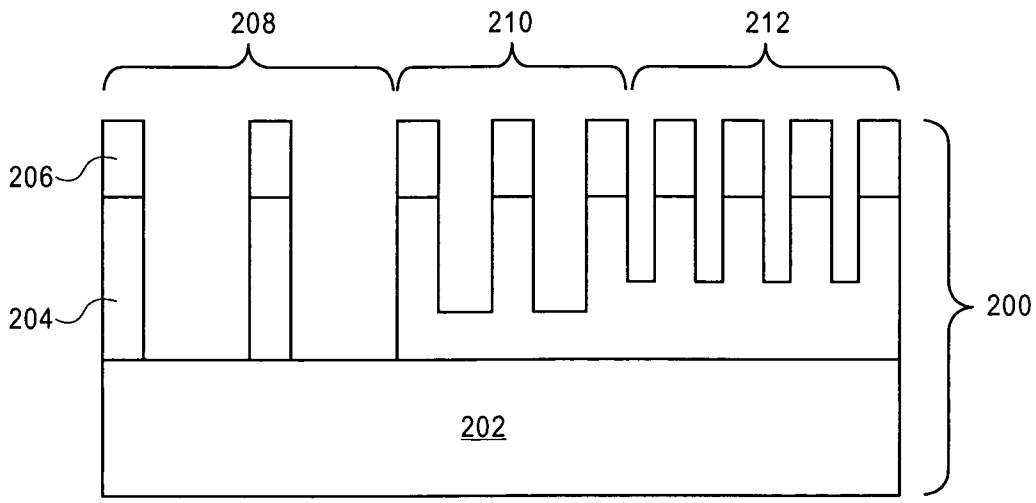

FIG. 2C

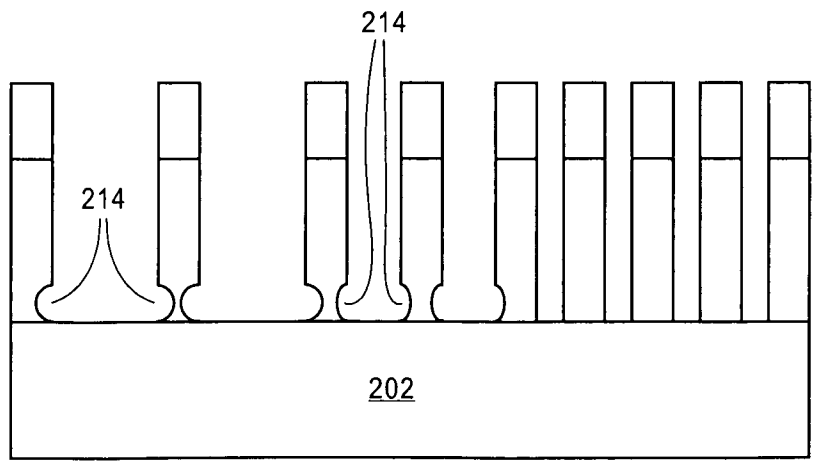

FIG. 2D

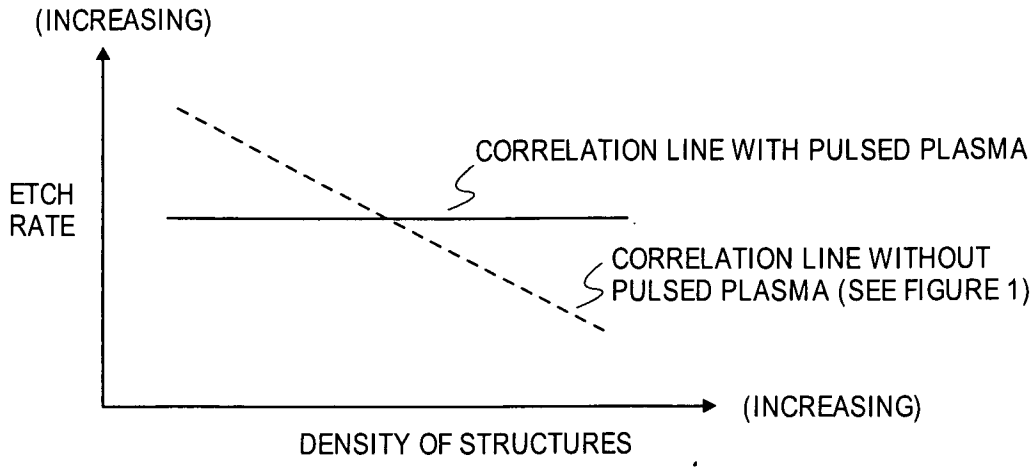
(INCREASING)
ETCH RATE
CORRELATION LINE WITH PULSED PLASMA
CORRELATION LINE WITHOUT PULSED PLASMA (SEE FIGURE 1)
(INCREASING)
DENSITY OF STRUCTURES

FIG. 3

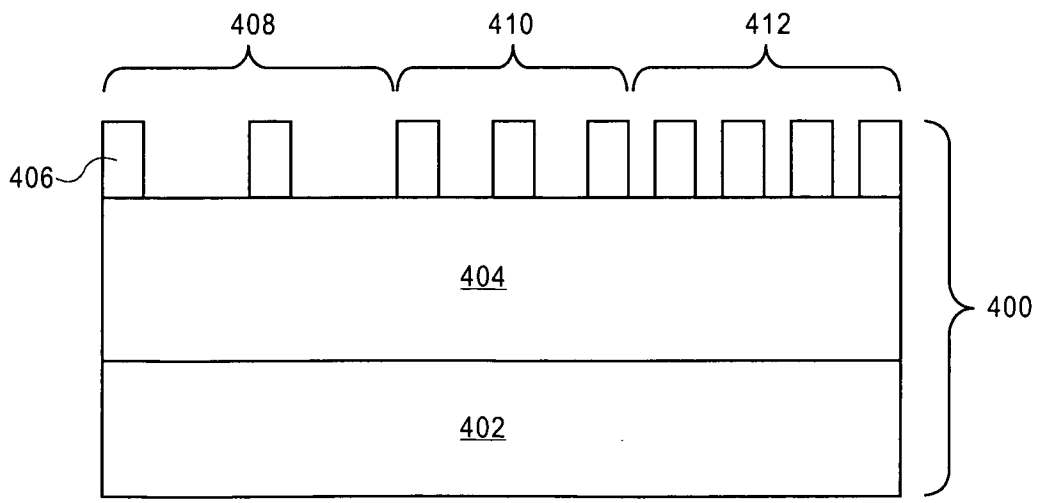
408
410
412
406
404
402
400

FIG. 4A

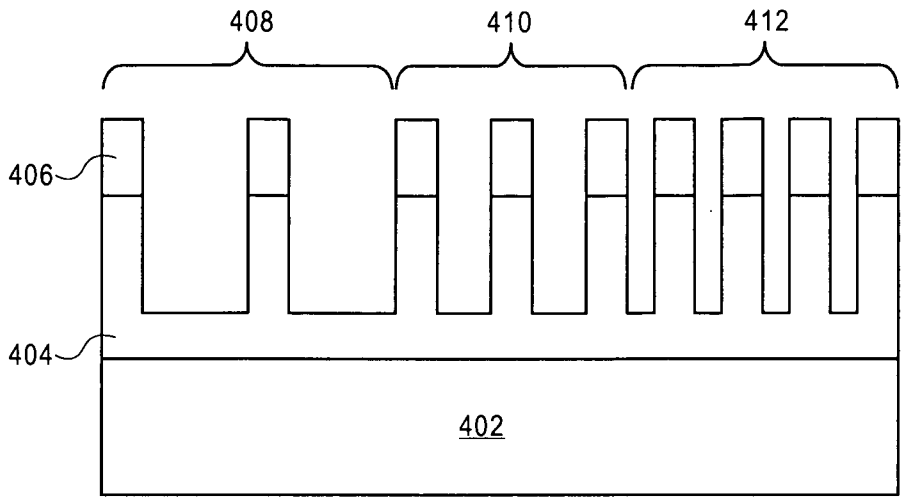

FIG. 4B

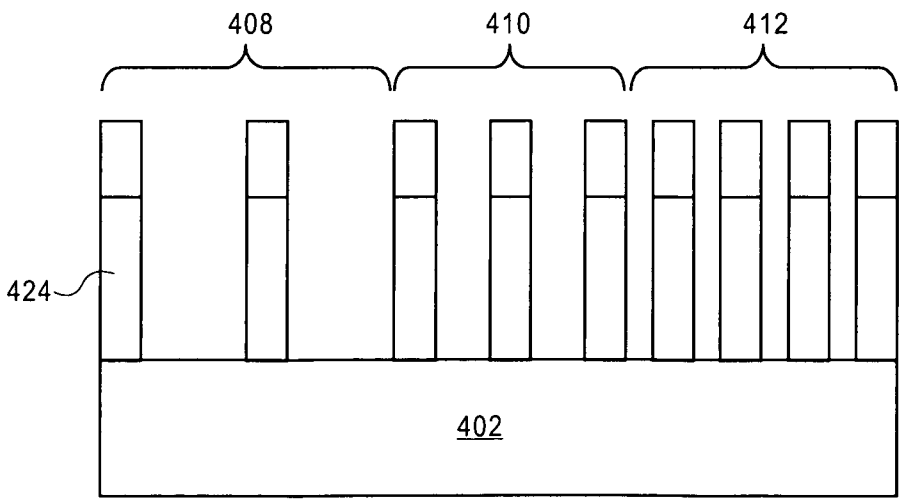

FIG. 4C

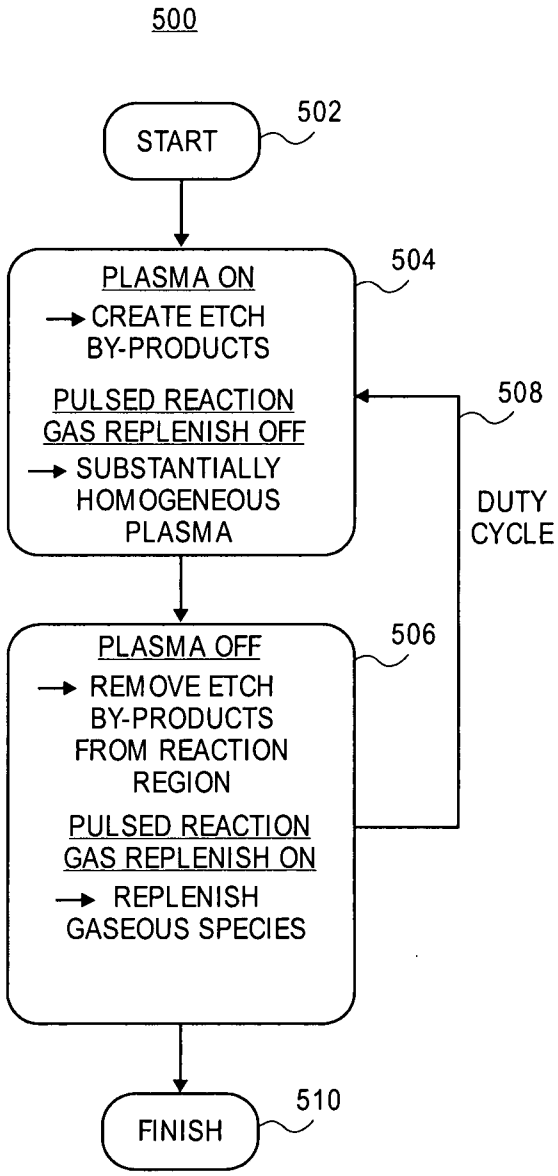
500
START
502
PLASMA ON
→ CREATE ETCH BY-PRODUCTS
PULSED REACTION GAS REPLENISH OFF
→ SUBSTANTIALLY HOMOGENEOUS PLASMA
504
508
DUTY CYCLE
PLASMA OFF
→ REMOVE ETCH BY-PRODUCTS FROM REACTION REGION
PULSED REACTION GAS REPLENISH ON
→ REPLENISH GASEOUS SPECIES
506
FINISH
510

FIG. 5A

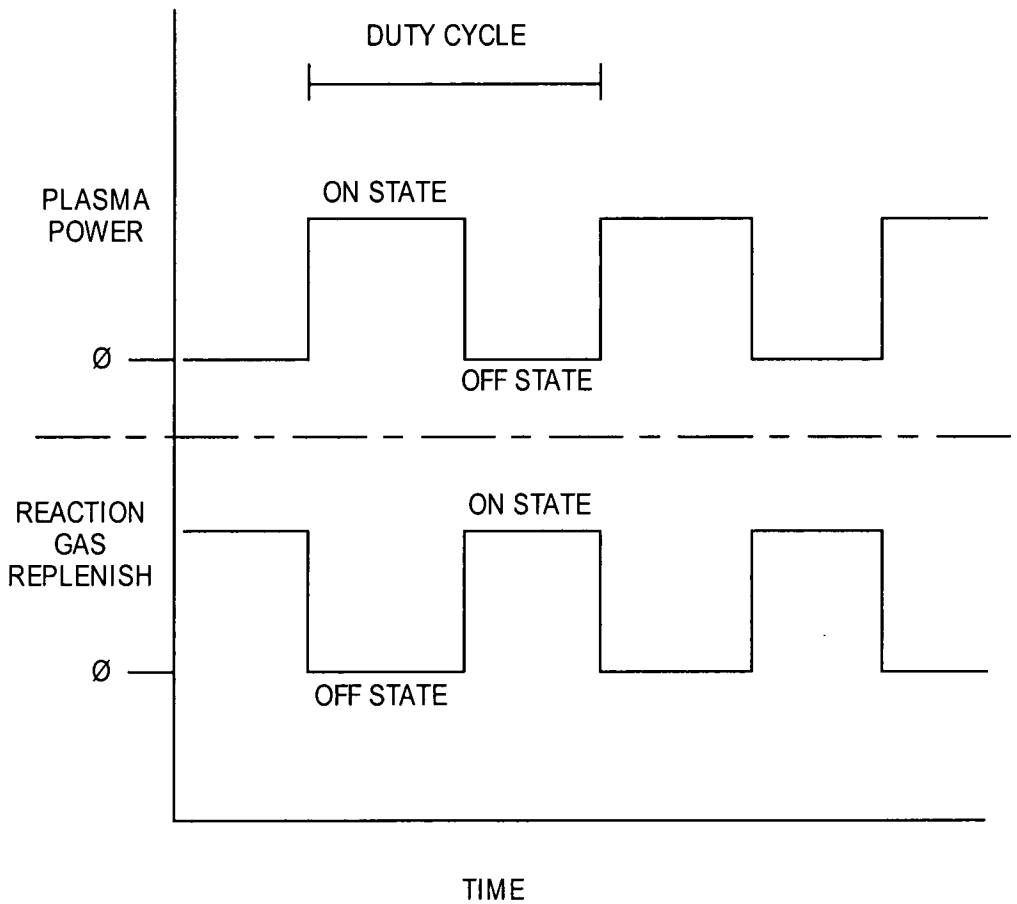
DUTY CYCLE
PLASMA POWER
ON STATE
Ø
OFF STATE
REACTION GAS REPLENISH
ON STATE
Ø
OFF STATE
TIME

FIG. 5B

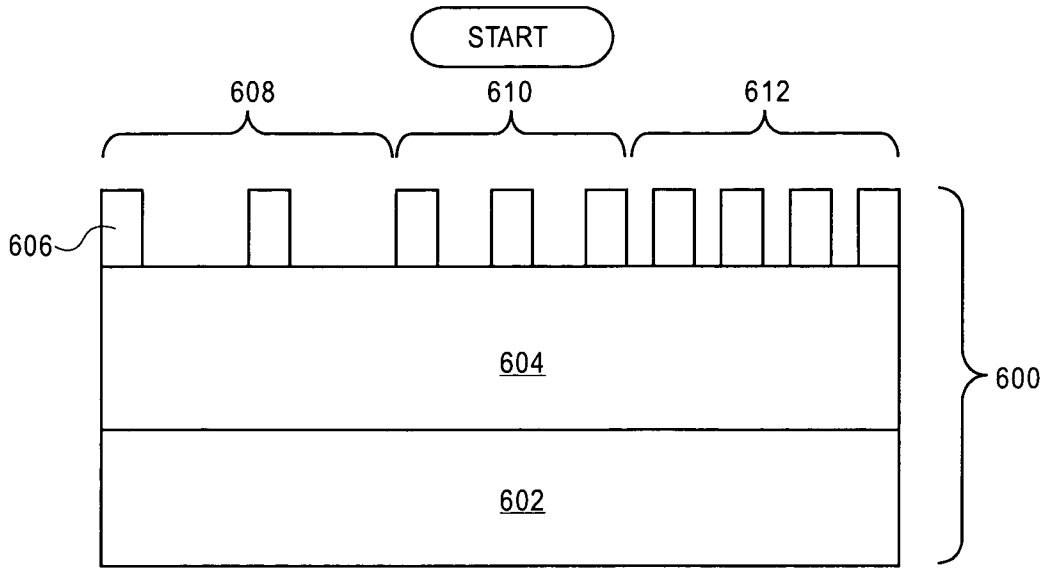
START
608
610
612
606
604
602
600

FIG. 6A

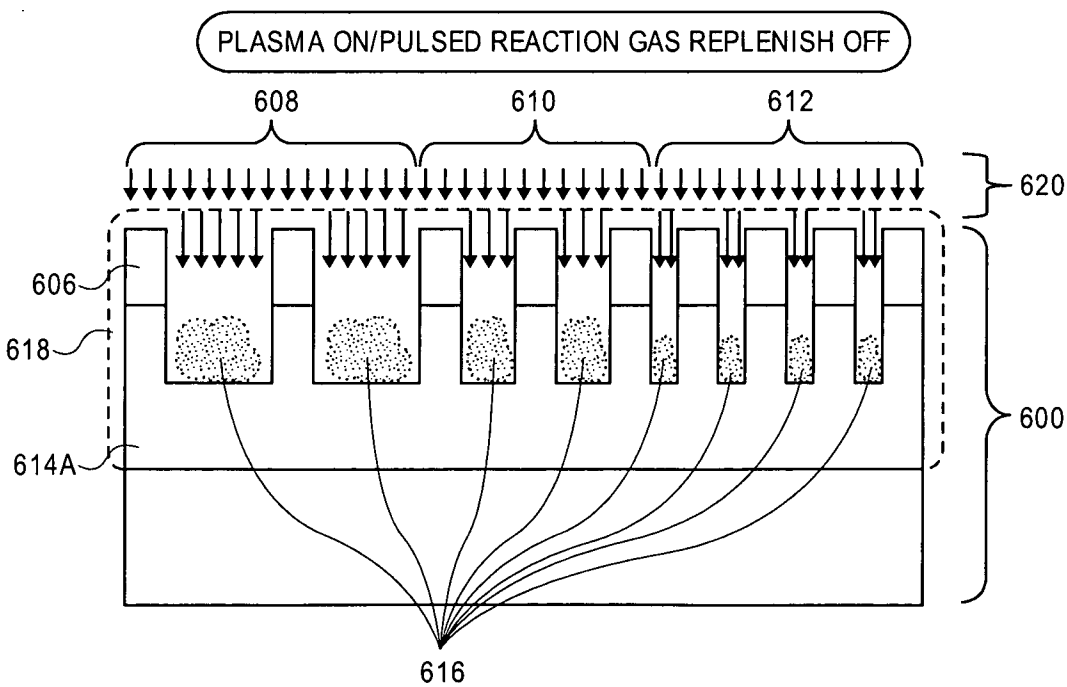
PLASMA ON/PULSED REACTION GAS REPLENISH OFF
608
610
612
620
606
618
614A
600
616

FIG. 6B

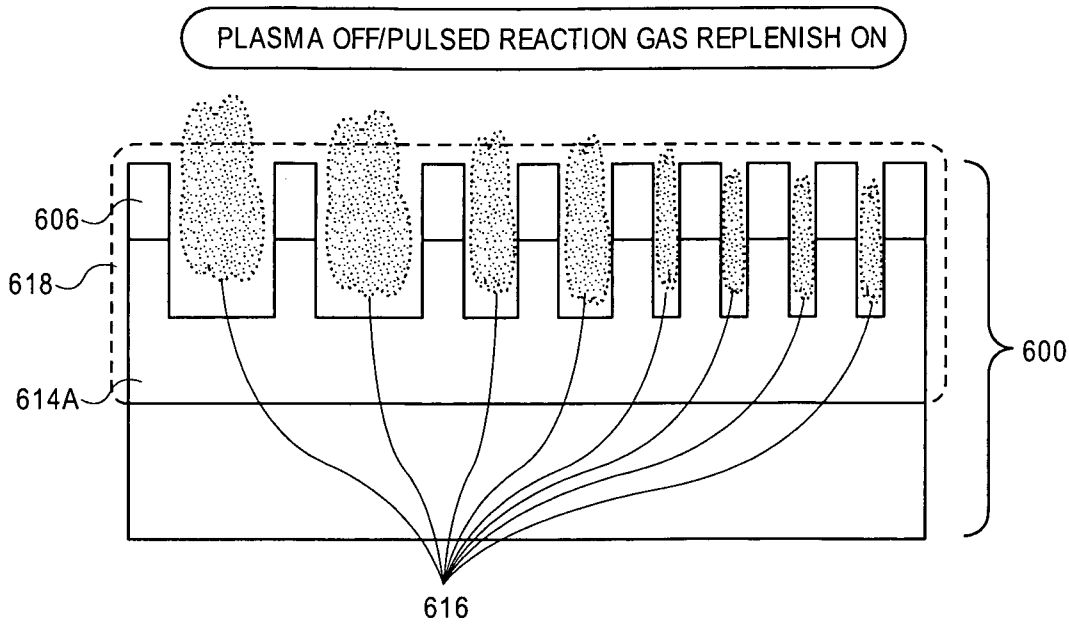
PLASMA OFF/PULSED REACTION GAS REPLENISH ON
606
618
614A
600
616

FIG. 6C

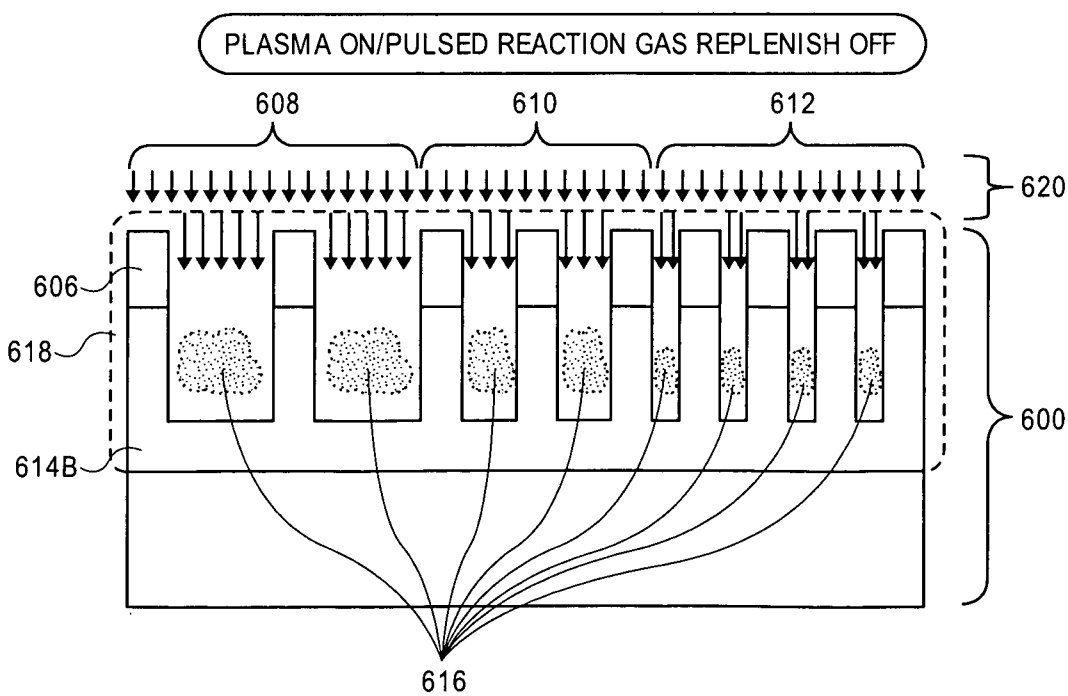
PLASMA ON/PULSED REACTION GAS REPLENISH OFF
608
610
612
620
606
618
614B
600
616

FIG. 6D

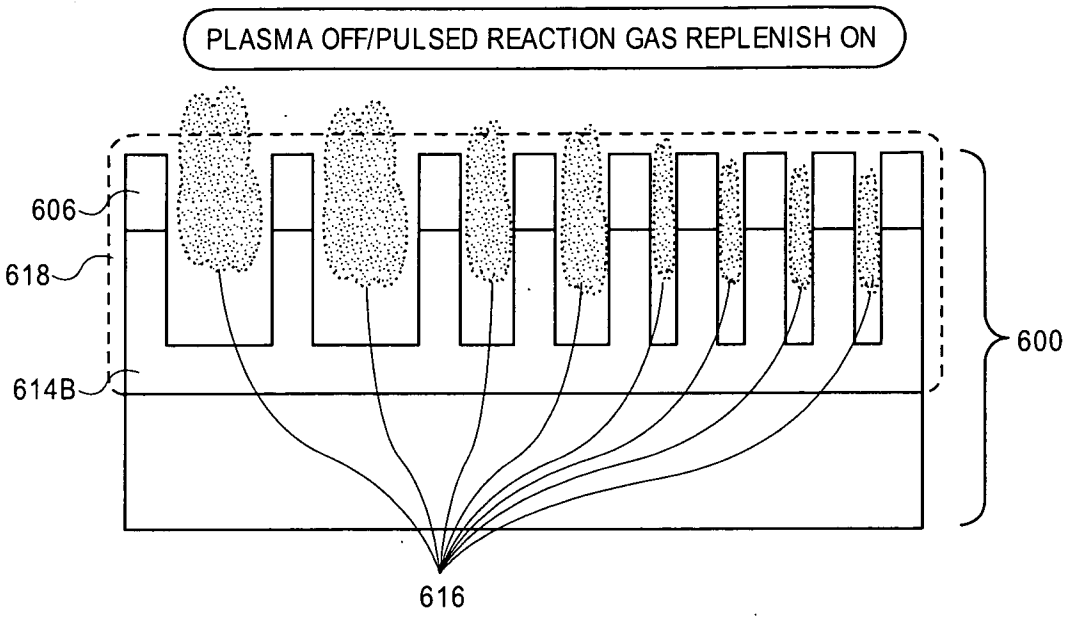
PLASMA OFF/PULSED REACTION GAS REPLENISH ON
606
618
614B
600
616

FIG. 6E

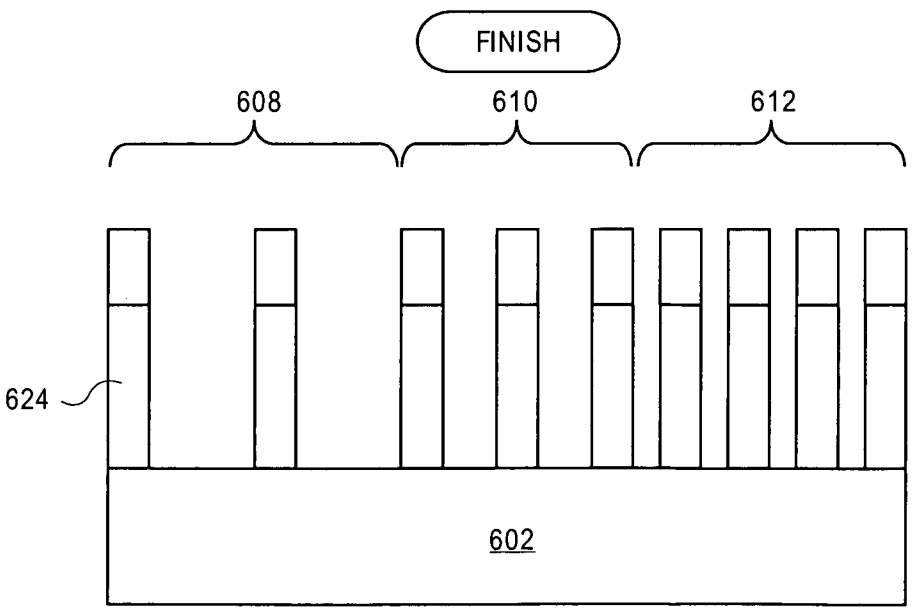
FINISH
608
610
612
624
602

FIG. 6F

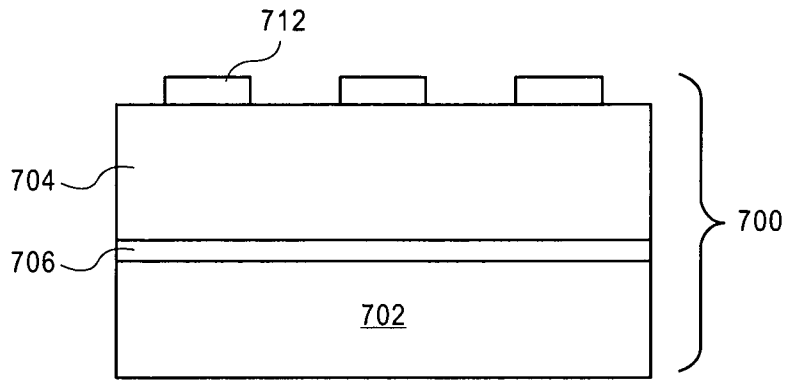

FIG. 7A

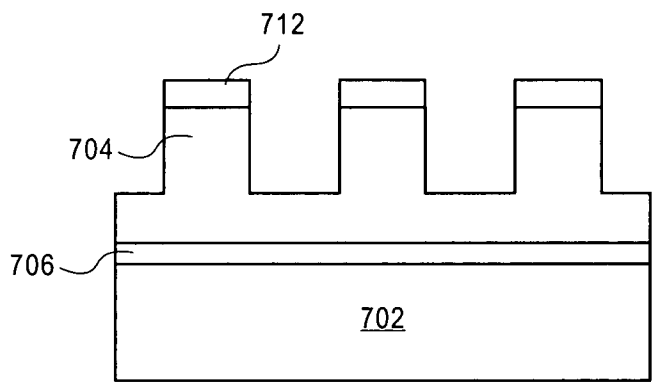

FIG. 7B

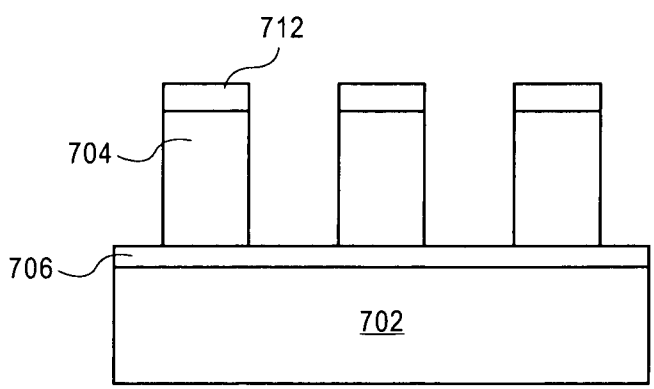

FIG. 7C

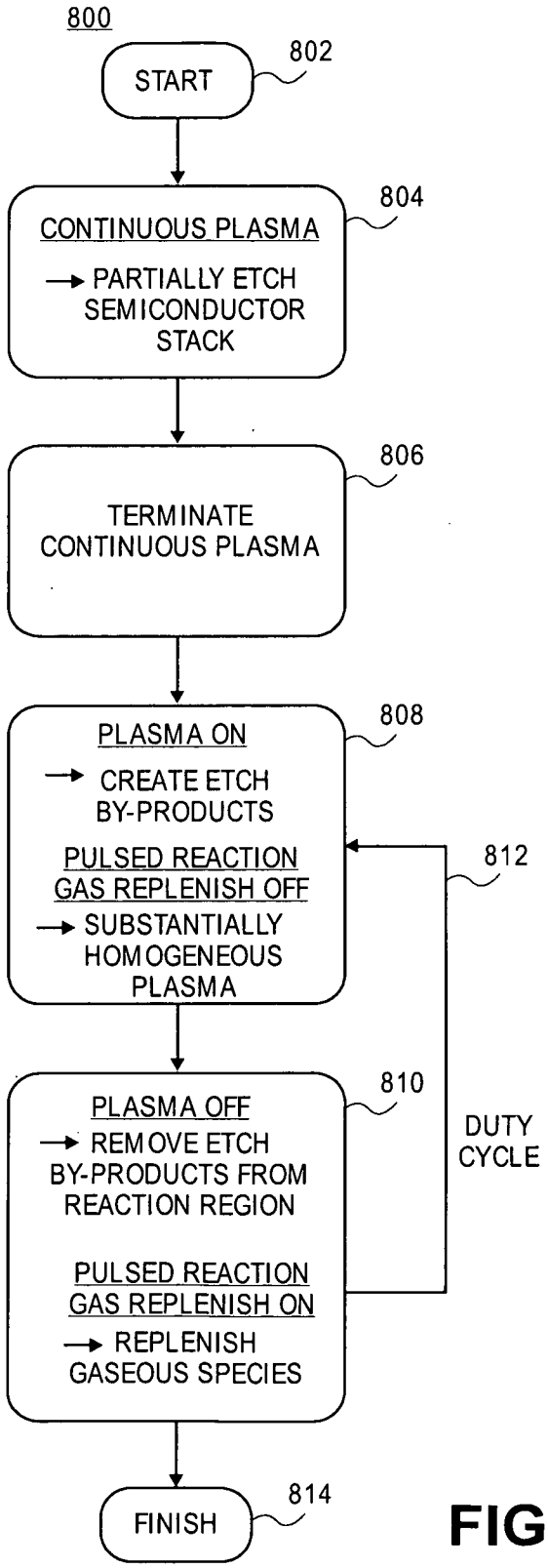
800
START
802
CONTINUOUS PLASMA
→ PARTIALLY ETCH SEMICONDUCTOR STACK
804
TERMINATE CONTINUOUS PLASMA
806
PLASMA ON
→ CREATE ETCH BY-PRODUCTS
PULSED REACTION GAS REPLENISH OFF
→ SUBSTANTIALLY HOMOGENEOUS PLASMA
808
812
PLASMA OFF
→ REMOVE ETCH BY-PRODUCTS FROM REACTION REGION
PULSED REACTION GAS REPLENISH ON
→ REPLENISH GASEOUS SPECIES
810
DUTY CYCLE
FINISH
814

FIG. 8

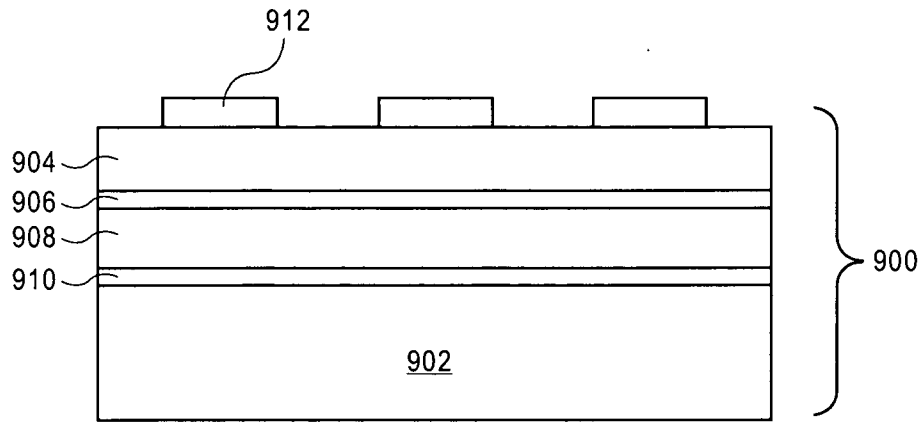

FIG. 9A

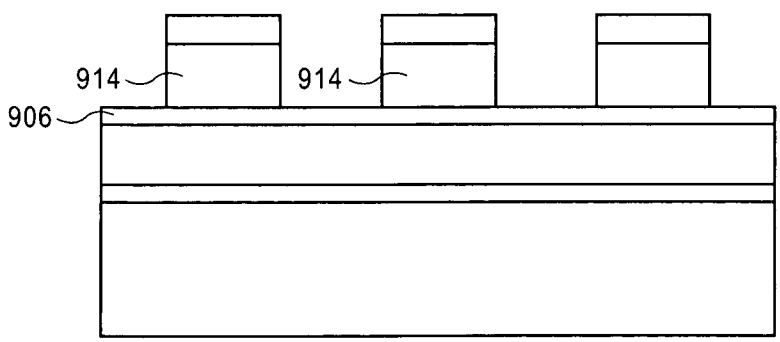

FIG. 9B

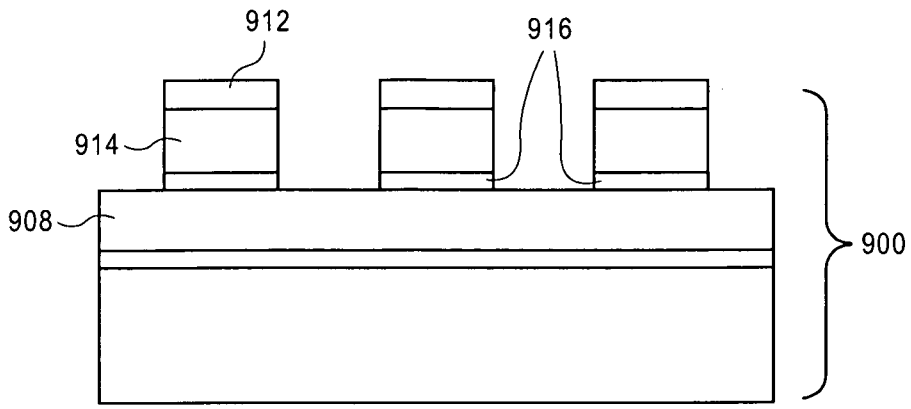

FIG. 9C

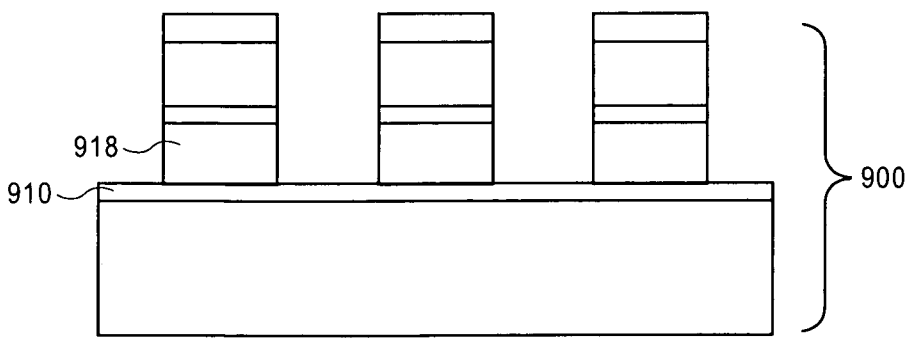

FIG. 9D

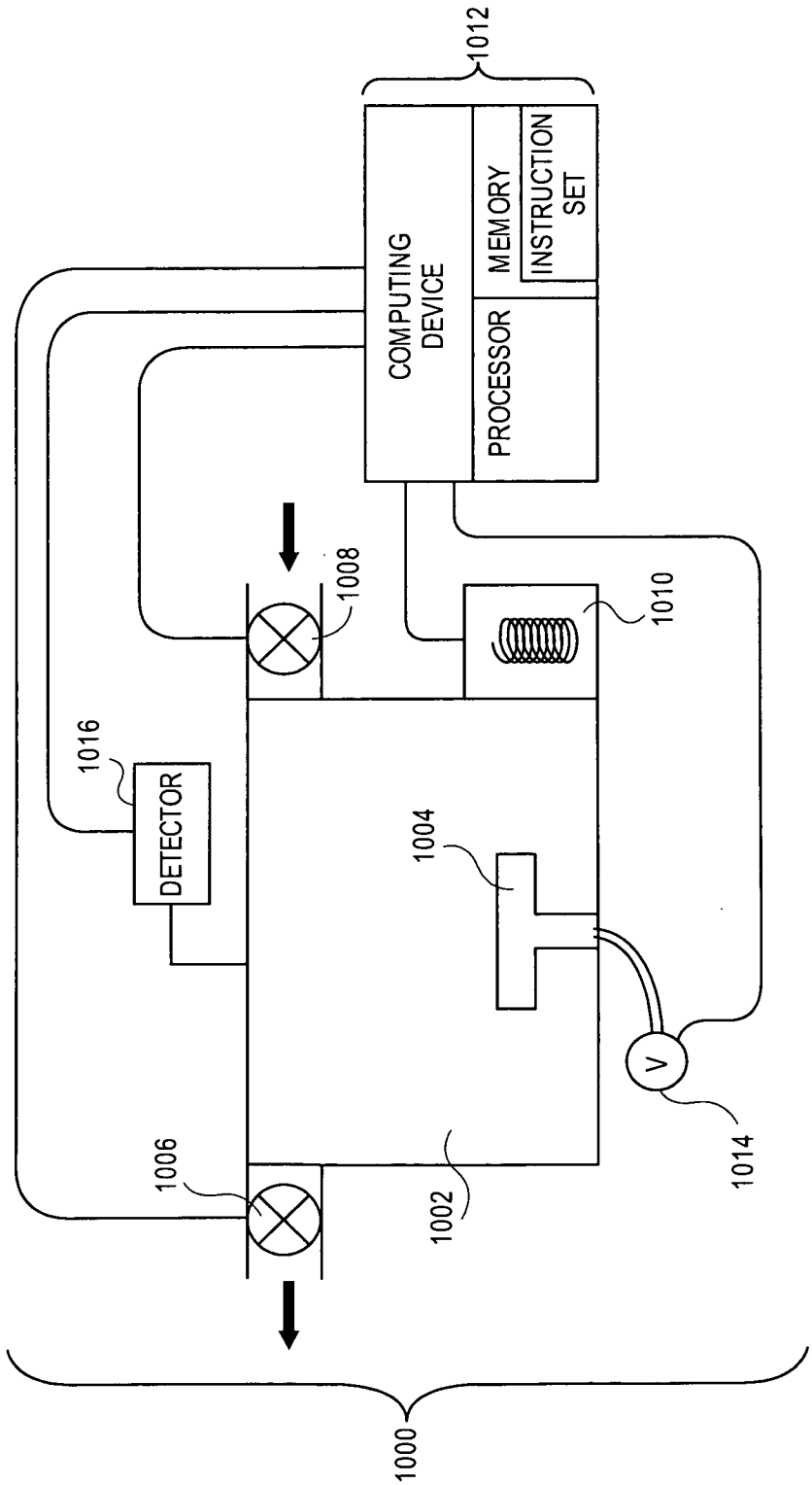
1012
COMPUTING DEVICE
MEMORY
INSTRUCTION SET
PROCESSOR
1008
1010
1016
DETECTOR
1004
V
1006
1002
1014
1000

FIG. 10

PLASMA ON

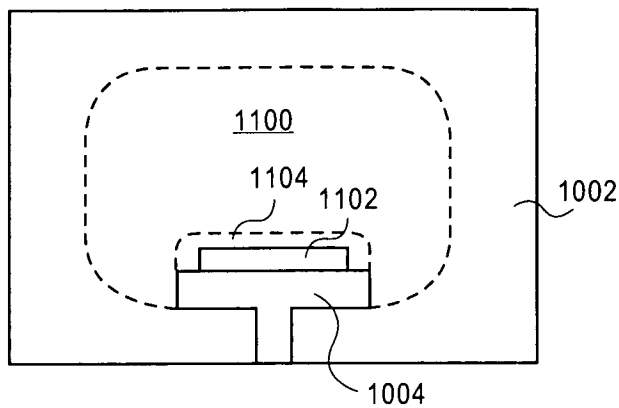

FIG. 11A

PLASMA OFF

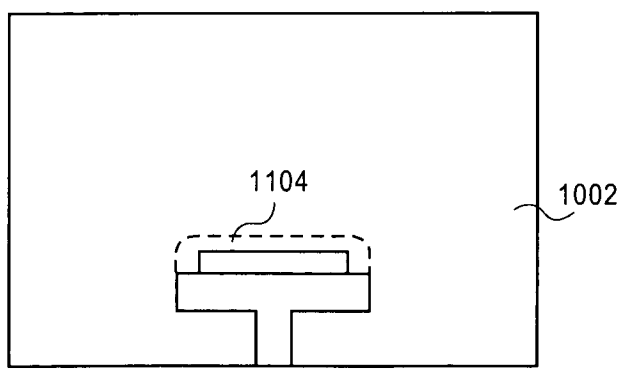

FIG. 11B

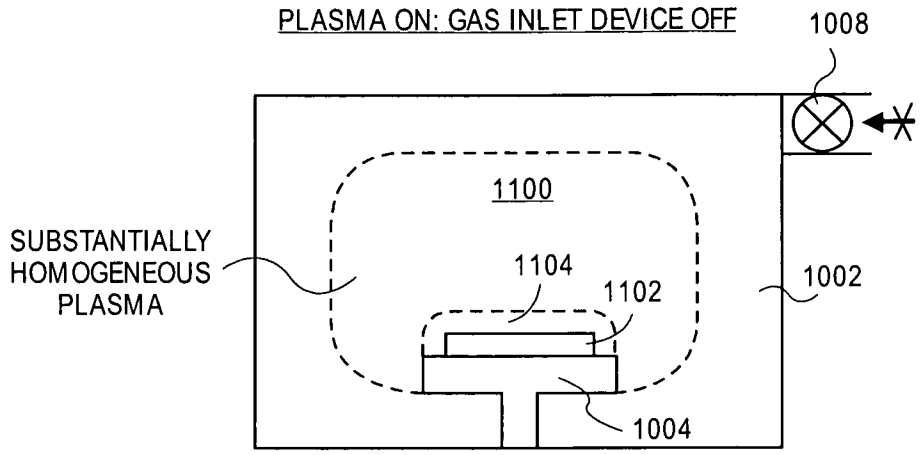

FIG. 12A

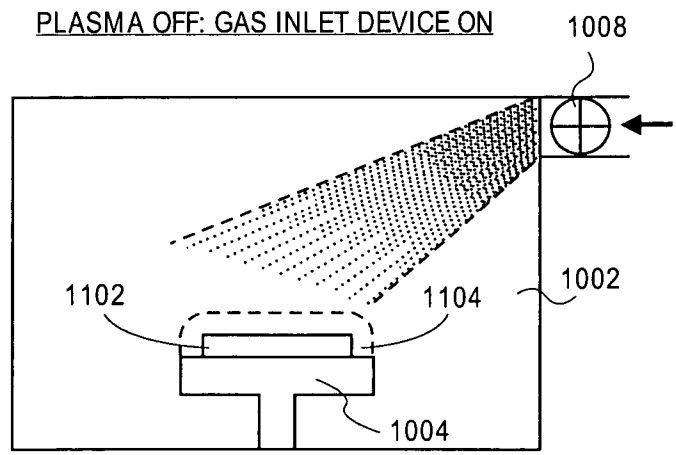

FIG. 12B

PLASMA ON: BIAS OFF

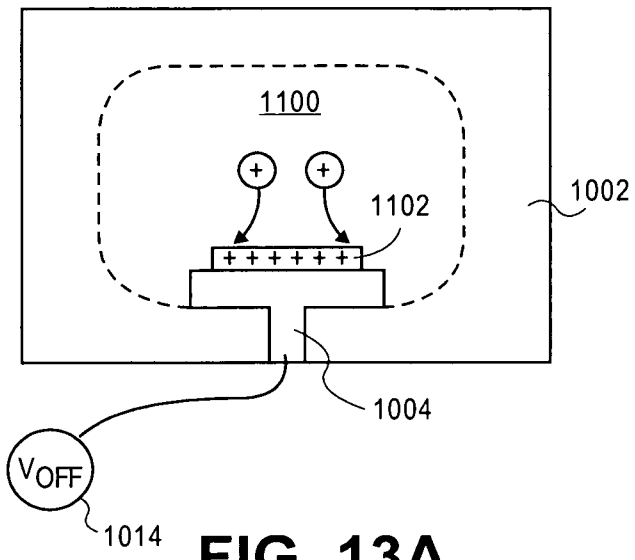

FIG. 13A

PLASMA ON: BIAS ON

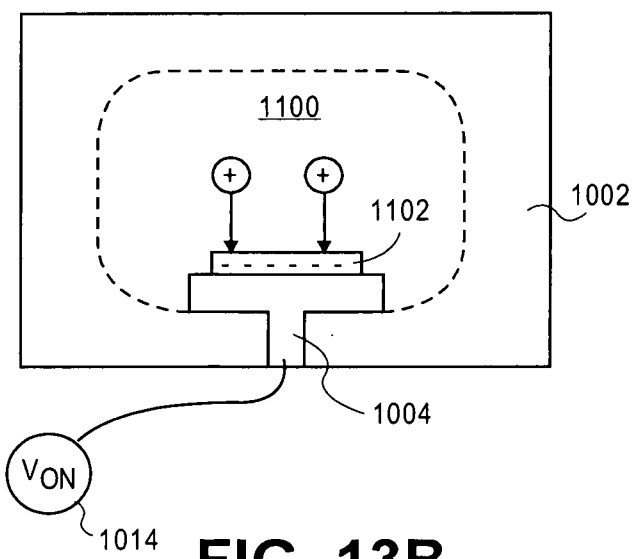

FIG. 13B

PLASMA OFF: BIAS ON

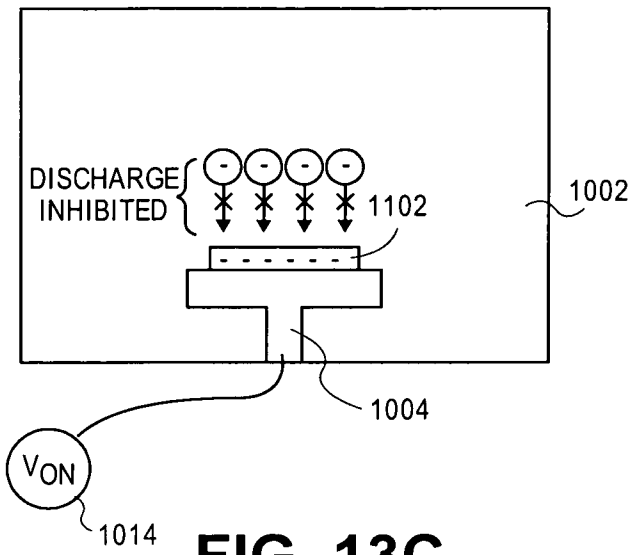

FIG. 13C

PLASMA OFF: BIAS OFF

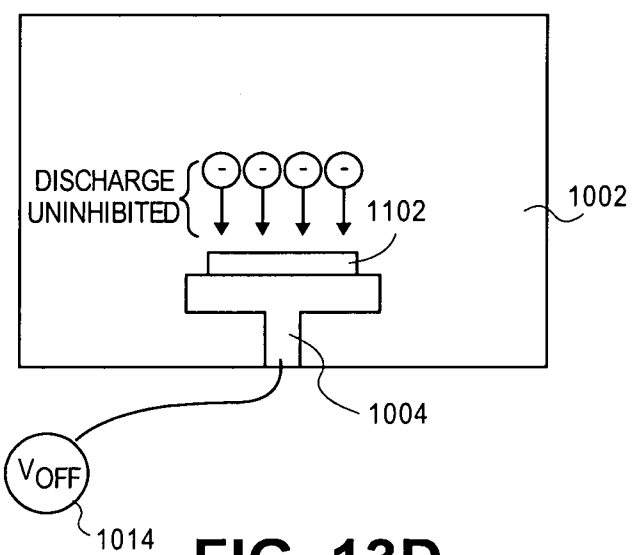

FIG. 13D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 08/02367

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/306, H01J 37/32 (2008.04)
USPC - 438/714; 156/345.35, 216/68
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC - 438/714; 156/345.35, 216/68

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC all classes, Google Internet - see key words below

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Searched US Pre-grant Publications, US Patent Full-Text, EPO Abstract, JPO Abstract, Google Internet Databases for semiconductor, plasma, etch, gas, composition, outlet, Kim, Lee, Patterson, Todorow, Desmukh

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002/0052111 A1 (Paterson et al.) 02 May 2002 (02.05.2002), entire document, especially para [0018]-[0025]	1-23
Y	US 2006/0270239 A1 (Triyoso et al.) 30 November 2006 (30.11.2006), entire document, especially para [0033] and [0034]	1-23
Y	US 5,877,407 A (Cadet et al.) 02 March 1999 (02.03.1999), entire document, especially col 6	2, 3, 10, 11, 17
A	US 2003/0196757 A1 (Todorow et al.) 23 October 2003 (23.10.2003), entire document	1-23

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 April 2008 (29.04.2008)	20 MAY 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (April 2007)