



Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Published:

- *without international search report and to be republished upon receipt of that report*

Description

Selection circuit and method for operating the selection circuit

Technical field

The invention relates to a selection circuit and method for operating the selection circuit. For example, the invention can be used for choosing the maximum supply voltage out of a set of supply voltages.

The power-up of chips that have several power supply sources is a difficult problem. Indeed, to work correctly any chip needs a minimum supply voltage. When there are several power supply sources with different voltage on each, it is necessary to determine which of these sources can provide a high enough voltage to the chip. Once this decision is taken, a mix of these valid power supply sources can be done to supply the chip. The decision or selection circuit is difficult to design because the decision circuit itself is also not supplied by one constant power supply source but by several and it has to work whatever the values of the voltages on these sources are.

Prior art

As known from the prior art figure 1 shows a solution for a decision circuit which is used to generate a power supply from two power supply sources VDD1 and VDD2. It is based on a feedback loop.

The circuit comprises a comparator CMP with a comparator input 1 connected to a first voltage input IN1 and a comparator input 2 connected to a second voltage input IN2. The first

comparator input 1 is applied with the first supply voltage VDD1 while the second comparator input 2 is applied with the second supply voltage VDD2. A first diode D1, which is connected in parallel to a first controllable switch SW1, is connected on the one side to the first voltage input IN1 and on the other side to a circuit output OVDD. A second diode D2, which is connected in parallel to a second controllable switch SW2, is connected on the one side to the second voltage input IN2 and on the other side to the circuit output OVDD. The control input of the first controllable switch is controlled by the output 3 of the comparator CMP. The output 3 of the comparator CMP is also connected to an inverter INV, whereby the output 6 of the inverter INV controls the control input of the second controllable switch SW2. Both power supply connectors 4 and 7 of the comparator CMP and the inverter INV are connected to the output voltage VDD.

The first switch SW1 is conducting, if the first control voltage SWVDD1 is lower than the difference between $VDD1 - V_t$ or if the first control voltage SWVDD1 is lower than the difference between $VDD - V_t$. In this case the first voltage VDD is VDD1. If the first control voltage SWVDD1 is higher than the difference between $VDD1 - V_t$ and higher than the difference between $VDD - V_t$, the first switch SW1 is not conducting and the voltages VDD and VDD1 are independent. The voltage V_t is a constant voltage. In principle this is also valid for the second switch SW2. The second switch SW2 is conducting, if the second control voltage SWVDD2 is lower than the difference between $VDD2 - V_t$ or if the second control voltage SWVDD2 is lower than the difference between $VDD - V_t$. In this case is the output voltage VDD is VDD2. If the second control voltage SWVDD2 is higher than the difference between $VDD2 - V_t$ and higher than the difference between $VDD - V_t$, the second switch SW2 is not conducting and the voltages VDD and VDD2 are independent.

At power-up, the diodes D1 and D2 pull up the node OVDD, which is the output of the circuit, to the voltage VDD equal to the maximum of the three values $VDD1 - V_{diode}$, $VDD2 - V_{diode}$ or 0. The voltage V_{diode} is the diode voltage and is equal for both diodes D1 and D2.

If this voltage VDD is lower than the constant voltage V_t , the comparator output 3 and the inverter output 6 will be floating and therefore be undefined. In some cases, this can lead to a large short circuit current. Let's assume for example that the first supply voltage $VDD1 = V_t + V_{diode}$, the second supply voltage $VDD2 = 0$, the first control voltage, also called comparator output voltage, $SWVDD1 = 0$ and also the second control voltage, also called inverter output voltage, $SWVDD2 = 0$. The first switch SW1 is conducting and will try to force the voltage $VDD = VDD1 = V_t + V_{diode}$ on the node OVDD. But because the control voltage $SWDVDD2 = 0$ and this is lower than $VDD - V_t = VDD1 - V_t = V_t + V_{diode} - V_t$, the second switch SW2 is also conducting and will try to force an output voltage $VDD = 0$ on the node OVDD.

In the following, the voltage difference $VDD1 - V_{diode}$ or the voltage difference $VDD2 - V_{diode}$ is supposed to be higher than the constant voltage V_t . The stable state of the circuit will be determined. The comparator output 3 will be 0 if the first voltage $VDD1$ is higher than the second voltage $VDD2$ and the comparator output 3 will be the maximum voltage if the second voltage $VDD2$ is higher than the first voltage $VDD1$. The maximum voltage is the higher value of the two values $VDD1 - V_{diode}$ or $VDD2 - V_{diode}$. The inverter INV, also supplied with the output voltage VDD, will produce a second control voltage $SWVDD2$, which is the maximum of $VDD1 - V_{diode}$ and $VDD2 - V_{diode}$, if the first control voltage $SWVDD1 = 0$. The inverter INV will produce a second control voltage $SWVDD2 = 0$ if the first control voltage $SWVDD1$ is the maximum of $VDD1 - V_{diode}$ and $VDD2 - V_{diode}$. The first control voltage $SWVDD1$ switches on the first switch SW1, this means the first

switch SW1 is conducting, and the second control voltage SWVDD2 switches off the second switch SW2, this means the second switch SW2 is not conducting, when the first voltage VDD1 is higher than the second voltage VDD2. The control voltages SWVDD1 and SWVDD2 switch off the first switch SW1 and switch on the second switch SW2 when the second voltage VDD2 is higher than the first voltage VDD1. The output voltage VDD is then going from $\max(VDD1, VDD2) - V_{diode}$ to $\max(VDD1, VDD2)$. Similarly, the control voltages SWVDD1 and SWVDD2 will either stay on 0 or go up to $\max(VDD1, VDD2)$.

This circuit has several drawbacks. It will not function, if the first voltage VDD1 and second voltage VDD2 are lower than $V_t + V_{diode}$. If the first voltage VDD1 and the second voltage VDD2 are lower than $V_t + V_{diode}$, there can be a high short circuit parasitic current.

The invention

An object of the invention is to provide a selection circuit and a method for operating the selection circuit which chooses the maximum supply voltage from two different supply voltages independent of the amount of these supply voltages.

An advantage of the selection circuit and the method for operating the selection circuit is that no short circuit currents can occur.

The object of the invention is solved by a selection circuit with the features according to claim 1 and a method for operating the selection circuit with the features according to claim 8.

The selection circuit according to the invention comprises a comparator with comparator inputs connected to a first and a second voltage input and a comparator output connected to a

control input of a first controllable switch and an inverter. The selection circuit further comprises a second controllable switch with a second control input connected to the inverter. The first voltage input is connectable to a selection circuit output by means of the first controllable switch and the second voltage input is connectable to the selection circuit output by means of the second controllable switch. The inverter with its power supply connector is connected to the first voltage input and at least the comparator with its power supply connector is connected to the second voltage input.

The method for operating a selection circuit according to the invention comprises the following steps:

A first voltage is applied at the first voltage input and/or a second voltage is applied at the second voltage input.

If the first voltage is higher than the second voltage, a pull down element pulls the output of the comparator down and the first voltage input is connected to the selection circuit output by means of the first controllable switch.

If the first voltage is lower than the second voltage, a further pull down element pulls the output of the inverter down and the second voltage input is connected to the selection circuit output by means of the second controllable switch.

Advantageous further developments of the invention arise from the characteristics indicated in the dependent patent claims.

In an embodiment according to the invention the selection circuit further comprises a controllable pull down element connected between the comparator output and a reference potential.

In another embodiment of the invention the selection circuit further comprises a further controllable pull down element connected between the inverter output and the reference potential.

Advantageously in the selection circuit according to the invention the pull down element and the further pull down element are NMOS transistors.

According to a preferred embodiment of the selection circuit the controllable pull down element comprises a control input connected to the first voltage input and can be controlled by a first supply voltage.

According to a another preferred embodiment of the selection circuit the further controllable pull down element comprises a control input connected to the second voltage input and can be controlled by a second supply voltage.

At least in the selection circuit according to the invention the comparator can be an operational amplifier.

Brief description of the drawings

Subsequently, the invention is further explained with the drawings.

Figure 1 shows an embodiment of a selection circuit according to the prior art.

Figure 2 shows an embodiment of a selection circuit according to the invention.

Description of an embodiment of the invention

Contrary to the solution presented above in figure 1, the solution according to the invention as shown in figure 2 is not based on a feedback loop.

The selection circuit comprises a comparator CMP with a comparator input 1 connected to a first voltage input IN1 and a comparator input 2 connected to a second voltage input IN2. The first comparator input 1 is applied with a first supply voltage VDD1 while the second comparator input 2 is applied with the second supply voltage VDD2 via the voltage inputs IN1 and IN2. A first controllable switch SW1 is connected on the one side to the first voltage input IN1 and on the other side to a circuit output O. A second controllable switch SW2 is connected on the one side to the second voltage input IN2 and on the other side to the circuit output O. The control input CI1 of the first controllable switch SW1 is controlled by the output 3 of the comparator CMP. The output 3 of the comparator CMP is also connected to an inverter INV whereby the output 6 of the inverter INV controls the control input CI2 of the second controllable switch SW2. The power supply connector 4 of the comparator CMP is supplied with the second voltage VDD2 while the power supply connector 7 of the inverter INV is supplied with the first voltage VDD1. The output 3 of the comparator CMP is further connected to a first pull down element PD1, which can be nonlinear. If the voltage at the control input CI3 of the first pull down element PD1 is higher than the voltage V_t , the output 3 of the comparator is pulled down to ground GND by means of the first pull down element PD1. The control input CI3 of the first pull down element PD1 is supplied with the first voltage VDD1. The output 6 of the inverter INV is further connected with a second pull down element PD2, which also can be nonlinear. If the voltage at the control input CI4 of the second pull down element PD2 is higher than the voltage V_t , the output 6 of the inverter INV is pulled down to ground GND by means of the second pull down element PD2. The control input CI4 of the second pull down element PD2 is supplied with the second voltage VDD2.

The pull down elements PD1 and PD2 are preferably transistors and work in the same way. If the voltages at the control in-

puts CI3 or CI4 of the pull down elements PD1 or PD2 are lower than the voltage V_t , the voltages SWVDD1 or SWVDD2 will be undefined. If the voltages at the pull down elements PD1 or PD2 are floating, the pull down elements can be ignored.

The pull down elements PD1 and PD2 are used to extend the range where the circuit is working. Without them the circuit would work only when the two supply voltages VDD1 and VDD2 are both higher than the voltage V_t . Normally, the first pull down element PD1 is a weak NMOS transistor and the second pull down element PD2 is also a weak NMOS transistor.

When the first supply voltage VDD1 is higher than the voltage V_t and the second supply voltage VDD2 is also higher than the voltage V_t , the pull down elements PD2 and PD1 enter in conflict with the output 3 of the comparator CMP or the output 6 of the inverter INV because both pull down elements PD1 and PD2 try to pull down the control voltages SWVDD1 and SWVDD2 to GND while either the comparator CMP or the inverter INV tries to pull these nodes SWVDD1 and SWVDD2 up to the second supply voltage VDD2 or the first supply voltage VDD1. But as the pull down elements PD2 and PD1 strengths are much lower than the comparator CMP and the inverter INV, it are these latter which fix the voltages SWVDD1 and SWVDD2.

When the first supply voltage VDD1 is lower than the voltage V_t and the voltage V_t is lower than the second supply voltage VDD2, all the elements using the first power supply VDD1 have their outputs floating. The first pull down element PD1 can be ignored and the inverter output 6 is floating. But thanks to the second pull down element PD2, the node SWVDD2 is pulled down to GND. Therefore the output 0 is connected to the second supply voltage VDD2 through the switch SW2.

When the second supply voltage VDD2 is lower than the voltage V_t and the voltage V_t is lower than the first supply voltage VDD1, all the elements using the second power supply VDD2

have their outputs floating. The pull down element PD2 can be ignored and the comparator output 3 is floating. But thanks to the first pull down element PD1, the node SWVDD1 is pulled down to GND. Therefore the output 0 is connected to the first supply voltage VDD1 through the switch SW1.

The switches SW1 and SW2 are preferably transistors and work in the same way. As example, in the following the way of working of the first switch SW1 is described.

The first switch SW1 is conducting, if the first control voltage SWVDD1 is lower than the difference between $VDD1 - V_t$ or the first control voltage SWVDD1 is lower than the difference between $VDD - V_t$. In this case the output voltage VDD is VDD1. If the first control voltage SWVDD1 is higher than difference between $VDD1 - V_t$ and higher than difference between $VDD - V_t$, the first switch SW1 is not conducting and the voltages VDD and VDD1 are independent.

The comparator CMP works as follows. If the voltage VDD2 at the comparator input 2 is higher than the voltage VDD1 at the comparator input 1, the comparator output 3 delivers a first control voltage SWVDD1 which is equal to the second voltage VDD2. If the voltage VDD2 at the comparator input 2 is lower than the voltage VDD1 at the comparator input 1, the comparator output 3 delivers a first control voltage SWVDD1 which is equal to 0. If the second voltage VDD2 is lower than the voltage V_t , the comparator output 3 is floating.

The inverter INV generates a second control voltage SWVDD2 = 0, if the voltage at its input 5 is VDD2. If the voltage at the input 5 of the inverter INV is 0, the inverter INV generates a second control voltage SWVDD2 = VDD1. If the first voltage VDD1, which is the operation voltage of the inverter INV, is lower than the voltage V_t , the inverter output 6 is floating.

There are basically five cases of functioning:

1. The second voltage VDD2 is lower than the constant voltage V_t :

Then the first control voltage SWVDD1 at the comparator output 3 is floating. If the first voltage VDD1 is higher than the constant voltage V_t , then the first pull down element PD1 will pull the first control voltage SWVDD1 to 0 and the output 0 is connected to the first voltage input IN1.

2. The first voltage VDD1 is lower than the constant voltage V_t :

Then the inverter output 6 is floating. If the second voltage VDD2 is higher than the constant voltage V_t , then the first control voltage SWVDD1 at the comparator output 3 is equal to the second voltage VDD2. The second pull down element PD2 will pull the second control voltage SWVDD2 at the inverter output 6 to 0.

3. The first voltage VDD1 is higher than the second voltage VDD2 and the second voltage VDD2 is higher than the voltage V_t :

The first control voltage SWVDD1 at the comparator output 3 goes to 0 and the second control voltage SWVDD2 at the inverter output 6 adopts the value of the first voltage VDD1.

4. The second voltage VDD2 is higher than the first voltage VDD1 and the first voltage VDD1 is higher than the voltage V_t :

The first control voltage SWVDD1 at the comparator output 3 becomes the second voltage VDD2 and the second control voltage SWVDD2 at the inverter output 6 becomes 0.

5. The first voltage VDD1 is lower than the voltage V_t and the second voltage VDD2 is lower than the voltage V_t :

11

Then the comparator output 3 and the inverter output 6 will be floating and the output voltage VDD at the circuit output 0 will be floating.

In all cases, the value of the output voltage VDD is always the maximum of the two voltages VDD1 and VDD2.

By using several selection circuits as shown in figure 2, it is possible to choose the maximum supply voltage from a set of different supply voltages V1 - Vn, whatever their number n is, thanks to the formula:

$$\max(V1, V2, V3, V4, \dots) = \max(\dots \max(\max(\max(V1, V2), V3), V4) \dots)$$

The advantages of the selection circuit according to the invention are among other things the following.

The selection circuit will work also with low voltages. If the first voltage VDD1 or the second voltage VDD2 is above the voltage Vt, the selection circuit delivers a non floating output voltage VDD at its output 0.

Another advantage is the low power consumption of the circuit. In general, the comparator CMP is consuming much more current than the inverter INV. So it is possible to optimize the power consumption on one power supply by connecting it to VDD1.

In all cases, this circuit is faster than the prior art solution as shown in figure 1 because it does not rely on a loop and it reaches its final state faster.

Having illustrated and described preferred embodiments for a novel selection circuit, it is noted that variations and modifications in the circuit can be made without departing from the spirit of the invention or the scope of the appended claims.

Reference list

VDD1	first supply voltage
VDD2	second supply voltage
VDD	output voltage
OVDD	circuit output
CMP	comparator
SW1	first switch
SW2	second switch
SWVDD1	first control voltage
SWVDD2	second control voltage
INV	inverter
PD1	first pull down element
PD2	second pull down element
D1	first diode
D2	second diode
1	first comparator input
2	second comparator input
3	comparator output
4	comparator power supply connector
5	inverter input
6	inverter output
7	inverter power supply connector
IN1	first voltage input
IN2	second voltage input
0	selection circuit output

Claims

1. Selection circuit, comprising
a comparator (CMP) with comparator inputs (1, 2) connected to a first and a second voltage input (IN1, IN2) and a comparator output (3) connected to a control input (CI1) of a first controllable switch (SW1) and an inverter (INV),
a second controllable switch (SW2) with a second control input (CI2) connected to said inverter (INV),
whereby said first voltage input (IN1) is connectable to a selection circuit output (O) by means of said first controllable switch (SW1) and said second voltage input (IN2) is connectable to said selection circuit output (O) by means of said second controllable switch (SW2),
whereby said inverter (INV) with its power supply connector (7) is connected to said first voltage input (IN1), and
whereby said comparator (CMP) with its power supply connector (4) is connected to said second voltage input (IN2).
2. Selection circuit according to claim 1, further comprising
a controllable pull down element (PD1) connected between the comparator output (3) and a reference potential (GND).
3. Selection circuit according to claim 1 or 2, further comprising
a further controllable pull down element (PD2) connected between the inverter output (6) and the reference potential (GND).
4. Selection circuit according to claim 2 or 3,
whereby the pull down element (PD1) and the further pull down element (PD2) are NMOS transistors.
5. Selection circuit according to any of the claims 2 to 4,
whereby the controllable pull down element (PD1) comprises a control input (CI3) connected to the first voltage input (IN1) and can be controlled by a first supply voltage (VDD1).

6. Selection circuit according to any of the claims 2 to 5, whereby the further controllable pull down element (PD2) comprises a control input (CI4) connected to the second voltage input (IN2) and can be controlled by a second supply voltage (VDD2).

7. Selection circuit according to any preceding claim, whereby the comparator (CMP) is an operational amplifier.

8. Method for operating a selection circuit according to any of the preceding claims 3 to 6, comprising the following steps:

applying a first voltage (VDD1) at the first voltage input (IN1) and/or a second voltage (VDD2) at the second voltage input (IN2),

if said first voltage (VDD1) is higher than said second voltage (VDD2), the voltage at the output (3) of the comparator (CMP) takes care that said first voltage input (IN1) is connected to the selection circuit output (O) by means of the first controllable switch (SW1), and

if said first voltage (VDD1) is lower than said second voltage (VDD2), the voltage at the output (6) of the inverter (INV) takes care that said second voltage input (IN2) is connected to said selection circuit output (O) by means of the second controllable switch (SW2).

9. Method according to claim 8, wherein

if the first voltage (VDD1) or the second voltage (VDD2) is lower than a minimum voltage (V_t), either

the pull down element (PD1) pulls the output (3) of the comparator (CMP) down and the first voltage input (IN1) is connected to the selection circuit output (O) by means of the first controllable switch (SW1), or

the further pull down element (PD2) pulls the output (6) of the inverter (INV) down and the second voltage input (IN2) is

15

connected to said selection circuit output (O) by means of the second controllable switch (SW2).

FIG 1

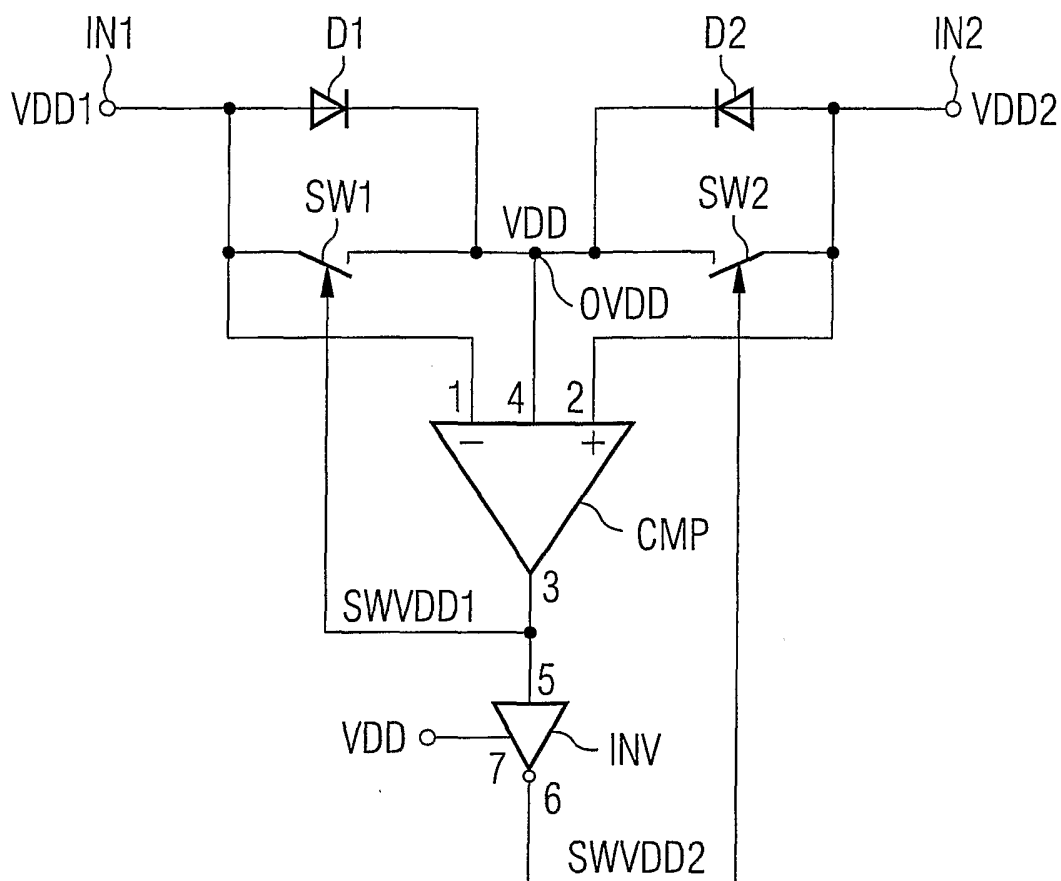


FIG 2

