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(71) **Applicant (for all designated States except US):** **KAGUTECH LTD.** [US/US]; 6425 Rockbluff Circle, Plano, Texas 75024 (US).

(72) **Inventors; and**

(75) **Inventors/Applicants (for US only):** **GUTTAG, Karl** [US/US]; 6425 Rockbluff Circle, Plano, Texas 75024 (US). **GUTTAG, Alvin** [US/US]; 415 Russell Avenue #108, Gaithersburg, Maryland 20877 (US).

(74) **Agent:** **JAGTIANI, Ajay**; 10363-A Democracy Lane, Fairfax, Virginia 22030 (US).

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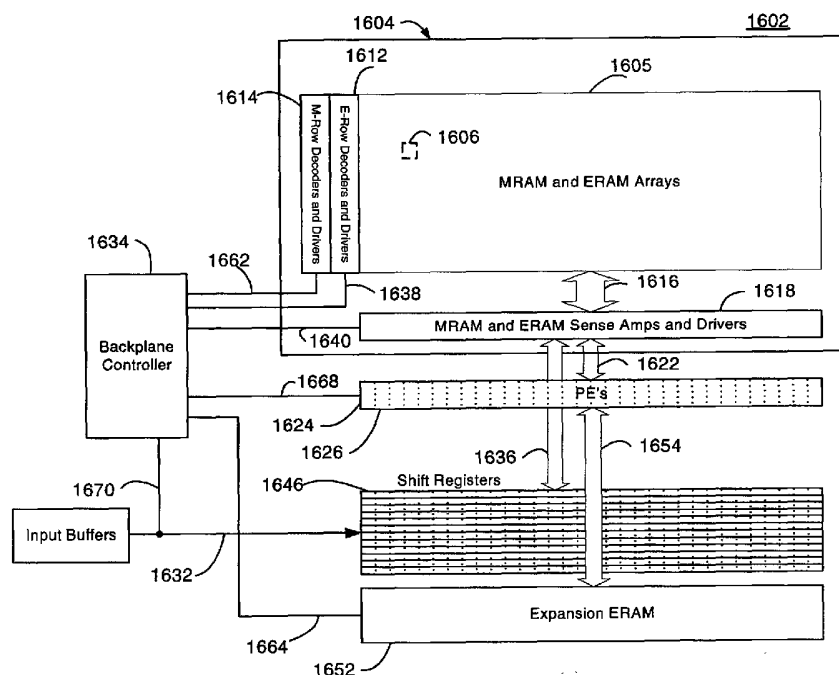
Declarations under Rule 4.17:
— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ,

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[Continued on next page]

(54) Title: DIGITAL BACKPLANE



(57) Abstract: The present invention provides a digital backplane and various methods, systems and devices for controlling a digital backplane and light modulating elements (Figure 16). In some embodiments of the present invention, a recursive feedback method is used to control a digital backplane and/or spatial light modulators.

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- CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)
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INTERNATIONAL SEARCH REPORT

International application No.

PCT/US04/15877

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G09G 03/36

US CL : 345/87,467,100,542, 364/413,372/92,359/141,166,382/54,399/74,49,348/614,455/52.3,340/635

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 345/87,467,100,542, 364/413,372/92,359/141,166,382/54,399/74,49,348/614,455/52.3,340/635

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,585,816 (Schaffer et al.) 17 December 1996 (17.12.1996) Col. 3, Lines 43-67, Col. 5, Line 42 to Col. 6, Line 67, Col. 10, Line 1 to col. 11, Line 43	1-15, 30-159
Y	6,542,142 B2 (Yumoto et al.) 1 April 2003 (01.04.2003) Col. 3, Line 39 to Col. 4, Line 9, Col. 5, Line 19-32, Col. 10, Line 61 to Col. 12, Line 9, Col. 12, Lines 49-63, Col. 13, Line 55 to Col. 15, Line 2, Col. 17, Line 53 to Col. 18, Line 51, Col. 18, Line 66 to col. 19, Line 9, Col. 25, line 31-37, Col. 26, Line 54 to Col. 27, Line 3, Col. 34, Lines 20-60, Col. 39, Lines 4-48, Col. 41, Lines 37-50	1-30
Y	US 4,847,854 (Van Dijk) 11 July 1989 (11.07.1989) Col. 4, Lines 4-6, Col. 14, lines 51-56, Col. 15, Lines 13-68, Col. 16, lines 17-60, Col. 2, lines 10-15, Col. 17, Lines 10-41, Col. 28, Lines 8-13, Col. 5, Lines 4-18, Col. 27, Lines 20-25	1-15,90-100
Y	US 20022039800 (Kang S. G.) 30 May 2002 (30.05.2002) page 2 detailed description.	15, 30-38, 47-84
Y	US 4,364,093 (Holmes) 14 December 1982 (14.12.1982) Col. 3, Lines 29 -67, Col. 4, Line 26 to Col. 5, Line 54	16-38,152-168
Y	US 5,920,322 (Ulichney) 6 July 1999 (6.07.1999), Col. 6, Lines 15-67, Col. 8, line 39 to Col. 12, Line 28	16-84



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	"&" document member of the same patent family

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Facsimile No. (703) 305-3230

Authorized officer

Prabodh Dharia

Telephone No. 571-272-7668

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C. (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,581,272 (Conner et al.) 03 December 1996 (03.12.1996) Col. 3, Line 3 to Col. 6, Line 33, Col. 8, Lines 11-37	46-88
Y	US 4,742,552 (Andrews) 05 May 1988 (05.05.1988) Col. 29, Line 27 to Col. 36, Line 10, Col. 27, Line 3 to Col. 29, Line 25	65-100
Y	US 6,107,979 (Chiu et al.) 22 August 2000 (22.08.2000) Col. 6, Line 29 to Col. 8, Line 67, Col. 10, Lines 14-58, Col. 11, Line 31 to Col. 15, Line 13	89,126-130,142-151
Y	US 6,118,500 (Kunzman) 12 September 2000 (12.09.2000) Col. 4, Line 55 to Col. 7, Line 54, Col. 8, Line 21 to Col. 10, Line 2	101-119
Y	US 6,023,263 (Wood) 08 February 2000 (08.02.2000) Col. 5, Line 3 to Col. 8, Line 9	101-119,142-151,160-168
Y	US 20010043177 A1 (Huston et al.) 22 November 2001 (22.11.2001) page 3, paragraphs 24-31, 33-34, Pge 4, paragraphs 34-40, page 5, paragraphs 81 to page 7, paragrph 102, page 8, paragraph 113 to page 10, paragarph 137, page 10, paragraph 141 to page 12, paragraph 161, page 17, paragraphs 257-263, page 18, paragraph263 to page 19, paragraph 285	101-151
Y	US 5,576,873 (Crossland et al.) 19 November 1996 (19.11.1996) Col. 4, Line 17 to Col. 6, Line 42, Col. 8, Line35 to Col. 10, Line 2, Col. 15, Lines 3 to Col. 16, Line 10	120-125
Y	US 6,046,719 (Dingwall) 04 April 2000 (04.04.2000) Col. 5, Line 18 to Col./ 6, Line 15, Col. 11, Line 49 to Col. 12, Line 11, Col. 12, Line 40 to Col. Col. 14, Line 27	126-130
Y	US 6,061,049 (Petitt et al.) 09 May 2000 (09.05.2000) Col. 2, Lines 1-14, Col. 1, Linesa 46-60, Col. 6, Line 19 to Col. 7, Line 50	126-130
Y	US 6,762,873 B1 (Coker et al.) 29 June 2000 (29.06.2000) Col. 3, Line 64 to Col. 5, Line 26, Col. 11, Line 14 to Col. 13, Line 55, Col. 23, Line 29 to Col. 24, Line 8	131-151
Y	US 5,771,060 (Nelson) 23 June 1998 (23.06.1998) Col. 6, Line 31 to Col. 8, Line 25	152-168
Y	US 6,717,222 (Zhang) 10 April 2003 (10.04.2003) Col. 10, Line 65 to Col. 11, Line 51	160-168
Y	US 6,329,987 B1 (Gottfried et al.) 11 December 2001 (11.12.2001) Col. 12, Line 34 to col. 13, Line 12, Col. 14, Lines 49-67	160-168
Y	US 6,809,734 B2 (Suzuoki et al.) 26 September 2002 (26.09.2002) Col. 15, Line 34 to Col. 18, Line 24	160-168

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Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
Please See Continuation Sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐
☐

The additional search fees were accompanied by the applicant's protest.

No protest accompanied the payment of additional search fees.

BOX III. OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

- I. Claims 1-15 are drawn to display driving by controlling light modulating element.
- II. Claims 16-29, 142, 143 are drawn to display, with series of stages each having stage value corresponding to pixel value of light modulating element.
- III. Claims 30-38 are drawn to display with storage bits corresponding to pixel value of light modulating element and mask write operation as updating means which also performs setting and resetting.
- IV. Claims 39-47 are drawn to display with two series of count steps LS count steps and MS count steps setting or clearing output bits to set pixel values for array of light modulating element.
- V. Claims 48-67 are drawn to display with logical bit serial operation such as arithmetic.
- VI. Claims 68-89 are drawn to two dimensional light array of light modulating element with means for computing a one dimensional array of control signals for output bits based on one or more sets one bit positions of pixel value.
- VII. Claims 90-125 are drawn to method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator.
- VIII. Claims 126-130 are drawn to digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element.
- IX. Claims 131-141 are drawn to array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements.
- X. Claims 144-157 are drawn to a spatial light modulator comprising an array of master slave bit pair stored in MRAM.
- XI. Claims 158-160 are drawn to Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.
- XII. Claims 161-168 are drawn to MRAM array storage bits arranged in MRAM columns.

The inventions are distinct, from each other listed in Groups I-XII and do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2 they lack the same or corresponding special technical features for the following reasons:

Invention I relates a display unit driving by controlling light modulating element; however, it does not relate to display with logical bit serial operation such as arithmetic, spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference or series of stages each having stage value corresponding to pixel value or providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM.

Invention II relates series of stages each having stage value corresponding to pixel value or providing memory on a spatial light modulator; however, it does not relate to display with logical bit serial operation such as arithmetic, reallocating available memory for

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data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.

Invention III relates to display with storage bits corresponding to pixel value of light modulating element and mask write operation as updating means which also performs setting however, it does not relate to stage value corresponding to pixel value or providing memory on a spatial light modulator; reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.

Invention IV relates to display with two series of count steps LS count steps and MS count steps setting or clearing output bits to set pixel values for array of light modulating element, however, it does not relate to display unit driving by controlling light modulating element; stage value corresponding to pixel value or providing memory on a spatial light modulator; reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.

Invention V relates to display with logical bit serial operation such as arithmetic, however, it does not relate to display unit driving by controlling light modulating element; stage value corresponding to pixel value or providing memory on a spatial light modulator; reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.

Invention VI relates to two dimensional light array of light modulating element with means for computing a one dimensional array of control signals for output bits based on one or more sets one bit positions of pixel value, however, it does not relate to display with logical bit serial operation such as arithmetic, spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference or series of stages each having stage value corresponding to pixel value or providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM.

Invention VII relates to method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator, however, it does not relate to digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements.

Invention VIII relates to digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, however, it does not relate to method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator, array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, a spatial light modulator comprising an array of master slave bit pair stored in MRAM, or two dimensional light array of light modulating element with means for computing a one dimensional array of control signals for output bits based on one or more sets one bit positions of pixel value.

Invention IX relates to array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, however, it does not relate to Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference, a spatial light modulator comprising an array of master slave bit pair stored in MRAM, or MRAM array storage bits arranged in MRAM columns.

Invention X relates to a spatial light modulator comprising an array of master slave bit pair stored in MRAM, however, it does not relate to display with logical bit serial operation such as arithmetic, digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator or display with two series of count steps LS count steps and MS count steps setting or clearing output bits to set pixel values for array of light modulating element.

Invention XI relates to Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference, however, it does not relate to display with logical bit serial operation such as arithmetic, digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator, display with two series of count steps LS count steps and MS count steps setting or clearing output bits to set pixel values for array of light modulating element or MRAM array storage bits arranged in MRAM columns; series of stages each having stage value corresponding to pixel value or providing memory on a spatial light modulator.

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Invention XII relates to MRAM array storage bits arranged in MRAM columns, however, it does not relate to a display unit driving by controlling light modulating element; Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference, a spatial light modulator comprising an array of master slave bit pair stored in MRAM, array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator; two dimensional light array of light modulating element with means for computing a one dimensional array of control signals for output bits based on one or more sets one bit positions of pixel value.