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(54) **METHOD OF SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE MODULE**

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See application file for complete search history.

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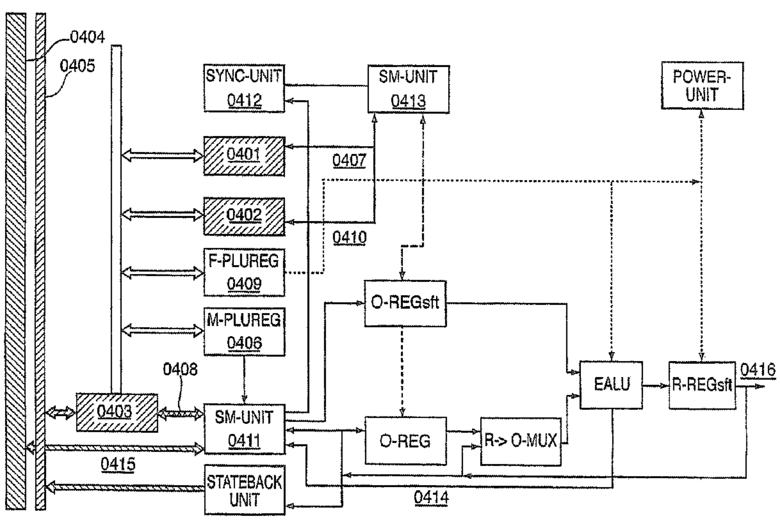
(57) **ABSTRACT**

A method of synchronizing and reconfiguring configurable elements in a programmable unit is provided. A unit has a two- or multi-dimensional, programmable cell architecture (e.g., DFP, DPGA, etc.), and any configurable element can have access to a configuration register and a status register of the other configurable elements via an interconnection architecture and can thus have an active influence on their function and operation. By making synchronization the responsibility of each element, more synchronization tasks can be performed at the same time because independent elements no longer interfere with each other in accessing a central synchronization instance.

121 Claims, 11 Drawing Sheets



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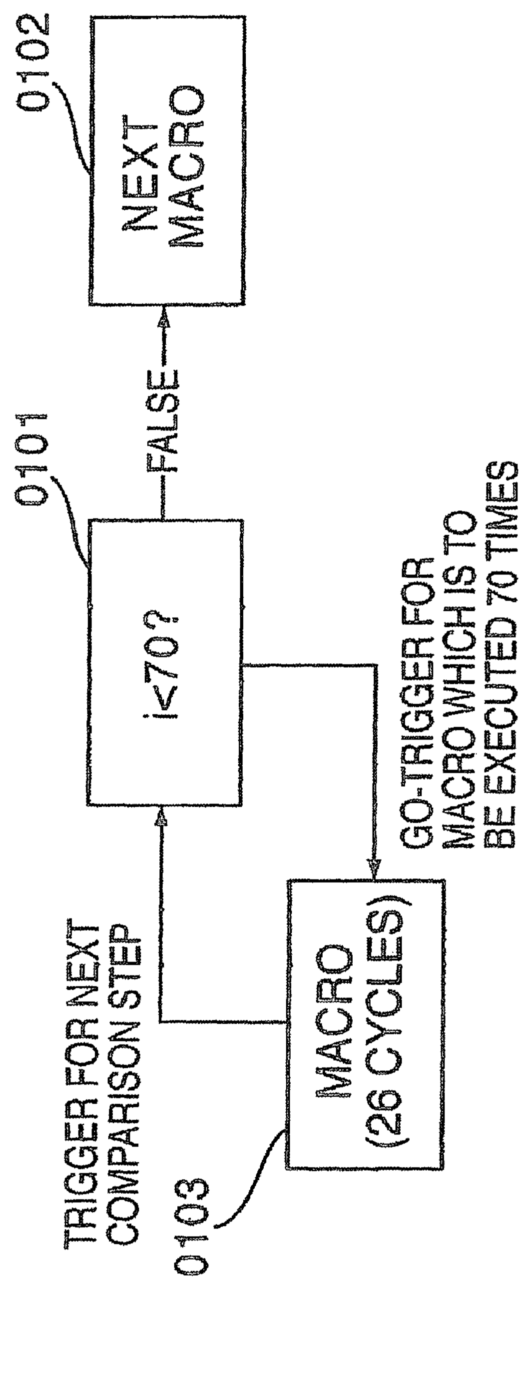

0102
NEXT MACRO
0101
FALSE
i<70?
GO-TRIGGER FOR MACRO WHICH IS TO BE EXECUTED 70 TIMES
TRIGGER FOR NEXT COMPARISON STEP
MACRO (26 CYCLES)
0103

FIG. 1

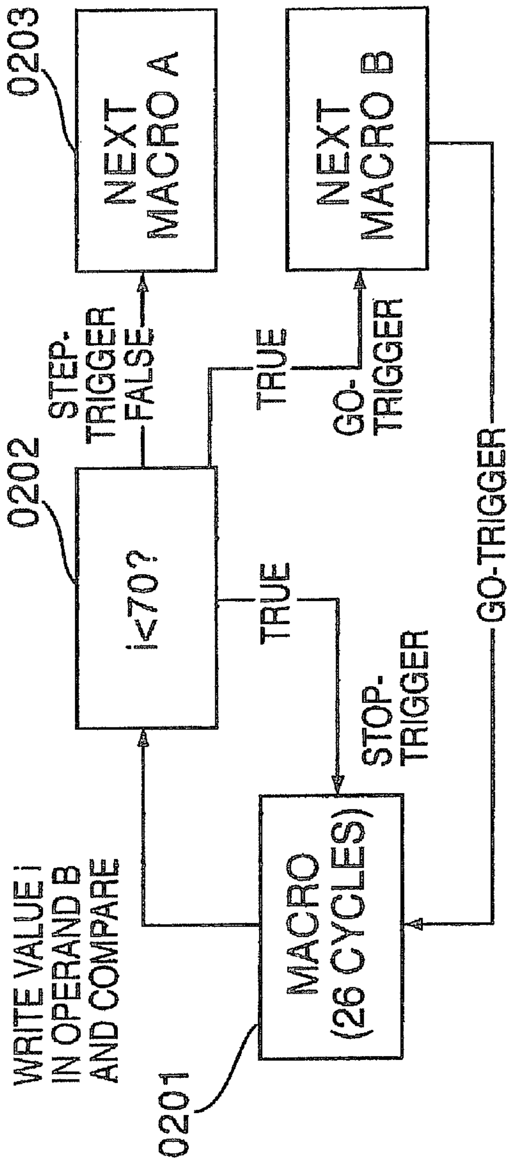
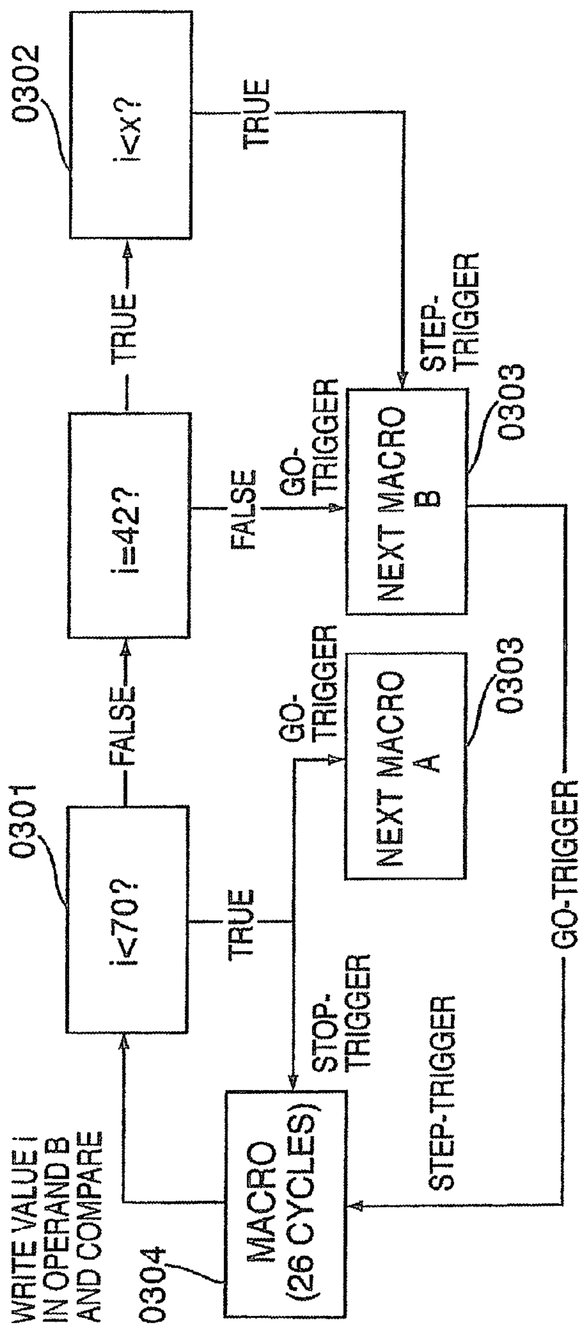

0201
MACRO
(26 CYCLES)
WRITE VALUE i
IN OPERAND B
AND COMPARE
0202
i<70?
TRUE
STOP-
TRIGGER
STEP-
TRIGGER
FALSE
TRUE
GO-
TRIGGER
0203
NEXT
MACRO A
NEXT
MACRO B
GO-TRIGGER

FIG. 2



0302
i<x?
TRUE
TRUE
STEP-TRIGGER
i=42?
FALSE
GO-TRIGGER
NEXT MACRO B
0303
FALSE
0301
i<70?
TRUE
GO-TRIGGER
NEXT MACRO A
0303
GO-TRIGGER
STOP-TRIGGER
STEP-TRIGGER
WRITE VALUE i IN OPERAND B AND COMPARE
0304
MACRO (26 CYCLES)

FIG. 3

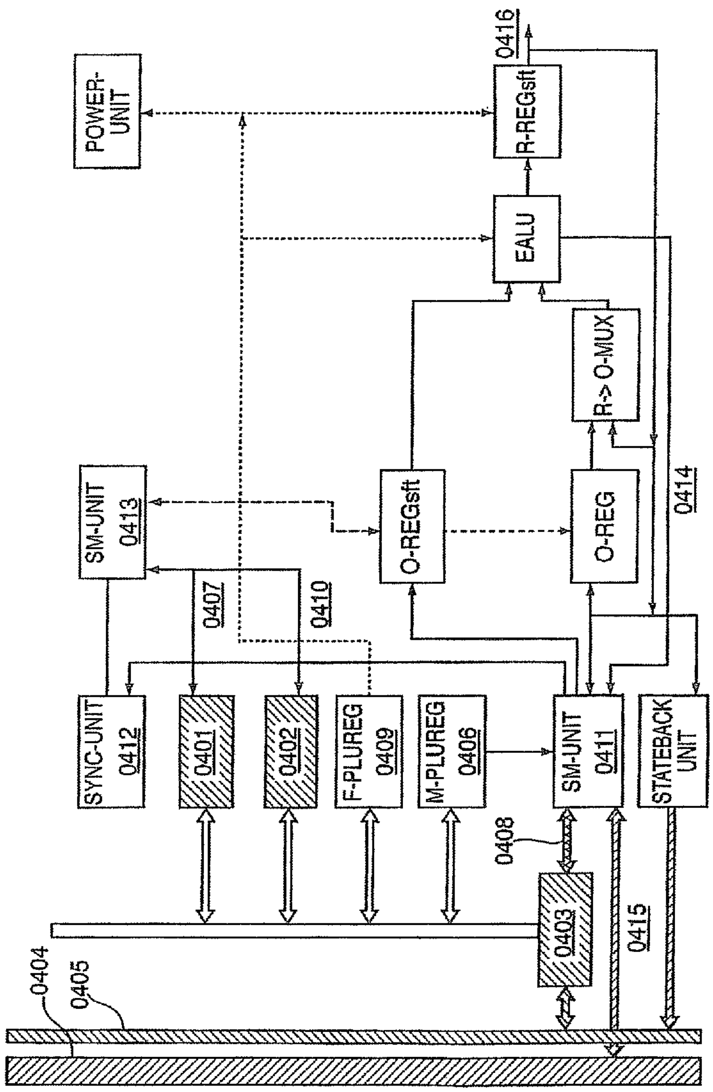

POWER-UNIT
R-REGsft
0416
EALU
R-> O-MUX
SM-UNIT
0413
O-REGsft
O-REG
0414
0407
0410
SYNC-UNIT
0412
0401
0402
F-PLUREG
0409
M-PLUREG
0406
SM-UNIT
0411
STATEBACK UNIT
0408
0403
0415
0404
0405

FIG. 4

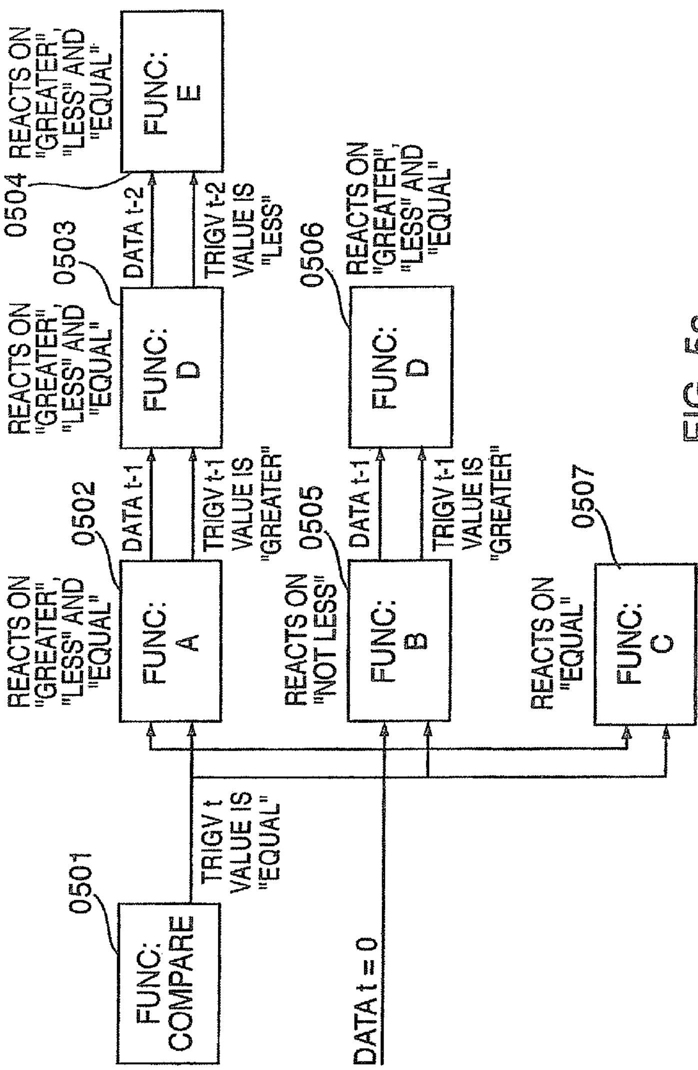

0501
FUNC: COMPARE
TRIGV t VALUE IS "EQUAL"
DATA t = 0
0502
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: A
DATA t-1
TRIGV t-1 VALUE IS "GREATER"
0503
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: D
DATA t-2
TRIGV t-2 VALUE IS "LESS"
0504
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: E
0505
REACTS ON "NOT LESS"
FUNC: B
DATA t-1
TRIGV t-1 VALUE IS "GREATER"
0506
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: D
0507
REACTS ON "EQUAL"
FUNC: C

FIG. 5a

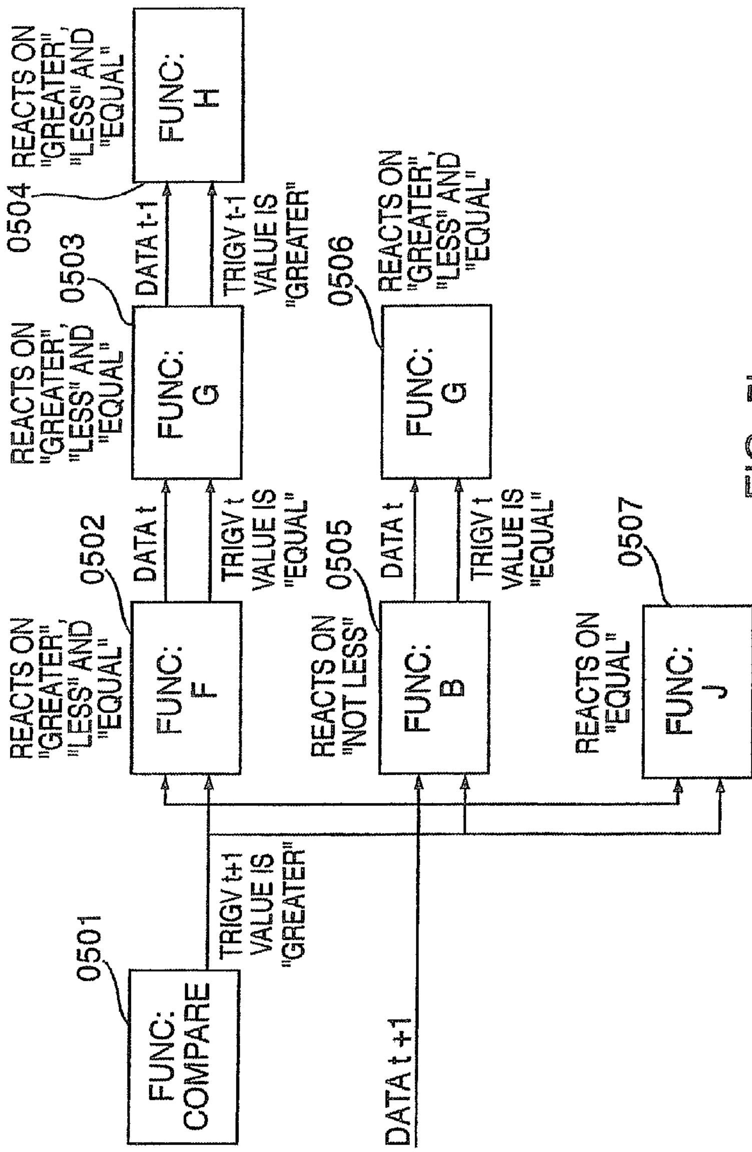

0501
FUNC: COMPARE
TRIGV t+1 VALUE IS "GREATER"
DATA t +1
REACTS ON "GREATER", "LESS" AND "EQUAL"
0502
FUNC: F
DATA t
TRIGV t VALUE IS "EQUAL"
REACTS ON "GREATER", "LESS" AND "EQUAL"
0503
FUNC: G
DATA t-1
TRIGV t-1 VALUE IS "GREATER"
0504
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: H
REACTS ON "NOT LESS"
0505
FUNC: B
DATA t
TRIGV t VALUE IS "EQUAL"
0506
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: G
REACTS ON "EQUAL"
0507
FUNC: J

FIG. 5b

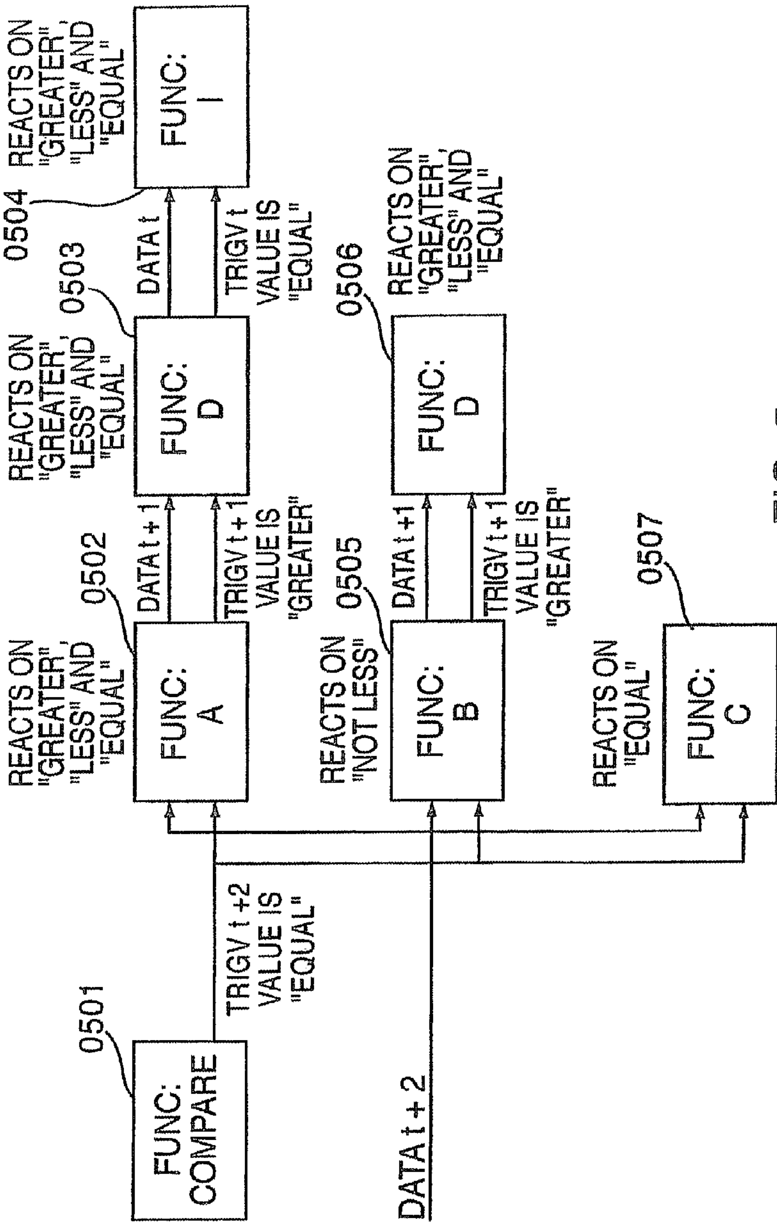
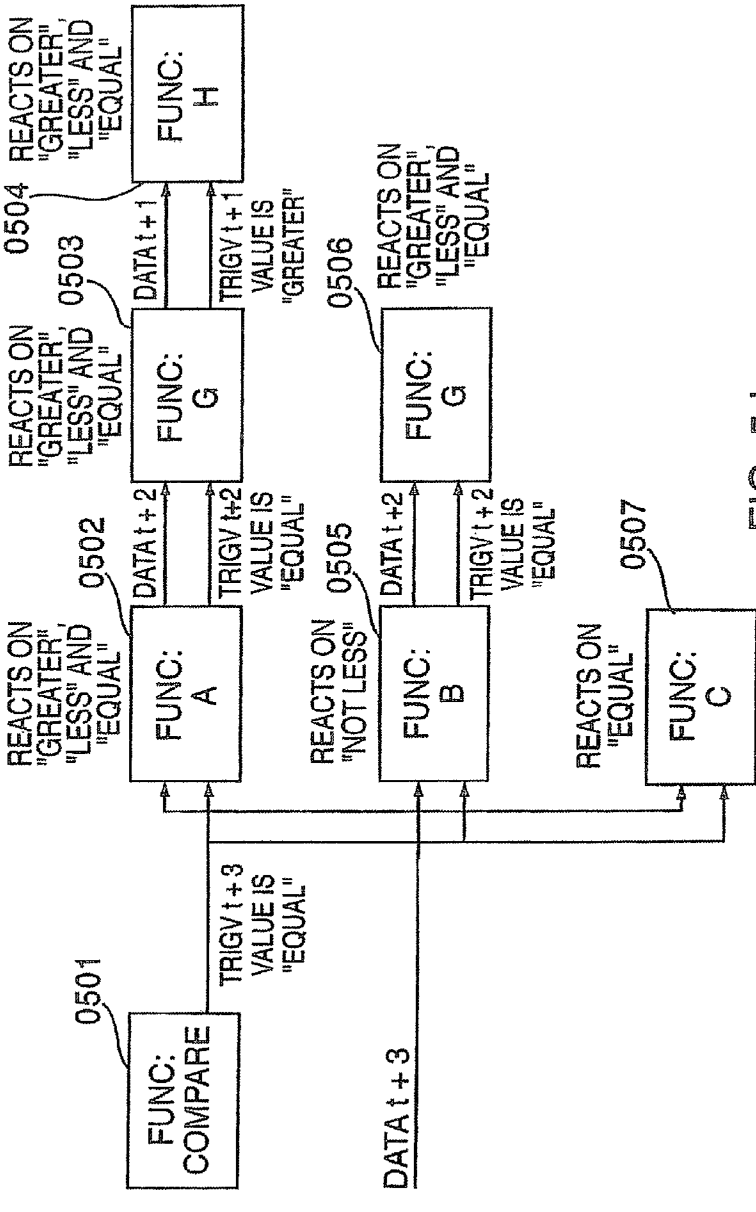

0501
FUNC: COMPARE
TRIGV t +2 VALUE IS "EQUAL"
DATA t + 2
0502
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: A
DATA t + 1
TRIGV t + 1 VALUE IS "GREATER"
0503
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: D
DATA t
TRIGV t VALUE IS "EQUAL"
0504
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: I
0505
REACTS ON "NOT LESS"
FUNC: B
DATA t + 1
TRIGV t + 1 VALUE IS "GREATER"
0506
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: D
0507
REACTS ON "EQUAL"
FUNC: C

FIG. 5C



FUNC: COMPARE
0501
TRIGV t + 3 VALUE IS "EQUAL"
DATA t + 3
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: A
0502
DATA t + 2
TRIGV t+2 VALUE IS "EQUAL"
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: G
0503
DATA t + 1
TRIGV t + 1 VALUE IS "GREATER"
0504
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: H
REACTS ON "NOT LESS"
FUNC: B
0505
DATA t + 2
TRIGV t + 2 VALUE IS "EQUAL"
0506
REACTS ON "GREATER", "LESS" AND "EQUAL"
FUNC: G
REACTS ON "EQUAL"
FUNC: C
0507

FIG. 5d

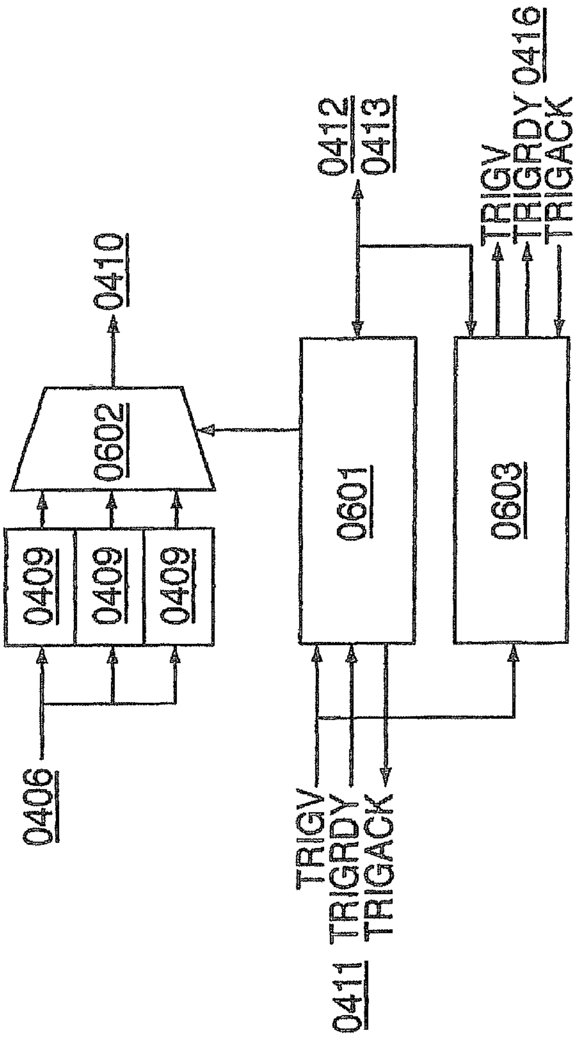

0406
0409
0409
0409
0602
0410
0601
0603
0412
0413
TRIGV
TRIGRDY
TRIGACK
0416
TRIGV
TRIGRDY
TRIGACK
0411

FIG. 6

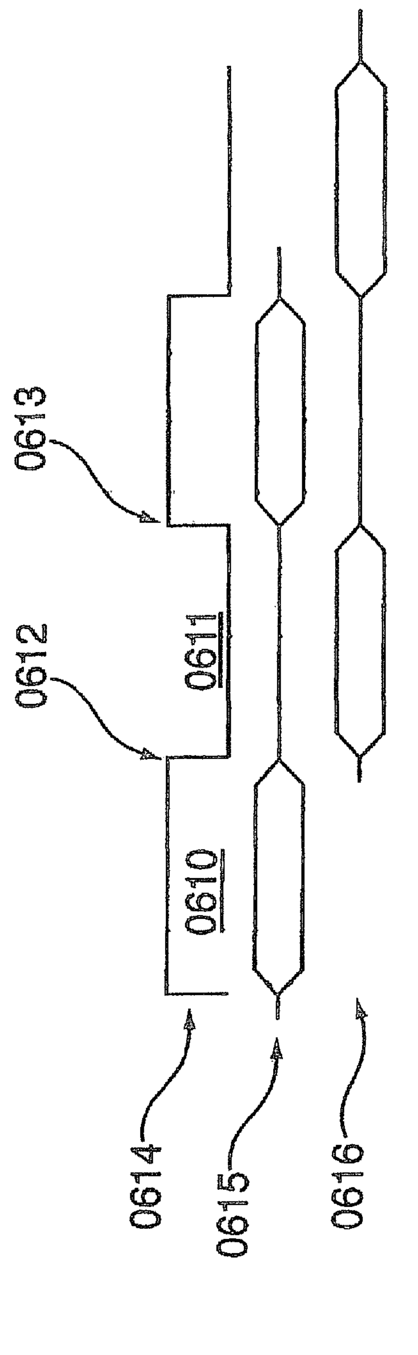


FIG. 6a

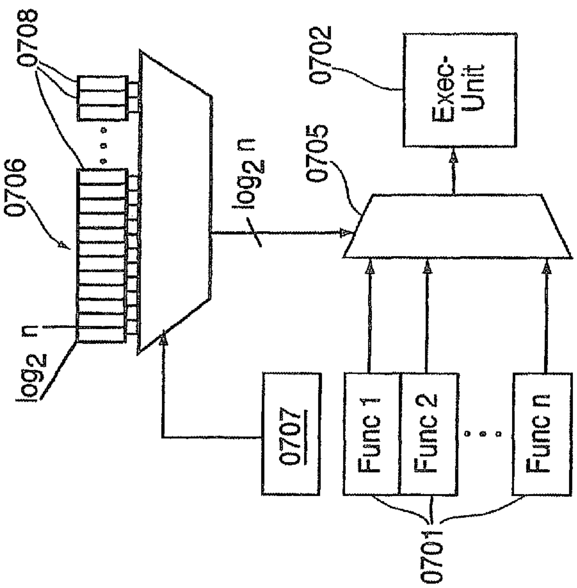


FIG. 7b

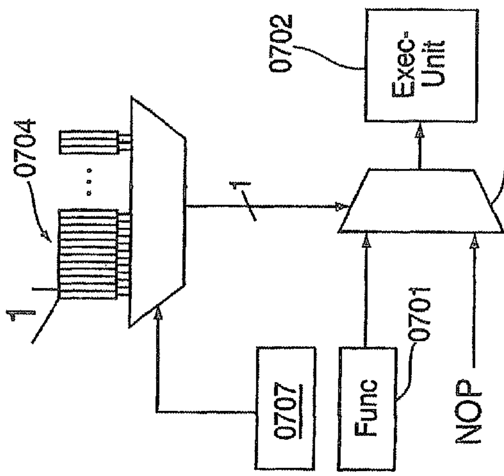


FIG. 7a
PRIOR ART

METHOD OF SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE MODULE

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

CROSS-REFERENCE TO RELATED APPLICATION

This application is a *divisional reissue of U.S. Reissue patent application Ser. No. 12/109,280, filed on Apr. 24, 2008, which is a reissue application of U.S. patent application Ser. No. 10/379,403, filed on Mar. 4, 2003, now U.S. Pat. No. 7,036,036, which is a* continuation of U.S. patent application Ser. No. 09/369,653, filed Aug. 6, 1999, now U.S. Pat. No. 6,542,998*,* which is a continuation-in-part of PCT/DE98/00334, filed on Feb. 7, 1998, and *is a continuation-in-part* of U.S. patent application Ser. No. 08/946,812*,* filed on Oct. 8, 1997, now U.S. Pat. No. 6,081,903*,* and claims the benefit of the priority [date] *dates* of these cases under 35 U.S.C. §120, each of which is expressly incorporated herein by reference in its entirety. This application also claims the benefit*, under 35 U.S.C. §119,* of the priority date of *German Application No.* DE 19704728.9, filed on Feb. 8, 1997[, under 35 U.S.C. §119], which is expressly incorporated herein by reference in its entirety. *Further, more than one reissue application of U.S. Pat. No. 7,036,036 has been filed. Specifically, the reissue applications are application Ser. No. 12/109,280, application Ser. No. 12/909,061, application Ser. No. 12/909,150, and application Ser. No. 12/909,203, the latter three of which were all filed on Oct. 21, 2010 as divisional reissue applications of application Ser. No. 12/109,280.*

BACKGROUND INFORMATION

Synchronization of configurable elements of today's modules, e.g., field programmable gate arrays ("FPGAs"), dynamically programmable gate arrays ("DPGAs"), etc., is usually accomplished using the clock of the module. This type of time-controlled synchronization poses many problems because it is often not known in advance how much time is needed for a task until a final result is available. Another problem with time-controlled synchronization is that the event on which the synchronization is based is not triggered by the element to be synchronized itself but rather by an independent element. In this case, two different elements are involved in the synchronization. This leads to a considerably higher administrative complexity.

European Patent No. 0 726 532 describes a method of controlling data flow in SIMD machines composed of several processors arranged as an array. An instruction is sent to all processors which dynamically selects the target processor of a data transfer. The instruction is sent by a higher-level instance to all processors (broadcast instruction) and includes a destination field and a target field. The destination field controls a unit in the processor element to dynamically determine the neighboring processor element to which the result is to be sent. The operand register of another processor element in which another result is to be stored is dynamically selected with the target field.

SUMMARY

The present invention relates to a method which permits self-synchronization of elements to be synchronized. Synchronization is neither implemented nor managed by a central entity. By shifting synchronization into each element, more synchronization tasks can also be performed simultaneously, because independent elements no longer interfere with one another when accessing the central synchronization entity.

In accordance with an example embodiment of the present invention, in a module, e.g., a data flow processor ("DFP") or a DPGA, with a two- or multi-dimensionally arranged programmable cell structure, each configurable element can access the configuration and status register of other configurable elements over an interconnecting structure and thus can have an active influence on their function and operation. A matrix of such cells is referred to below as a processing array (PA). The configuration can thus be accomplished by a load logic from the PA in addition to the usual method.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows how a loop construct can be implemented by using triggers, in accordance with an example embodiment of the present invention.

FIG. **2** shows how a comparison construct can be implemented by using multiple triggers, according to an example embodiment of the present invention.

FIG. **3** shows how a comparison construct with multiple outputs can be implemented by using multiple triggers and interleaving them, according to an example embodiment of the present invention.

FIG. **4** shows the required expansions, according to an example embodiment of the present invention, in comparison with conventional FPGAs and DFPs.

FIGS. **5**a-**5**d show an example of the selection of different functions of the configurable elements by triggers, according to the present invention.

FIGS. **6** and **6**a show an implementation of multiple configuration registers controlled by triggers for executing different functions, according to an example embodiment of the present invention.

FIGS. **7**a and **7**b shows an implementation of the method from FIG. **6** in microprocessors, according to an example embodiment of the present invention.

DETAILED DESCRIPTION

The present invention provides a module which is freely programmable during the running time and can also be reconfigured during the running time. Configurable elements on the chip have one or more configuration registers for different functions. Both read and write access to these configuration registers is permitted. In the method described here, it is assumed that a configuration can be set in an element to be configured for the following information.

- Interconnection register. In this register, the type of connection to other cells is set.
- Command register. The function of the configurable element to be executed is entered in this register.
- Status register. The cell stores its instantaneous status in this register. This status provides other elements of the module with information regarding which processing cycle the cell is in.

A cell is configured by a command which determines the function of the cell to be executed. In addition, configuration data is entered to set the interconnection with other cells and the contents of the status register. After this operation, the cell is ready for operation.

To permit flexible and dynamic cooperation of many cells, each cell can have read or write access to all the configuration registers of another cell. Which of the many configuration registers is accessed by reading or writing is specified by the type of command with which the cell has been configured. Each command that can be executed by the cell exists in as many different types of addressing as there are different independent configuration registers in an element to be configured.

Example: A cell has the configuration register described above (interconnection, command and status) and is to execute the command ADD which performs an addition. It is then possible to select through the various types of ADD command where the result of this function is to be transferred.

ADD-A. The result is transferred to operand register A of the target cell.

ADD-B. The result is transferred to operand register B of the target cell.

ADD-V. The result is transferred to the interconnecting register of the target cell.

ADD-S. The result is transferred to the status register of the target cell.

ADD-C. The result is transferred to the command register of the target cell.

Control and Synchronization Trigger: In addition to the result, each cell can generate a quantity of trigger signals. The trigger signals need not necessarily be transferred to the same target cell as the result of processing the configured command. One trigger signal or a combination of multiple trigger signals triggers a certain action in the target cell or puts the cell in a certain state. A description of the states is also to be found in the text below. The following are examples of trigger signals:

GO trigger. The GO trigger puts the target cell in the READY state.

RECONFIG trigger. The RECONFIG trigger puts the target cell in the RECONFIG state, so the cell can be reprogrammed. This trigger is very useful, especially in conjunction with switching tables. If it is assumed that the data to be processed is loaded into the operand register at the rising edge of the clock pulse, processed in the period of the H level and written to the output register at the trailing edge, then the cell can be reconfigured at the trailing edge. The new configuration data is written to the command register at the trailing edge. The period of the L level is sufficient to conclude the reconfiguration successfully.

STEP trigger. The STEP trigger initiates unique execution of the configured command in the target cell in the WAIT state.

STOP trigger. The STOP trigger stops the target cell by putting the cell in the STOP state.

Due to the possibility of indicating in the processing cell into which register of the target cell the result is to be entered and which type of trigger signal is to be generated, a quantity of management data can be generated from a data stream. This management data is not a result of the actual task to be processed by the chip, but instead it serves only the functions of management, synchronization, optimization, etc. of the internal state.

Each cell can assume the following states which are represented by suitable coding in the status register, for example:

READY. The cell is configured with a valid command and can process data. Processing takes place with each clock cycle. The data is entered into the register of the target cell on the basis of the type of addressing of the cell sending the data.

WAIT. The cell has been configured with a valid command and can process data. Processing takes place on the basis of a trigger signal which can be generated by other elements of the module. The data is entered into the register of the target cell on the basis of the type of addressing of the cell sending the data.

CONFIG. This cell is not configured with a valid command. The data package sent to the cell with the next clock cycle is entered into the command register. The data package is entered into the command register in any case, regardless of which type of addressing was used by the cell sending the data.

CONFIG-WAIT. This cell is not configured with a valid command. A data package is entered with the next trigger signal which can be generated by other elements of the module and is written to the command register. The data package is entered into the command register in any case, regardless of which type of addressing was used by the cell sending the data.

RECONFIG. The cell is configured with a valid command, but it does not process any additional data, nor does it accept data. The cell can be reconfigured by another element of the module.

STOP. The cell is configured with a valid command, but it is not processing any data at the moment. The data is accepted by the cell (transferred to the input register) but is not processed further.

Due to these various states and the possibility of read and write access to the various registers of a cell, each cell can assume an active administrative role. In contrast with that, all existing modules of this type have a central management entity which must always know and handle the entire state of the module.

To achieve greater flexibility, there is another class of commands which change types after the first execution. Based on the example of the ADD command, a command is then as follows:

ADD-C-A. The result of the ADD function is written to the command register of the target cell with the first execution of the command. With each additional execution, the result is written to operand register A.

This possibility can be expanded as desired, so that even commands of the type ADD-C-V-A-C- . . . -B are conceivable. Each command can assume all permutated combinations of the various types of addressing and triggers.

Reconfiguration Control by RECONFIG Trigger: In the previous method, each element to be configured received a RECONFIG trigger from an external entity to enter the “reconfigurable” state. This, had the disadvantage that distribution of the RECONFIG trigger necessitated a considerable interconnection and configuration expense: Due to the structure of the interconnection, this disadvantage can be eliminated. All configurable elements which are related by the interconnecting information represent a directional graph. Such a graph may have multiple roots (sources) and multiple leaves (targets). The configurable elements are expanded so that they propagate an incoming RECONFIG trigger in the direction of either their outgoing registers, their ingoing registers or a combination thereof. Due to this propagation, all the configurable elements that are directly connected to the configurable element also receive the RECONFIG trigger.

A configuration (graph) can be brought completely into the “reconfigurable” state by sending a RECONFIG trigger to all the roots and propagating the RECONFIG trigger in the direction of the output registers. The quantity of roots in a graph to which a RECONFIG trigger must be sent is considerably smaller than the total quantity of nodes in the graph.

This greatly minimizes the complexity. Of course, a RECONFIG trigger may also be sent to all leaves. In this case, the RECONFIG trigger is propagated in the direction of the input registers.

Due to the use of both options or a combination of both methods, a minimum quantity of configurable elements to which a RECONFIG trigger must be sent can be calculated.

The configurable elements can receive an addition record to their status register, indicating whether or not an incoming RECONFIG trigger is to be propagated. This information is needed when two or more different graphs are connected at one or more points (i.e., they have a transition) and it is not desirable for one of the other graphs to enter the "reconfigurable" state. One or more configurable elements thus behave like a lock.

In addition, the status register can be expanded so that an additional entry indicates the direction in which an incoming RECONFIG trigger is to be relayed.

The method described here can be applied to all types of triggers and/or data. In this way, it is possible to establish an automatic distribution hierarchy needing very few access opportunities from the outside to set it in operation.

Implementation of Multiple Functions Simultaneously in the Same Configurable Elements

Basic Function and Required Triggers: An especially complex variant of calling up various macros by a condition is presented below: In execution of a condition (IF COMP THEN A ELSE B; where COMP is a comparison, and A and B are operations to be executed), no GO and STOP triggers are generated. Instead, a trigger vector (TRIGV) is generated, indicating to which result the comparison COMP has led. The trigger vector can therefore assume the states "equal," "greater" or "less."

The vector is sent to a following cell which selects exactly a certain configuration register (corresponding to A or B) from a plurality of configuration registers on the basis of the state of the vector. What this achieves is that, depending on the result of the preceding comparison, another function is performed over the data. States such as "greater-equal," "less-equal" and "equal-not equal" are triggered by writing the same configuration data to two configuration registers. For example, with "greater-equal" the configuration register "greater" and the configuration register "equal" are written with the same configuration word, while the configuration register "less" contains another configuration word.

In implementating trigger vectors TRIGV, no restriction to the states "greater," "less" and "equal" is necessary. To analyze large "CASE . . . OF" constructs, any number n representing the state of the CASE may be relayed as trigger vectors TRIGV-m to the downstream cell(s). In other words, n indicates the comparison within the CASE which was correct in analysis of the applied data. For implementation of the function assigned to the comparison within the CASE, n is relayed to the executing cells to select the corresponding function. Although the cells need at least three configuration registers in the "greater/less/equal" case, the number of configuration registers must correspond exactly to at least the maximum value of n (max (n)) when using TRIGV-m.

Propagation of the Required Function by Triggers: TRIGV/TRIGV-m are sent to the first cell processing the data. In this cell, TRIGV/TRIGV-M are analyzed and the data is processed accordingly. TRIGV/TRIGV-m are relayed (propagated) together with the data to the downstream cells. They are propagated to all cells executing a certain function on the basis of the analysis (IF or CASE). Propagation is linked directly to propagation of data packages, i.e., propagation is synchronous with the data. TRIGV/TRIGV-m generated at time t are linked to data present at time t at first processing cells CELLS1 (see FIG. **5**: **0502**, **0505**, **0507**). TRIG/TRIG-V are propagated so that the vectors are applied to the second processing cells with the data at time t+1, and at time t+2 they are applied to the third processing cells, etc., until TRIG/TRIG-V and the data are present at time t+m to the $(m-1)^{th}$ cells and at the same time to the last cells which depend on the comparison IF/CASE triggered by TRIG/TRIG-V.

A link is by no means such that the TRIG/TRIG-V generated at time t are linked to data applied to CELLS**1** at time t_{old}<t.

Reacting to the Presence or Absence of Triggers: In special cases, it is necessary to react to the absence of a trigger, i.e., a trigger state occurs, but no change in trigger vector is initiated. Appropriate and important information can also be transferred to the downstream cells in this case. For example, in a comparison of "greater," "less," "equal," the trigger signal "equal" is not present and does not change when switching from the state "less" to the state "greater." Nevertheless, the absence of "equal" does contain information, namely "not equal."

To be able to react to both states "present" and "not present," an entry in the configuration register of the cell is added, indicating which of the states is to be reacted to.

Furthermore, a signal TRIGRDY indicating the presence of a trigger is added to trigger vector TRIGV representing states "equal," "greater" and "less." This is necessary because the state "not present" on one of the vectors does not provide any more information regarding the presence of a trigger per se.

TRIGRDY can be used as a handshake protocol between the transmitting cell and the receiving cell by having the receiving cell generate a TRIGACK as soon as it has analyzed the trigger vectors. Only after arrival of TRIGACK does the transmitting cell cancel the trigger state.

On the basis of an entry into the configuration register, a determination is made as to whether to wait for receipt of a TRIGACK or whether the trigger channel is to proceed unsynchronized when a trigger vector is sent out.

Use in Microprocessors

In microprocessors of the most recent architecture, conditional jumps are no longer executed by the known method of branch prediction, i.e., prediction of a jump. Speculative prediction of jumps introduced to increase processor performance calculated jumps in advance on the basis of speculative algorithms and had to reload the entire processor pipeline if the calculations were faulty, which led to a considerable loss of power.

To eliminate these losses, the new predicate/NOP method was introduced. A status flag one bit wide is assigned to each command, indicating whether the command is to be executed—or not. There may be any desired quantity of status flags. Commands are assigned to status flags by a compiler during the translation of the code. The status flags are managed by comparison operations assigned to them at the time of execution and indicate the result of the respective comparison.

Depending on the state of a status flag assigned to a command, the command is then executed by the processor (if the status flag indicates "execute") or the command is not executed and is replaced by an NOP (if the status flag indicates "not execute"). NOP stands for "No OPERATION," which means that the processor does not execute any operation in this cycle. Therefore, the cycle is lost for meaningful operations.

Two options are proposed for optimizing the cycle loss:

Multiple Command Registers per Computer Unit: A modern microprocessor has several relatively independent processors.

According to the trigger principle presented here, the individual processors are each equipped with several command registers, with a command register of a processor of a microprocessor being synonymous with a configuration register according to conventional FPGA, DFP, etc. modules. The respective active command register is selected

a) on the basis of trigger vectors generated by other processors on the basis of comparisons,

b) on the basis of multibit status flags (hereinafter referred to as status vectors) allocated to compare commands according to today's related art method.

Revised VLIW Command Set: One special embodiment is possible through VLIW command sets. Thus, several possible commands depending on one comparison can be combined to give one command within one command word. A VLIW word of any width is subdivided into any desired quantity of commands (codes). Each individual one of these codes is referenced by a trigger vector or a status vector. This means that one of the existing codes is selected from the VLIW word and processed during the running time.

The table illustrates a possible VLIW word with four codes referenced by a 2-bit trigger vector or a 2-bit status flag:

VLIW Command Word:

Code 0	Code 1	Code 2	Code 3

Assignment:

Trigger Vector/Status Flag:

00	01	10	11

Expansion of Hardware in Comparison with Conventional FPGAs and DFPs.

Additional Registers: A status register and a configuration register are added to the configuration registers conventionally used in DFPs. Both registers are controlled by the PLU bus and have a connection to the state machine of the sequence control system of the respective cell.

Change in PLU Bus: The configurable registers M-/F-PLUREG in FPGAs and DFPs are managed exclusively over the PLU bus, which represents the connection to the load logic. To guarantee the function according to the present invention, an additional access option must be possible through the normal system bus between the cells. The same thing is true for the new status register and configuration register.

The only part of the system bus relevant for the registers is the part that is interconnected to the PAE over the BM UNIT, i.e., the interface between the system buses and the PAE. Therefore, the bus is relayed from the BM UNIT to the registers where upstream multiplexers or upstream gates are responsible for switching between the PLU bus and the system bus relevant for the PAE. The multiplexers or gates are switched so that they always switch the system bus relevant for the PAE through, except after resetting the module (RESET) or when the RECONFIG trigger is active.

Expansions of Configurable Elements (PAEs) with Respect to Conventional FPGAs and DFPs: Trigger Sources: A configurable element can receive triggers from several sources at the same time. Due to this possibility, flexible semantics of the triggers can be achieved with the help of masking registers.

Multiple Configuration Registers: Instead of one configuration register, a PAE has multiple (max(n)) configuration registers.

Configuration State Machine and Multiplexer: Downstream from the configuration registers is a multiplexer which selects one of the possible configurations.

The multiplexer is controlled by a separate state machine or a state machine integrated into the PAE state machine, controlling the multiplexer on the basis of incoming trigger vectors.

Trigger Analysis and Configuration: A configurable element may contain a masking register in which it is possible to set the trigger inputs to which a trigger signal must be applied, so that the conditions for an action of the configurable element are met. A configurable element reacts not only to a trigger, but also to a set combination of triggers. In addition, a configurable element can perform prioritization of simultaneously incoming triggers.

Incoming triggers are recognized on the basis of the TRIGRDY signal. The trigger vectors are analyzed here according to configuration data also present in the configuration registers.

Trigger Handshake: As soon as the trigger vectors have been analyzed, a TRIGACK is generated for confirmation of the trigger vector.

BM UNIT: The BM UNIT is expanded so that it relays triggers coming from the bus to the sync unit and SM unit according to the configuration in M-PLUREG. Triggers generated by the EALU (e.g., comparator values "greater," "less," "equal," 0 detectors, plus and minus signs, carryovers, error states (division by 0, etc.), etc.) are relayed from the BM UNIT to the bus according to the wiring information in M-PLUREG.

Expansions of System Bus: The system bus, i.e., the bus system between the cells (PAEs), is expanded so that information is transferred together with the data over the target register. This means that an address which selects the desired register on receipt of the data is also sent. Likewise, the system bus is expanded by the independent transfer of trigger vectors and trigger handshakes.

DETAILED DESCRIPTION OF DIAGRAMS AND EMBODIMENTS

FIG. **1** shows how a loop construct can be implemented by using triggers. In this example, a macro **0103** is to be executed 70 times. One execution of the macro takes 26 clock cycles. This means that counter **0101** may be decremented by one increment only once in every 26 clock cycles. One problem with freely programmable modules is that it is not always possible to guarantee that processing of macro **0103** will actually be concluded after 26 clock cycles. For example, a delay may occur due to the fact that a macro which is to supply the input data for macro **0103** may suddenly require 10 more clock cycles. For this reason, the cell in macro **0103** sends a trigger signal to counter **0101**, causing the result of the calculation to be sent to another macro. At the same time, processing of macro **0103** by the same cell is stopped. This cell "knows" exactly that the condition for termination of a calculation has been reached.

In this case the trigger signal sent is a STEP trigger, causing counter **0101** to execute its configured function once. The counter decrements its count by one and compares whether it has reached a value of 0. If this is not the case, a GO trigger is sent to macro **0103**. This GO trigger signal causes macro **0103** to resume its function.

This process is repeated until counter **0101** has reached a value of 0. In this case, a trigger signal is sent to macro **0102**, where it triggers a function.

A very fine synchronization can be achieved due to this interaction of triggers.

FIG. **2** shows how a comparison construct can be implemented by using multiple triggers. FIG. **2** corresponds to the basic idea of FIG. **1**. However, in this case the function in element **0202** is not a counter but a comparator. Macro **0201** also sends a comparison value to comparator **0202** after each processing run. Depending on the output of the comparison, different triggers are again driven to prompt an action in macros **0203**, for example. The construct implemented in FIG. **2** corresponds to that of an IF query in a programming language.

FIG. **3** shows how a comparison construct with multiple outputs can be implemented by using multiple triggers and interleaving them. Here, as in FIG. **2**, several comparators **0301**, **0302** are used here to implement construction of an IF-ELSE-ELSE construct (or multiple choice). Due to the use of a wide variety of types of triggers and connections of these triggers to macros **0303**, **0304**, very complex sequences can be implemented easily.

FIG. **4** shows an example of some of the differences between the present invention and, for example, conventional FPGAs, and DFPs. Additional configuration register **0401** and additional status register **0402** are connected to the SM UNIT over bus **0407**. Registers **0401**, **0402**, F-PLUREG and M-PLUREG are connected to a gate **0403** by an internal bus **0206**. Depending on position, this gate connects internal bus **0406** to PLU bus **0405** to permit configuration by the PLU or to the BM UNIT by a bus **0408**. Depending on the address on data bus **0404**, the BM UNIT relays the data to the O-REG or to addressed register **0401**, **0402**, F-PLUREG or M-PLUREG.

BM UNIT **0411** sends trigger signals over **0415** to SYNC UNIT **0412**. **0411** receives results from the EALU over **0414** ("equal," "greater," "less," "result=0" "result positive," "result negative," carry-over (positive and negative), etc.) to convert the results into trigger vectors. As an alternative, states generated by the SYNC UNIT or the STATE MACHINE can be relayed to the BM UNIT over **0415**.

The trigger signals transmitted by the BM UNIT to bus **0404** can be used there as STEP/STOP/GO triggers, RECONFIG triggers or for selecting a configuration register, depending on the configuration of the configurable elements to be analyzed. Which function a generated trigger will execute in the configurable elements to be analyzed is determined by interconnection **0404** and the configuration of the respective configurable element. One and the same trigger may have different functions with different configurable elements. **0416** is the result output of R-REGsft to bus system **0404** and the following configurable elements.

FIG. **5** shows the time response between generated triggers and the configuration registers selected by the triggers as an example. **0501** generates by comparison a trigger vector TRIGV, which can assume values "equal," "greater," or "less." Configurable elements **0502-0504** process data independently of comparison **0501**. Processing depends on comparison values "equal," "greater" and "less." Processing is pipelined, i.e., a data word is modified first by **0502**, then by **0503** and finally by **0504**. **0505** also processes data as a function of **0501**. However, this is limited to the dependence on the comparison values "less"; "greater" and "equal" cause the same function to be carried out. Thus, a distinction is made between the values "less" and "greater than or equal to." **0506** is connected downstream in pipeline **0505**. **0506** reacts differently to "equal," "greater" and "less" (see **0503**). **0507** also depends on **0501**, but a distinction is made between the values "equal" and "not equal (less or greater)." This embodiment begins at time t (FIG. **5**a) and ends at time t+3. If the data passes through one of pipelines **0502**, **0503**, **0504** or **0505**, **0506**, it is delayed by one clock cycle in each execution in one of macros **0502-0506**. Longer and especially different delays may also occur. Since there is a handshake mechanism between the data and trigger signals for automatic synchronization (according to the related art or this application (TRIGACK/TRIGRDY)), this case need not be discussed separately.

Due to the delays, data and trigger signals of the earlier time t−2 are available at time t between the second and third pipeline steps, for example.

FIGS. **5**a through **5**d show the sequence of three clock cycles t through t+2.

The trigger vectors (i.e., the results of the comparison) generated by **0501** look as follows over t:

Time t	Result of comparison
t − 2	less
t − 1	greater
t	equal
t + 1	greater
t + 2	equal

FIG. **6** shows the integration of several configuration registers into one configurable element. In this embodiment there are three configuration registers **0409** according to FIG. **4**. These are configured over bus **0406**. A control unit **0601** (which may also be designed as a state machine) receives signals TRIGV and TRIGRDY over bus system **0411**. Depending on TRIGV, the control unit switches one of the configuration registers over multiplexer **0602** to bus system **0401** leading to the control mechanisms of the configurable element. For synchronization of the trigger signals with the internal sequences of the configurable element, **0601** has a synchronization output leading to synchronization unit **0412** or to state machine **0413**. For synchronization of the trigger sources, **0601** generates handshake signal TRIGACK after processing the incoming trigger. In this embodiment, each configuration register **0409** is assigned to one TRIGV of the type "equal," "greater," "less." If other operations are executed with each type of trigger, then each configuration register is occupied differently. For example, if a distinction is made only between "equal" and "not equal" then the configuration registers are occupied equally for the types "less" and "greater," namely with the configuration for "not equal." The configuration register for "equal" is occupied differently. This means that the comparison can be made more specific on the basis of the occupancy of the configuration registers, each configurable element being able to design this specification differently.

TRIGV is relayed together with the result over register **0603** to the downstream configurable elements to permit pipelining according to FIGS. **5**a-d. The register and the handshake signals are controlled by **0412** or **0413**. Trigger information together with the result from R-REGsft or with a time offset, i.e., before the result, can be sent over interface **0416** to downstream configurable elements.

A time-offset transfer offers the advantage that no additional time is necessary for setting the configuration registers in the downstream configurable elements, because the setting is made before receiving the data (simultaneously with the release of the result). FIG. **6**a shows a corresponding timing (based on sequences conventional for DFP). Trigger vectors **0615** are generated at rising edge **0613** of module clock **0614**. Triggers are analyzed in the configurable elements at trailing edge **0612**. Data is phase shifted, i.e., released at **0612** and entered at **0613**. The trigger vectors are transferred over the bus and data is calculated during **0610**. Data is transferred over the bus and triggers are calculated during **0611**, or configuration registers of the configurable elements are selected according to data stored at **0613** and the configuration is set accordingly.

FIG. **7**a shows the management of jumps according to the predicate/NOP method of the related art. In execution of a comparison, an entry is made in predicate register **0704**. This entry is queried during the execution of commands, determining whether a command is being executed (the command is inside the code sequence addressed by the conditional jump) or is replaced by an NOP (the command is in a different code sequence from that addressed by the conditional jump). The command is in command register **0701**. The predicate register contains a plurality of entries allocated to a plurality of operations and/or a plurality of processors. This allocation is issued at the compile time of the program of the compiler. Allocation information **0707** is allocated to the command entered into the command register, so that a unique entry is referenced by the respective command.

0703 selects whether the command from **0701** or an NOP is to be executed. In execution of an NOP, one clock cycle is lost. **0703** has a symbolic character, because executing unit **0702** could also in principle be controlled directly by **0704**.

In FIG. **7**b there are n command registers (**0701**: Func **1** . . . Func n). In executing a comparison/conditional jump, the command register to be addressed, i.e., the result of the comparison, is deposited as an entry **0708** in predicate register **0706**, where **0706** has a plurality of such entries. Respective entry **0708** in **0706** is so wide that all possible command registers of an executing unit **0702** can be addressed by it, which means that the width of an entry is $\log_2(n)$ with n command registers. The predicate register contains a plurality of entries allocated to a plurality of operations and/or a plurality of processors. This allocation is issued by the compiler at the compile time of the program. Allocation information **0707** is allocated to the quantity of commands entered into the command registers, so that an unambiguous entry is referenced by the respective commands.

The multiplexer selects which command register supplies the code for the instantaneous execution.

Due to this technology, a valid command is executed instead of an NOP even in the worst case with conditional jumps, so no clock cycle is wasted.

The following provides an explanation of various names, functions and terms described above.

Name Convention

Assembly group	UNIT
Type of operation	MODE
Multiplexer	MUX
Negated signal	not
Register for PLU visible	PLUREG

-continued

Register internal	REG
Shift register	sft

Function Convention
NOT Function!

I	Q
0	1
1	0

AND Function &

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

OR Function #

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

GATE Function G

EN	B	Q
0	0	—
0	1	—
1	0	0
1	1	1

DEFINITION OF TERMS

BM UNIT: Unit for switching data to the bus systems outside the PAE. Switching is done over multiplexers for the data inputs and gates for the data outputs. OACK lines are implemented as open collector drivers. The BM UNIT is controlled by the M-PLUREG.

Data receiver: The unit(s) that process(es) the results of the PAE further.

Data transmitter: The unit(s) that make(s) available the data for the PAE as operands.

Data word: A data word consists of a bit series of any desired length. This bit series represents a processing unit for a system. Commands for processors or similar modules as well as pure data can be coded in a data word.

DFP: Data flow processor according to German Patent/Unexamined Patent No. 44 16 881.

DPGA: Dynamically configurable FPGAs. Related art.

EALU: Expanded arithmetic logic unit. ALU which has been expanded by special functions which are needed or appropriate for operation of a data processing system according to German Patent No. 441 16 881 A1. These are counters in particular.

Elements: Collective term for all types of self-contained units which can be used as part of an electronic module.

Elements thus include:

- configurable cells of all types
- clusters
- blocks of RAM
- logic
- processors
- registers
- multiplexers
- I/O pins of a chip

Event: An event can be analyzed by a hardware element of any type suitable for use and can prompt a conditional action as a reaction to this analysis. Events thus include, for example:

- clock cycle of a computer
- internal or external interrupt signal
- trigger signal from other elements within the module
- comparison of a data stream and/or a command stream with a value
- input/output events
- sequencing, carry-over, reset, etc. of a counter
- analysis of a comparison

FPGA: Programmable logic module. Related art.

F-PLUREG: Register in which the function of the PAE is set. Likewise, the one shot and sleep mode are also set. The register is written by the PLU.

H level: Logic 1 level, depending on the technology used..

Configurable element: A configurable element is a unit of a logic module which can be set for a special function by a configuration word. Configurable elements are thus all types of RAM cells, multiplexers, arithmetic logic units, registers and all types of internal and external network writing, etc.

Configurable cell: See logic cells.

Configure: Setting the function and interconnecting a logic unit, an (FPGA) cell or a PAE (see: Reconfigure).

Configuration data: Any quantity of configuration words.

Configuration memory: The configuration memory contains one or more configuration words.

Configuration word: A configuration word consists of a bit series of any desired length. This bit series represents a valid setting for the element to be configured, so that a functional unit is obtained.

Load logic: Unit for configuring and reconfiguring the PAE. Embodied by a microcontroller specifically adapted to its function.

Logic cells: Configurable cells used in DFPs, FPGAs, DPGAs, fulfilling simple logic or arithmetic functions according to their configuration.

L level: Logic 0 level, depending on the technology used.

M-PLUREG: Register in which the interconnection of the PAE is set. The register is written by the PLU.

O-REG: Operand register for storing the operands of the EALU. Permits independence of the PAE of the data transmitters in time and function. This simplifies the transfer of data because it can take place in an asynchronous or package-oriented manner. At the same time, the possibility of reconfiguring the data transmitters independently of the PAE or reconfiguring the PAE independently of the data transmitters is created.

PLU: Unit for configuring and reconfiguring the PAE. Embodied by a microcontroller specifically adapted to its function.

Propagate: Controlled relaying of a received signal.

RECONFIG: Reconfigurable state of a PAE.

RECONFIG trigger: Setting a PAE in the reconfigurable state.

SM UNIT: State machine UNIT. State machine controlling the EALU.

Switching table: A switching table is a ring memory which is addressed by a control. The entries in a switching table may accommodate any desired configuration words. The control can execute commands. The switching table reacts to trigger signals and reconfigures configurable elements on the basis of an entry in a ring memory.

Synchronization signals: Status signals generated by a configurable element or a processor and relayed to other configurable elements or processors to control and synchronize the data processing. It is also possible to return a synchronization signal with a time lag (stored) to one and the same configurable element or processor.

TRIGACK/TRIGRDY: Handshake of the triggers.

Trigger: Synonymous with synchronization signals.

Reconfigure: Configuring any desired quantity of PAEs again while any desired remaining quantity of PAEs continue their own function (see: Configure).

Processing cycle: A processing cycle describes the period of time needed by a unit to go from one defined and/or valid state into the next defined and/or valid state.

VLIW: Very large instruction word. Coding of microprocessors, prior art method.

Cells: Synonymous with configurable elements.

What is claimed is:

[1. A method for controlling data processing by an integrated circuit that includes a plurality of data processing elements that are arranged for at least one of arithmetically and logically processing data using a sequence of commands, the sequence including jumps, the method comprising:

- for each of a plurality of the processing elements that each include at least one corresponding register:
  - predefining at least one corresponding configuration command; and
  - storing each of the at least one corresponding configuration command in one of the at least one register corresponding to the processing element;
- processing data in at least one first processing element;
- obtaining at least one of a comparison, a sign, a carryover, and an error state during the processing of the data in the at least one first processing element;
- in response to the at least one of the comparison, the sign, the carry-over, and the error state, generating for the at least one second processing element at least one first synchronization signal within a data stream during runtime;
- processing data in at least one second processing element in a stream-like manner; and
- in response to the at least one first synchronization signal, selecting at least one particular command from the stored configuration commands in order to control a jump in the sequence.]

2. A Field Programmable Gate Array integrated circuit, comprising: a multi-dimensionally arranged configurable element structure including configurable elements;

- *an interconnection system for interconnecting the configurable elements; and*
- *at least one of a unit and an interface for configuring the configurable elements;*

wherein:

- *each of at least one of the configurable elements:*
- *is adapted for data processing;*
- *includes:*
- *at least one configuration register adapted for receiving and storing therein during runtime at least one configuration code, each of the at least one configuration code representing only one of a single respective function and a single respective interconnection;*

at least two data inputs and at least one data output connected to the interconnection system;

at least one arithmetic-logic-unit; and at least one status information input from the interconnection system; and is adapted for being configured by the at least one of the unit and the interface

with at least one of the respective single function and the respective single interconnection represented by one or more of the at least one configuration code.

3. The Field Programmable Gate Array integrated circuit according to claim 2, wherein configuration registers of different configurable elements are adapted for receiving therein different configuration codes, for the different configurable elements to be accordingly simultaneously configured with different at least one of functions and interconnections.

4. The Field Programmable Gate Array integrated circuit according to claim 2, wherein the at least one of the configurable elements comprises a configuration interface input for receiving from at least one other of the configurable element the at least one configuration code via the interconnection system.

5. The Field Programmable Gate Array integrated circuit according to claim 4, wherein the Field Programmable Gate Array is adapted for the at least one configuration code to be generated at runtime.

6. The Field Programmable Gate Array integrated circuit according to claim 4, wherein the Field Programmable Gate Array is adapted for the at least one configuration code to be the processing result of the at least one other of the configurable elements.

7. The Field Programmable Gate Array integrated circuit according to claim 4, wherein the at least one of the configurable elements comprises at least one status information output to the interconnection system.

8. The Field Programmable Gate Array integrated circuit according to either of claims 4 and 7, wherein the at least one of the configurable elements comprises at least one adder.

9. The Field Programmable Gate Array integrated circuit according to claim 8, further comprising a feed back channel for feeding back a result of the at least one adder to an operand input of the at least one adder via a multiplexer.

10. The Field Programmable Gate Array integrated circuit according to claim 8, wherein the at least one of the configurable elements comprises at least one comparator.

11. The Field Programmable Gate Array integrated circuit according to claim 4, wherein the at least one of the configurable elements comprises:

at least one adder; at least one comparator adapted for generating the status information; and at least one output for providing the status information to the interconnection system.

12. The Field Programmable Gate Array integrated circuit according to claim 4, wherein the status information is the equal status.

13. The Field Programmable Gate Array integrated circuit according to claim 8, wherein the at least one of the configurable elements comprises at least one state-machine.

14. The Field Programmable Gate Array integrated circuit according to claim 8, wherein the at least one of the configurable elements is adapted for inclusion therein of the status information generated by the at least one adder.

15. The Field Programmable Gate Array integrated circuit according to claim 14, wherein the status information is the equal status.

16. A Field Programmable Gate Array integrated circuit comprising: a multi-dimensionally arranged configurable element structure including a plurality of configurable elements;

an interconnection system for interconnecting the configurable elements; and at least one of a unit and an interface for configuring and reconfiguring the configurable elements;

wherein each of at least one of the configurable elements: is adapted for data processing; includes: at least two data inputs and at least one data output connected to the interconnection system;

at least one arithmetic-logic-unit; a configuration interface input; and at least one configuration register adapted for receiving, during runtime, from at least one other of the configurable elements, and via the configuration interface input and the interconnection system, and storing during runtime, at least one configuration code, each of the at least one configuration code representing only one of a single respective function and a single respective interconnection; and

is adapted to be configured with at least one of the respective single function and the respective single interconnection represented by one or more of the at least one configuration code.

17. The Field Programmable Gate Array integrated circuit according to claim 16, wherein the Field Programmable Gate Array is adapted for the at least one configuration code to be generated by the at least one other of the configurable elements at runtime.

18. The Field Programmable Gate Array integrated circuit according to claim 17, wherein the Field Programmable Gate Array is adapted for the at least one configuration code to be transmitted at runtime.

19. The Field Programmable Gate Array integrated circuit according to claim 18, wherein the Field Programmable Gate Array is adapted for the at least one configuration code to be the processing result of the at least one other of the configurable elements.

20. The Field Programmable Gate Array integrated circuit according to claim 17, wherein the at least one of the configurable elements comprises at least one status information output to the interconnection system.

21. The Field Programmable Gate Array integrated circuit according to any one of claims 17 and 20, wherein the at least one of the configurable elements comprises at least one adder.

22. The Field Programmable Gate Array integrated circuit according to claim 21, further comprising a feed back channel for feeding back a result of the a least one adder to an operand input of the at least one adder via a multiplexer.

23. The Field Programmable Gate Array integrated circuit according to claim 21, wherein the at least one of the configurable elements comprises at least one comparator.

24. The Field Programmable Gate Array integrated circuit according to claim 17, wherein the at least one of the configurable elements comprises:

at least one adder; at least one comparator adapted for generating the status information; and at least one output for providing the status information to the interconnection system.

25. The Field Programmable Gate Array integrated circuit according to claim 24, wherein the status information is an equal status.

26. The Field Programmable Gate Array integrated circuit according to claim 21, wherein the at least one of the configurable elements comprises at least one state-machine.

27. The Field Programmable Gate Array integrated circuit according to claim 21, wherein the at least one adder is adapted for generating status information.

28. The Field Programmable Gate Array integrated circuit according to claim 27, wherein the status information is an equal status.

29. A configurable element arrangement adapted for implementation in an integrated circuit, the integrated circuit comprising:

a multi-dimensionally arranged configurable element structure including a plurality of configurable elements;

an interconnection system for interconnecting the configurable elements; and at least one of a unit and an interface for configuring the configurable elements; wherein each of at least one of the configurable elements:

comprises: at least two data inputs and at least one data output connected to the interconnection system;

at least one arithmetic-logic-unit; a configuration interface input; and at least one configuration register adapted for receiving, during runtime, via the configuration interface input and the interconnection system, and from a unit other than the at least one of the unit and the interface, and storing during runtime, at least one configuration code, each of the at least one configuration code representing only one of a single respective function and a single respective interconnection;

is adapted for being configured with at least one of the respective single function and the respective single interconnection represented by one or more of the at least one configuration code; and

is adapted for data processing.

30. The configurable element arrangement according to claim 29, wherein the configurable element is adapted for receiving at runtime the at least one configuration code from at least one other configurable element.

31. The configurable element arrangement according to claim 30, wherein the configurable element arrangement is adapted for the at least one configuration code from the at least one other configurable element to be generated at runtime.

32. The configurable element arrangement according to claim 30, wherein the configurable element arrangement is adapted for the at least one configuration code from the at least one other configurable element to be a processing result of the at least one other configurable element.

33. The configurable element arrangement according to claim 29, further comprising at least one status information input from the interconnection system.

34. The configurable element arrangement according to claim 29, further comprising at least one status information output to the interconnection system.

35. The configurable element arrangement according to any one of claims 29 and 34, further comprising at least one adder.

36. The configurable element arrangement according to claim 35, further comprising a feed back channel for feeding back, via a multiplexer, a result of the at least one adder to an operand input of the at least one adder.

37. The configurable element arrangement according to claim 35, further comprising at least one comparator.

38. The configurable element arrangement according to claim 35, further comprising at least one state-machine.

39. The configurable element arrangement according to claim 29, further comprising:

at least one adder adapted for generating status information; and at least one status information output for outputting the status information to the interconnection system.

40. The configurable element arrangement according to claim 29, wherein the status information is an equal status.

41. The configurable element arrangement according to claim 39, wherein the configurable elements are implemented in a Field Programmable Gate Array integrated circuit.

42. The configurable element arrangement according to claim 39, wherein the configurable elements are implemented in a runtime configurable Field Programmable Gate Array.

43. The configurable element arrangement according to claim 39, wherein the configurable elements are implemented in a configurable processor integrated circuit.

44. The configurable element arrangement according to claim 39, wherein the configurable elements are implemented in a runtime configurable processor integrated circuit.

45. The configurable element arrangement according to claim 39, wherein the configurable elements are implemented in one of a configurable arithmetic processor integrated circuit and a configurable arithmetic coprocessor integrated circuit.

46. The configurable element arrangement according to claim 29, further comprising:

at least one adder adapted for generating status information; at least one comparator; and

at least one status information output for outputting the status information to the interconnection system.

47. The configurable element arrangement according to claim 46, wherein the status information is an equal status.

48. The configurable element arrangement according to claim 46, wherein the configurable elements are implemented in a Field Programmable Gate Array integrated circuit.

49. The configurable element arrangement according to claim 46, wherein the configurable elements are implemented in a runtime configurable Field Programmable Gate Array integrated circuit.

50. The configurable element arrangement according to claim 46, wherein the configurable elements are implemented in a configurable processor integrated circuit.

51. The configurable element arrangement according to claim 46, wherein the configurable elements are implemented in a runtime configurable processor integrated circuit.

52. The configurable element arrangement according to claim 46, wherein the configurable elements are implemented in one of a configurable arithmetic processor integrated circuit and a configurable arithmetic coprocessor integrated circuit.

53. A data processing integrated circuit, comprising: a multi-dimensionally arranged configurable element structure including a plurality of configurable elements;

at least one of the configurable elements: comprises: at least two data inputs and at least one data output connected to the interconnection system;

at least one arithmetic-logic-unit; a configuration interface input; and at least one configuration register adapted for receiving, during runtime and via the configuration interface input and the interconnection system, and storing during runtime, at least one configuration code, each of the at least one configuration code representing only one of a single respective function and a single respective interconnection;

is adapted for being configured, by (a) the at least one of the unit and the interface and (b) at least one other of the configurable elements, and with at least one of the respective single function and the respective single *interconnection represented by one or more of the at least one configuration code; and*

adapted for data processing.

54. The data processing integrated circuit according to claim 53, wherein the data processing integrated circuit is adapted for the at least one configuration code to be a processing result of the at least one other of the configurable elements.

55. The data processing integrated circuit according claim 53, wherein the each of the at least one of the configurable elements comprises at least one status information output to the interconnection system.

56. The data processing integrated circuit according to any one of claims 53 and 55, wherein the each of the at least one of the configurable elements comprises at least one adder.

57. The data processing integrated circuit according to claim 56, comprising a feed back channel for feeding back a result of the at least one adder to an operand input of the at least one adder via a multiplexer.

58. The data processing integrated circuit according claim 56, wherein the each of the at least one of the configurable elements comprises at least one comparator.

59. The data processing integrated circuit according to claim 56, wherein the each of the at least one of the configurable elements comprises at least one state-machine.

60. The data processing integrated circuit according to claim 53, wherein the each of the at least one of the configurable elements comprises:

at least one adder adapted for generating status information; and at least one status information output adapted for providing the status information to the interconnection system.

61. The data processing integrated circuit according to claim 60, wherein the status information is an equal status.

62. The data processing integrated circuit according to claim 53, wherein the each of the at least one of the configurable elements comprises:

at least one adder; at least one comparator adapted for generating status information; and at least one status information output adapted for providing the status information to the interconnection system.

63. The data processing integrated circuit according to claim 62, wherein the status information is an equal status.

64. A data processing integrated circuit comprising:

configurable elements arranged in a multi-dimensional pattern;

an interconnection system for interconnecting the configurable elements; and

at least one of a unit and an interface for configuring the configurable elements; wherein each of at least some of the configurable elements: comprises: at least one arithmetic unit; at least two operand registers; at least one result register; at least one input interface to the interconnection system for receiving status information generated by another of the configurable elements from the interconnection system;

at least one configuration data input; and at least one configuration register adapted for receiving, at runtime and via the at least one configuration data input, and storing during runtime, at least one configuration code, each of the at least one configuration code representing only one of a single respective function and a single respective interconnection;

is adapted for being configured with at least one of the respective single function and the respective single interconnection represented by one or more of the at least one configuration code; and

is adapted to process the at least two operands arithmetically according to the at least one configuration code and received status information.

65. The data processing integrated circuit according to claim 64, wherein the each of the at least some of the configurable elements is adapted for the receipt of the at least one configuration code to be from at least one other of the configurable elements at runtime.

66. The data processing integrated circuit according to claim 64, wherein the each of the at least some of the configurable elements is adapted for the receipt of the at least one configuration code to be from at least one other of the configurable elements via the interconnection system.

67. The data processing integrated circuit according to claim 64, wherein the at least one configuration data input is adapted for obtaining the at least one configuration code from at least one other of the configurable elements at runtime.

68. The data processing integrated circuit according to claim 67, wherein the at least one configuration data input is connected to the at least one other of the configurable elements via the interconnection system.

69. The data processing integrated circuit according to any of claims 67 and 68, wherein the data processing integrated circuit is adapted for the at least one configuration code received by the each of the at least one of the configurable elements to be generated by at least one other of the configurable elements at runtime.

70. The data processing integrated circuit according to claim 64, wherein the at least one configuration data input is adapted to be connected to at least one other of the configurable elements at runtime via the interconnection system.

71. The data processing integrated circuit according to claim 64, wherein the at least one configuration data input is interconnected to a plurality of configurable elements via the interconnection system.

72. The data processing integrated circuit according to claim 64, wherein the each of the at least some of the configurable elements is adapted to be configured by the at least one of the unit and the interface, and is adapted for the at least one configuration code to be received at the input interface at runtime via the interconnection system from at least one other of the configurable elements.

73. The data processing integrated circuit according to any one of claims 65, 67, and 72, wherein the each of the at least some of the configurable elements comprises at least one output interface to the interconnection system for sending status information generated by the at least one other of the configurable elements via the interconnection system to another of the configurable elements.

74. The data processing integrated circuit according to claim 73, wherein the data processing integrated circuit is adapted for the status information to be generated by an adder within at least one arithmetic unit.

75. The data processing integrated circuit according to claim 74, wherein said adder has a feed back channel for feeding back the result of said adder to an operand input of said adder via a multiplexer.

76. The data processing integrated circuit according to claim 64, wherein the status information is an equal status of a comparator located inside the at least some of the configurable elements.

77. The data processing integrated circuit according to claim 64, wherein the data processing integrated circuit is one of a configurable arithmetic processor and a configurable arithmetic coprocessor.

78. The data processing integrated circuit according to claim 64, wherein the data processing integrated circuit is configurable at runtime.

79. The data processing integrated circuit according to claim 74, wherein the data processing integrated circuit is one of a configurable arithmetic processor and a configurable arithmetic coprocessor.

80. The data processing integrated circuit according to claim 74, wherein the data processing integrated circuit is configurable at runtime.

81. A Field Programmable Gate Array integrated circuit comprising: configurable elements arranged in a multi-dimensional pattern; an interconnection system for interconnecting the configurable elements; and at least one of a unit and an interface for configuring the configurable elements; wherein each of at least some of the configurable elements: comprises: at least one arithmetic unit; at least two operand registers; at least one result register;

at least one input interface to the interconnection system for receiving status information generated by another of the configurable elements from the interconnection system;

at least one configuration data input; and at least one configuration register adapted for receiving, during runtime and via the at least one configuration data input, and storing during runtime at least one configuration code, each of the at least one configuration code representing only one of a single respective function and a single respective interconnection;

is adapted to be configured with at least one of the respective single function and the respective single interconnection represented by one or more of the at least one configuration code; and

is adapted to process the at least two operands arithmetically according to the configuration data and received status information.

82. The data processing integrated circuit according to claim 81, wherein the each of the at least some of the configurable elements is adapted for the runtime receipt of the at least one configuration code to be from at least one other of the configurable elements.

83. The data processing integrated circuit according to claim 81, wherein the each of the at least some of the configurable elements is adapted for the runtime receipt of the at least one configuration code to be from at least one other of the configurable elements via the interconnection system.

84. The data processing integrated circuit according to claim 81, wherein the at least one configuration data input is adapted for obtaining the at least one configuration code from at least one other of the configurable elements at runtime.

85. The Data Processing Integrated Circuit according to claim 84, wherein the at least one configuration data input is connected to the at least one other of the configurable elements via the interconnection system.

86. The data processing integrated circuit according to any of claims 84 and 85, wherein the data processing integrated circuit is adapted for the at least one configuration code to be generated by at least one other of the configurable elements at runtime.

87. The data processing integrated circuit according to claim 81, wherein the at least one configuration data input is adapted for connection to at least one other of the configurable elements at runtime via the interconnection system.

88. The data processing integrated circuit according to claim 81, wherein the at least one configuration data input is interconnected to a plurality of configurable elements via the interconnection system.

89. The data processing integrated circuit according to claim 81, wherein the each of the at least some of the configurable elements is adapted to be configured by the at least one of the unit and the interface and is adapted for the runtime receipt of the at least one configuration code to be from at least one other of the configurable elements.

90. The data processing integrated circuit according to any one of claims 82, 84, and 89, wherein the each of the at least some of the configurable elements comprises at least one output interface to the interconnection system for sending status information generated by the at least one other of the configurable elements via the interconnection system to another of the configurable elements.

91. The data processing integrated circuit according to claim 90, wherein the data processing integrated circuit is adapted for the status information to be generated by an adder within at least one arithmetic unit.

92. The data processing integrated circuit according to claim 91, wherein said adder has a feed back channel for feeding back the result of said adder to an operand input of said adder via a multiplexer.

93. The data processing integrated circuit according to claim 91, wherein the status information is generated by a comparator.

94. The data processing integrated circuit according to claim 93, wherein the status information is an equal status of a comparator located inside the at least some of the configurable elements.

95. A Field Programmable Gate Array integrated circuit comprising:

configurable elements arranged in a multi-dimensional pattern; an interconnection system for interconnecting the configurable elements; and at least one of a unit and an interface for configuring the configurable elements; wherein each of at least some of the configurable elements:

is adapted to receive at least one configuration code from said at least one of the unit and the interface;

comprises: at least one arithmetic unit; at least two operand registers; at least one result register; at least one configuration data input for receiving at runtime, from at least one other of the configurable elements and via the interconnection system, at least one additional configuration code, each of the at least one additional configuration code representing only one of a single respective function and a single respective interconnection of the configurable element; and

at least one configuration register adapted for storing therein at runtime the at least one additional configuration code;

is adapted to be configured with at least one of the respective single function and the respective single interconnection represented by one or more of the at least one additional configuration code; and

is adapted to process at least two operands of the at least two operand registers arithmetic-logically according to the at least one additional configuration code received from the configuration data input and the at least one configuration code provided by said at least one of the unit and the interface.

96. The Field Programmable Gate Array integrated circuit according to claim 95, wherein the each of at least some of the configurable elements comprises at least one input interface *to the interconnection system for receiving status information generated by another of the configurable elements from the interconnection system.*

97. The Field Programmable Gate Array integrated circuit according to anyone of claims 95 and 96 wherein, the each of at least some of the configurable elements comprises at least one output interface to the interconnection system for sending status information generated by the configurable element via the interconnection system to at least one other of the configurable elements.

98. The Field Programmable Gate Array integrated circuit according to claim 97, wherein the at least some of the configurable elements are adapted to process the at least two operands arithmetic-logically additionally according to the statns information.

99. The Field Programmable Gate Array integrated circuit according to claim 98, wherein the status information is generated by an adder inside the at least one arithmetic unit.

100. The Field Programmable Gate Array integrated circuit according to claim 99, wherein said adder has a feed back channel for feeding back a result of said adder to an operand input of said adder via a multiplexer.

101. The Field Programmable Gate Array integrated circuit according to claim 99, wherein the status information is generated by a comparator inside the at least some of the configurable elements.

102. The Field Programmable Gate Array integrated circuit according to claim 101, wherein the status information is an equal status of a comparator located inside the each of the at least some of the configurable elements.

103. A data processing integrated circuit comprising:

configurable elements arranged in a multi-dimensional pattern;

an interconnection system for interconnecting the configurable elements; and at least one of a unit and an interface for configuring the configurable elements; wherein each of at least some of the configurable elements: is adapted to receive at least one configuration code from said at least one of the unit and the interface;

comprises: at least one arithmetic unit; at least two operand registers; at least one result register; at least one configuration data input for receiving at runtime, from at least one other of the configurable elements and via the interconnection system, at least one additional configuration code, each of the at least one additional configuration code representing only one of a single respective function and a single respective interconnection of the configurable element; and

at least one configuration register adapted for storing therein at runtime the at least one additional configuration code;

is adapted to be configured with at least one of the respective single function and the respective single interconnection represented by one or more of the at least one additional configuration code; and

is adapted to process at least two operands of the at least two operand registers arithmetic-logically according to the at least one additional configuration code received from the configuration data input and the at least one configuration code provided by said at least one of the unit and the interface.

104. The data processing integrated circuit according to claim 103, wherein the each of at least some of the configurable elements comprises at least one input interface to the interconnection system for receiving status information generated by another of the configurable elements from the interconnection system.

105. The data processing integrated circuit according to anyone of claims 103 and 104 wherein, the each of at least some of the configurable elements comprises at least one output interface to the interconnection system for sending status information generated by the configurable element via the interconnection system to at least one other of the configurable elements.

106. The data processing integrated circuit according to claim 105, wherein the at least some of the configurable elements are adapted to process the at least two operands arithmetic-logically additionally according to the status information.

107. The data processing integrated circuit according to claim 106, wherein the data processing integrated circuit is adapted for the status information to be generated by an adder inside the at least one arithmetic unit.

108. The data processing integrated circuit according to claim 107, wherein said adder has a feed back channel for feeding back a result of said adder to an operand input of said adder via a multiplexer.

109. The data processing integrated circuit according to claim 107, wherein the data processing integrated circuit is adapted for the status information to be generated by a comparator inside the at least some of the configurable elements.

110. The data processing integrated circuit according to claim 109, wherein the status information is an equal status of a comparator located inside the each of the at least some of the configurable elements.

111. The data processing integrated circuit according to claim 109, wherein the data processing integrated circuit is one of a configurable arithmetic processor integrated circuit and a configurable arithmetic coprocessor integrated circuit.

112. The data processing integrated circuit according to claim 109, wherein the data processing integrated circuit is configurable at runtime.

113. The data processing integrated circuit according to claim 107, wherein the data processing integrated circuit is one of a configurable arithmetic processor integrated circuit and a configurable arithmetic coprocessor integrated circuit.

114. The data processing integrated circuit according to claim 107, wherein the data processing integrated circuit is configurable at runtime.

115. A runtime configurable integrated data processing circuit, comprising:

a plurality of configurable elements arranged in a multi-dimensional structure; and a configurable interconnection for connecting the plurality of configurable elements; wherein: each of at least some of the plurality of configurable elements: includes: at least two operand registers for receiving operand data from the configurable interconnection;

at least one result register for transmitting result data to the configurable interconnection;

at least one arithmetic unit; at least one configuration input for configuring at least an operation performed by the at least one arithmetic unit;

at least one multiplexer located between at least one of the operand registers and the arithmetic unit, the at least one of the operand registers being adapted for feeding at least a first one of inputs of the multiplexer; and

at least one feedback from the at least one result register to at least one input of the at least one multiplexer adapted for feeding result data back to the at least one arithmetic unit; and

is adapted for transmitting at runtime its result as at least one configuration code to the configuration input of at *least one other of the at least some of the plurality of configurable elements via the interconnection;*

each of the at least one other of the at least some of the plurality of configurable elements:

includes at least one configuration register adapted for storing therein during runtime the at least one configuration code, each of the at least one configuration code representing only one of a single respective function and a single respective interconnection; and

is adapted to be configured with at least one of the respective single function and the respective single interconnection represented by one or more of the at least one configuration code; and

at least some of the configurable elements are adapted for processing data according to their configuration.

116. The runtime configurable integrated data processing circuit according to claim 115, wherein at least some of the at least some of the plurality of configurable elements comprise at least one respective configuration input adapted for configuring an interconnection of the at least some of the at least some of the plurality of the configurable elements to at least one other of the configurable elements.

117. The runtime configurable integrated data processing circuit according to any one of claims 115 and 116, wherein the runtime configurable integrated data processing circuit is a Field Programmable Gate Array Integrated Circuit (FPGA).

118. A runtime configurable integrated data processing circuit, comprising:

a plurality of configurable elements arranged in a multidimensional structure; and a configurable interconnection for connecting the plurality of configurable elements; wherein: each of at least some of the plurality of configurable elements: includes: at least two operand registers; at least one result register;

at least one arithmetic-logic unit adapted to perform a computer operation producing a result;

at least one configuration input for configuring at least the computer operation performed by the at least one arithmetic-logic unit;

at least one multiplexer located between at least one of the operand registers and the arithmetic-logic unit, the at least one of the operand registers adapted for feeding at least a first one of inputs of the multiplexer; and

at least one feedback from the at least one result register to at least one input of the at least one multiplexer adapted for feeding result data back to the at least one arithmetic-logic unit; and

is adapted for transmitting its output as at least one configuration code to the configuration input of at least one other of the at least some of the plurality of configurable elements via the interconnection;

each of the at least one other of the at least some of the plurality of configurable elements:

includes at least one configuration register adapted for storing therein during runtime the at least one configuration code, each of the at least one configuration code representing only one of a single respective function and a single respective interconnection; and

is adapted to be configured with at least one of the respective single function and the respective single interconnection represented by one or more of the at least one configuration code; and

at least some of the configurable elements are adapted to process data according to their configuration.

119. The runtime configurable integrated data processing circuit according to claim 118, wherein the at least one arithmetic-logic unit of at least some of the at least some of the plurality of configurable elements comprises at least one of an adder and an ALU.

120. The runtime configurable integrated data processing circuit according to claim 118, wherein the at least one of the adder and the ALU includes a feed back channel for feeding back a result of the at least one of the adder and the ALU to an operand input of the at least one of the adder and the ALU via a multiplexer.

121. The runtime configurable integrated data processing circuit according to claim 117, wherein each of at least some of the at least some of the plurality of configurable elements comprises at least one respective configuration input for configuring the interconnection of the respective configurable elements to at least one other of the configurable elements.

122. The runtime configurable integrated data processing circuit according to any one of claims 119 and 121, wherein the runtime configurable integrated data processing circuit is a Field Programmable Gate Array Integrated Circuit (FPGA).

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