Abstract: A method of arranging components in an integrated circuit includes providing two or more circuit cells of a first type and providing two or more circuit cells of a second type. The circuit cells of the first type are configured to operate in conjunction with the circuit cells of the second type. The method further includes arranging the circuit cells of the first and second types in an alternating pattern such that each circuit cell of the first type is adjacent to at least one circuit cell of the second type. The alternating pattern may be an array of rows and columns and may include a repeating pattern of one first type cell and one second type cell in each of the columns. The alternating pattern may include a repeating pattern of one cell of the first type and two cells of the second type in each of the columns.
before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

Published:

— with international search report (Art. 21(3))
VOLTAGE REFERENCE AND CURRENT SOURCE MIXING METHOD FOR VIDEO DAC

RELATED APPLICATION(S)

[0001] This application claims the benefit of U.S. Provisional Application No. 62/049,612, filed on September 12, 2014, and U.S. Provisional Application No. 61/936,553, filed on February 6, 2014. The entire teachings of the above applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] Mobile computing devices, such as notebook PCs, smart phones, and tablet computing devices, are now common tools used for producing, analyzing, communicating, and consuming data in both business and personal life. Consumers continue to embrace a mobile digital lifestyle as the ease of access to digital information increases with high-speed wireless communications technologies becoming ubiquitous. Popular uses of mobile computing devices include displaying large amounts of high-resolution computer graphics information and video content, often wirelessly streamed to the device.

[0003] While these devices typically include a display screen, the preferred visual experience of a high-resolution, large format display cannot be easily replicated in such mobile devices because the physical size of such device is limited to promote mobility. Another drawback of the aforementioned device types is that the user interface is hands-dependent, typically requiring a user to enter data or make selections using a keyboard (physical or virtual) or touch-screen display.

[0004] As a result, consumers are now seeking a hands-free high-quality, portable, color display solution to augment or replace their hands-dependent mobile devices.

[0005] Integrated circuits used in such color display solutions may be vulnerable to unavoidable process variations that occur when the integrated circuits are fabricated. The process variations may occur across several batches of fabrication or across the same batch, and may result in performance degradation of the integrated circuit.
SUMMARY OF THE INVENTION

[0006] Recently developed micro-displays can provide large-format, high resolution color pictures and streaming video in a very small form factor. One application for such displays can be integrated into a wireless headset computer worn on the head of the user with a display within the field of view of the user, similar in format to eyeglasses, audio headset or video eyewear. A "wireless computing headset" device includes one or more small high-resolution micro-displays and optics to magnify the image. The WVGA micro-displays can provide super video graphics array (SVGA) (800 x 600) resolution or extended graphic arrays (XGA) (1024 x 768) or even higher resolutions. A wireless computing headset contains one or more wireless computing and communication interfaces, enabling data and streaming video capability, and provides greater convenience and mobility through hands dependent devices. For more information concerning such devices, see co-pending patent applications entitled "Mobile Wireless Display Software Platform for Controlling Other Systems and Devices," U.S. Application No. 12/348, 648 filed January 5, 2009, "Handheld Wireless Display Devices Having High Resolution Display Suitable For Use as a Mobile Internet Device," PCT International Application No. PCT/US09/38601 filed March 27, 2009, and "Headset Computer (HSC) As Auxiliary Display With ASR and HT Input," U.S. Application No. 13/799,570 filed March 13, 2013, each of which are incorporated herein by reference in their entirety.

[0007] The terms, "HSC" headset computers, "HMD" head mounted display device, and "wireless computing headset" may be used interchangeably herein.

[0008] A micro-display used in conjunction with a HSC requires highly-integrated circuitry in support of the pixel array that actually produces an image. The support circuitry often implements functionality that is highly sensitive to variations in circuit topologies and layout geometries. Slight process variations that occur during fabrication of integrated circuits can be enough to exploit these sensitive functionalities. A process variation that occurs uniformly across certain components may help to reduce the sensitivity to the variations. The embodiments described herein address techniques for reducing sensitivity to process variations.

[0009] Methods embodying the present invention arrange components in an integrated circuit by providing two or more circuit cells of a first type and providing two or more circuit cells of a second type. The circuit cells of the first type are configured to operate in
conjunction with the circuit cells of the second type. The method further includes arranging the circuit cells of the first and second types in an alternating pattern such that each circuit cell of the first type is adjacent to at least one circuit cell of the second type. The alternating pattern may be an array of rows and columns and may include a repeating pattern of one first type cell and one second type cell in each of the columns.

[0010] In other embodiments, the alternating pattern may include a repeating pattern of one cell of the first type and two cells of the second type in each of the columns.

[0011] In one aspect, the invention may be a method of arranging components in an integrated circuit, including providing two or more circuit cells of a first type, and providing two or more circuit cells of a second type. The circuit cells of the first type are configured to operate in conjunction with the circuit cells of the second type. The method may further include arranging the circuit cells of the first type and the circuit cells of the second type in an alternating pattern such that each circuit cell of the first type is adjacent to at least one circuit cell of the second type.

[0012] In one embodiment, the alternating pattern is an array of rows and columns. In another embodiment, the alternating pattern includes a repeating pattern of one cell of the first type and one cell of the second type in each of the columns. In another embodiment, the alternating pattern includes a repeating pattern of one cell of the first type and two cells of the second type in each of the columns.

[0013] In one embodiment, the circuit cells of the first type provide a reference to the circuit cells of the second type. In one embodiment, the reference is a voltage reference. In another embodiment, the reference is a current reference.

[0014] In one embodiment, the circuit cells of the first type include a reference cell and the circuit cells of the second type include a video DAC cell.

[0015] In another aspect, the invention may be an integrated circuit, comprising two or more circuit cells of a first type, and two or more circuit cells of a second type. The circuit cells of the first type are configured to operate in conjunction with the circuit cells of the second type, e.g., the circuit cells of the first and second type may operate together to accomplish a certain function. The circuit cells of the first type and the circuit cells of the second type are arranged in an alternating pattern such that each circuit cell of the first type is adjacent to at least one circuit cell of the second type.
[0016] In one embodiment, the alternating pattern is an array of rows and columns. In another embodiment, the alternating pattern includes a repeating pattern of one cell of the first type and one cell of the second type in each of the columns.

[0017] In another embodiment, the alternating pattern includes a repeating pattern of one cell of the first type and two cells of the second type in each of the columns. In one embodiment, the circuit cells of the first type provide a reference voltage to the circuit cells of the second type. In one embodiment, the circuit cells of the first type include a reference cell and the circuit cells of the second type include a video DAC cell.

[0018] In another aspect, the invention may be method of arranging components in an integrated circuit, comprising providing a digital to analog converter (DAC) configured to generate a ramped voltage output, and providing two amplifiers, each of which receives the ramped voltage output. The method further includes arranging the two amplifiers to each drive one or more columns of a pixel array.

[0019] One embodiment further includes arranging the two amplifiers to drive the columns of the pixel array from two sides of the pixel array. In one embodiment, the amplifiers further drive a common terminator element.

[0020] In another aspect, the invention may be an integrated circuit, comprising a digital to analog converter (DAC) configured to generate a ramped voltage output, a first amplifier configured to receive the ramped voltage output, and a second amplifier configured to receive the ramped voltage output. The first and second amplifiers are arranged to each drive one or more columns of a pixel column of a video display.

[0021] In one embodiment, the first and second amplifiers are configured to drive the columns of the pixel array from two sides of the pixel array. In another embodiment, the first and second amplifiers are configured to drive a terminator element.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The foregoing will be apparent from the following more particular description of example embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating embodiments of the present invention.
FIG. 1 illustrates a simple example of a micro-display according to the embodiments.

FIG. 2 illustrates an expanded view of the column driver of shown in FIG. 1.

FIG. 3 shows an example of a digital to analog converter in the column driver of FIG. 1.

FIG. 4 shows an example of a DAC architecture that uses a matrix array of reference cells and a matrix array of video DAC cells.

FIG. 5 shows an example of one way of laying out the reference cell array and the video DAC cell array.

FIG. 6 illustrates an example of another way of laying out the reference cell array and the video DAC cell array.

FIG. 7 illustrates an example of an arrangement of reference and video DAC cells according to the described embodiments.

FIG. 8 illustrates another example of an arrangement of reference and video DAC cells according to the described embodiments.

FIG. 9 shows a ramp DAC arrangement integrated with the pixel array according to the described embodiments.

DETAILED DESCRIPTION OF THE INVENTION

A description of example embodiments of the invention follows.

The micro-displays described herein generally include a pixel array 102 driven by a number of data and control signals, as shown in the simple example of FIG. 1. This exemplary micro-display 100 includes 20 columns and 16 rows for a total of 320 pixels, although as described above, actual micro-displays typically have many more pixels (e.g., XGA with 1024 columns and 768 rows).

The micro-display includes column drivers 104 and row drivers 106 that together provide information to the pixel array 102. The column drivers 104 generally provide image information to the pixels, and the row drivers 106 provide control information to the pixels. A column driver signal 108 for a particular a particular pixel column 110 may include multiple signals.

FIG. 2 shows an expanded view of a column driver 104 for a Red-Green-Blue (RGB) pixel array. FIG. 2 shows the first two pixels 202 for a single column 204 of the
array. Each pixel 202 includes a red component 206, a green component 208 and a blue component 210. For each column, the column driver 204 drives three information signals; a red signal 212, a green signal 214 and a blue signal 216. These information signals extend to all of the pixels in the column 204.

[0036] The information signals that drive the pixels are generally analog signals, generated from digital signals by way of a digital to analog converter (DAC). FIG. 3 shows an example of such a conversion for one pixel column. A digital buffer 302 drives 30 bits of information (10 bits of red information, 10 bits of green information and 10 bits of blue information) and provides the 30 bits to a three channel DAC 304. Each channel within the three channel DAC 304 converts 10 bits of information to an analog signal; in other words, the three channel DAC 304 includes a 10 bit red DAC 306, a 10 bit green DAC 308 and a 10 bit blue DAC 310.

[0037] A video DAC, such as DAC 304 in FIG. 3, may include a matrix array of reference cells and a matrix array of video DAC cells. FIG. 4 shows an example of a DAC architecture that uses a matrix array of reference cells 402 and a matrix array of video DAC cells 404. The reference cells 402 generally provide a reference standard to the video DAC cells 404, such as, for example, a reference voltage or a reference current. Carefully laying out the reference cell array and the video DAC cell array may help to minimize the effect of fabrication process variations.

[0038] FIG. 5 illustrates an example of one way of laying out the reference cell array and the video DAC cell array. In this example, the reference cells 502 are arranged in a first block and the video DAC cells 504 are arranged in a second block. The second block is physically separated from the first block. With the arrangement shown in FIG. 5, a process variation that affects the reference cells 502 may be localized such that it affects the reference cells 502 but not the video DAC cells 504. Such a discrepancy between physical characteristics of the reference cells and the video DAC cells may degrade the performance of the associated DAC.

[0039] FIG. 6 shows an example of another way of laying out the reference cell array and the video DAC array. In this example, the reference cells 602 are arranged in a block, surrounded by a ring of video DAC cells 604. With this arrangement, many of the reference cells 602 are adjacent to video DAC cells 604. Process variations will generally affect components in close proximity to one another similarly, such that the effects of the process
variation may be reduced as compared to an arrangement where the cells are more widely distributed. Some of the reference cells, however, are not adjacent to video DAC cells, so a potential for process variation degradation may still exist.

[0040] FIG. 7 shows an example of an arrangement of reference and video DAC cells according to one of the described embodiments. In this example, the reference cells 702 and the video DAC cells 704 are mixed one-by-one, in what amounts to a "checkerboard" pattern. The same visual convention that is used in FIGs. 4-6 to distinguish reference cells from video DAC cells is also used in FIG. 7 and FIG. 8 (i.e., the reference cells are lightly shaded and the video DAC cells are more darkly shaded. For clarity, not all of the cells are labeled with reference numbers.

[0041] The arrangement of the example embodiment in FIG. 7 places each reference cell 702 adjacent to at least one video DAC cell 704. As described elsewhere herein, process variations will generally affect components in close proximity to one another similarly, such that the effects of the process variation may be reduced as compared to an arrangement where the cells are more widely distributed.

[0042] FIG. 8 shows another example of an arrangement according to the described embodiments. In this example, the reference cells 802 are mixed "one-by-two," which again places each reference cell 802 adjacent to at least one video DAC cell 804. This exemplary embodiment, while similar to the arrangement shown in FIG. 7, provides a different distribution of the video DAC cells with respect to the reference cells. This distribution may provide improved response to certain types of process variations.

[0043] The embodiments exemplified by those shown in FIGs. 7 and 8 may, for certain process variations, mitigate degradations with respect to the arrangement shown in FIG. 6. Further, the arrangement shown in FIG. 6 may be limited to certain layout topologies. For example, the ring of video DAC cells 604 may be limited to a square configuration for better performance as compared to rectangular or other shapes. The arrangements of the embodiments shown in FIGs. 7 and 8 may permit many aspect ratios while still delivering acceptable performance. This flexibility facilitates better and easier layout design and circuit integration.

[0044] The arrangements of FIGs. 7 and 8 are examples, and are not intended to be limiting. Other arrangements that place reference cells and DAC cells in close proximity are also within the scope of embodiments of the invention.
In some embodiments, such as for a LCoS (Liquid Crystal on Silicon) display device, the column drivers shown in FIG. 1 may include a ramp DAC and amplifier, which together produce a voltage ramp. The voltage ramp can be sampled and held at a particular time to produce a desired fixed voltage output for use by the associated column of pixels. Varying the sample time varies the fixed voltage output.

Due to requirement for precise control of the column voltage provided to the column of pixels, the ramp DAC generally needs to be a high performance device. An embedded ramp DAC may not provide such precise control. Consequently, an LCoS display system may utilize a ramp DAC that is external to the LCoS device. An external ramp DAC is not limited by the size and power constraints of the LCoS architecture, which may result in better performance. The external loading required for this arrangement, however, may increase the power consumption of the LCoS device.

An example of an external ramp DAC may include a DAC, driving a low pass filter, with the output of the low pass filter feeding an amplifier. The amplifier drives an external port of the LCoS device. This arrangement provides increased performance at the cost of increased power consumption.

FIG. 9 illustrates an example of a ramp DAC arrangement integrated within an LCoS device, according to an embodiment of the invention. This arrangement includes a single ramp DAC 902, which drives a first amplifier 904 and a second amplifier 906. In this embodiment, the amplifiers 904, 906 are arranged to drive a pixel array 908 from two sides of the array 908. In this example, the two sides are the top and bottom of the array, although other arrangements may also be used. This arrangement provides an improvement in performance as compared to conventional embedded ramp DACs.

The amplifiers also drive a common terminator element 910, which serves to mitigate or eliminate offset of the amplifiers 904, 906. The terminator element 910 may be a real resistance or a complex impedance.

It will be apparent that one or more embodiments, described herein, may be implemented in many different forms of software and hardware. Software code and/or specialized hardware used to implement embodiments described herein is not limiting of the invention. Thus, the operation and behavior of embodiments were described without reference to the specific software code and/or specialized hardware - it being understood that
one would be able to design software and/or hardware to implement the embodiments based on the description herein.

[0051] Further, certain embodiments of the invention may be implemented as logic that performs one or more functions. This logic may be hardware-based, software-based, or a combination of hardware-based and software-based. Some or all of the logic may be stored on one or more tangible computer-readable storage media and may include computer-executable instructions that may be executed by a controller or processor. The computer-executable instructions may include instructions that implement one or more embodiments of the invention. The tangible computer-readable storage media may be volatile or non-volatile and may include, for example, flash memories, dynamic memories, removable disks, and non-removable disks.

[0052] While this invention has been particularly shown and described with references to example embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.
CLAIMS

What is claimed is:

1. A method of arranging components in an integrated circuit, comprising:
   providing two or more circuit cells of a first type;
   providing two or more circuit cells of a second type, the circuit cells of the first type being configured to operate in conjunction with the circuit cells of the second type;
   arranging the circuit cells of the first type and the circuit cells of the second type in an alternating pattern such that each circuit cell of the first type is adjacent to at least one circuit cell of the second type.

2. The method of claim 1, wherein the alternating pattern is an array of rows and columns.

3. The method of claim 2, wherein the alternating pattern includes a repeating pattern of one cell of the first type and one cell of the second type in each of the columns.

4. The method of claim 2, wherein the alternating pattern includes a repeating pattern of one cell of the first type and two cells of the second type in each of the columns.

5. The method of claim 1, wherein the circuit cells of the first type provide a reference to the circuit cells of the second type.

6. The method of claim 5, wherein the reference is a voltage reference.

7. The method of claim 5, wherein the reference is a current reference.

8. The method of claim 1, wherein the circuit cells of the first type include a reference cell and the circuit cells of the second type include a video DAC cell.

9. An integrated circuit, comprising:
   two or more circuit cells of a first type;
   two or more circuit cells of a second type, the circuit cells of the first type being configured to operate in conjunction with the circuit cells of the second type;
the circuit cells of the first type and the circuit cells of the second type
arranged in an alternating pattern such that each circuit cell of the first type is adjacent
to at least one circuit cell of the second type.

10. The integrated circuit of claim 9, wherein the alternating pattern is an array of rows
and columns.

11. The integrated circuit of claim 10, wherein the alternating pattern includes a repeating
pattern of one cell of the first type and one cell of the second type in each of the
columns.

12. The integrated circuit of claim 10, wherein the alternating pattern includes a repeating
pattern of one cell of the first type and two cells of the second type in each of the
columns.

13. The integrated circuit of claim 9, wherein the circuit cells of the first type provide a
reference voltage to the circuit cells of the second type.

14. The integrated circuit of claim 9, wherein the circuit cells of the first type include a
reference cell and the circuit cells of the second type include a video DAC cell.

15. A method of arranging components in an integrated circuit, comprising:
   providing a digital to analog converter (DAC) configured to generate a ramped
   voltage output;
   providing two amplifiers, each of which receives the ramped voltage output;
   arranging the two amplifiers to each drive one or more columns of a pixel
   array.

16. The method of claim 15, further including arranging the two amplifiers to drive the
columns of the pixel array from two sides of the pixel array.

17. The method of claim 15, wherein the amplifiers further drive a common terminator
element.

18. An integrated circuit, comprising:
a digital to analog converter (DAC) configured to generate a ramped voltage output;

a first amplifier configured to receive the ramped voltage output;

a second amplifier configured to receive the ramped voltage output;

the first and second amplifiers arranged to each drive one or more columns of a pixel column of a video display.

19. The integrated circuit of claim 17, wherein the first and second amplifiers are configured to drive the columns of the pixel array from two sides of the pixel array.

20. The integrated circuit of claim 17, wherein the first and second amplifiers are configured to drive a terminator element.
VIDEO DAC Maximum Output Voltage = \( \frac{V_{\text{ref}}}{R_{\text{ref}}} \times \frac{M}{N} \) \times R_{\text{out}}

VIDEO DAC Power Consumption = \( I_{\text{amp}} + I_{\text{ref}} + (I_{\text{out}_b} + I_{\text{out}_d}) \)
**INTERNATIONAL SEARCH REPORT**

**A. CLASSIFICATION OF SUBJECT MATTER**

INV. G09G3/20

ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>US 2007/133328 A1 (KOIDE YASUNORI [JP]) 14 June 2007 (2007-06-14)</td>
<td>1,2,4-6, 9,10,12, 13</td>
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<tr>
<td>A</td>
<td>paragraph [0059]; figures 2,9,10</td>
<td>3,7,8, 11,14</td>
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<td>A</td>
<td>figure 2a</td>
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**X** Further documents are listed in the continuation of Box C.  

| X | See patent family annex. |

* Special categories of cited documents:
  
* "A" document defining the general state of the art which is not considered to be of particular relevance
  
* "E" earlier application or patent but published on or after the international filing date
  
* "L" document which may throw doubts on priority claim(s) on which is cited to establish the publication date of another citation or other special reason (as specified)
  
* "O" document referring to an oral disclosure, use, exhibition or other means
  
* "P" document published prior to the international filing date but later than the priority date claimed
  
* "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
  
* "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
  
* "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
  
* "A" document member of the same patent family

Date of the actual completion of the international search  

6 July 2015

Date of mailing of the international search report  

14/07/2015

Name and mailing address of the ISA/  

European Patent Office, P.B. 5818 Patentlaan 2  
NL-2280 HV Rijswijk  
Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016

Authorized officer  

Gundlach, Harald
### DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<tr>
<td>X</td>
<td>wo 2005/057532 A2 (GENOA COLOR TECHNOLOGIES LTD [IL]; ROTH SHMUEL [IL]; BEN-CHORIN MOSHE) 23 June 2005 (2005-06-23) page 10, line 12 - line 16; figures 3a, 3b</td>
<td>1, 2, 5, 9, 10</td>
</tr>
</tbody>
</table>
INTERNATIONAL SEARCH REPORT

Box No. II  Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
   because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
   because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
   because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III  Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

   see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant’s protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant’s protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.
<table>
<thead>
<tr>
<th>Claims</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-14</td>
<td>A method or an integrated circuit related to the arrangement of circuit cells of two different types, so as to reduce the effect of process variations (see par. 38, 39).</td>
</tr>
<tr>
<td>15-20</td>
<td>A method and an integrated circuit related to the generation of a ramped voltage output by means of an analog converter and two amplifiers.</td>
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<td>Patent document cited in search report</td>
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