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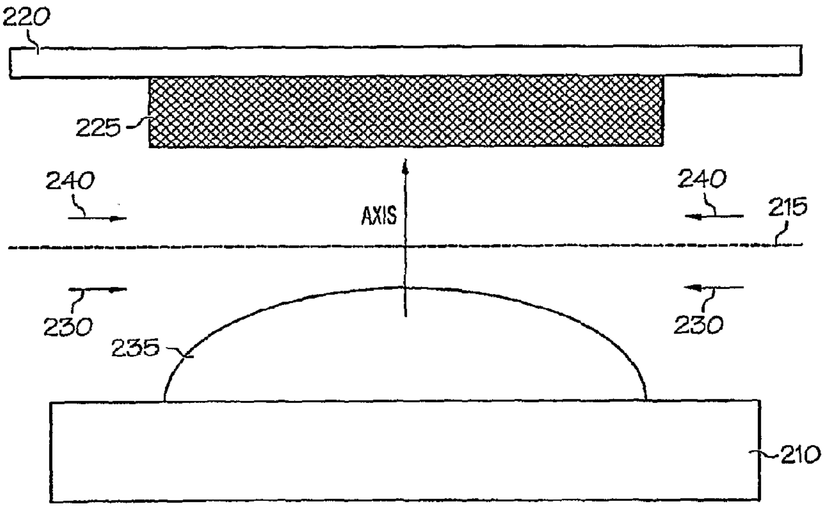
(54) Title: METHOD OF MAKING AN ENCAPSULATED PLASMA SENSITIVE DEVICE



(57) Abstract: A method of making an encapsulated plasma sensitive device. The method comprises: providing a plasma sensitive device adjacent to a substrate; depositing a plasma protective layer on the plasma sensitive device using a process selected from non-plasma based processes, or modified sputtering processes; and depositing at least one barrier stack adjacent to the plasma protective layer, the at least one barrier stack comprising at least one decoupling layer and at least one barrier layer, the plasma sensitive device being encapsulated between the substrate and the at least one barrier stack, wherein the decoupling layer, the barrier layer, or both are deposited using a plasma process, the encapsulated plasma sensitive device having a reduced amount of damage caused by the plasma compared to an encapsulated plasma sensitive device made without the plasma protective layer. An encapsulated plasma sensitive device is also described.

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METHOD OF MAKING AN ENCAPSULATED PLASMA SENSITIVE DEVICE

The present invention relates generally to encapsulated devices, and more particularly to encapsulated plasma sensitive devices, and to methods of making encapsulated plasma sensitive devices.

Many devices are subject to degradation caused by permeation of environmental gases or liquids, such as oxygen and water vapor in the atmosphere or chemicals used in the processing of the electronic product. The devices are usually encapsulated in order to prevent degradation.

Various types of encapsulated devices are known. For example, U.S. Patent Nos. 6,268,695, entitled "Environmental Barrier Material For Organic Light Emitting Device And Method Of Making," issued July 31, 2001; 6,522,067, entitled "Environmental Barrier Material For Organic Light Emitting Device And Method Of Making," issued February 18, 2003; and 6,570,325, entitled "Environmental Barrier Material For Organic Light Emitting Device And Method Of Making", issued May 27, 2003, all of which are incorporated herein by reference, describe encapsulated organic light emitting devices (OLEDs). U.S. Patent No. 6,573,652, entitled "Encapsulated Display Devices", issued June 3, 2003, which is incorporated herein by reference, describes encapsulated liquid crystal displays (LCDs), light emitting diodes (LEDs), light emitting polymers (LEPs), electronic signage using electrophoretic inks, electroluminescent devices (EDs), and phosphorescent devices. U.S. Patent No. 6,548,912, entitled "Semiconductor Passivation Using Barrier Coatings," issued April 15, 2003, which is incorporated herein by reference, describes encapsulated microelectronic devices, including integrated circuits, charge coupled devices, light emitting diodes, light emitting polymers, organic light emitting devices, metal sensor pads, micro-disk lasers, electrochromic devices, photochromic devices, microelectromechanical systems, and solar cells.

Generally, encapsulated devices can be made by depositing barrier stacks adjacent to one or both sides of the device. The barrier stacks typically include at least one barrier layer and at least one decoupling layer. There could be one decoupling layer and one barrier layer, there could be multiple decoupling layers on one side of one or more barrier layers, or there could be one or more decoupling layers on both sides of one or more barrier layers. The important feature is that the barrier stack has at least one decoupling layer and at least one barrier layer.

One embodiment of an encapsulated display device is shown in Fig. 1. The encapsulated display device 100 includes a substrate 105, a display device 110, and a barrier stack 115. The barrier stack 115 includes a barrier layer 120 and a decoupling layer 125. The barrier stack 115 encapsulates the display device 110, preventing environmental oxygen and water vapor from degrading the display device.

The barrier layers and decoupling layers in the barrier stack can be made of the same material or of a different material. The barrier layers are typically about 100-400 Å thick, and the decoupling layers are typically about 1000-10,000 Å thick.

Although only one barrier stack is shown in Fig. 1, the number of barrier stacks is not limited. The number of barrier stacks needed depends on the level of water vapor and oxygen permeation resistance needed for the particular application. One or two barrier stacks should provide sufficient barrier properties for some applications. The most stringent applications may require five or more barrier stacks.

The barrier layers can be deposited using a vacuum process, such as sputtering, chemical vapor deposition (CVD), metalorganic chemical vapor deposition (MOCVD), plasma enhanced chemical vapor deposition (PECVD), evaporation, sublimation, electron cyclotron resonance-plasma enhanced vapor deposition (ECR-PECVD), and combinations thereof. Suitable barrier materials include, but are not limited to, metals, metal oxides, metal nitrides, metal carbides, metal oxynitrides, metal oxyborides, and combinations thereof.

The decoupling layers can be deposited using a vacuum process, such as flash evaporation with *in situ* polymerization under vacuum, or plasma deposition and polymerization, or atmospheric processes, such as spin coating, ink jet printing, screen printing, or spraying. Suitable materials for the decoupling layer include, but are not limited to, organic polymers, inorganic polymers, organometallic polymers, hybrid organic/inorganic polymer systems, and silicates.

As an example, an OLED can be encapsulated with a barrier stack including one or more polymeric decoupling layers and one or more barrier layers. The polymeric decoupling layers can be formed from acrylate functional precursors which are deposited using flash evaporation and polymerized by ultraviolet (UV) exposure. The barrier layers can be reactively sputtered aluminum oxide.

Depositing multi-layer barrier stacks on relatively insensitive substrates such polymer films does not typically result in damage to the substrate. In fact, several patents disclose the use of plasma treatment to improve properties for a multi-layer barrier on a substrate. U.S. Patent No. 6,083,628 discloses plasma treatment of polymeric film substrates and polymeric layers from acrylates deposited using a flash evaporation process as a means of improving properties. U.S. Patent No. 5,440,466 similarly discusses plasma treatment of substrates and acrylate layers to improve properties.

However, we have found that some of the devices being encapsulated have been damaged by the plasma used in depositing the barrier and/or decoupling layers. Plasma damage has occurred when a substrate with a plasma sensitive device on it, such as an OLED, is encapsulated with a multi-layer barrier stack in which a plasma based and/or assisted process is used to deposit a barrier layer or decoupling layer. For example, plasma damage has occurred when reactively sputtering a barrier layer of AlO_x under conditions suitable for achieving barrier properties, sputtering a barrier layer of AlO_x onto the top surface of a plasma sensitive device, and/or sputtering a barrier layer of AlO_x on a vacuum deposited, acrylate based polymeric layer. The damage observed when depositing a barrier layer onto a previously deposited decoupling layer is distinct, and is the subject of co-pending application Serial No. 60/711,136 (VIT 0062 MA).

Plasma damage associated with deposition of a barrier layer, a decoupling layer, or another layer essentially has a negative impact on the electrical and/or luminescent characteristics of a device resulting from encapsulation. The effects will vary by the type of device, the manufacturer of the device, and the wavelength of the light emitted. It is important to note that plasma damage is dependent on the design of the device to be encapsulated. For example, OLEDs made by some manufacturers show little to no plasma damage while OLEDs made by other manufacturers show significant plasma damage under the same deposition conditions. This suggests that that there are features within the device that affect its sensitivity to plasma exposure.

One way to detect plasma damage is to measure the voltage needed to achieve a specified level of luminescence. Another way is to measure the intensity of the luminescence. Plasma damage results in higher voltage requirements to achieve the same level of luminescence (typically 0.2 to 0.5 V higher for an OLED), and/or lower luminescence.

Although not wishing to be bound by theory, plasma damage that is observed when a decoupling layer employing plasma, a sputtered AlO_x, or another layer employing plasma is formed (deposited) directly on an OLED or other sensitive device is believed to be due to an adverse interaction with one or more components of the plasma, including charged or neutral species, UV radiation, and high thermal input.

Thus, there is a need for a method of preventing the damage caused by processes utilizing plasma in the encapsulation of various devices.

The present invention meets this need by providing a method of making an encapsulated plasma sensitive device comprising: providing a plasma sensitive device adjacent to a substrate; depositing a plasma protective layer on the plasma sensitive device using a process selected from non-plasma based processes, or modified sputtering processes; and depositing at least one barrier stack adjacent to the plasma protective layer, the at least one barrier stack comprising at least one decoupling layer and at least one barrier layer, the plasma sensitive device being encapsulated between the substrate and the at least one barrier stack, wherein the decoupling layer, the barrier layer, or both are deposited using a plasma process, the encapsulated plasma sensitive device having a reduced amount of damage caused by the plasma compared to an encapsulated plasma sensitive device made without the plasma protective layer.

Another aspect of the invention is an encapsulated plasma sensitive device. The encapsulated plasma sensitive device includes a substrate; a plasma sensitive device adjacent to a substrate; a plasma protective layer on the plasma sensitive device, the plasma protective layer deposited using a process selected from non-plasma based processes, or modified sputtering processes; and at least one barrier stack adjacent to the protective layer, the at least one barrier stack comprising at least one decoupling layer and at least one barrier layer, the plasma sensitive device being encapsulated between the substrate and the at least one barrier stack, wherein the encapsulated plasma sensitive device has a reduced amount of damage caused by a plasma compared to an encapsulated plasma sensitive device made without the plasma protective layer. By "adjacent," we mean next to, but not necessarily directly next to.

There can be additional layers intervening between the substrate and the barrier stacks. By "on," we mean deposited directly on the previous layer without any intervening layers.

Fig. 1 is a cross-section of a portion of one embodiment of an encapsulated display device.

Fig. 2 is a diagram of one embodiment of a modified sputtering process according to the present invention.

Fig. 3 is a diagram of another embodiment of a modified sputtering process according to the present invention.

Fig. 4 are graphs showing a comparison of the voltage shift with and without a plasma protective layer.

Fig. 5 are graphs showing a comparison of the leakage current with and without a plasma protective layer.

Fig. 6 are graphs showing a comparison of the light output with and without a plasma protective layer.

Fig. 7 is a graph showing the voltage shift as a function of the thickness of a plasma protective layer deposited using thermal evaporation.

Fig. 8 is a graph showing the voltage shift as a function of DF (irradiation time x discharge power).

Fig. 9 is a graph showing the voltage shift as a function of the thickness of a plasma protective layer deposited using a modified sputtering process.

The addition of a layer to shield the underlying device from exposure to the plasma (from deposition of the barrier layer, the decoupling layer, or both) has been shown to reduce or avoid plasma damage.

One method involves the deposition of a plasma protective layer using a non-plasma based process. Suitable non-plasma based processes include both vacuum processes and atmospheric processes. Suitable vacuum processes include, but are not limited to, thermal evaporation, electron beam evaporation, chemical vapor deposition (CVD), and metalorganic chemical vapor deposition (MOCVD), catalytic chemical vapor deposition, laser thermal transfer, or evaporation or chemical vapor deposition followed by ion assisted densification. Suitable atmospheric processes include, but are not limited to, spin coating, ink jet printing, screen printing, spraying, gravure printing, offset printing, and laser thermal transfer. With atmospheric processes, the working gases should be free of O_2 and H_2O content.

The plasma protective layer can be made of inorganic and organic materials. Suitable inorganic materials include, but are not limited to, metal halides, such as LiF_2, MgF_2, CaF_2, and SiO_x. Suitable organic materials include, but are not limited to, aluminum tris 8-8-hydroxyquinoline, phthalocyanines, naphthalocyanines, and similar polycyclic aromatics.

Another method involves depositing the plasma protective layer using a modified sputtering process. Modified sputtering processes include, but are not limited to, modified reactive sputtering processes. By changing the sputtering configuration and/or the process conditions of the sputtering, a less energetic process in terms of the impact on the receiving surface can be obtained. This expands the range of plasma protective layers to include a wider range of inorganic compounds, e.g., AlO_x and SiO_x based layers, which have advantages including being dielectrics and chemically inert. However, the changes impact the physical and, to a lesser degree, the chemical properties of the deposited layers. For example, the density (increased porosity), stress, and grain size can be altered. One result of this can be the loss of barrier properties, despite the demonstrated ability to shield the underlying OLED from plasma damage. For example, a layer of AlO_x could be deposited under conditions that avoid plasma damage, and a second layer of AlO_x could be deposited as a barrier layer when the encapsulation is designed with the barrier layer first.

One modification of the sputtering process involves the use of a screen placed between the target cathode (the source of at least a part of the material to be deposited) and the substrate with the device to be sputter coated. A diagram of this process is shown in Fig. 2. The cathode 210 is on one side of the screen 215, while the substrate 220 with the OLED 225 is on the other side. The inert sputtering gas 230 is introduced on the cathode side, and the sputtering plasma 235 is also on that side. The reactive gas 240 is fed on the substrate/device side. The presence of the screen 215 reduces the reaction of the reactive gas with the surface of the cathode 210.

Another modification of the sputtering process involves off-axis sputtering. A diagram of one embodiment of this process is shown in Fig. 3. The substrate/device receiving the sputtered material is placed at a position removed from (and oblique to) the sputtering plasma. Fig. 3 shows a "facing target" or "facing cathode" arrangement. There are two cathodes 250, 255 facing each other. The sputtering plasma 260 is positioned between the two cathodes 250, 255. The substrate/device 265 is located off to the side and perpendicular to the two cathodes 250, 255. This arrangement eliminates a direct path from the cathodes 250, 255 to the substrate/device 265. The sputtered species will reach the substrate only after multiple collisions and lose most of their energy along the way. This will reduce radical generation in the decoupling polymer layer. Another advantage of the off-axis sputtering process is the mitigation of the thermal impact of sputter deposition on thermally sensitive substrates, i.e., the indirect path of less energetic species results in less heating of receiving surfaces. There are other variations of off-axis sputtering which result in similar deposition schemes and which could be used.

Instead of changing the sputtering configuration, or in addition to it, it is also possible to vary the process parameters for the sputtering, including the exposure time or the energy/power of the plasma. Experimental results have shown that the longer the device is exposed to the plasma, the greater the plasma damage. This has led to increasing the process speed in order to reduce or eliminate the plasma damage.

Typically, for a sputtering configuration that has been determined to deposit a satisfactory barrier layer (cathode, magnet placements, spacing, gas feeds, etc.), barrier layers are deposited at a track speed of about 30 cm/min at a power of about 2000 watts. One modified process involves increasing the track speed to about 90 cm/min (about three times standard track speed) and increasing the power to 2500 watts. The increase in track speed offsets the higher power resulting in decreased overall exposure to the plasma. Alternatively, the track speed can be decreased to about 20 cm/min and the power decreased to about 500 watts. The power reduction offsets the slower speed, resulting in lower exposure to the plasma.

Example 1

OLEDs made by two manufacturers were tested for voltage shift and light decrease. The OLEDs were supplied by the manufacturers on glass substrates. They were then encapsulated. The first layer was a thick layer (1000 Å) of AlO_x followed by 4 acrylate polymer (0.5 microns)/AlO_x (300 Å) pairs. The oxide layers were sputtered without a screen (Configuration I).

The results are shown in Table 1. A blue OLED made by manufacturer 1 showed a voltage shift of 0.5-0.8 V, and a moderate light decrease. A green OLED made by manufacturer 3 showed a voltage shift of 1 V, with a strong light decrease.

Voltage shift and light decrease for OLEDs encapsulated by sputtering the oxide layer with a screen were measured (Configuration II). The OLEDs were encapsulated with a first thick layer (1000 Å) of AlO_x followed by either 4 or 6 acrylate polymer (0.5 microns)/AlO_x (300 Å) pairs. The OLEDs were processed at the standard track speed of 30 cm/min and the standard power of 2000 watts.

The results are shown in Table 1. OLEDs from different manufacturers showed varying amounts of voltage shift and light decrease. Furthermore, different colored OLEDs from the same manufacturer showed different amounts of voltage shift and light decrease. This confirms that there is a variation in the plasma damage for OLEDs from different manufacturers, and for different colored OLEDs.

Table 1

OLED		Configuration I		Configuration II	
				Standard	
		Voltage Shift	Light Decrease	Voltage Shift	Light Decrease
Mfr 1	blue	0.5-0.8	moderate	0-0.3	no
Mfr 2	blue			0.2	moderate
	green			0.5	strong
	red			0.3-0.4	strong
	red 1				
Mfr 3	green	1	strong	0.6	moderate
Mfr 4	green			0.2	no
Mfr 5				0.1-0.5	no
Mfr 6	green				1.8
Mfr 7	yellow			1	strong

Example 2

Several encapsulated OLEDs were made with a plasma protective layer of 300 Å of LiF. The LiF was deposited using a thermal evaporation process. The OLEDs had a thick layer (1000 Å) of AlO_x followed by either 4 or 6 acrylate polymer (0.5 microns)/AlO_x (300 Å) pairs.

The OLEDs were tested for voltage shift, leakage current, and lightout. For comparison, several OLEDs were made without the LiF protective layer. The results are shown in Figs. 4-6 and Table 2. The LiF protective layer eliminated the voltage shift induced by exposure to the plasma during sputtering deposition of the thick barrier layer.

Fig. 7 shows the voltage shift for various thicknesses of LiF. A layer of LiF was deposited on the OLEDs followed by a layer of AlO_x as a barrier layer. The results suggest that a thickness of at least about 300 Å may be needed to eliminate the voltage shift.

Table 2

OLED		Configuration II			
		Standard		LiF protection	
		Voltage shift	Light Decrease	Voltage shift	Light Decrease
Mfr 1	blue	0-0.3	no	0	no
Mfr 2	blue	0.2	moderate	na	na
	green	0.5	strong	0	no
	red	0.3-0.4	strong	na	na
	red 1				
Mfr 3	green	0.6	moderate	0.1-0.2	no
Mfr 4	green	0.2	no	0	no
Mfr 5		0.1-0.5	no		
Mfr 6	green		1.8		
Mfr 7	yellow	1	strong	0	no

Example 3

The effect of process parameters on voltage shift was evaluated. Table 3 shows a comparison of the effect of exposure time on plasma damage. The modified conditions involved increasing the track speed to 90 cm/min (about three time standard track speed) and increasing the power to 2500 watts, and decreasing track speed to 20 cm/min and the power to 500 watts. The voltage shift and light decrease of the OLEDs made using Configuration II and standard sputtering conditions for the barrier (power of 2000 watts, track speed of 30 cm/min) are included for comparison. The voltage shift and light decrease are reduced or eliminated when the exposure time is reduced.

Fig. 8 shows the voltage shift as a function of discharge factor. Discharge factor is an approach to quantifying the exposure of a receiving surface, such as a polymer, an OLED, etc., to reactive species present in sputtering plasmas. It is related to the irradiation dose (energy/area) and is calculated by multiplying irradiation time by discharge power. Voltage shift increased with increasing discharge factor, as shown by Fig. 8. A comparable voltage shift can be obtained under different deposition conditions, e.g., power or track speed. The dominant factor is exposition time, with power having a lesser influence. This suggests that decreasing the exposition time should decrease the voltage shift.

The voltage shift was also measured as a function of aluminum oxide protective layer thickness. By changing the process conditions (increasing the track speed to 90 cm/min (about three time standard track speed) and increasing the power to 2500 watts, and decreasing track speed to 20 cm/min and the power to 500 watts.), the thickness of the aluminum oxide protective layer was varied. As shown in Fig. 9, there is a minimum thickness of about 100 Å above which no further voltage shift is induced by the plasma process.

Table 3

OLED		Configuration II			
		Standard		Modified	
		Voltage shift	Light Decrease	Voltage shift	Light Decrease
Mfr 1	blue	0-0.3	no	0	no
Mfr 2	blue	0.2	moderate	0.1	no
	green	0.5	strong	0.15-.35	no
	red	0.3-0.4	strong	0.1/0.4*	no
	red 1			0.1-0.3	no
Mfr 3	green	0.6	moderate		
Mfr 4	green	0.2	no		
Mfr 5		0.1-0.5	no		
Mfr 6	green		1.8	no	
Mfr 7	yellow	1	strong		

While certain representative embodiments and details have been shown for purposes of illustrating the invention, it will be apparent to those skilled in the art that various changes in the compositions and methods disclosed herein may be made without departing from the scope of the invention, which is defined in the appended claims.

Claims

1. A method of making an encapsulated plasma sensitive device comprising:

providing a plasma sensitive device adjacent to a substrate;

depositing a plasma protective layer on the plasma sensitive device using a process selected from non-plasma based processes, or modified sputtering processes; and

depositing at least one barrier stack adjacent to the plasma protective layer, the at least one barrier stack comprising at least one decoupling layer and at least one barrier layer, the plasma sensitive device being encapsulated between the substrate and the at least one barrier stack, wherein the decoupling layer, the barrier layer, or both are deposited using a plasma process, the encapsulated plasma sensitive device having a reduced amount of damage caused by a plasma compared to an encapsulated plasma sensitive device made without the plasma protective layer.

2. The method of claim 1 wherein the plasma protective layer is deposited using the non-plasma based process.

3. The method of claim 2 wherein the non-plasma based process is a process performed under a vacuum.

4. The method of claim 2 wherein the non-plasma based process is selected from thermal evaporation, electron beam evaporation, chemical vapor deposition, metalorganic chemical vapor deposition, catalytic chemical vapor deposition, laser thermal transfer, evaporation or chemical vapor deposition followed by ion densification, or combinations thereof.

5. The method of claim 2 wherein the non-plasma based process is a process performed at atmospheric pressure.

6. The method of claim 2 wherein the non-plasma based process is selected from spin coating, ink jet printing, screen printing, spraying, gravure printing, offset printing, laser thermal transfer, or combinations thereof.

7. The method of claim 2 wherein the plasma protective layer is an inorganic coating.

8. The method of claim 7 wherein the inorganic coating is selected from LiF, MgF_2, CaF_2, or combinations thereof.

9. The method of claim 2 wherein the plasma protective layer is an organic coating.

10. The method of claim 9 wherein the organic coating is selected from aluminum tris 8-hydroxyquinoline, phthalocyanines, naphthalocyanines, polycyclic aromatics, or combinations thereof.

11. The method of claim 1 wherein the plasma protective layer is deposited using the modified sputtering process.

12. The method of claim 11 wherein the modification comprises providing a screen between a target cathode and the plasma sensitive device.

13. The method of claim 11 wherein the modification comprises applying off-axis sputtering.

14. The method of claim 11 wherein the modification comprises reducing a time of exposure of the plasma sensitive device to a plasma.

15. The method of claim 11 wherein the modification comprises reducing the energy of a plasma.

16. The method of claim 11 wherein the plasma protective layer is selected from AlO_x, SiO_2, or combinations thereof.

17. The method of claim 11 wherein the plasma protective layer is not a barrier layer.

18. The method of claim 11 wherein the modified sputtering process comprises a modified reactive sputtering process.

19. The product produced by the method of claim 1.

20. The product produced by the method of claim 2.

21. The product produced by the method of claim 11.

22. An encapsulated plasma sensitive device comprising:
a substrate;
a plasma sensitive device adjacent to a substrate;
a plasma protective layer on the plasma sensitive device, the plasma protective layer deposited using a process selected from non-plasma based processes, or modified sputtering processes; and
at least one barrier stack adjacent to the plasma protective layer, the at least one barrier stack comprising at least one decoupling layer and at least one barrier layer, the plasma sensitive device being encapsulated between the substrate and the at least one barrier stack, wherein the encapsulated plasma sensitive device has a reduced amount of damage caused by a plasma compared to an encapsulated plasma sensitive device made without the plasma protective layer.

23. The encapsulated plasma sensitive device of claim 22 wherein the plasma protective layer is an inorganic coating.

24. The encapsulated plasma sensitive device of claim 23 wherein the inorganic coating is selected from LiF, MgF_2, CaF_2, AlO_x, SiO_2, or combinations thereof.

25. The encapsulated plasma sensitive device of claim 22 wherein the plasma protective layer is an organic coating.

26. The encapsulated plasma sensitive device of claim 25 wherein the organic coating is selected from aluminum tris 8-hydroxyquinoline, phthalocyanines, naphthalocyanines, polycyclic aromatics, or combinations thereof.

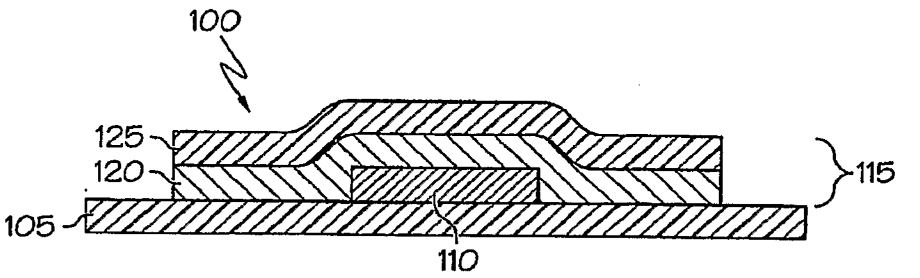


FIG. 1

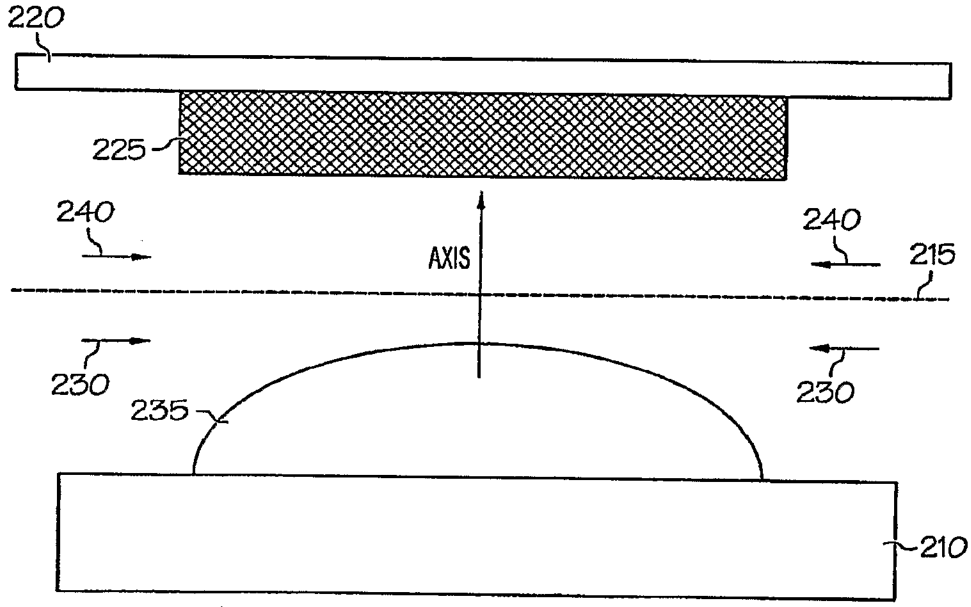


FIG. 2

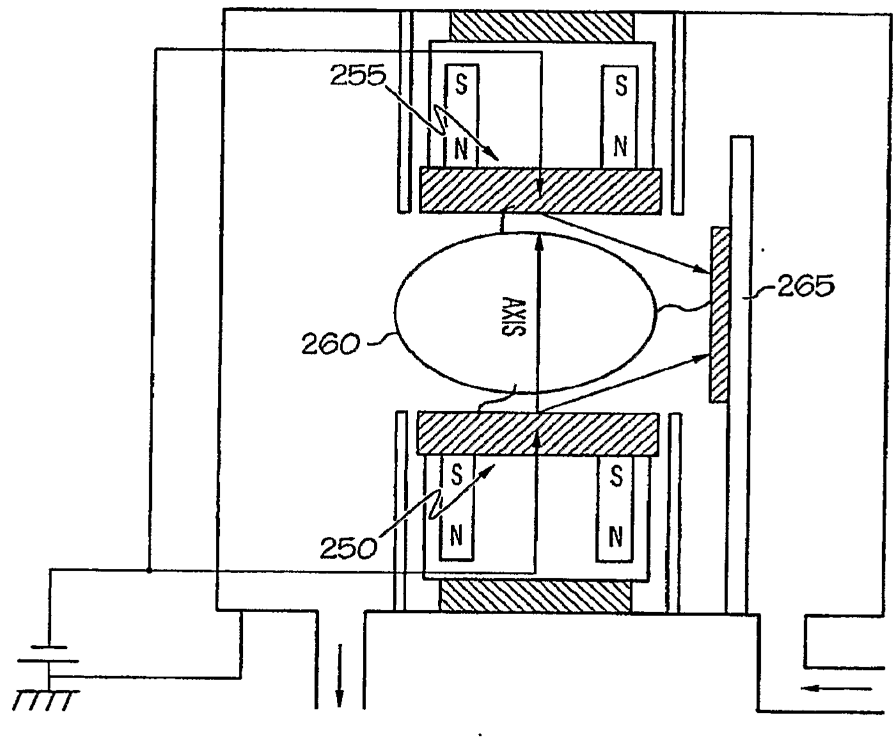
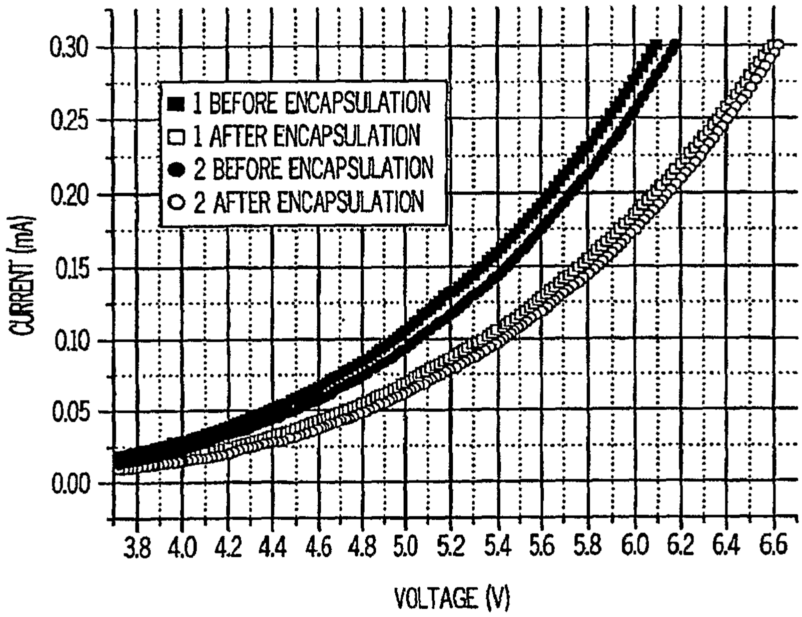
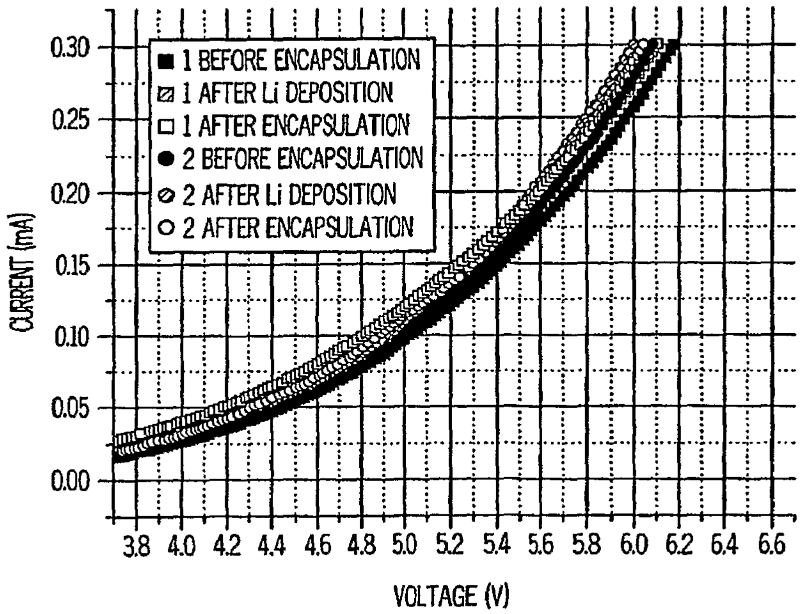


FIG. 3



1 BEFORE ENCAPSULATION
1 AFTER ENCAPSULATION
2 BEFORE ENCAPSULATION
2 AFTER ENCAPSULATION
CURRENT (mA)
0.30
0.25
0.20
0.15
0.10
0.05
0.00
3.8 4.0 4.2 4.4 4.6 4.8 5.0 5.2 5.4 5.6 5.8 6.0 6.2 6.4 6.6
VOLTAGE (V)

FIG. 4a



1 BEFORE ENCAPSULATION
1 AFTER Li DEPOSITION
1 AFTER ENCAPSULATION
2 BEFORE ENCAPSULATION
2 AFTER Li DEPOSITION
2 AFTER ENCAPSULATION
CURRENT (mA)
0.30
0.25
0.20
0.15
0.10
0.05
0.00
3.8 4.0 4.2 4.4 4.6 4.8 5.0 5.2 5.4 5.6 5.8 6.0 6.2 6.4 6.6
VOLTAGE (V)

FIG. 4b

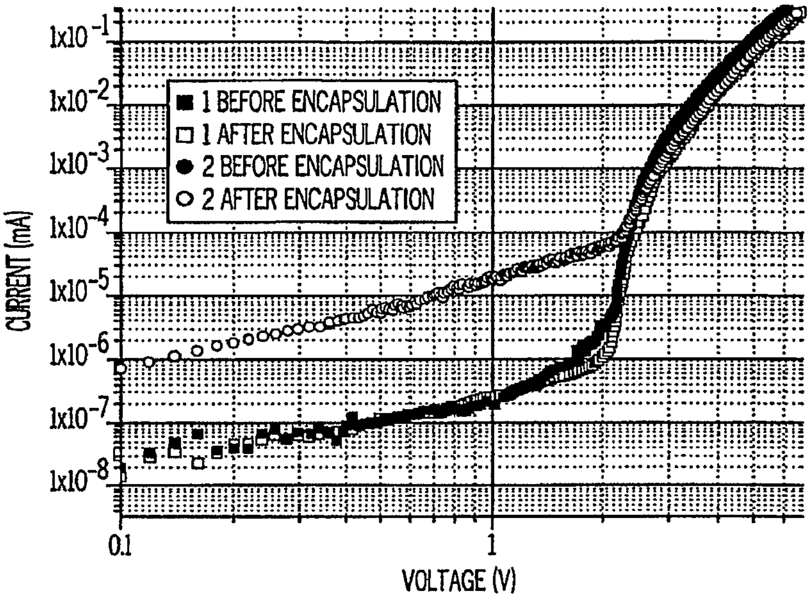

1 BEFORE ENCAPSULATION
1 AFTER ENCAPSULATION
2 BEFORE ENCAPSULATION
2 AFTER ENCAPSULATION
1x10^-1
1x10^-2
1x10^-3
1x10^-4
1x10^-5
1x10^-6
1x10^-7
1x10^-8
CURRENT (mA)
0.1
1
VOLTAGE (V)

FIG. 5a

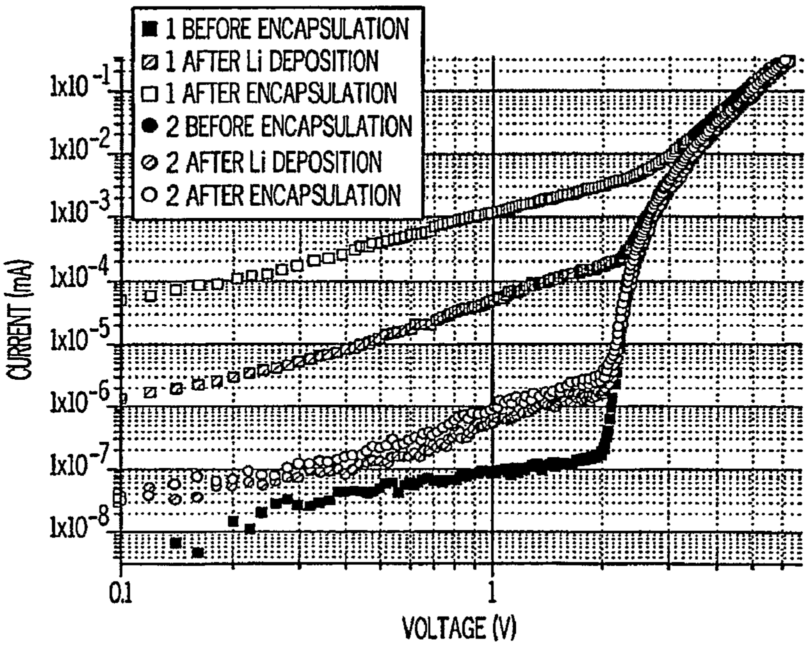
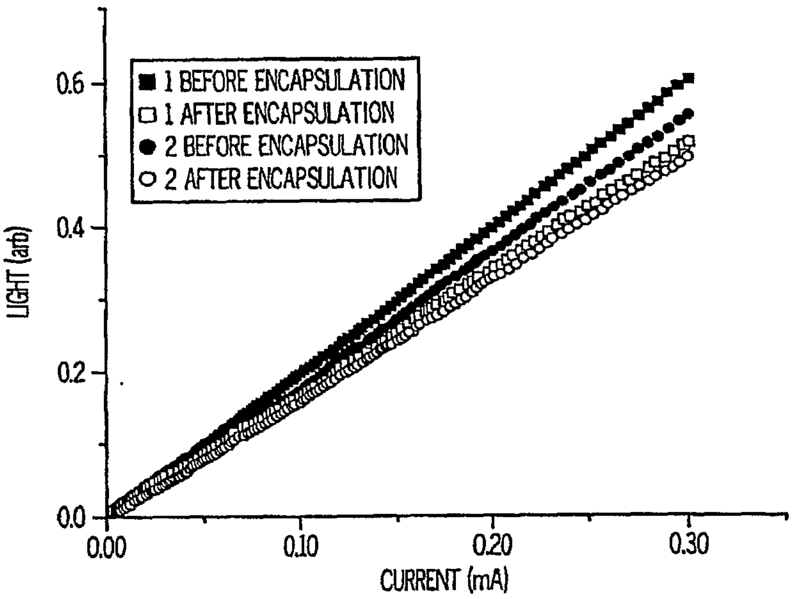
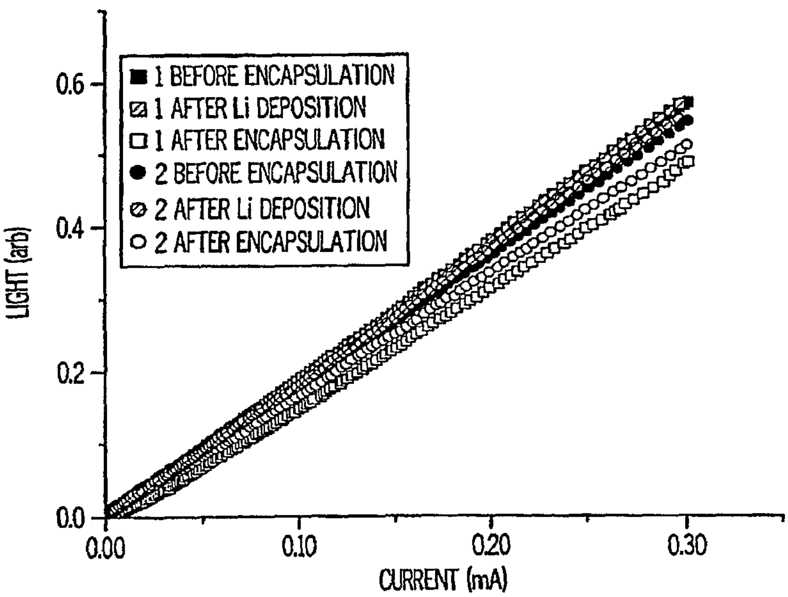

1 BEFORE ENCAPSULATION
1 AFTER Li DEPOSITION
1 AFTER ENCAPSULATION
2 BEFORE ENCAPSULATION
2 AFTER Li DEPOSITION
2 AFTER ENCAPSULATION
1x10^-1
1x10^-2
1x10^-3
1x10^-4
1x10^-5
1x10^-6
1x10^-7
1x10^-8
CURRENT (mA)
0.1
1
VOLTAGE (V)

FIG. 5b



1 BEFORE ENCAPSULATION
1 AFTER ENCAPSULATION
2 BEFORE ENCAPSULATION
2 AFTER ENCAPSULATION
LIGHT (arb)
0.0
0.2
0.4
0.6
0.00
0.10
0.20
0.30
CURRENT (mA)

FIG. 6a



1 BEFORE ENCAPSULATION
1 AFTER Li DEPOSITION
1 AFTER ENCAPSULATION
2 BEFORE ENCAPSULATION
2 AFTER Li DEPOSITION
2 AFTER ENCAPSULATION
LIGHT (arb)
0.0
0.2
0.4
0.6
0.00
0.10
0.20
0.30
CURRENT (mA)

FIG. 6b

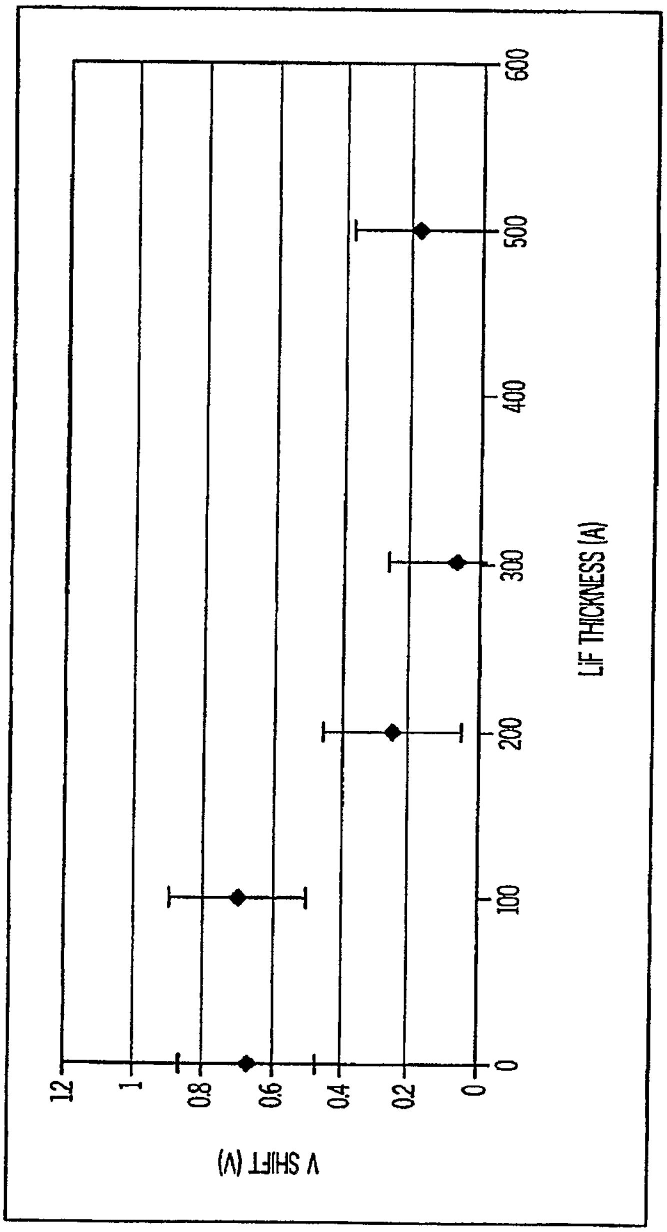

V SHIFT (V)
12
1
0.8
0.6
0.4
0.2
0
0
100
200
300
400
500
600
LIF THICKNESS (A)

FIG. 7

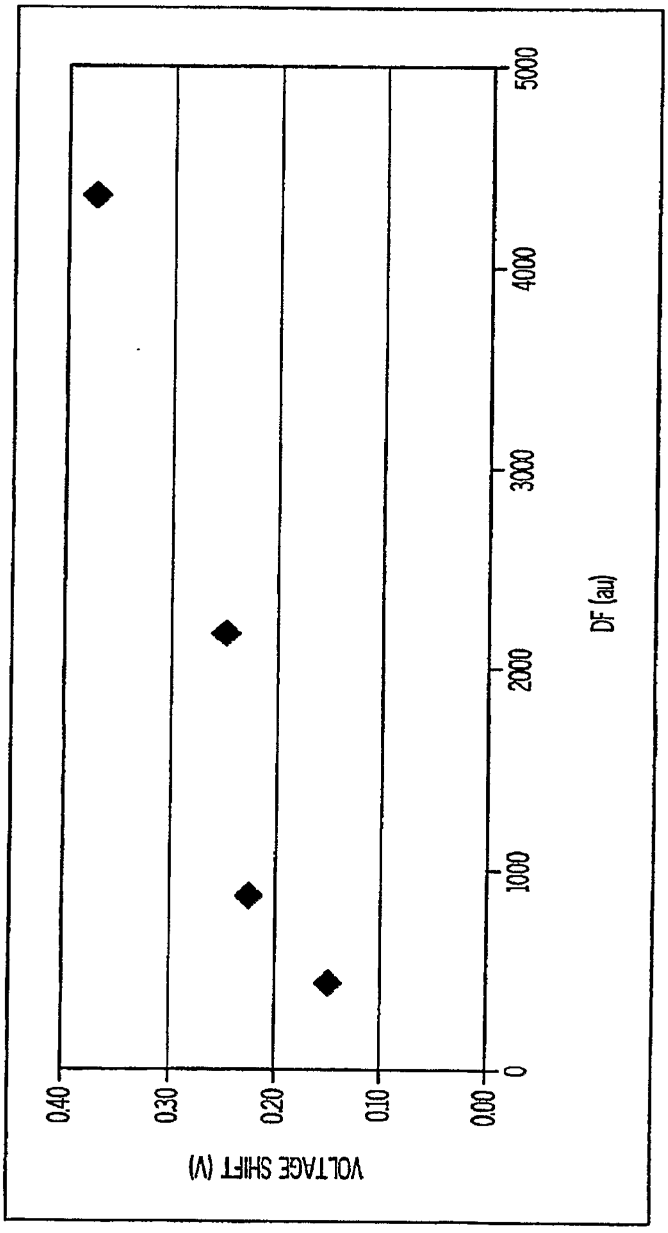

VOLTAGE SHIFT (V)
0.00
0.10
0.20
0.30
0.40
0
1000
2000
3000
4000
5000
DF (au)

FIG. 8

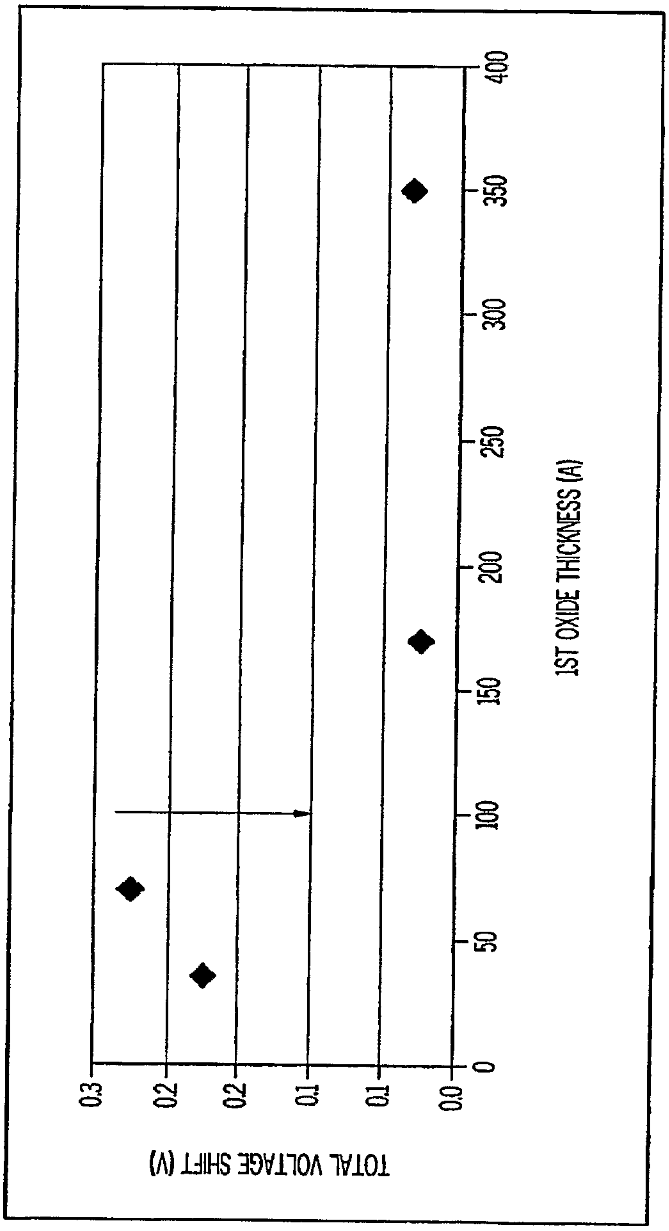

TOTAL VOLTAGE SHIFT (V)
0.3
0.2
0.2
0.1
0.1
0.0
0
50
100
150
200
250
300
350
400
1ST OXIDE THICKNESS (A)

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/010068

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L51/52 H01L51/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/239294 A1 (ROSENBLUM MARTIN P [US] ET AL) 27 October 2005 (2005-10-27) paragraphs [0014], [0016], [0053], [0084], [0088], [0094] - [0096], [0098], [0099] ----- -/--	1-4,7-9, 11,12, 14-25

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 October 2007	29/10/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	De Laere, Ann

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MORO L L ET AL: "Process and design of a multilayer thin film encapsulation of passive matrix OLED displays" PROCEEDINGS OF THE SPIE - THE INTERNATIONAL SOCIETY FOR OPTICAL ENGINEERING SPIE-INT. SOC. OPT. ENG USA, vol. 5214, no. 1, 2004, pages 83-93, XP002454383 ISSN: 0277-786X	1,19,22
Y	paragraph [3.3.1]	2-7, 9-11,13, 20-26
Y	HAN-KI KIM ET AL: "Magnetic field shape effect on electrical properties of TOLEDs in the deposition of ITO top cathode layer" ELECTROCHEMICAL AND SOLID-STATE LETTERS ELECTROCHEM. SOC USA, vol. 8, no. 12, December 2005 (2005-12), pages H103-H105, XP002454384 ISSN: 1099-0062 page H103, column 1	2,9-11, 13,20, 21,25,26
Y	US 2003/117068 A1 (FORREST STEPHEN [US] ET AL) 26 June 2003 (2003-06-26) paragraphs [0007], [0008], [0010], [0036], [0039], [0040], [0061]	2-7,9, 10,20, 22-26

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2007/010068

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		WO 03054960 A2	03-07-2003
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