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(54) **MOS-TYPE SEMICONDUCTOR DEVICE AND METHOD FOR MAKING SAME**

(76) Inventors: **Tatsuo Shimizu**, Ibaraki (JP); **Mieko Matsumura**, Ibaraki (JP); **Shigenobu Kimura**, Ibaraki (JP); **Yutaka Hirose**, Ibaraki (JP); **Yasuhiro Nishioka**, Ibaraki (JP)

Correspondence Address:
**TEXAS INSTRUMENTS INCORPORATED**
**P O BOX 655474, M/S 3999**
**DALLAS, TX 75265**

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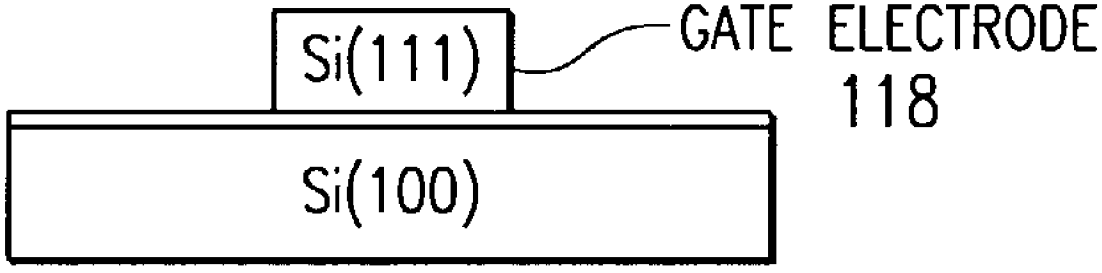
(52) **U.S. Cl.** ..... **257/627**

(57) **ABSTRACT**

An MOS-type semiconductor device comprises two semiconductors separated by an insulator. The two semiconductors comprise monocrystal semiconductors, each having a crystallographic orientation with respect to the insulator (or other crystallographic/semiconductor property) different to the crystallographic orientation (or other respective property) of the other semiconductor. This arrangement of crystallographic orientations (and other crystallographic/semiconductor properties) can yield reduced unintended electron tunneling or current leakage through the insulator vis a vis a semiconductor device in which such an arrangement is not used. Methods for forming the MOS-type semiconductor devices of the invention are also provided.



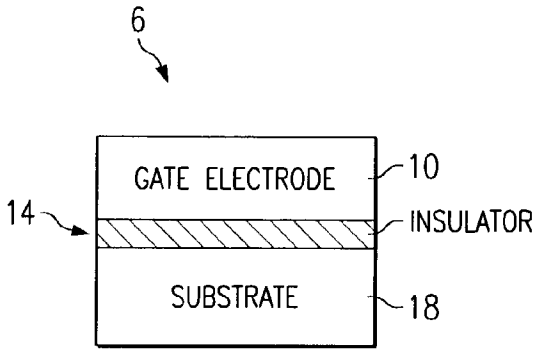



FIG. 1

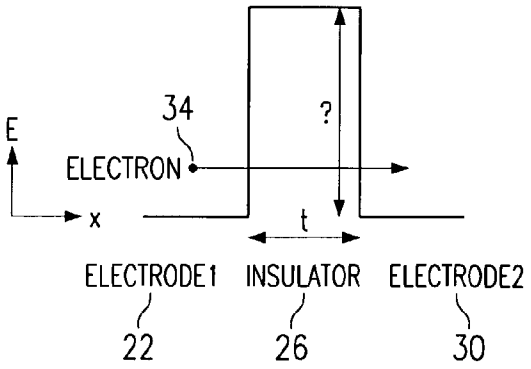



FIG. 3

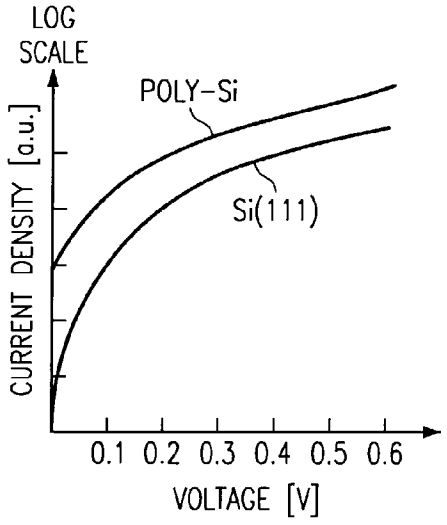



FIG. 2

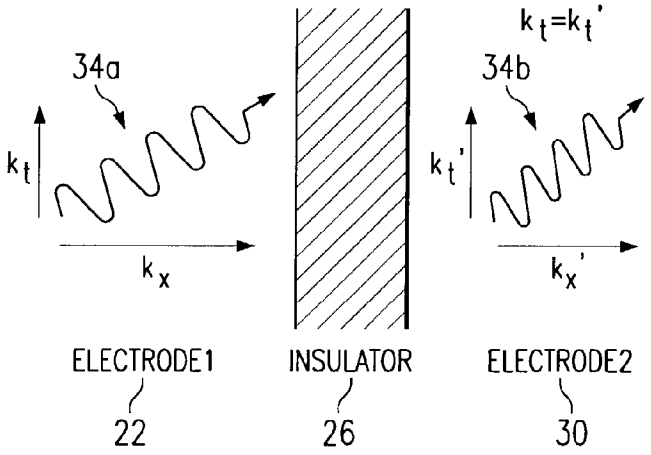



FIG. 4

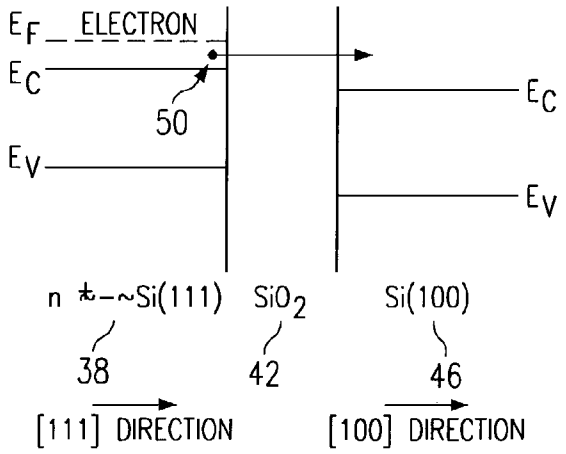



FIG. 5

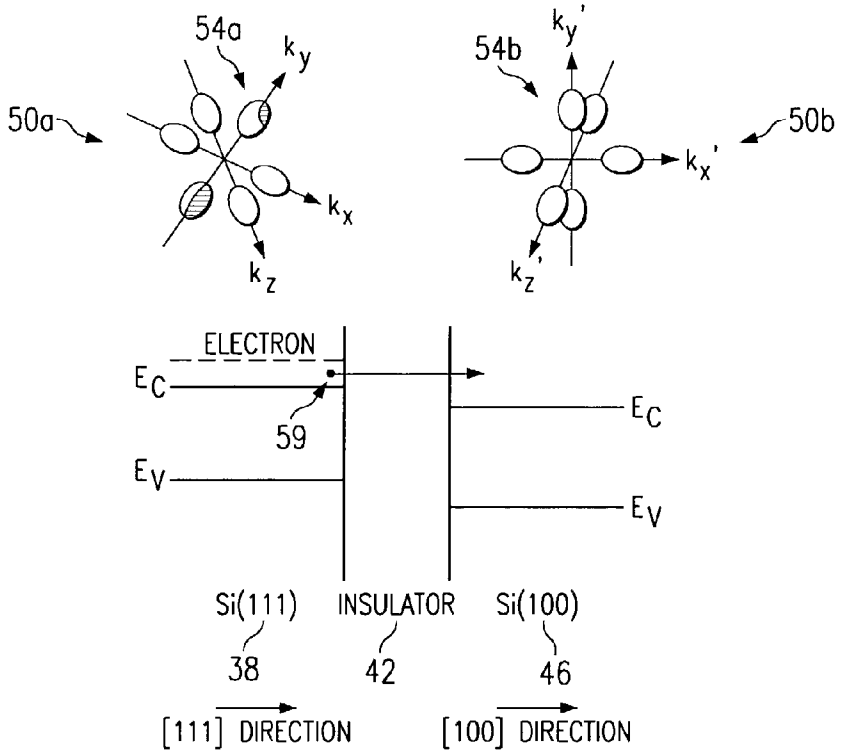

54a
$k_y$
50a
$k_x$
$k_z$
54b
$k_y'$
50b
$k_x'$
$k_z'$
ELECTRON
$E_C$
59
$E_V$
$E_C$
$E_V$
Si(111)
INSULATOR
Si(100)
38
42
46
[111] DIRECTION
[100] DIRECTION

*FIG. 6*

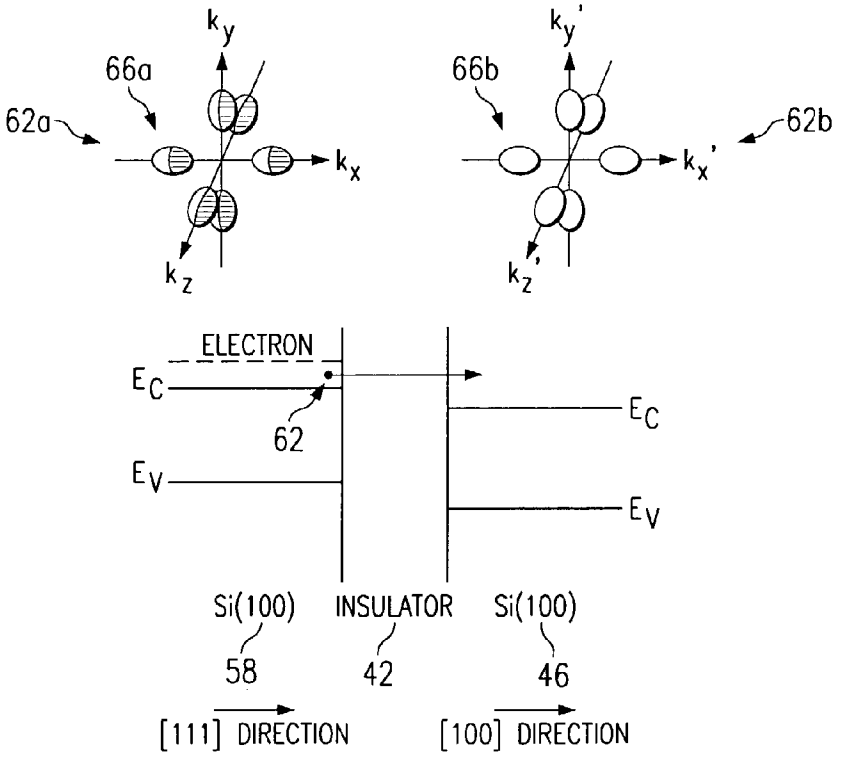

$k_y$
66a
62a
$k_x$
$k_z$
$k_y'$
66b
62b
$k_x'$
$k_z'$
ELECTRON
$E_C$
62
$E_V$
$E_C$
$E_V$
Si(100)
INSULATOR
Si(100)
58
42
46
[111] DIRECTION
[100] DIRECTION

*FIG. 7*

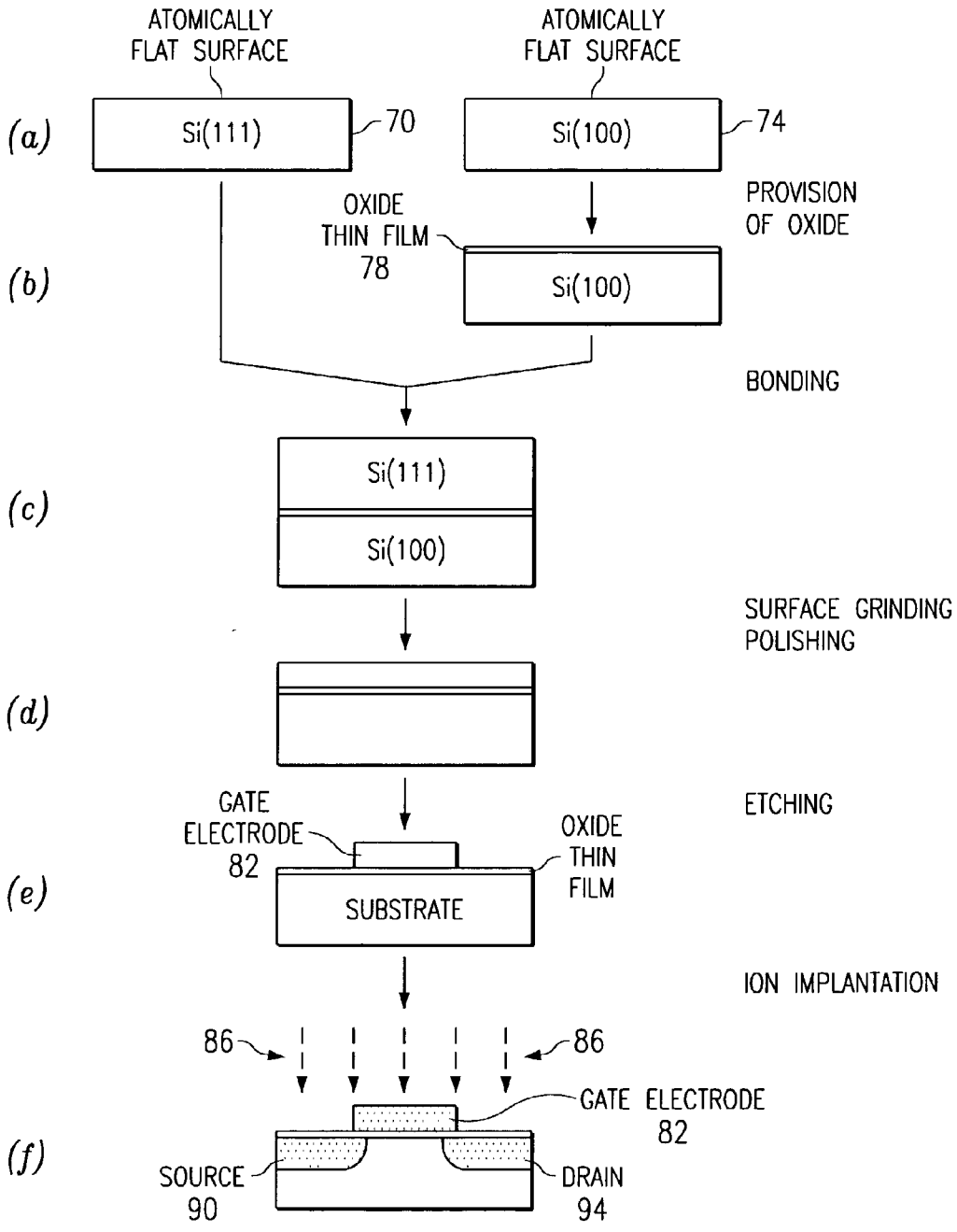

ATOMICALLY FLAT SURFACE
ATOMICALLY FLAT SURFACE
(a)
Si(111)
70
Si(100)
74
PROVISION OF OXIDE
OXIDE THIN FILM 78
(b)
Si(100)
BONDING
Si(111)
(c)
Si(100)
SURFACE GRINDING POLISHING
(d)
ETCHING
GATE ELECTRODE 82
OXIDE THIN FILM
(e)
SUBSTRATE
ION IMPLANTATION
86
86
GATE ELECTRODE 82
(f)
SOURCE 90
DRAIN 94

*FIG. 8*

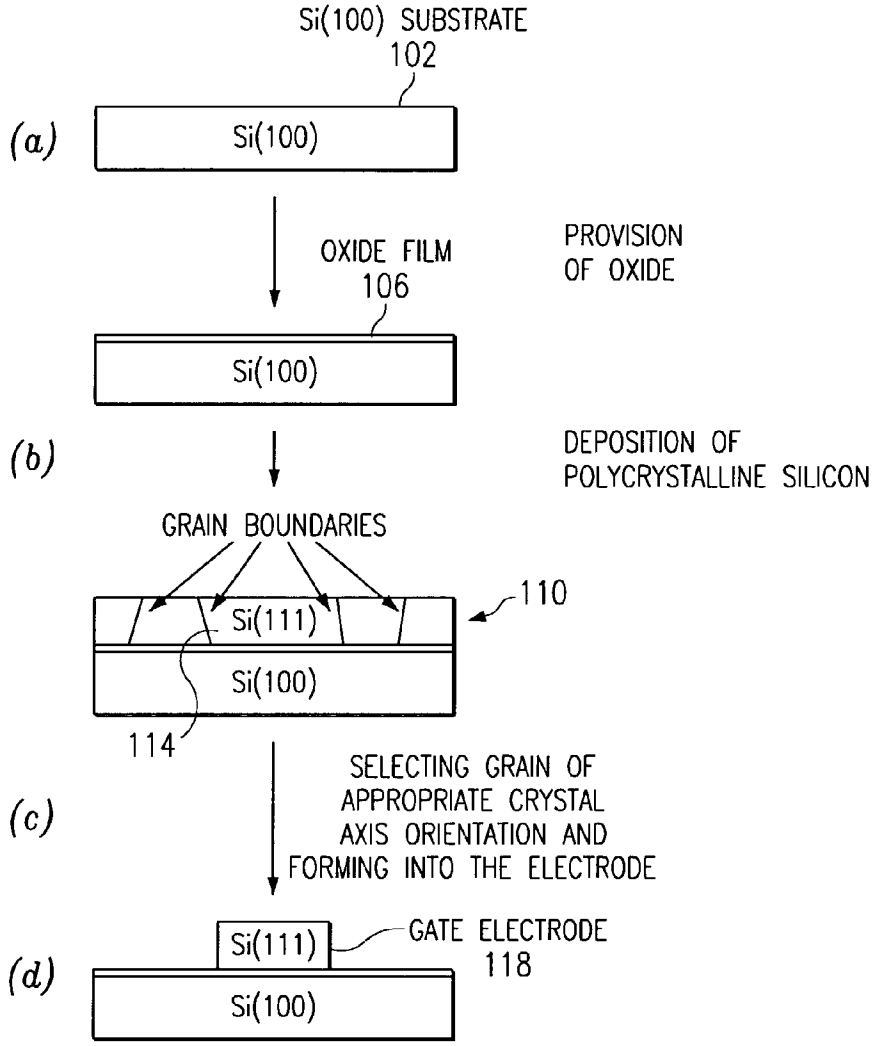

Si(100) SUBSTRATE
102
(a)
Si(100)
OXIDE FILM
106
PROVISION
OF OXIDE
Si(100)
(b)
DEPOSITION OF
POLYCRYSTALLINE SILICON
GRAIN BOUNDARIES
110
Si(111)
Si(100)
114
(c)
SELECTING GRAIN OF
APPROPRIATE CRYSTAL
AXIS ORIENTATION AND
FORMING INTO THE ELECTRODE
Si(111)
GATE ELECTRODE
118
(d)
Si(100)

FIG. 9

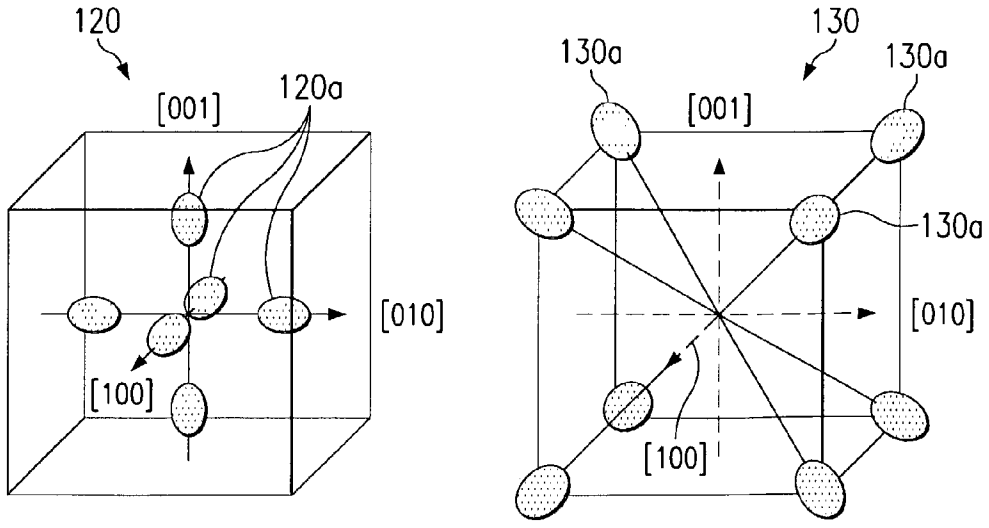

120
[001]
120a
[010]
[100]
130
130a
130a
[001]
130a
[010]
[100]

FIG. 10

# MOS-TYPE SEMICONDUCTOR DEVICE AND METHOD FOR MAKING SAME

## TECHNICAL FIELD OF THE INVENTION

[0001] This invention relates generally to the field of electronic devices, and more particularly to an improvement in MOS-type semiconductor devices and a method for making the same.

## BACKGROUND OF THE INVENTION

[0002] A Metal-Oxide-Semiconductor Field-Effect-Transistor ("MOSFET") is a four-terminal electronic semiconductor device and consists of: (1) a p- (or n) type semiconductor substrate into which two n+(or p+) regions, the source and the drain, are formed; and (2) a metal contact called a gate formed on top of a gate oxide. In integrated circuits ("ICs"), MOSFETS serve as switches. That is, they may switch current within the IC from the source into the drain "on" or "off" according to the potential difference between the gate and the substrate. The function played by the gate oxide is that of a dielectric layer in order to induce an inversion layer or a channel between the source and the drain, and an insulating layer that insulates the gate from the semiconductor.

[0003] It has been deemed desirable within ICs to scale-down, or miniaturize, the physical size of the IC. This may require, inter alia, scaling down of MOSFETS and other IC components, including scaling-down of the thickness of vertical layers out of which such components are formed. But in the case of gate oxide of a MOSFET, when the thickness of a gate oxide layer is reduced beyond a certain level (for instance, below the level of 2 or 3 nanonmeters (nm)), it has been found that certain difficulties may ensue. Specifically, the quantum electronic event known as electron tunneling (or leakage) may cause a current to pass through such very thin gate oxide layers at undesired times, thus possibly causing three serious problems: (1) an increase of the power consumption of the IC because of current flows in MOSFET even when the MOSFET is intended to be in its "off" state; (2) a decrease in the IC's operating speed because of unintended current flow; and (3) accelerated buildup of gate oxide defects as a result of higher-than-intended current density through the gate, resulting in premature dielectric breakdown of the oxide and thus of the IC.

[0004] Most of the previous attempts at solving the problem of tunneling-induced leakage through the gate oxide of a MOSFET concentrated upon increasing the dielectric constant of the gate insulating layer, i.e., obtaining the same desired charge storage capability with the use of a thicker dielectric film of increased dielectric constant, and hence reducing the tunneling current flowing through the gate.

[0005] In such prior art attempts to reduce tunneling current, three general methods for increasing the dielectric constant may be mentioned. First, incorporation of nitrogen into the $SiO_2$ film forming the gate oxide. Secondly, nitridation of the $SiO_2$ film. Thirdly, replacing the $SiO_2$ film with a completely different gate oxide material having a higher dielectric constant than that of $SiO_2$. Materials having such higher dielectric constants may include $Si_3N_4$, $TiO_2$, $Ta_2O_5$, and $Al_2O_3$.

[0006] In a crystal, the atoms that construct the crystal are positioned in such fashion that the atoms have periodicity along certain dimensional orientations. One can consider three basic vectors $a_1$, $a_2$, and $a_3$ as representing the three dimensions or axes within a crystal, and hence may use such vectors in describing the periodic regulation of atom positioning. These basic vectors may be referred to as primitive translation vectors. When one wishes to specify a particular orientation in a crystal, he can use the three primitive translation vectors and represent the particular orientation using a designation such as [xyz], (wherein x, y, and z are all integers), in which case the orientation is parallel to the vector $xa_1+ya_2+za_3$. Next, let us consider an origin point at a certain atom within a crystal. It is possible to consider a plane that crosses three atoms whose positions are represented by three vectors, $pa_1$, $qa_2$, and $ra_3$, respectively, from the origin point. In this case, we represent the plane in question by using the designation, (xyz), (wherein x, y and z are all integers). Here, the integers, x, y, and z, are chosen to make the absolute values of the integers as small as possible, and to make the ratio between x, y, and z to be the same as the ratio between 1/p, 1/q, and 1/r. We may use the designation, (xyz), for all the planes parallel to the plane thus considered.

[0007] Each of the above-described prior art approaches to reducing leakage current by increasing dielectric constant of the gate oxide may have some utility for reduction of tunneling and leakage current. However, in all of the above-described prior art methods for reducing leakage current, the crystalline orientation of the gate electrode has generally not been taken into account as another possible parameter whose variation could be employed for further reducing the leakage current.

## SUMMARY OF THE INVENTION

[0008] Accordingly, a need has arisen in the art for an improved MOS-type semiconductor device, in which the MOSFET has a gate oxide providing further-reduced current leakage/tunneling by virtue of judicious utilization of the crystallographic orientation (and/or other physical parameters that influence semiconducting properties) of the gate oxide layer. The present invention provides such a MOSFET and a method for making it that may substantially improve the leakage current properties of the MOSFET and hence the performance of an IC.

[0009] In accordance with the present invention, a MOSFET comprises a first semiconductor adjacent an insulating film, in turn adjacent a second semiconductor, wherein the first semiconductor and the second semiconductor are monocrystalline semiconductors and wherein the crystalline axes of the first and second semiconductors are arranged in different directions to each other. More specifically, the MOSFET of the present invention may be formed by selecting a first semiconductor whose [100] crystallographic direction is orthogonal with respect to the surface of the insulating film, and a second semiconductor whose [111] crystallographic direction is orthogonal with respect to the surface of the insulating film.

[0010] The technical advantages of the present invention include the provision of enhanced leakage current reduction within a MOSFET by appropriate selection not only of a gate insulator having high dielectric constant, but also of appropriate semiconductors on either side of the gate insulator layer so that tunneling current is also dependent upon (and reduced by) the crystallographic orientation of the gate electrode and the substrates.

[0011] Another technical advantage of the present invention is that it provides a number of possible particular combinations of constituent semiconductors for a MOSFET, wherein the semiconductors are chosen for advantageous crystallographic orientations (and/or other physical parameters that influence semiconducting properties) and leakage reduction. A further advantage of the present invention is that it provides fabrication methods for formation of MOSFETS wherein each of the semiconductors is assembled in proper crystallographic orientation with respect to the insulating oxide layer.

[0012] Other technical advantages of the present invention will be readily apparent to those skilled in the art from the following drawings, descriptions, and claims.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0013] For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings in which like reference numbers indicate like features and wherein:

[0014] **FIG. 1** illustrates a schematic cross-sectional view of a generic MOS structure within a field-effect-transistor.

[0015] **FIG. 2** illustrates exemplary voltage dependences for tunneling currents through insulator film based upon gate electrodes having different crystallographic orientations.

[0016] **FIG. 3** illustrates a generic schematic view of an energy barrier inserted between two electrodes.

[0017] **FIG. 4** illustrates a cross-sectional view of a generic structure comprising a first electrode adjacent an insulator film adjacent a second electrode, wherein an electron is illustrated (in wave form) as impinging upon (and subsequently being emitted on the opposite side of) the insulator film.

[0018] **FIG. 5** illustrates a generic schematic of the energy-band of a MOS structure of the type having crystallographic orientations Si(100)—$SiO_2$—Si(111).

[0019] **FIG. 6** illustrates a schematic cross-sectional view in connection with a generic electron-tunneling scenario from an Si(111) gate electrode to an Si(100) substrate through an insulating layer.

[0020] **FIG. 7** illustrates a schematic cross-sectional view in connection with a generic electron-tunneling scenario from an Si(100) gate electrode to an Si(100) substrate through an insulating layer.

[0021] **FIG. 8** illustrates a flow chart or schematic process diagram for a method of fabricating a MOSFET wherein the gate electrode and substrate are semiconductors of different crystallographic orientation.

[0022] **FIG. 9** illustrates a flow chart or schematic process diagram for a further method of fabricating a MOSFET wherein the gate electrode is formed out of a deposited polycrystalline layer.

[0023] **FIG. 10** provides a conceptual illustration of the respective carrier pockets of monocrystal silicon and monocrystal germanium in connection with an embodiment of the present invention in which monocrystal semiconductors of identical crystallographic orientation may be used to achieve reduced current leakage.

## DETAILED DESCRIPTION OF THE INVENTION

[0024] The present invention is best understood with reference to the drawings, which may be used for understanding (a) the generic configuration of any MOSFET structure (including both those of the prior art and those of the present invention); (b) the specific MOSFET structure of the present invention; and (c) a method for forming the MOSFET of the present invention.

[0025] **FIG. 1** illustrates a schematic cross-sectional view of a generic MOS structure within a field-effect-transistor **6**. Gate electrode **10** comprises a first semiconductor. This may be a semiconductor of any appropriate chosen type, for instance, silicon. Insulator **14** comprises a gate insulator. This may be a substantially non-conductive material of desired variety, such as, for instance, silicon dioxide. Substrate **18** comprises a second semiconductor. This again may be a semiconductor of desired type.

[0026] **FIG. 2** illustrates exemplary voltage dependences for tunneling currents through an insulator film based upon gate electrodes having different crystallographic orientations.

[0027] In accordance with the present invention, it is determined that the crystallographic orientation of the gate electrode may influence the tunneling current density through the insulator film. **FIG. 2** illustrates how this current density (as a function of applied voltage) may vary depending upon the chosen gate electrode semiconductor. In **FIG. 2**, the horizontal axis represents the applied voltage and the vertical axis represents the logarithmic current density. Curves are shown for the case in which the gate electrode comprises (a) monocrystal silicon having Si(111) crystallographic orientation (the lower curve) and (b) polycrystalline silicon (the upper curve).

[0028] (The difference between monocrystal silicon and polycrystalline ("polysilicon" or "poly-Si") may be understood as follows: Consider a bulk crystal that has a finite volume. When the bulk crystal maintains a periodicity of atomic spacing throughout its volume, the crystal may be referred to as a monocrystal. On the other hand, when the bulk crystal dose not maintain such periodicity throughout its volume, and consists of many small pieces of single crystals with different orientations, the crystal may be referred to as a poly-crystal).

[0029] In connection with **FIG. 2**, it can be observed that considerable variation of current density may result depending upon the crystalline orientation of the gate electrode. In the specific example of **FIG. 2**, the lower curve reflects a lower tunneling current density for orientated monocrystal Si(111) gate electrode. The polysilicon gate electrode (whose higher tunneling current density is shown in the upper curve of **FIG. 2**) has no single crystallographic orientation (that is, it comprises many grains of moncrystalline silicon in an aggregate, the crystallographic orientations of such individual monocrystal grains being randomly oriented with respect to those of other monocrystal grains, such that the polysilicon aggregate as a whole has no single crystallographic orientation).

[0030] **FIG. 3** illustrates a generic schematic view of an energy barrier inserted between two electrodes.

[0031] In **FIG. 3**, wherein the horizontal axis denotes translational distance and the vertical axis denotes a voltage potential, a first semiconductor electrode (indicated generally at **22**) is positioned directly adjacent insulator **26**, which in turn is positioned, on its other side, directly adjacent a second semiconductor electrode **30**. Electron **34** is shown as impinging upon insulator **26**, which has potential $\Phi$. In connection with **FIG. 3**, the first semiconductor electrode **22** may be viewed as either the substrate electrode or the gate electrode of a MOSFET, and likewise the second semiconductor electrode **30** may be viewed as, respectively, either the gate electrode or the substrate electrode of the MOSFET.

[0032] **FIG. 4** illustrates a cross-sectional view of a generic structure comprising a first semiconductor electrode **22** adjacent an insulator **26** adjacent a second semiconductor electrode **30**, wherein an electron (**34***a*, **34***b*) is illustrated (in wave form) as impinging upon (and subsequently being emitted on the opposite side of) the insulator film.

[0033] In **FIG. 4**, the electron is depicted as both an incident electron wave **34***a* and an emitted electron wave **34***b*. The incident electron wave **34***a* represents the electron as it is travelling through first semiconductor electrode **22** and impinging upon insulator **26**, and emitted electron wave **34***b* represents the electron as it is being emitted from the opposite side of insulator **26** and travelling from there through second semiconductor electrode **30**.

[0034] Incident electron wave **34***a* and emitted electron wave **34***b* are illustrated as resolved into their component wave number vectors $k_x$ and $k_x'$(the wave number vector components parallel to the direction of travel of electron **34**) and $k_t$ and $k_t'$ (the wave number vector components orthogonal to the plane of the interfaces between the insulator **26** and the first semiconductor electrode **22** and second semiconductor electrode **30**).

[0035] The wave number vector is used to represent an electron as a wave. It is proportional to the crystallographic momentum of the electron. Wave number vectors define a wave number vector space ("k-space"). That is, when considering the properties of an electron, we can treat electrons in a crystal by their wave number vectors rather than by their positions within the crystal. The space consisting of these wave number vectors is wave number vector space (k-space).

[0036] In connection with **FIG. 4**, it will be observed that the wave number vector component parallel to the plane of the interface between insulator **26** and first and second semiconductor electrodes **22** and **30** is the same in both incident electron wave **34***a* and emitted electron wave **34***b*. That is, $k_t=k_t'$.

[0037] **FIG. 5** illustrates a generic schematic of the energy-band of a MOS structure of the type having crystallographic orientations Si(111)—$SiO_2$—Si(100).

[0038] In **FIG. 5, a** first semiconductor electrode (indicated generally at **38**) comprises $n^+$-doped monocrystal silicon of the [111] crystallographic orientation ($n^+$-Si(111) and is positioned directly adjacent one side of an $SiO_2$ insulating layer **42**. Positioned directly adjacent the opposite side of insulating layer **42** is a second semiconductor electrode (indicated generally at **46**) comprising undoped monocrystal silicon of the [100] crystallographic orientation.

[0039] Electron **50** is depicted as approaching insulating layer **42** through first semiconductor electrode **38**. The designations $E_F$, $E_C$, and $E_V$ represent, respectively: the energy levels of Fermi energy (a critical energy threshold; most of the states whose potential is lower than the $E_F$ will be occupied by electrons, whereas most of the states whose potential is higher than the $E_F$ level will not be occupied by electrons); the energy level ($E_C$) of the conduction band; and the energy level ($E_V$) of the valence band.

[0040] **FIG. 6** illustrates a schematic cross-sectional view in connection with a generic electron tunneling scenario when the first semiconductor electrode **38** described above in connection with **FIG. 5** is a gate electrode in a MOSFET and the second semiconductor electrode **46** described above in connection with **FIG. 5** is a substrate electrode in a MOSFET, and electron **50** is impingement upon insulator **42**.

[0041] As a general characteristic of semiconductors, there exist valence bands and conduction bands within the semiconductor material. In the valence bands, holes (that is, vacancies of electrons), can move. In the conduction bands, electrons can move.

[0042] The states in k-space for electrons existing in the conduction band are known as "carrier pockets."

[0043] In connection with **FIG. 6**, electron **50** is represented, on the respective electron-impinging and electron-emitting sides of insulator **42**, by vectorized incident electron **50***a* and vectorized emitted electron **50***b* (wherein the vectorized representations of incident and emitted electron **50***a* and **50***b* are vectorized representations in k space).

[0044] The ellipsoid spheres **54***a* and **54***b* represent the respective carrier pockets (in the bottom of the Si conduction bands) for the respective incident and emitted electrons **50***a* and **50***b* in the respective first (gate) semiconductor electrode **38** and second (substrate) semiconductor electrode **46**.

[0045] With reference to incident electron **50***a*, only those electrons **50***a* whose specific wave vector component along a given axis lies within the shaded portion of the carrier pocket **54***a* for that wave vector component axis can contribute to the tunneling (or leakage) process. The specific wave vector components for incident electrons **50***a*, and the specific shaded portions of carrier pocket **54***a* corresponding to each such wave vector component, depend, inter alia, upon the crystallographic orientation of the first semiconductor electrode **38** with respect to insulator **42**.

[0046] **FIG. 7** illustrates a schematic cross-sectional view in connection with a generic electron tunneling scenario when (in contrast to the situation described in connection with **FIG. 6**), a first semiconductor electrode **58** is a gate electrode comprising not monocrystal Si(111) but rather monocrystal Si(100) in a MOSFET and the second semiconductor electrode **46** is, as in **FIG. 6, a** substrate electrode comprising Si(100) in a MOSFET, and electron **62** is impingement upon insulator **42**. That is, the configurations of **FIGS. 6 and 7** are analogous except that in **FIG. 6** the first semiconductor electrode **38** and the second semicon-

ductor electrode **46** (corresponding respectively to the gate electrode and substrate electrode) are of disparate crystallographic orientation, whereas in **FIG. 7** the first semiconductor **58** and the second semiconductor electrode **46** are of identical type and crystallographic orientation.

[**0047**] In connection with **FIG. 7**, electron **62** is represented, on the respective electron-impinging and electron-emitting sides of insulator **42**, by vectorized incident electron **62***a* and vectorized emitted electron **62***b* (wherein the vectorized representations of incident and emitted electron **62***a* and **62***b* are vectorized representations in k space). The ellipsoid spheres **66***a* and **66***b* represent the respective carrier pockets (in the bottom of the Si conduction bands) for the respective incident and emitted electrons **66***a* and **66***b* in the respective first (gate) semiconductor electrode **58** and second (substrate) semiconductor electrode **46** of **FIG. 7**.

[**0048**] Just as mentioned in connection with **FIG. 6**, only those electrons **62***a* whose specific wave vector component along a given axis lies within the shaded portion of the carrier pocket **66***a* for that wave vector component axis can contribute to the tunneling (or leakage) process in **FIG. 7**. It will be noted that the shaded portions of carrier packets **66***a* in **FIG. 7** have a total volume substantially greater than the volume represented by the shaded portions of carrier packets **54***a* of **FIG. 6**. This greater volume of shaded carrier packets denotes the fact that a greater amount of electron tunneling (and hence a greater leakage current) can occur in the MOSFET of **FIG. 7** than in the MOSFET of **FIG. 6**. This is so because, although all other properties of the respective MOSFETS of **FIGS. 6 and 7** may be assumed to be substantially identical, the crystallographic orientations of first semiconductor electrodes **38** and **58**, respectively, differ. It is thus found that choosing a first semiconductor electrode of crystallographic orientation different from that of the second semiconductor electrode **46** is more effective for preventing leakage current than choosing a first semiconductor electrode of the same crystallographic orientation as that of the second semiconductor electrode **46**.

[**0049**] In connection with **FIGS. 6 and 7**, the diminution of electron current leakage that is obtained by employing the structure of **FIG. 6** rather than the structure of **FIG. 7** may be explained as follows. The energy and the parallel momentum (with respect to the interface with insulator **42**) of an electron **50** or **62** must be conserved in the process of tunneling through the insulator **42** (which may be viewed as an energy barrier). The energy barrier of insulator **42** is the difference between the highest energy level that can be occupied in the first semiconductor electrode **38** or **58** and the conduction band level of the insulator **42**. The density of states in the first semiconductor electrode **38** or **58** in which an electron can tunnel through the insulator **42** and into the second semiconductor electrode **46** can be confined if the crystal axes of the respective first and second semiconductors are arranged so as to minimize the overlap between the carrier pocket of the first semiconductor electrode (**38** or **58**) and the carrier pocket of the second semiconductor electrode **46** (as projected to the momentum space of the first semiconductor electrode **38** or **58**). In such a configuration (as shown in **FIG. 6**), the density of states in the second semiconductor electrode **46** in which an electron can tunnel "back" through the insulator **42** into the first semiconductor electrode **38** is also confined. Thus, the leakage current between the first and second semiconductor electrodes (in either direction) can be reduced vis a vis the case, for example, in which the carrier pockets of the first and second semiconductors electrode (e.g., **66***a* and **66***b*) exactly overlap in momentum space, as in the scenario depicted in connection with **FIG. 7**, wherein the first semiconductor electrode **58** is of crystallographic orientation (with respect to insulator **42**) identical to that of second semiconductor electrode **46**.

[**0050**] **FIG. 8** illustrates a flow chart or schematic process diagram for a method of fabricating a MOSFET wherein the gate electrode and substrate are semiconductors of different crystallographic orientation.

[**0051**] The method illustrated in connection with **FIG. 8** is an application of wafer bonding technology known and used generally in connection with Silicon On Insulator (SOI) materials. It is illustrated in connection with an exemplary case in which it is desired to form a gate electrode out of a quantity of monocrystal silicon of [111] orientation upon a substrate of monocrystal silicon of [100] orientation, the gate electrode and the substrate electrode being separated by oxide thin film, but the process is more generally applicable to gate electrodes and substrates of other chosen materials and other particular crystallographic orientations, so long as the crystallographic orientations of the gate electrode and substrate electrode are different one from the other.

[**0052**] In connection with **FIG. 8**, gate electrode piece **70** comprises a quantity of monocrystal Si(111) and substrate electrode piece **74** comprises a quantity of monocrystal Si(111). In step (a) of the process illustrated in **FIG. 8**, gate electrode piece **70** and substrate electrode piece **74** are prepared so that at least one contacting surface is atomically flat. It is possible to create an atomically-flat surface upon gate electrode piece **70** by treating it in an $NH_4F$ solution, and to create an atomically flat surface upon surface electrode piece **74** by annealing it in an $H_2$ atmosphere.

[**0053**] In step (b), an oxide thin film (as, for instance, a thin film of $SiO_2$) is formed upon the atomically-flat surface of substrate electrode piece **74** by (a) conventional thin film deposition techniques or (b) thermal oxidation processing performed upon the material of the substrate itself.

[**0054**] In step (c), the atomically-flat surface of the gate electrode piece **70** is bonded to the oxide thin film **78** formed on top of the atomically flat surface of substrate electrode piece **74**. The bond between gate electrode piece **70** and the thin oxide film **78** (and hence the substrate electrode piece **74**) may be completed by annealing the bonded pieces in high ambient temperature. Thus, the crystallographic orientation of gate electrode piece **70** with respect to oxide thin film **78** is orthogonal when compared to the crystallographic orientation of substrate electrode piece **74** with respect to the opposite side of oxide thin film **78**.

[**0055**] In step (d), gate electrode piece **70** is ground and polished (on the side opposite the side previously bonded to oxide thin film **78**) so as to reduce the thickness of gate electrode piece **70** to the required thickness for formation of a gate electrode as required within the particular MOSFET and IC.

[**0056**] In step (e), gate electrode piece **70** is etched (using known techniques for photolithographic etching within semiconductors) to form gate electrode **82**.

[0057] In step (f), the conductivity of certain regions of the aggregate gate electrode-substrate electrode piece is altered by known processes (e.g., ion implantation) in order to dope the gate electrode **82** and portions of the substrate electrode piece **74** with dopant (indicated generally at **86**) of chosen conductive properties to form doped gate electrode **82**, as well as source region **90** and drain region **94** within substrate electrode piece **74**. Following this doping step, the entire assembly (gate electrode **86** bonded to oxide thin film **78** bonded to substrate electrode piece **74**) is annealed for activation.

[0058] **FIG. 9** illustrates an exemplary flow chart or schematic process diagram for a further method of fabricating a MOSFET wherein the gate electrode is formed out of a deposited polycrystalline layer. In step (a), monocrystal Si(100) semiconductor substrate **102** is provided, having a relatively flat upper surface.

[0059] In step (b), oxide film **106** is provided on the upper surface of the semiconductor substrate **102**. (Oxide film **106** may be provided by, for example, thin layer deposition processes known in the art or by thermal oxidation processing of the substrate itself).

[0060] In step (c), a polycrystalline silicon layer **110** is deposited on top of oxide film **106**. Polycrystalline silicon layer **110** contains an aggregate of individual monocrystal silicon crystal grains, each having a distinct crystallographic orientation, and each separated by a grain boundary. For example, monocrystal grain **114** is a monocrystal Si(111) crystal within the polycrystalline silicon layer **110**.

[0061] In step (d), one of the particular monocrystal grains is identified and selected for use—in this example, it could be selected only if (for instance) monocrystal grain **114** were determined to be a Si(111) grain having [111] plane parallel to the surface of substrate **102**. Once such particular monocrystal grain is identified and selected, the other grains in polycrystalline silicon layer **110** are removed, and monocrystal grain **114** is shaped, by etching or other processes, in order to form monocrystal grain **114** into gate electrode **118**. Doping can then be performed for formation of the necessary conductivity paths for the MOSFET. Because gate electrode **118** consists of monocrystal silicon with crystallographic orientation orthogonal to that of monocrystal substrate **102**, the fabrication method just described in conjunction with **FIG. 9** provides an additional alternative, employing polycrystalline silicon as one building block, for forming a MOSFET achieving the advantages of the present invention.

[0062] Further to the discussion set forth regarding FIGS. **3-9**, and to the general advantages provided by the present invention and its use (and method for forming) of gate electrodes and substrate electrodes having crystallographic orientations (as evaluated with reference to the insulator layer separating the electrodes) that differ one from the other, a brief discussion of the likely bases for, and extent of, these advantages, follows herewith.

[0063] The gate-voltage vs. channel-current behavior of MOSFETs is affected by the selection of crystallographic planes of substrate, because the speed of carriers (electrons and/or holes) travelling through channel region is dictated in part or whole by the carrier mobility (the ability of electron and/or hole to move in silicon crystal). For most silicon MOS transistors, silicon substrates (wafers) whose surfaces are parallel to Si(100) planes have in the past been used because the carrier mobility along the Si(100) plane is large compared to other crystallographic planes.

[0064] The additional leakage current reduction gained by applying the present invention to MOS-type structures may be theoretically calculated to show how the leakage current between gate electrode and substrate can be reduced when the crystallographic axes of gate electrode and substrate are arranged in directions different to each other.

[0065] Let us consider a process in which an electron **34**, having a certain energy, tunnels through a barrier (e.g., insulator **26** shown in **FIG. 4**), whose potential $\Phi$ is higher than the energy of the electron, and travels from a first semiconductor electrode **22** to a second semiconductor electrode **30**. As shown in **FIG. 4**, the physics of the movement of the electron can be separated into two different components, one a component parallel to the x-axis, and the other a component orthogonal to the x-axis.

[0066] The momentum component $k_t$, whose direction is orthogonal to the x-axis, does not change if and when electron **34** tunnels through insulator **26**. The probability, T, of an electron **34** tunneling through the potential barrier (i.e., insulator **26**) is decided by the energy of electron **34**, the barrier height, $\Phi$, and the barrier thickness, t. The probability, T, is a function of geometry of the device.

[0067] The current density J caused by electrons **34** tunneling through the insulator **26** from the first semiconductor electrode **22** to the second semiconductor electrode **30** is expressed by the following equation:

$$J \iiint d^2k_t dk_x \cdot v_x \cdot T \cdot f_1(E) \cdot D_2(E) \cdot [1-f_2(E)] \qquad \text{EQUATION 1}$$

[0068] in which $K_x$ is 1D wave vector parallel to the tunneling direction, $K_t$ is 2D wave vector in a plane perpendicular to the tunneling direction, $v_x$ is the velocity of electron **34** along the x-axis in the first semiconductor electrode **22**, E is the energy of electron **34** decided by the magnitudes of $k_t$ and $k_x$, $f_1(E)$ is the probability that a state having the energy, E, will be occupied by an electron in the first semiconductor electrode **22**, $D_2(E)$ is the density of state having the energy, E, in the second semiconductor electrode **30**, and $[1-f_2(E)]$ is the probability that a state having the energy, E, will not be occupied by any electron.

[0069] The integral of EQUATION 1 is done in the momentum space, ($k_x$, $k_t$), of first semiconductor electrode **22**. Considering the aforementioned principle of the momentum conservation of $k_t$ as between its pre-tunneling and post-tunneling states, the integral in EQUATION 1 becomes very small in the case when the crystallographic axes of first semiconductor electrode **22** and second semiconductor electrode **30** are arranged in directions different (with respect to the plane of the electrodes' respective interfaces with insulator **26**) to each other.

[0070] Having described the basic configuration of the MOSFETs of the present invention, having given exemplary descriptions of specific gate electrodes and substrate electrodes that might be chosen, and having described a method for fabricating such MOSFETS, certain further examples may be given of advantageous combinations of gate electrodes, insulators, and substrate electrodes in accordance with the present invention. Examples of such additional combinations include (but are not limited to):

[0071] (a) MOSFETs comprising an Si(111) substrate and a single-crystal silicon gate electrode (plus a conventional insulator layer separating substrate and gate electrode), in which the [100] direction of the gate electrode is orthogonal to the substrate surface;

[0072] (b) MOSFETs comprising Si(100) substrate and a single-crystal silicon gate electrode, in which the [111] direction of the gate electrode is orthogonal to the substrate surface, and the gate electrode is grown on top of an arsenic insulating layer on top of the silicon substrate;

[0073] (c) MOSFETs comprising an Si(100) substrate and a single-crystal silicon gate electrode, in which the [111] direction of the gate electrode is vertical to the substrate surface, and the gate electrode is grown on top of a tantalum oxide insulating layer on top of the silicon substrate;

[0074] (d) MOSFETs comprising a Si(100) substrate and a single-crystal germanium gate electrode in which the [100] direction of the gate electrode is orthogonal to the substrate surface and a conventional oxide insulator is employed to separate the electrodes; and

[0075] (e) MOSFETs comprising Ge(100) substrate and a single-crystal silicon gate electrode in which the [100] direction of the gate electrode is vertical to the substrate surface and a conventional oxide insulator is employed to separate the electrodes.

[0076] While most of the above examples of embodiments of the present invention illustrate it in connection with the advantageous situating of a substrate semiconductor and a gate electrode semiconductor with a crystallographic orientation orthogonal to that of the substrate (with both gate and substrate semiconductors in most cases comprising monocrystal silicon), this invention also includes embodiments in which the gate electrode semiconductor and substrate semiconductor have the identical monocrystal crystallographic orientation (with respect to the oxide insulating layer), so long as the gate electrode semiconductor and the substrate semiconductor are otherwise sufficiently different types of semiconductor to achieve the benefits of this invention. That is, even if gate and substrate share the same crystallographic orientation, they may still have sufficiently different semiconductor properties (which are still related, in part, to the specific crystallographic properties of the respective semiconductors) that leakage is reduced.

[0077] **FIG. 10** provides a conceptual illustration of the respective carrier pockets of monocrystal silicon and monocrystal germanium in connection with an embodiment of the present invention in which monocrystal semiconductors of identical crystallographic orientation may be used to achieve reduced current leakage. Indicated generally is silicon crystal **120**. It has carrier pockets **120***a*. Also indicated generally is germanium crystal **130**. It has carrier pockets **130***a*. Although both silicon crystal **120** and germanium crystal **130** are monocrystal, and both share homologous crystallographic axes, a reduced-leakage MOSFET might still be formed from a substrate comprising such monocrystal silicon and a gate electrode comprising such monocrystal germanium (or vice versa) even if the two semiconductors were joined with non-opposed crystallographic orientations. This is so because, as shown in **FIG. 10**, the shapes and positions of the carrier pockets (**120***a*, **130***a*) of the respective substrate and gate electrode semiconductors (**120**, **130***a*) are completely different and thus the likelihood of leakage is reduced, similar to in the earlier-described embodiments in which carrier pockets are made not to overlap by providing opposed crystallographic orientations for substrate and gate electrode.

[0078] Thus, because germanium monocrystals are different from silicon monocrystals (whereas two different silicon monocrystals share more properties in common), the exemplary silicon:germanium MOSFET could provide reduced leakage even though the substrate and gate semiconductors have non-opposed crystallographic directions, whereas a silicon:silicon arrangement of substrate and gate with non-opposed crystallographic directions would not reduce leakage in such fashion, given the high degree of overlap in substrate and gate electrode carrier pockets. Carrier pocket shape and position are influenced in part by crystallographic structure and other semiconductor properties. Accordingly, it is seen that providing orthogonal crystallographic orientation in gate electrodes and substrate is not the only way to reduce leakage in accordance with this invention; rather, any combination and situating of gate electrode semiconductor and substrate semiconductor in which the two semiconductors have sufficiently-different semiconductor properties (as influenced by crystallographic structure, etc.) may potentially provide reduced leakage.

[0079] Although the present invention has been described herein in detail, it should be understood that various changes, substitutions, and alterations could be made hereto without departing from the spirit and scope of the present invention as defined by the appended claims.

What is claimed is:

**1**. An MOS-type semiconductor device comprising a first semiconductor, an insulator adjacent said first semiconductor, and a second semiconductor, wherein said first and second semiconductors are monocrystalline semiconductors having crystallographic axes and wherein the crystallographic axes of said first and second semiconductors are arranged in directions different to each other.

**2**. The MOS-type semiconductor device of claim 1, wherein said first and second semiconductors comprise silicon electrodes.

**3**. The MOS-type semiconductor device of claim 1 wherein said insulator comprises an oxide thin layer.

**4**. The MOS-type semiconductor of claim 2, wherein said insulator comprises an oxide thin layer.

**5**. The MOS-type semiconductor of claim 1, wherein said insulator comprises an insulator formed by oxidation of a portion of said first semiconductor and wherein said second semiconductor has an atomically-flat surface bonded to said insulator.

**6**. The MOS-type semiconductor of claim 1, wherein said first semiconductor comprises an integrated circuit substrate and said second semiconductor comprises a gate electrode.

**7**. The MOS-type semiconductor of claim 1, wherein the [100] crystallographic orientation of said first semiconductor is orthogonal to a plane defined by the junction between said first semiconductor and said insulator and the [111] crystallographic orientation of said second semiconductor is orthogonal to the same plane.

**8**. The MOS-type semiconductor of claim 7, wherein said first and second semiconductors comprise silicon electrodes.

**9**. The MOS-type semiconductor device of claim 8, wherein said insulator comprises an oxide thin layer.

**10**. The MOS-type semiconductor of claim 8, wherein said insulator comprises an insulator formed by oxidation of a portion of said first semiconductor and wherein said second semiconductor has an atomically-flat surface bonded to said insulator.

**11**. The MOS-type semiconductor of claim 8, wherein said first semiconductor comprises an integrated circuit substrate and said second semiconductor comprises a gate electrode.

**12**. The MOS-type semiconductor of claim 8, wherein the conductivity of at least a portion of said first semiconductor and said second semiconductor are altered by an added dopant.

**13**. The MOS-type semiconductor of claim 1, wherein said second semiconductor comprises germanium.

**14**. The MOS-type semiconductor of claim 1, wherein said insulator comprises tantalum oxide.

**15**. An MOS-type semiconductor device comprising a gate electrode for electrically coupling a transistor source and drain in an integrated circuit substrate in conjunction with an insulator, wherein said gate electrode has crystallographic properties distinct from respective crystallographic properties of said substrate, whereby electron tunneling through said insulator is reduced as compared to that which would occur if said gate electrode had crystallographic properties identical to the respective crystallographic properties of said substrate.

**16**. The MOS-type semiconductor device of claim 15, wherein said gate electrode has a [111] crystallographic direction that is orthogonal to the crystallographic orientation of an opposing surface of said substrate.

**17**. The MOS-type semiconductor of claim 15, wherein said gate electrode and said substrate both share a same crystallographic orientation but are formed of different chemical substances.

**18**. A method for forming an MOS-type semiconductor device comprising the steps of:

(a) selecting first and second monocrystal semiconductor pieces (said pieces having crystallographic axes and wherein the crystallographic axes of said first and second pieces are arranged in directions different to each other) and providing each of said pieces with an atomically-flat surface;

(b) providing an oxide layer on said atomically-flat surface of said second piece;

(c) bonding said atomically-flat surface of said first piece to said oxide layer on said second piece;

(d) performing processing upon said first piece to form it into an electrode; and

(e) doping at least a portion of said first and second pieces.

**19**. The method of claim 18, wherein said first piece comprises monocrystal silicon of [111] crystallographic orientation and said second piece comprises monocrystal silicon of [100] orientation and wherein the step of performing processing upon said first piece to form it into an electrode comprises:

(1) grinding and polishing a surface of said first piece opposite said atomically-flat surface to reduce said first piece to a desired thickness; and

(2) etching said first piece.

**20**. The method of claim 18 wherein the step of providing an oxide layer on said atomically-flat surface of said second piece comprises conducting oxidation upon said atomically-flat surface of said second piece.

**21**. A method for forming an MOS-type semiconductor device comprising the steps of:

(a) selecting a first monocrystal semiconductor piece (said piece having crystallographic axes and a substantially-flat surface);

(b) providing an oxide layer on said substantially-flat surface of said first piece;

(c) providing a layer comprising polycrystalline semiconductor material on said oxide layer, said polycrystalline semiconductor material layer comprising a plurality of bounded grains of monocrystal semiconductor material;

(d) selecting at least one of said bounded grains of monocrystal semiconductor material;

(e) performing processing upon said polycrystalline semiconductor material layer to:

(1) remove substantially all of said polycrystalline semiconductor material layer but for said selected bounded grain of monocrystal semiconductor material; and

(2) form said selected bounded grain of monocrystal semiconductor material into an electrode; and

(f) doping at least a portion of said first and second pieces.

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