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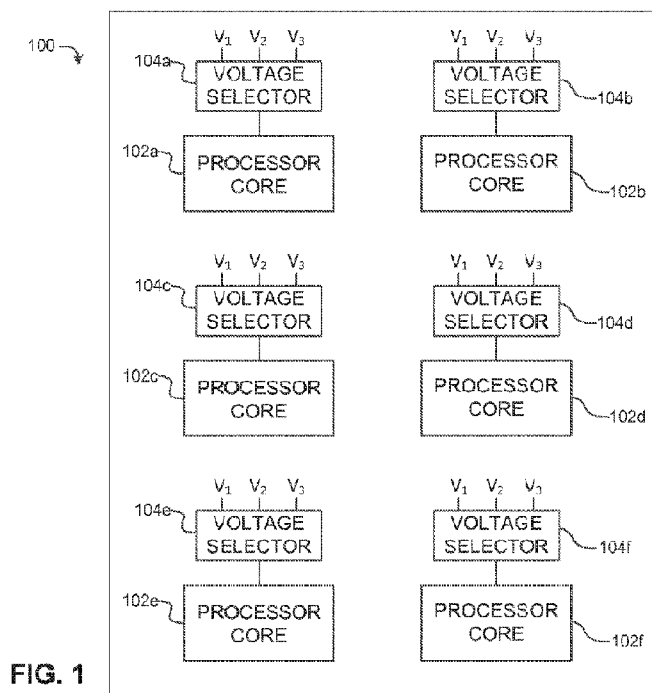


FIG. 1

(57) Abstract: Example implementations relate to coupling processor cores to various voltage rails. In example implementations, each of a plurality of voltage selectors may be coupled to a respective one of a plurality of processor cores. Each of the plurality of voltage selectors may be capable of coupling the respective one of the plurality of processor cores to any of a plurality of voltage rails used to power the plurality of processor cores.

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VOLTAGE SELECTORS COUPLED TO PROCESSOR CORES

BACKGROUND

[0001] Processor cores in an electronic device may perform various operations. Different processor cores may use different supply voltages. Dynamic power consumption of a processor core may be proportional to the square of the supply voltage of the processor core.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The following detailed description references the drawings, wherein:

[0003] FIG. 1 is a block diagram of an example device in which processor cores may be coupled to various voltage rails;

[0004] FIG. 2 is a block diagram of an example device that enables grouping of processor cores into clusters;

[0005] FIG. 3 is a block diagram of an example data structure that may be used to store characteristics of a cluster of processor cores;

[0006] FIG. 4 is a block diagram of an example device that includes a machine-readable storage medium encoded with instructions to enable coupling of processor cores to various voltage rails;

[0007] FIG. 5 is a block diagram of an example device that includes a machine-readable storage medium encoded with instructions to enable grouping of processor cores into clusters;

[0008] FIG. 6 is a flowchart of an example method for selecting voltage rails to couple to various processor cores;

[0009] FIG. 7 is a flowchart of an example method for changing a voltage rail coupled to a processor core; and

[0010] FIG. 8 is a flowchart of an example method for grouping processor cores into clusters.

DETAILED DESCRIPTION

[0011] As transistor devices get smaller, they become more susceptible to imperfections in the manufacturing process. With transistor channels spanning a few atoms wide, variation in the number of atoms applied as part of the doping

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process may affect the switching speed of transistors as a function of the supply voltage. Thus, within the same chip, design-identical processor cores may achieve a targeted operating frequency at different voltage levels. To deal with this variation, the supply voltage may be padded to account for the worst-case variation. However, such an approach may waste energy because various processor cores may be running at voltages higher than their minimum operating voltage. In addition, running various regions of the chip at different voltages may not adequately compensate for the variation because physically adjacent processor cores may have different process variation profiles.

[0012] In light of the above, the present disclosure provides for the capability of coupling any processor core on a chip to any voltage rail available on the chip, such that each processor core on the chip may be coupled to the voltage rail closest to, and greater than, its minimum operating voltage. Thus, a processor core may be coupled to any voltage rail regardless of the physical location of the processor core on the chip. Such a capability may allow physically adjacent processor cores to be coupled to different voltage rails, and may reduce wasted energy.

[0013] Referring now to the figures, FIG. 1 is a block diagram of an example device 100 in which processor cores may be coupled to various voltage rails. Device 100 may be an electronic user device, such as a notebook computer, a desktop computer, a workstation, a tablet computing device, a mobile phone, or an electronic book reader. In some implementations, device 100 may operate as and/or be part of a server. In FIG. 1, device 100 includes a plurality of processor cores (102a, 102b, 102c, 102d, 102e, and 102f) and a plurality of voltage selectors (104a, 104b, 104c, 104d, 104e, and 104f). As used herein, the terms "include", "have", and "comprise" are interchangeable and should be understood to have the same meaning.

[0014] Processor cores 102a-f may be in a multi-core processor, and may read and execute program instructions. Having multiple processor cores may allow device 100 to run multiple instructions at the same time (e.g., each of processor cores 102a-f may run a different instruction at a given time). Thus, device 100 may perform parallel computing and increase overall speed for programs. In some

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implementations, a multi-core processor may be part of an integrated circuit (IC) chip.

[0015] Each of voltage selectors 104a-f may be coupled to a respective one of processor cores 102a-f. Each of voltage selectors 104a-f may be capable of coupling the respective one of processor cores 102a-f to any of a plurality of voltage rails used to power any of processor cores 102a-f. As used herein, the term “voltage rails” should be understood to refer to voltages provided by power supplies. A voltage rail may be used as a supply voltage for electronic components/circuits. Different electronic components/circuits in a device may use different supply voltages, and thus a power supply of the device may provide multiple voltage rails, or the device may use multiple power supplies to provide respective voltage rails having different voltages.

[0016] In some implementations, voltage selectors 104a-f may include multiplexers. For example, if four voltage rails are available to power processor cores in device 100, a voltage selector may include a 4-to-1 multiplexer. In some implementations, voltage selectors 104a-f may include switches. For example, if three voltage rails are available to power processor cores in device 100, a voltage selector may include a triple-throw switch.

[0017] In device 100, three voltage rails V_1 , V_2 , and V_3 may be available to power processor cores in device 100. Each voltage rail may have a different voltage (e.g., V_1 may be 5 volts, V_2 may be 7 volts, and V_3 may be 12 volts). Each of voltage selectors 104a-f may select any of the available voltage rails. The voltage rail selected by a voltage selector may be coupled to the processor core that is coupled to the voltage selector. Thus, each of processor cores 102a-f may be coupled to (e.g., powered by) any of the available voltage rails in device 100. Although three voltage rails are shown in FIG. 1, it should be understood that more voltage rails or less voltage rails may be available to processor cores in a device, and that the concepts discussed herein may be applicable to a device having any number of voltage rails.

[0018] Processor cores may operate at various performance states. As used herein, the term “performance state”, or “P-state”, should be understood to refer to a frequency and operating point of a processor core. Different P-states may use different frequencies and/or voltages, resulting in different processing speeds

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and/or levels of power consumption. For example, some P-states may use lower frequencies and lower voltages, resulting in slower processing speeds and lower power consumption. Processor cores operating in such P-states may be coupled (e.g., with respective voltage selectors) to a voltage rail of a lower voltage. Some P-states may use higher frequencies and higher voltages, resulting in higher processing speeds and higher power consumption. Processor cores operating in such P-states may be coupled (e.g., with respective voltage selectors) to a voltage rail of a higher voltage. Other P-states may use higher frequencies and lower voltages, resulting in higher processing speeds and lower power consumption. Processor cores operating in such P-states may be coupled (e.g., with respective voltage selectors) to a voltage rail of a lower voltage.

[0019] In some implementations, processor cores 102a-f may be grouped, based on minimum operating voltages of processor cores 102a-f, into a plurality of clusters. Minimum operating voltages of processor cores may depend on respective P-states of the processor cores. For example, processor cores operating in P-states that use lower voltages may have lower minimum operating voltages. Each of the plurality of clusters may correspond to a respective one of a plurality of voltage rails used to power any of processor cores 102a-f. Voltage selectors, that are coupled to processor cores in the same cluster, may couple the respective processor cores to a voltage rail corresponding to the cluster.

[0020] Processor cores grouped into the same cluster may not be physically adjacent to one another. For example, processor cores 102a and 102f may be grouped into a first cluster corresponding to V_1 , processor cores 102b and 102c may be grouped into a second cluster corresponding to V_2 , and processor cores 102d and 102e may be grouped into a third cluster corresponding to V_3 . Voltage selectors 104a and 104f, which correspond to processor cores in the first cluster, may select V_1 , and thus processor cores 102a and 102f may both be coupled to V_1 . Similarly, voltage selectors 104b and 104c may select V_2 , and voltage selectors 104d and 104e may select V_3 , resulting in processor cores 102b and 102c being coupled to V_2 , and processor cores 102d and 102e being coupled to V_3 . It should be understood that different clusters may not have the same number of processor cores, and that a processor core may be in a cluster by itself. Although six processor cores and six voltage selectors are shown in FIG. 1, it should be

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understood that device 100 may include more processor cores or less processor cores, each processor core being coupled to a respective voltage selector, and that the concepts discussed herein may be applicable to a device having any number of processor cores coupled to respective voltage selectors.

[0021] FIG. 2 is a block diagram of an example device 200 that enables grouping of processor cores into clusters. Device 200 may be an electronic user device, such as a notebook computer, a desktop computer, a workstation, a tablet computing device, a mobile phone, or an electronic book reader. In some implementations, device 200 may operate as and/or be part of a server. Device 200 may include a plurality of processor cores (202a-f) and a plurality of voltage selectors (204a-f). Processor cores 202a-f and voltage selectors 204a-f of FIG. 2 may be analogous to (e.g., have functions and/or components similar to) processor cores 102a-f and voltage selectors 104a-f, respectively, of FIG. 1. Although six processor cores and six voltage selectors are shown in FIG. 2, it should be understood that device 200 may include more processor cores or less processor cores, each processor core being coupled to a respective voltage selector.

[0022] Device 200 may include self-test module 206, storage module 208, and clustering module 210. A module may include a set of instructions encoded on a machine-readable storage medium and executable by a processor of device 200. In addition or as an alternative, a module may include a hardware device comprising electronic circuitry for implementing the functionality described below.

[0023] Self-test module 206 may determine a minimum operating voltage for each of a plurality of processor cores in device 200. Self-test module 206 may include a Basic Input/Output System (BIOS). In some implementations, self-test module 206 may run a self-test on each processor core during boot time of device 200, before handing off the processor cores to an operating system (OS). During a self-test of a processor core, the voltage supplied to the processor core may be decremented until the processor core fails. The lowest voltage supplied to the processor core before failure may be determined to be the minimum operating voltage for the processor core.

[0024] In some implementations, self-test module 206 may run a self-test on a processor core during runtime of device 200. Self-test module 206 may issue an interrupt to the processor core and remove the processor core from normal operation

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in a manner that is transparent to the OS. For example, self-test module 206 may move operations running on the processor core to another processor core before running the self-test. Self-test module 206 may periodically run self-tests on processor cores during runtime of device 200, as minimum operating voltages of processor cores may change as their P-states change.

[0025] Storage module 208 may store the determined minimum operating voltages and identifiers of their respective processor cores. An identifier of a processor core may include a number or symbol that may be used to refer to the processor core when storing information related to the processor core and/or issuing commands to the processor core. In some implementations, storage module 208 may store a list of the determined minimum operating voltages and identifiers of their respective processor cores. The list may be ordered from lowest minimum operating voltage to highest minimum operating voltage. For example, the list may include processor core identifier-minimum operating voltage pairs, with the pairs ordered from lowest to highest minimum operating voltage.

[0026] Clustering module 210 may group, based on the determined minimum operating voltages, the plurality of processor cores into a plurality of clusters. Each of the plurality of clusters may correspond to a respective one of a plurality of voltage rails used to power any of the processor cores in device 200. For example, if three voltage rails are available to power processor cores in device 200, as illustrated in FIG. 2, clustering module 210 may group processor cores in device 200 into three clusters (e.g., a first cluster corresponding to V_1 , a second cluster corresponding to V_2 , and a third cluster corresponding to V_3).

[0027] Clustering module 210 may group processor cores into clusters such that the total power consumption of the processor cores is minimized. In some implementations, clustering module 210 may make multiple passes through a list of minimum operating voltages and identifiers of processor cores ordered from lowest to highest minimum operating voltage, grouping a pair of processor cores, that correspond to adjacent identifiers in the list, together with each pass. For a list with m cores, clustering module 210 may begin with m clusters, with each processor core being in its own cluster corresponding to the respective minimum operating voltage of the processor core. Clustering module 210 may make $(m-1)$ passes through the list; for each pass, a different pair of processor cores corresponding to adjacent

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identifiers in the list may be grouped together, and clustering module 210 may calculate the total power that would be consumed by all the processor cores if that pair of processor cores were grouped into the same cluster and coupled to the same voltage rail, the voltage rail having a voltage equal to the higher minimum operating voltage of the pair. Clustering module 210 may identify the grouping that results in the lowest total power consumption, and may group the appropriate pair of processor cores into a cluster, such that there are $(m-1)$ clusters after the $(m-1)$ passes have been made. Clustering module 210 may then make $(m-2)$ passes through the $(m-1)$ clusters, calculating the total power consumption for each pass to determine the two clusters (i.e., processor cores corresponding to identifiers in adjacent clusters) that should be combined next, and so on until the number of clusters is equal to the number of available voltage rails. Clustering module 210 may use data structures associated with respective clusters during the grouping process, as discussed below with respect to FIG. 3.

[0028] FIG. 3 is a block diagram of an example data structure 300 that may be used to store characteristics of a cluster of processor cores. Data structure 300 may correspond to a cluster, and may include a core count field 302, a cluster voltage field 304, and a pointer field 306. Core count field 302 may store the number of processor cores in the cluster. Cluster voltage field 304 may store the voltage to be used as the supply voltage for all processor cores grouped into the cluster. Pointer field 306 may store a pointer to a list of identifiers corresponding to processor cores grouped into the cluster.

[0029] When two clusters are combined, for example during the process described above with respect to FIG. 2, the data structures corresponding to the clusters may be combined. The data structure created by combining two data structures may have a core count field value equal to the sum of the core count field values of the data structures that are combined. The data structure created by combining two data structures may have a cluster voltage field value equal to the greater cluster voltage field value of the data structures that are combined. The pointer field value of the data structure created by combining two data structures may store a pointer to a list that is created by merging the respective lists pointed to by the data structures that are combined. When the number of clusters is equal

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to the number of available voltage rails, each cluster may correspond to the voltage rail whose value is closest to, and greater than, the cluster voltage field value.

[0030] FIG. 4 is a block diagram of an example device 400 that includes a machine-readable storage medium encoded with instructions to enable coupling of processor cores to various voltage rails. Device 400 may be an electronic user device, such as a notebook computer, a desktop computer, a workstation, a tablet computing device, a mobile phone, or an electronic book reader. In some implementations, device 400 may operate as and/or be part of a server. In FIG. 4, system 400 includes processor 402 and machine-readable storage medium 404.

[0031] Processor 402 may include a central processing unit (CPU), microprocessor (e.g., semiconductor-based microprocessor), and/or other hardware device suitable for retrieval and/or execution of instructions stored in machine-readable storage medium 404. Processor 402 may fetch, decode, and/or execute instructions 406 and 408 to enable coupling of processor cores to various voltage rails, as described below. As an alternative or in addition to retrieving and/or executing instructions, processor 402 may include an electronic circuit comprising a number of electronic components for performing the functionality of instructions 406 and/or 408.

[0032] Machine-readable storage medium 404 may be any suitable electronic, magnetic, optical, or other physical storage device that contains or stores executable instructions. Thus, machine-readable storage medium 404 may include, for example, a RAM, an Electrically Erasable Programmable Read-Only Memory (EEPROM), a storage device, an optical disc, and the like. In some implementations, machine-readable storage medium 404 may include a non-transitory storage medium, where the term "non-transitory" does not encompass transitory propagating signals. As described in detail below, machine-readable storage medium 404 may be encoded with a set of executable instructions 406 and 408.

[0033] Instructions 406 may group, based on minimum operating voltages for a plurality of processor cores, the plurality of processor cores into a plurality of clusters. The plurality of processor cores may be part of a multi-core processor in device 400. Each of the plurality of clusters may correspond to a respective one of a plurality of voltage rails used to power the plurality of processor cores. For example, if four voltage rails are available to power the plurality of processor cores, the plurality

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of processor cores may be grouped into four clusters, with each cluster corresponding to one of the available voltage rails. The plurality of processor cores may be grouped using a process similar to that discussed above with respect to FIG. 2.

[0034] Instructions 408 may select, based on the plurality of clusters, one of the plurality of voltage rails for each of the plurality of processor cores. A voltage rail selected for a respective processor core may correspond to a cluster into which the respective processor core is grouped. For example, for processor cores grouped into a particular cluster, instructions 408 may select the voltage rail whose value is closest to, and greater than, the cluster voltage field value in the data structure corresponding to the particular cluster, as discussed above with respect to FIG. 3. Each of the plurality of processor cores may be coupled to a respective one of a plurality of voltage selectors. Each of the plurality of voltage selectors may be capable of coupling the respective one of the plurality of processor cores to any of the plurality of voltage rails.

[0035] FIG. 5 is a block diagram of an example device 500 that includes a machine-readable storage medium encoded with instructions to enable grouping of processor cores into clusters. Device 500 may be an electronic user device, such as a notebook computer, a desktop computer, a workstation, a tablet computing device, a mobile phone, or an electronic book reader. In some implementations, device 500 may operate as and/or be part of a server. In FIG. 5, system 500 includes processor 502 and machine-readable storage medium 504.

[0036] As with processor 402 of FIG. 4, processor 502 may include a CPU, microprocessor (e.g., semiconductor-based microprocessor), and/or other hardware device suitable for retrieval and/or execution of instructions stored in machine-readable storage medium 504. Processor 502 may fetch, decode, and/or execute instructions 506, 508, 510, 512, and 514 to enable grouping of processor cores into clusters, as described below. As an alternative or in addition to retrieving and/or executing instructions, processor 502 may include an electronic circuit comprising a number of electronic components for performing the functionality of instructions 506, 508, 510, 512, and/or 514.

[0037] As with machine-readable storage medium 404 of FIG. 4, machine-readable storage medium 504 may be any suitable physical storage device that stores executable instructions. Instructions 506 and 508 on machine-readable

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storage medium 504 may be analogous to instructions 406 and 408, respectively, on machine-readable storage medium 404. Instructions 510 may determine a minimum operating voltage for each of a plurality of processor cores. Each of the plurality of processor cores may be coupled to a respective one of a plurality of voltage selectors. In some implementations, instructions 510 may be executed during boot time of a chip (e.g., IC) that includes the plurality of processor cores. For example, a minimum operating voltage for each of a plurality of processor cores may be determined by running a self-test on each processor core during boot time, before the plurality of processor cores are handed off to an OS. During a self-test of a processor core, the voltage supplied to the processor core may be decremented until the processor core fails. The lowest voltage supplied to the processor core before failure may be determined to be the minimum operating voltage for the processor core.

[0038] In some implementations, instructions 510 may be executed during runtime of a chip (e.g., IC) that includes the plurality of processor cores. For example, an interrupt may be issued to a processor core during runtime, and the processor core may be removed from normal operation in a manner that is transparent to the OS, as discussed above with respect to FIG. 2. Instructions 510 may be periodically executed during runtime of the chip, as minimum operating voltages of processor cores may change as their P-states change.

[0039] Instructions 512 may store a list of the determined minimum operating voltages and identifiers of their respective processor cores. The list may be ordered from lowest minimum operating voltage to highest minimum operating voltage. In some implementations, the list may include processor core identifier-minimum operating voltage pairs, with the pairs ordered from lowest to highest minimum operating voltage.

[0040] Instructions 514 may group a pair of processor cores, that correspond to adjacent identifiers in the list, into a cluster. The pair of processor cores that are grouped into the cluster may be determined, for example, using the process discussed above with respect to FIG. 2. Instructions 514 may be executed multiple times for a list of processor core identifier-minimum operating voltage pairs, until the number of clusters into which processor cores are grouped is equal to the number of voltage rails available to power the processor cores.

[0041] Machine-readable storage medium 504 may include a plurality of data structures 516. Each of the plurality of data structures may correspond to a respective one of a plurality of clusters. Each of the plurality of data structures may include a core count field, a cluster voltage field, and a pointer field, as discussed above with respect to FIG. 3.

[0042] Methods related to coupling processor cores to voltage rails are discussed with respect to FIGS. 6-8. FIG. 6 is a flowchart of an example method 600 for selecting voltage rails to couple to various processor cores. Although execution of method 600 is described below with reference to processor 502 of FIG. 5, it should be understood that execution of method 600 may be performed by other suitable devices, such as processor 402 of FIG. 4. Method 600 may be implemented in the form of executable instructions stored on a machine-readable storage medium and/or in the form of electronic circuitry.

[0043] Method 600 may start in block 602, where processor 502 may determine a minimum operating voltage for each of a plurality of processor cores. Each of the plurality of processor cores may be coupled to a respective one of a plurality of voltage selectors. In some implementations, minimum operating voltages of a plurality of processor cores may be determined during boot time of a chip (e.g., IC) that includes the plurality of processor cores. For example, a minimum operating voltage for each of a plurality of processor cores may be determined by running a self-test on each processor core during boot time, before the plurality of processor cores are handed off to an OS. During a self-test of a processor core, the voltage supplied to the processor core may be decremented until the processor core fails. The lowest voltage supplied to the processor core before failure may be determined to be the minimum operating voltage for the processor core.

[0044] In some implementations, minimum operating voltages of a plurality of processor cores may be determined during runtime of a chip (e.g., IC) that includes the plurality of processor cores. For example, an interrupt may be issued to a processor core during runtime, and the processor core may be removed from normal operation in a manner that is transparent to the OS, as discussed above with respect to FIG. 2. Processor 502 may periodically determine minimum operating voltages of processor cores during runtime of the chip, as minimum operating voltages of processor cores may change as their P-states change.

[0045] Next, in block 604, processor 502 may group, based on the determined minimum operating voltages, the plurality of processor cores into a plurality of clusters. In some implementations, the plurality of processor cores may be grouped during boot time of a chip that includes the plurality of processor cores. Each of the plurality of clusters may correspond to a respective one of a plurality of voltage rails used to power the plurality of processor cores. Each of the plurality of voltage selectors may be capable of coupling the respective one of the plurality of processor cores to any of the plurality of voltage rails. In some implementations, processor 502 may group the plurality of processor cores using a process similar to that discussed above with respect to FIG. 2.

[0046] Finally, in block 606, processor 502 may select, based on the plurality of clusters, one of the plurality of voltage rails for each of the plurality of processor cores. In some implementations, processor 502 may select one of the plurality of voltage rails for each of the plurality of processor cores during boot time of a chip that includes the plurality of processor cores. A voltage rail selected for a respective processor core may correspond to a cluster into which the respective processor core is grouped. For example, for processor cores grouped into a particular cluster, processor 502 may select the voltage rail whose value is closest to, and greater than, the cluster voltage field value in the data structure corresponding to the particular cluster, as discussed above with respect to FIG. 3.

[0047] FIG. 7 is a flowchart of an example method 700 for changing a voltage rail coupled to a processor core. Although execution of method 700 is described below with reference to processor 502 of FIG. 5, it should be understood that execution of method 700 may be performed by other suitable devices, such as processor 402 of FIG. 4. Some blocks of method 700 may be performed in parallel with and/or after method 600. Method 700 may be implemented in the form of executable instructions stored on a machine-readable storage medium and/or in the form of electronic circuitry.

[0048] Method 700 may start in block 702, where processor 502 may group one of a plurality of processor cores into a first cluster of a plurality of clusters during boot time of a chip. The first cluster may correspond to a first voltage rail of a plurality of voltage rails. The first voltage rail may be selected for the one of the plurality of processor cores during boot time of the chip.

[0049] In block 704, processor 502 may change, during runtime of the chip, a performance state of the one of the plurality of processor cores. The P-state after the change may use a different voltage than the P-state prior to the change. For example, the P-state after the change may use the voltage of a second voltage rail that corresponds to another cluster of the plurality of clusters. In some implementations, processor 502 may change the P-state of a processor core to allow the processor core to perform operations more quickly, and/or to consume less power.

[0050] Finally, in block 706, processor 502 may couple, in response to the change in performance state, the one of the plurality of processor cores to a second voltage rail of the plurality of voltage rails instead of to the first voltage rail. For example, processor 502 may send a command to a voltage selector, that is coupled to the one of the plurality of processor cores, to select the second voltage rail. In some implementations, processor 502 may change the grouping of the one of the plurality of processor cores from the first cluster to a second cluster of the plurality of clusters that corresponds to the second voltage rail.

[0051] FIG. 8 is a flowchart of an example method 800 for grouping processor cores into clusters. Although execution of method 800 is described below with reference to processor 502 of FIG. 5, it should be understood that execution of method 800 may be performed by other suitable devices, such as processor 402 of FIG. 4. Some blocks of method 800 may be performed in parallel with and/or after method 600 or 700. Method 800 may be implemented in the form of executable instructions stored on a machine-readable storage medium and/or in the form of electronic circuitry.

[0052] Method 800 may start in block 802, where processor 502 may determine a minimum operating voltage for each of a plurality of processor cores, as discussed above with respect to FIG. 6. Next, in block 804, processor 502 may store a list of the determined minimum operating voltages and identifiers of their respective processor cores. The list may be ordered from lowest minimum operating voltage to highest minimum operating voltage. In some implementations, the list may include processor core identifier-minimum operating voltage pairs, with the pairs ordered from lowest to highest minimum operating voltage.

[0053] In block 806, processor 502 may group a pair of processor cores, that correspond to adjacent identifiers in the list, into a cluster. The pair of processor cores

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that are grouped into the cluster may be determined, for example, using the process discussed above with respect to FIG. 2. Processor 502 may perform block 806 multiple times for a list of processor core identifier-minimum operating voltage pairs, until the number of clusters into which processor cores are grouped is equal to the number of voltage rails available to power the processor cores.

[0054] In block 808, processor 502 may store a plurality of data structures. Each of the plurality of data structures may correspond to a respective one of a plurality of clusters. Each of the plurality of data structures may include a core count field, a cluster voltage field, and a pointer field, as discussed above with respect to FIG. 3.

[0055] The foregoing disclosure describes selecting various voltage rails for processor cores. Example implementations described herein enable coupling any processor core on a chip to any voltage rail available on the chip, reducing wasted energy.

I claim:

1. A device comprising:
a plurality of processor cores; and
a plurality of voltage selectors, wherein:
each of the plurality of voltage selectors is coupled to a respective one of the plurality of processor cores; and
each of the plurality of voltage selectors is capable of coupling the respective one of the plurality of processor cores to any of a plurality of voltage rails used to power any of the plurality of processor cores.
2. The device of claim 1, wherein:
the plurality of processor cores are grouped, based on minimum operating voltages of the plurality of processor cores, into a plurality of clusters;
each of the plurality of clusters corresponds to a respective one of the plurality of voltage rails; and
voltage selectors, that are coupled to processor cores in the same cluster, are to couple the respective processor cores to a voltage rail corresponding to the cluster.
3. The device of claim 1, wherein the plurality of voltage selectors comprise multiplexers or switches.
4. The device of claim 1, further comprising:
a self-test module to determine a minimum operating voltage for each of the plurality of processor cores; and
a storage module to store the determined minimum operating voltages and identifiers of their respective processor cores.
5. The device of claim 4, further comprising a clustering module to group, based on the determined minimum operating voltages, the plurality of processor cores into a plurality of clusters.

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6. A machine-readable storage medium encoded with instructions executable by a processor of a device, the machine-readable storage medium comprising:

instructions to group, based on minimum operating voltages for a plurality of processor cores, the plurality of processor cores into a plurality of clusters, wherein each of the plurality of clusters corresponds to a respective one of a plurality of voltage rails used to power the plurality of processor cores; and

instructions to select, based on the plurality of clusters, one of the plurality of voltage rails for each of the plurality of processor cores, wherein:

each of the plurality of processor cores is coupled to a respective one of a plurality of voltage selectors; and

each of the plurality of voltage selectors is capable of coupling the respective one of the plurality of processor cores to any of the plurality of voltage rails.

7. The machine-readable storage medium of claim 6, wherein a voltage rail selected for a respective processor core corresponds to a cluster into which the respective processor core is grouped.

8. The machine-readable storage medium of claim 6, further comprising:

instructions to determine a minimum operating voltage for each of the plurality of processor cores; and

instructions to store a list of the determined minimum operating voltages and identifiers of their respective processor cores, wherein the list is ordered from lowest minimum operating voltage to highest minimum operating voltage.

9. The machine-readable storage medium of claim 8, further comprising instructions to group a pair of processor cores, that correspond to adjacent identifiers in the list, into a cluster.

10. The machine-readable storage medium of claim 6, further comprising a plurality of data structures, wherein:

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each of the plurality of data structures corresponds to a respective one of the plurality of clusters; and

each of the plurality of data structures comprises a core count field, a cluster voltage field, and a pointer field.

11. A method comprising:

determining a minimum operating voltage for each of a plurality of processor cores;

grouping, based on the determined minimum operating voltages, the plurality of processor cores into a plurality of clusters, wherein each of the plurality of clusters corresponds to a respective one of a plurality of voltage rails used to power the plurality of processor cores; and

selecting, based on the plurality of clusters, one of the plurality of voltage rails for each of the plurality of processor cores, wherein:

each of the plurality of processor cores is coupled to a respective one of a plurality of voltage selectors; and

each of the plurality of voltage selectors is capable of coupling the respective one of the plurality of processor cores to any of the plurality of voltage rails.

12. The method of claim 11, wherein the grouping and selecting are performed during boot time of a chip comprising the plurality of processor cores.

13. The method of claim 12, wherein one of the plurality of processor cores is grouped into a first cluster of the plurality of clusters during boot time of the chip, the first cluster corresponding to a first voltage rail of the plurality of voltage rails, and wherein the first voltage rail is selected for the one of the plurality of processor cores during boot time of the chip, the method further comprising:

changing, during runtime of the chip, a performance state of the one of the plurality of processor cores; and

coupling, in response to the change in performance state, the one of the plurality of processor cores to a second voltage rail of the plurality of voltage rails instead of to the first voltage rail.

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14. The method of claim 11, further comprising:

storing a list of the determined minimum operating voltages and identifiers of their respective processor cores, wherein the list is ordered from lowest minimum operating voltage to highest minimum operating voltage; and

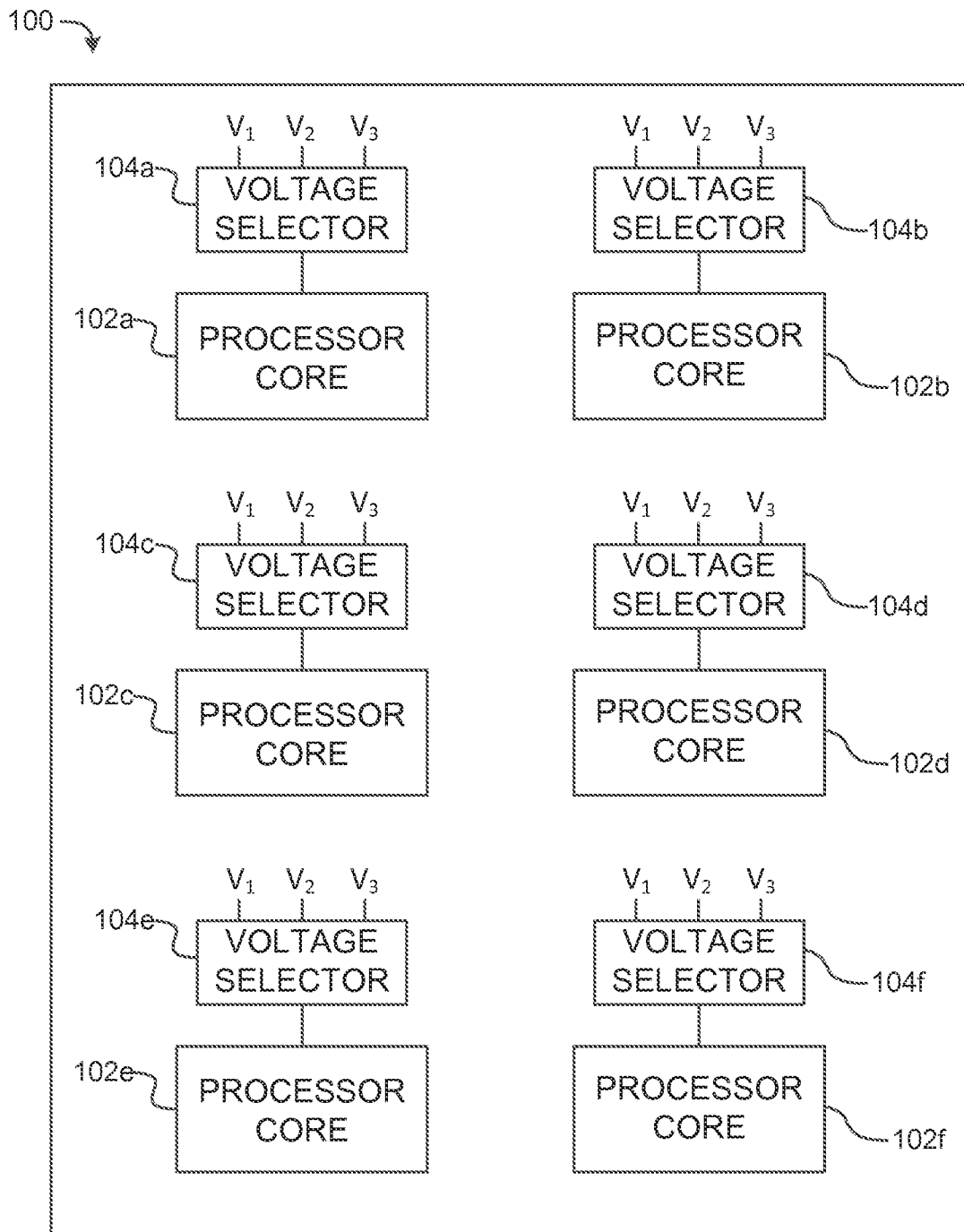
grouping a pair of processor cores, that correspond to adjacent identifiers in the list, into a cluster.

15. The method of claim 11, further comprising storing a plurality of data structures, wherein:

each of the plurality of data structures corresponds to a respective one of the plurality of clusters; and

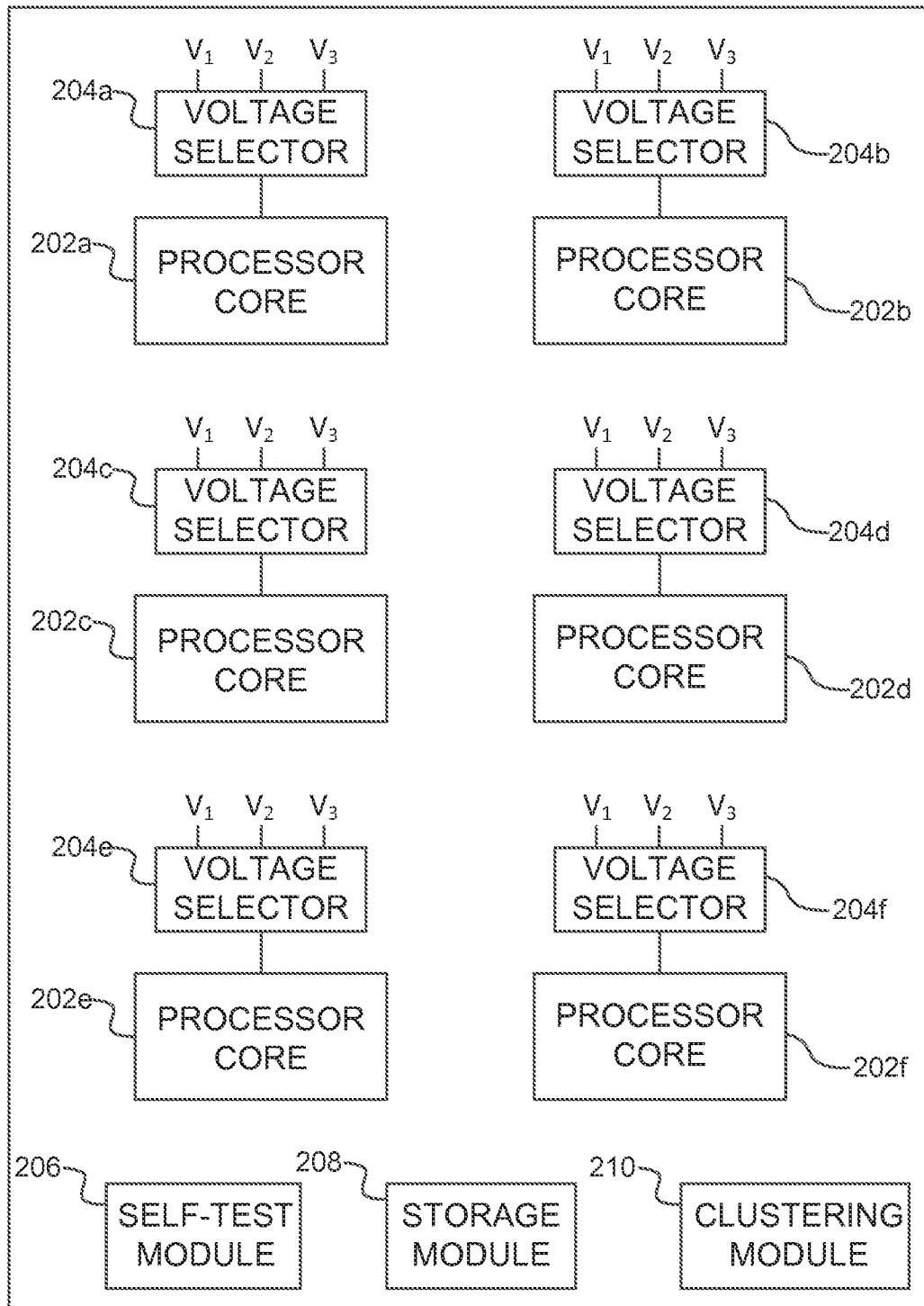
each of the plurality of data structures comprises a core count field, a cluster voltage field, and a pointer field.

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**FIG. 1**

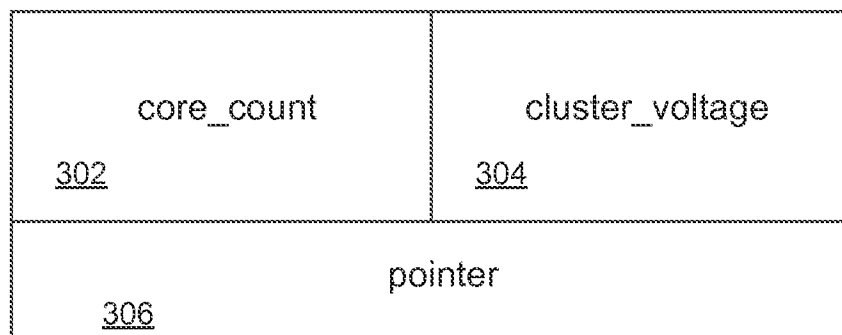
2/6

200

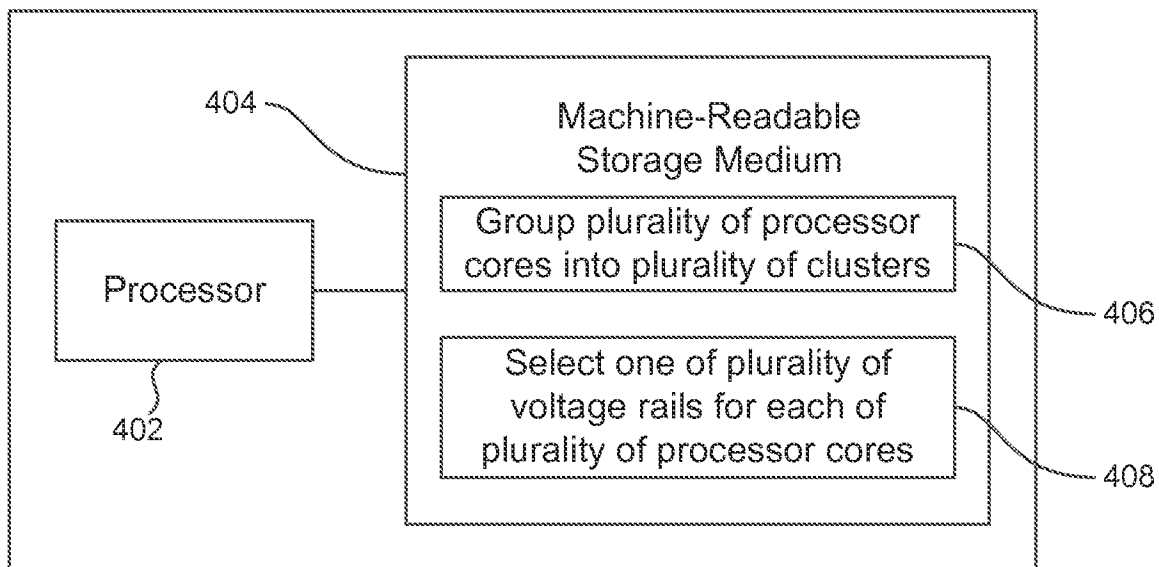
**FIG. 2**

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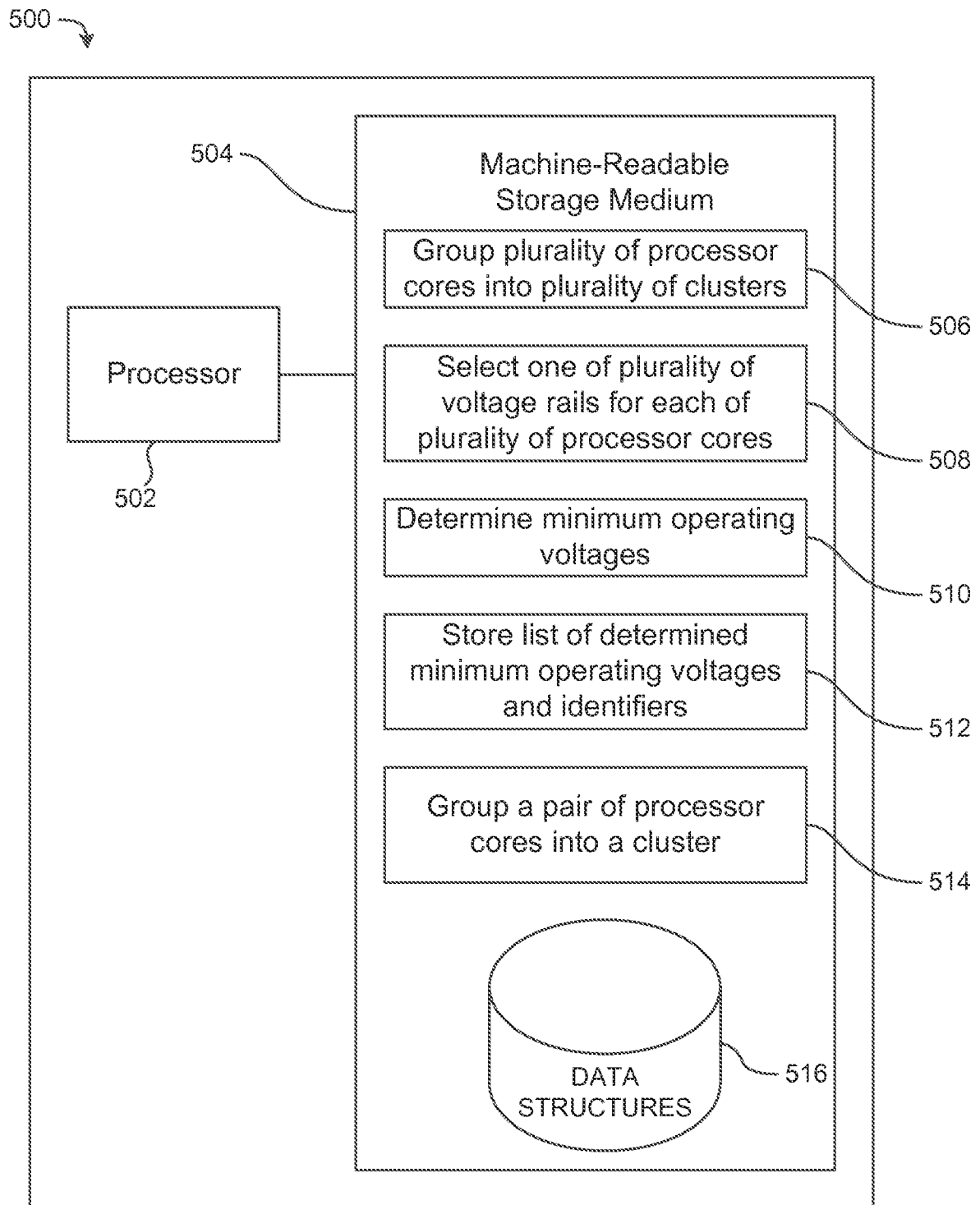
300

**FIG. 3**

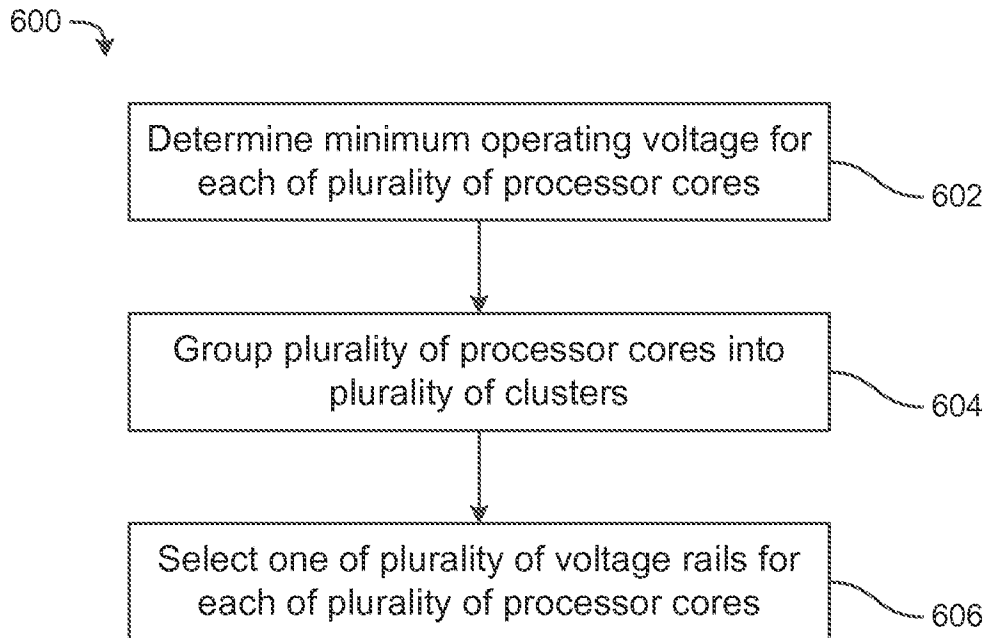
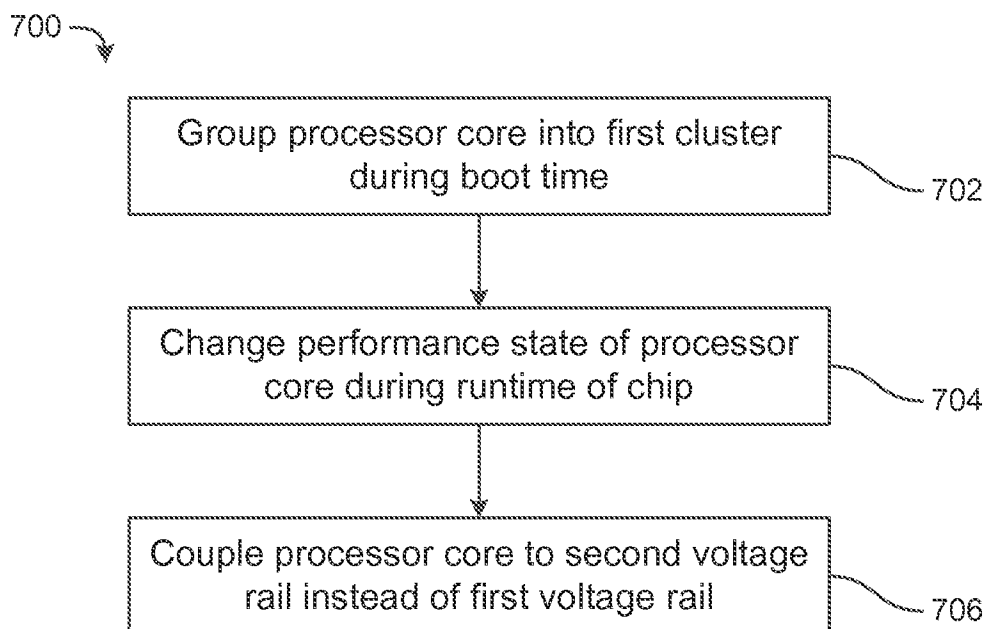
400

**FIG. 4**

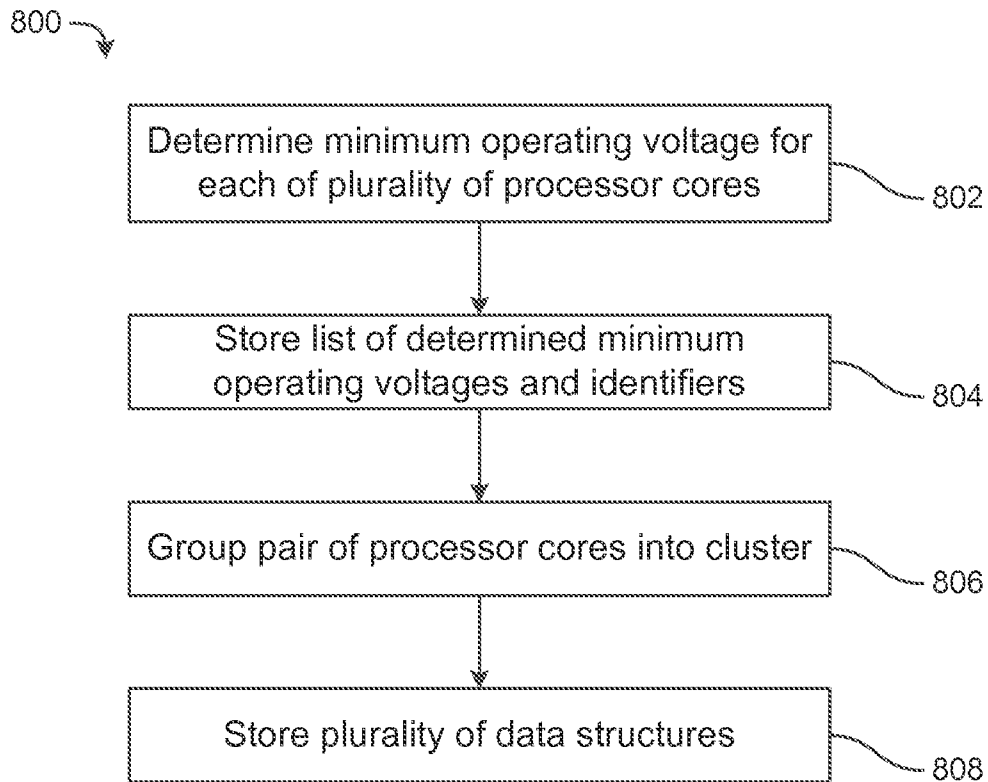
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**FIG. 5**

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**FIG. 6****FIG. 7**

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**FIG. 8**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/039902**A. CLASSIFICATION OF SUBJECT MATTER****G06F 1/26(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 1/26; H04W 88/02; G06F 17/50; G11C 5/14; H04W 52/02; G05F 1/618; G06F 1/00; H03L 7/08; H01L 21/82

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: processor core, voltage selector, voltage rail, minimum voltage, group, cluster

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2013-101718 A1 (INTEL CORPORATION) 04 July 2013 See page 11, lines 9-27; page 13, lines 4-6; and figures 14-15, 17.	1,3
Y		4
A		2,5-15
Y	US 2008-0052542 A1 (LOUIS BENNIE CAPPS et al.) 28 February 2008 See paragraphs [0035]-[0039], [0062]-[0065]; claim 14; and figure 2, 9A.	4
A	KR 10-2013-0076683 A (SAMSUNG ELECTRONICS CO., LTD.) 08 July 2013 See paragraphs [0119]-[0135]; and figure 8.	1-15
A	US 2010-0033151 A1 (CHAO-CHUNG WU et al.) 11 February 2010 See paragraphs [0025]-[0030]; and figure 4.	1-15
A	JP 2011-018137 A (TOSHIBA CORP.) 27 January 2011 See paragraphs [0022]-[0033]; and figure 2.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search

10 February 2015 (10.02.2015)

Date of mailing of the international search report

11 February 2015 (11.02.2015)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2014/039902

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