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(54) SEMICONDUCTOR STRUCTURE AND PREHEATING METHOD THEREFOR

(57) A semiconductor structure and a preheating method therefor. The semiconductor structure comprises: a storage chip; a temperature measurement unit used to measure a temperature of the storage chip before startup of the storage chip; a control chip used to heat the storage chip before startup of the storage chip, to determine whether the temperature obtained by the temperature measurement unit reaches a set threshold, and to control the storage chip to start up if the temperature reaches the set threshold. When a semiconductor structure of the present invention is operating in a low temperature environment, a control chip can be used to raise a temperature of a storage chip to a set threshold, thereby preventing resistances of a bit line, a word line and a metal connection line (metal contact portion) in the storage chip from increasing due to an excessively low ambient temperature, reducing a write time required to write data to a storage device at a low temperature environment, and improving write stability of the storage device.

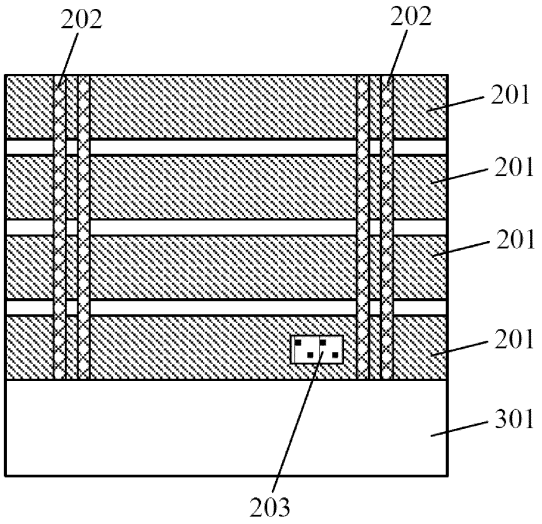

FIG. 2

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Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to Chinese Patent Application No.: 202010216794.0, entitled "SEMICONDUCTOR STRUCTURE AND PREHEATING METHOD THEREFOR", filed on March 25, 2020, the disclosure of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to the field of memory, and in particular, to a semiconductor structure and a preheating method thereof.

BACKGROUND

[0003] A dynamic random-access memory (DRAM) is a semiconductor storage device commonly used in a computer. The storage array of the DRAM includes many duplicate storage units. Each storage unit usually includes a capacitor and a transistor. The gate of the transistor is connected to a word line, the drain of the transistor is connected to a bit line, and the source of the transistor is connected to the capacitor. The voltage signal on the word line can control the ON or OFF of the transistor, and data can subsequently be read from or written into the capacitor through the bit line.

[0004] In the related techniques, a low temperature may prolong the write time for writing data into a memory and adversely affect the stability of the data to be written.

SUMMARY

[0005] The technical problem to be solved by the present disclosure is how to reduce write time in writing data into a memory at a low temperature and improve the stability of the data to be written.

[0006] One aspect of the present disclosure is directed to a semiconductor structure. The semiconductor structure includes a storage chip, a temperature detection unit, and a control chip.

[0007] The temperature detection unit is configured to detect the temperature of the storage chip before the storage chip initiates.

[0008] The control chip is configured to, before the storage chip initiates, heat the storage chip, determine whether the temperature detected by the temperature detection unit reaches a specified threshold, and, in response to the temperature reaching the specified threshold, control the storage chip to initiate.

[0009] In some embodiments, the semiconductor structure may include one or more storage chips. When the semiconductor structure includes two or more storage chips, the two or more storage chips may be sequentially stacked vertically.

[0010] In some embodiments, the one or more storage chips may be located on the control chip and electrically connected to the control chip.

[0011] In some embodiments, the semiconductor structure may further include a line substrate. The line substrate may have a connection line. The one or more storage chips and the control chip may both be located on the line substrate, and the one or more storage chips and the control chip may be connected through the connection line in the line substrate.

[0012] In some embodiments, the semiconductor structure may include one or more temperature detection units electrically connected to the control chip. The one or more temperature detection units may be in the control chip, in the one or more storage chips, or on the line substrate between the one or more storage chips and the control chip.

[0013] In some embodiments, the semiconductor structure may include only one temperature detection unit. And the control chip may be configured to: upon determining that the temperature detected by the temperature detection unit reaches the specified threshold, control all the one or more storage chips to initiate.

[0014] In some embodiments, the semiconductor structure may include only one temperature detection unit and two or more storage chips. And the control chip may be configured to: upon determining that the temperature detected by the temperature detection unit reaches the specified threshold, first, control a storage chip closest to the control chip to initiate, and then control other storage chips on the storage chip to sequentially initiate.

[0015] In some embodiments, the semiconductor structure may include two or more temperature detection units and two or more storage chips. Each storage chip may have one temperature detection unit. The control chip may be configured to: sequentially determine whether a respective temperature detected by each of the temperature detection units reaches the specified threshold; and, in response to the temperature detected by one of the temperature detection units reaching the specified threshold, control the storage chip corresponding to the temperature detection unit to initiate.

[0016] In some embodiments, the control chip is further configured to: after the storage chip initiates, control the storage chip to perform write, read, and erase operations.

[0017] In some embodiments, the control chip may initiate before the control chip heats the storage chip, and the control chip may be configured to: heat the storage chip using heat generated by the control chip after the control chip initiates.

[0018] In some embodiments, the control chip may have a heating circuit configured to heat the storage chip.

[0019] In some embodiments, the control chip may be configured to: before or after the control chip heats the storage chip, determine whether the temperature of the storage chip detected by the temperature detection unit reaches the specified threshold; and, in response to the temperature not reaching the specified threshold, control

the heating circuit to heat the storage chip; or, in response to the temperature reaching the specified threshold, control the heating circuit to stop heating the storage chip.

[0020] In some embodiments, the storage chip may be a Dynamic Random Access Memory (DRAM) storage chip.

[0021] Another aspect of the present disclosure is directed to a semiconductor structure preheating method. The method includes providing a semiconductor structure, where the semiconductor structure includes a storage chip, a control chip electrically connected to the storage chip, and a temperature detection unit; initiating the control chip; heating, by the control chip and before the storage chip initiates, the storage chip; detecting a temperature of the storage chip by the temperature detection unit; and determining, by the control chip, whether the temperature detected by the temperature detection unit reaches a specified threshold; and, in response to the temperature reaching the specified threshold, initiating the storage chip.

[0022] In some embodiments, the semiconductor structure may include one or more temperature detection units and one or more storage chips. When the semiconductor structure includes two or more storage chips, the two or more storage chips may be sequentially stacked vertically.

[0023] In some embodiments, the semiconductor structure may include only one temperature detection unit. The control chip may be configured to: upon determining that the temperature detected by the temperature detection unit reaches the specified threshold, control all the one or more storage chips to initiate.

[0024] In some embodiments, the semiconductor structure may include only one temperature detection unit and two or more storage chips. The control chip is configured to: upon determining that the temperature detected by the temperature detection unit reaches the specified threshold, first, control the storage chip closest to the control chip to initiate, and then control other storage chips on the storage chip to sequentially initiate.

[0025] In some embodiments, the semiconductor structure may include two or more temperature detection units and two or more storage chips. Each storage chip may have one temperature detection unit. The control chip may be configured to: sequentially determine whether a respective temperature detected by each of the temperature detection units reaches the specified threshold; and, in response to the temperature detected by one of the temperature detection units reaching the specified threshold, control the storage chip corresponding to the temperature detection unit to initiate.

[0026] In some embodiments, the control chip is further configured to: after the storage chip initiates, control the storage chip to perform write, read, and erase operations.

[0027] Compared with the related techniques, the technical solutions provided by the present disclosure have the following advantages.

[0028] The semiconductor structure provided in the present disclosure may include a storage chip, a temperature detection unit, and a control chip. The temperature detection unit may be configured to detect the temperature of the storage chip before the storage chip initiates. The control chip may be configured to, before the storage chip initiates, heat the storage chip and determine whether the temperature detected by the temperature detection unit reaches a specified threshold; and, if the temperature reaches the specified threshold, control the storage chip to initiate. The control chip may be configured to cooperate with the temperature detection unit. The control chip may heat the storage chip before the storage chip initiates. The temperature detection unit may detect the temperature of the storage chip before the storage chip initiates. And the control chip may determine whether the temperature detected by the temperature detection unit reaches the specified threshold, and, if the temperature reaches the specified threshold, control the storage chip to initiate. Therefore, when the semiconductor structure provided in the present disclosure works at a low temperature, the storage chip may be heated to the specified threshold by the control chip, thereby preventing an increase of the resistances of the bit line, the word line, and the metal connection line (metal contact part) in the storage chip due to an excessively low temperature, reducing the write time for writing data into the memory at the low temperature and improving the write stability of the memory.

[0029] In some embodiments, the semiconductor structure may include only one temperature detection unit. The temperature detection unit may be in the control chip, in the one or more storage chips, or on the line substrate between the one or more storage chips and the control chip. The control chip may be configured to: upon determining that the temperature detected by the temperature detection unit reaches the specified threshold, control all the storage chips to initiate. When there are multiple storage chips in the semiconductor structure, the aforementioned control structure and control manner may be relatively simple, and may reduce the write time for writing data into the storage chip at a low temperature and improve the write stability of the storage chip.

[0030] In some embodiments, the semiconductor structure may include only one temperature detection unit and two or more storage chips. The control chip may be configured to: upon determining that the temperature detected by the temperature detection unit reaches the specified threshold, first, control the storage chip closest to the control chip to initiate, and then control other storage chips on the storage chip to sequentially initiate. When there are multiple storage chips in the semiconductor structure, the aforementioned control structure and control manner may cause each storage chip to initiate after reaching the specified threshold, thereby improving the precision of the initiation of each storage chip, reducing the write time for writing data into each storage chip at a low temperature and improving the write stability of each storage chip.

[0031] In some embodiments, the semiconductor structure may include two or more temperature detection units and two or more storage chips. Each storage chip may have one temperature detection unit. The control chip may be configured to: sequentially determine whether a respective temperature detected by each of the temperature detection units reaches the specified threshold; and, in response to the temperature detected by one of the temperature detection units reaching the specified threshold, control the storage chip corresponding to the temperature detection unit to initiate. When there are multiple storage chips in the semiconductor structure, the aforementioned control structure and control manner may further improve the precision of the initiation of each storage chip, thereby reducing the write time for writing data into each storage chip at a low temperature and further improving the write stability of each storage chip.

[0032] In some embodiments, the control chip may initiate before the control chip heat the storage chip. And the control chip may heat the storage chip using heat generated by the control chip after the control chip initiates. Therefore, no additional heating circuit may be needed, thereby simplifying the semiconductor structure.

[0033] In some embodiments, the control chip may have an additional heating circuit configured to heat the storage chip. Before or after the control chip heats the storage chip, the control chip may be configured to determine whether the temperature of the storage chip detected by the temperature detection unit reaches the specified threshold. If the temperature does not reach the specified threshold, the control chip may control the heating circuit to heat the storage chip. If the temperature reaches the specified threshold, the control chip may control the heating circuit to stop heating the storage chip. Therefore, the heating process may be accurately controlled, so that the temperature of the storage chip can be kept near the specified threshold, thereby preventing the temperature of the storage chip from being excessively high or excessively low, and always keeping the write time of the memory relatively short.

[0034] In the semiconductor structure preheating method provided in the present disclosure, before a storage chip initiates, the storage chip may be heated by a control chip. The temperature of the storage chip may be detected by a temperature detection unit. The control chip may be configured to determine whether the temperature detected by the temperature detection unit reaches a specified threshold. If the temperature reaches the specified threshold, the storage chip may be controlled to initiate. Therefore, when the semiconductor structure provided in the present disclosure works at a low temperature, the storage chip may be heated to the specified threshold by using the control chip, thereby preventing an increase of the resistances of the bit line, the word line, and the metal connection line (metal contact part) in the storage chip due to an excessively low temperature, reducing the write time for writing data into the memory at the low temperature and improving the write stability of the memory.

BRIEF DESCRIPTION OF DRAWINGS

[0035]

FIGs. 1, 2, 3, 4, 5, 6, and 7 are schematic structural diagrams of a semiconductor structure according to one or more embodiments of the present disclosure.

FIG. 8 is a flowchart of a semiconductor structure preheating method according to one or more embodiments of the present disclosure.

DESCRIPTION OF EMBODIMENTS

[0036] As described in the Background section, in the related techniques, a lower temperature may prolong the write time for writing data into a memory and adversely affect the stability of the data to be written.

[0037] When a conventional memory works at a low temperature, the resistances of the bit line, the word line, the metal connection line (metal contact part), and the like in the memory would increase due to the low temperature. The write time for writing data into the memory would change or increase due to the resistance increase, thereby affecting the write stability of the memory.

[0038] The present disclosure presents a semiconductor structure and a preheating method thereof to address the foregoing issues.

[0039] The semiconductor structure may include a storage chip, a temperature detection unit, and a control chip. The temperature detection unit may be configured to detect the temperature of the storage chip before the storage chip initiates. The control chip may be configured to, before the storage chip initiates, heat the storage chip and determine whether the temperature detected by the temperature detection unit reaches a specified threshold, and, if the temperature reaches the specified threshold, control the storage chip to initiate. The control chip may be configured to cooperate with the temperature detection unit. The control chip may heat the storage chip before the storage chip initiates. The temperature detection unit may detect the temperature of the storage chip before the storage chip initiates. The control chip may determine whether the temperature detected by the temperature detection unit reaches the specified threshold. If the temperature reaches the specified threshold, the control chip may control the storage chip to initiate. Therefore, when the semiconductor structure provided in the present disclosure works at a low temperature, the storage chip may be heated to the specified threshold by the control chip, thereby preventing an increase of the resistances of the bit line, the word line, and the metal connection line (metal contact part) in the storage chip due to an excessively low temperature, reducing the write time for writing data into the memory at the low temperature and improving the write stability of the memory.

[0040] To make the foregoing objects, features, and

advantages of the present disclosure clearer and easier to understand, the specific implementations of the present disclosure will be described through the following detailed description with reference to the accompanying drawings. When describing the embodiments of the present disclosure in detail, for the sake of illustration, the schematic diagrams may be enlarged partially. The schematic diagrams are exemplary and should not constitute a limitation on the protection scope of the present disclosure herein. Additionally, three-dimensional spatial sizes of length, width, and depth should be included in actual production.

[0041] FIGs. 1, 2, 3, 4, 5, 6, and 7 are schematic structural diagrams of a semiconductor structure according to one or more embodiments of the present disclosure. FIG. 8 is a schematic flowchart of a semiconductor structure preheating method according to one or more embodiments of the present disclosure.

[0042] Referring to FIG. 1, a semiconductor structure is provided. The semiconductor structure may include a storage chip 201, a temperature detection unit 203, and a control chip 301. The temperature detection unit 203 may be configured to detect the temperature of the storage chip 201 before the storage chip 201 initiates. The control chip 301 may be configured to, before the storage chip 201 initiates, heat the storage chip 201 and determine whether the temperature detected by the temperature detection unit 203 reaches a specified threshold, and, if the temperature reaches the specified threshold, control the storage chip 201 to initiate.

[0043] The storage chip 201 may be a memory that can perform data write, data read, and/or data deletion. The storage chip 201 may be formed by using a semiconductor integrated production process. Specifically, the storage chip 201 may include a storage array and a peripheral circuit connected to the storage array. The storage array may include several storage units, and a bit line, a word line, and a metal connection line (metal contact part) that are connected to each storage unit. The storage unit may be configured to store data. The peripheral circuit may be a related circuit used when performing an operation on the storage array. In some embodiments, the storage chip 201 may be a DRAM storage chip. The DRAM storage chip may include several storage units. Each of the storage units may include a capacitor and a transistor. The gate of the transistor may be connected to a word line, the drain of the transistor may be connected to a bit line, and the source of the transistor may be connected to the capacitor. In some embodiments, the storage chip 201 may be other types of storage chips.

[0044] The number of storage chips 201 may be at least 1. Specifically, the number of storage chips 201 may be 1 or greater than or equal to 2. When the number of storage chips is greater than or equal to 2, the storage chips may be sequentially stacked vertically to form a stacked storage chip structure. Referring to FIG. 2, in some embodiments, the number of storage chips 201 may be 4. The four storage chips 201 may be sequentially stacked from bottom to top to form a stacked storage chip structure. Adjacent storage chips 201 may be bonded together through a bonding process or an adhering process. In some embodiments, a through-silicon via (TSV) may be formed in the storage chip 201. The storage chip 201 may be electrically connected to the control chip 301 through the through-silicon via (TSV). When multiple storage chips 201 are stacked, each storage chip 201 may be connected to the control chip 301 through a different through-silicon via (TSV). In some embodiments, the storage chip 201 may be alternatively connected to the control chip 301 by using a metal lead (formed by a lead bonding process).

[0045] In some embodiments, the storage chip 201 may be located on the control chip 301 and electrically connected to the control chip 301. When there is only one storage chip 201, the control chip 301 may be bonded to the storage chip 201. When there are multiple storage chips 201 forming a stacked storage chip structure, the control chip 301 may be bonded to the storage chip 201 at the bottom layer in the stacked structure.

[0046] In some embodiments, the storage chip 201 and the control chip 301 may be connected in different manners. Referring to FIG. 4 (or referring to FIGs. 4, 5, 6, and 7), the semiconductor structure may further include a line substrate 401. The line substrate 401 may have a connection line. The storage chip 201 and the control chip 301 may both be located on the line substrate 401, and the storage chip 201 and the control chip 301 may be connected by using the connection line in the line substrate 401. The line substrate 401 may be a PCB substrate.

[0047] Referring to FIGs. 1 and 4, the control chip 301 may be formed by using the semiconductor integrated production process. The control chip 301 may be configured to heat the storage chip 201, so that the temperature of the storage chip 201 can reach the specified threshold. The specified threshold may be set in the control chip 301 based on an actual need or experience. The control chip 301 may be further configured to control the initiation of the storage chip 201 and perfrom related operations on the storage chip 201. The initiation of the strorage chip may include power-on and self-testing. The performing of related operations on the storage chip 201 may include writing data into the storage chip 201, reading data from the storage chip 201, deleting data stored in the storage chip 201, and the like.

[0048] The semiconductor structure may further include the temperature detection unit 203. The temperature detection unit 203 may be configured to measure the temperature of the storage chip 201 before the storage chip 201 initiates. The temperature detection unit 203 may be electrically connected to the control chip 301. The temperature detected by the temperature detection unit 203 may be sent to the control chip 301, and may serve as the basis for controlling, by the control chip 301, the storage chip 201 to initiate. Specifically, the control

chip 301 may be configured to cooperate with the temperature detection unit 203. The control chip 301 may heat the storage chip 201 before the storage chip 201 initiates. The temperature detection unit 203 may detect the temperature of the storage chip 201 before the storage chip 201 initiates. And the control chip 301 may determine whether the temperature detected by the temperature detection unit 203 reaches the specified threshold, and, if the temperature reaches the specified threshold, control the storage chip 201 to initiate. Therefore, when the semiconductor structure provided in the present disclosure works at a low temperature, the storage chip 201 may be heated to the specified threshold by using the control chip 301, thereby preventing an increase of the resistances of the bit line, the word line, and the metal connection line (metal contact part) in the storage chip due to an excessively low temperature, reducing the write time for writing data into the memory at the low temperature, and improving the write stability of the memory.

[0049] The temperature detection unit 203 may include a temperature sensor. The temperature sensor may be configured to sense a temperature and convert the sensed temperature into an electrical signal. In some embodiments, the temperature sensor may be a P-N junction temperature sensor or a capacitive temperature sensor. The temperature sensor may be formed by using the semiconductor integrated production process, and may be located in the storage chip 201, in the control chip 301, or located on the line substrate 401 between the storage chip 201 and the control chip 301, as shown in FIG. 5.

[0050] The number of temperature detection units 203 may be 1 or greater than or equal to 2. The temperature detection unit 203 may be in the control chip 301 or in the storage chip 201.

[0051] In some embodiments, the number of temperature detection units 203 may be 1. Specifically, the temperature detection unit 203 may be in the control chip 301, as shown in FIGs. 1 and 4. Alternatively, the temperature detection unit 203 may be in the storage chip 201. When there is only one storage chip 201, the temperature detection unit 203 may be directly located in the storage chip 201. When there are multiple storage chips 201 forming a stacked structure, the temperature detection unit 203 may be located in one of the storage chips 201, and may be preferably located in the storage chip 201 at the bottom layer in the stacked structure, as shown in FIGs. 2 and 6. The temperature detection unit 203 may be on the line substrate 401 between the storage chip 201 and the control chip 301, as shown in FIG. 5. Upon determining that the temperature detected by the temperature detection unit 203 reaches the specified threshold, the control chip 301 may control all storage chips 201 to initiate. When there are multiple storage chips 201 in the semiconductor structure, the aforementioned control structure and control manner may be relatively simple, and may reduce the write time for writing data into the storage chip 201 at a low temperature and improve the write stability of the storage chip 201.

[0052] In some embodiments, referring to FIG. 1 (or referring to FIGs. 2, 4, 5, and 6), the number of temperature detection units 203 may be 1 and the number of storage chips 201 may be greater than or equal to 2. Upon determining that the temperature detected by the temperature detection unit 203 reaches the specified threshold, the control chip 301 may first control the storage chip 201 closest to the control chip 301 to initiate, and then control other storage chips 201 above the storae chip 201 to sequentially initiate. Referring to FIG. 2, when there are four storage chips 201, upon determining that the temperature detected by the temperature detection unit 203 reaches the specified threshold, the control chip 301 may first control the storage chip 201 closest to the control chip 301 (the storage chip at the bottom layer in the stacked structure) to initiate, and then control the other three storage chips 201 above to sequentially initiate. When there are multiple storage chips 201 in the semiconductor structure, the aforementioned control structure and control manner may cause each storage chip 201 to initiate after the specified threshold temperature is reached, thereby improving the precision of the initiation of each storage chip 201, reducing the write time for writing data into each storage chip 201 at a low temperature and improving the write stability of each storage chip 201.

[0053] In some embodiments, referring to FIG. 3 (or referring to FIG. 7), the number of temperature detection units 203 may be greater than or equal to 2 and the number of storage chips 201 may be greater than or equal to 2. Each storage chip 201 may have one temperature detection unit 203. The control chip 301 may sequentially determine whether a respective temperature detected by each of the temperature detection units 203 reaches the specified threshold, and, if the temperature detected by one of the temperature detection units 203 reaches the specified threshold, control the storage chip corresponding to the temperature detection unit 203 to initiate. There may be four storage chips 201 in a stacked structure, as shown in FIG. 3 (or FIG. 7), and each storage chip 201 may correspondingly have one temperature detection unit 203. Therefore, each temperature detection unit 203 may detect a respective temperature of a corresponding storage chip 201, thereby obtaining four detected temperatures. The control chip 301 may sequentially determine whether a respective temperature detected by each of the four temperature detection units 203 reaches the specified threshold, and, if the temperature detected by one of the temperature detection units 203 reaches the specified threshold, control the storage chip corresponding to the temperature detection unit 203 to initiate. For example, when the temperature detected by the temperature detection unit 203 in the storage chip 201 at the bottom layer in the stacked structure first reaches the specified threshold, the control chip 301 may first control the storage chip 201 at the bottom layer in the stacked

structure to initiate. Then, when the temperature detected by the corresponding temperature detection unit 203 in the storage chip 201 at the penultimate layer in the stacked structure also reaches the specified threshold, the control chip 301 may control the storage chip 201 at the penultimate layer in the stacked structure to initiate. The initiation of the storage chips 201 on the two upper layers may be conducted in the same manner. When there are multiple storage chips 201 in the semiconductor structure, the aforementioned control structure and control manner may further improve the precision of the of each storage chip 201, reduce the write time for writing data into each storage chip 201 at a low temperature and improve the write stability of each storage chip 201.

[0054] In some embodiments, before the control chip 301 heats the storage chip 201, the control chip 301 may need to initiate. In one example, the control chip 301 may need to be powered on and self-tested. When the control chip 301 initiates, the control chip 301 may not give an instruction to the storage chip 201. Only when the temperature detected by the temperature detection unit reaches the specified threshold, the control chip 301 may control the storage chip 201 to initiate. The control chip 301 may heat the storage chip using the heat generated by the control chip 301 after the control chip 301 initiates. Therefore, no additional heating circuit may be needed, thereby simplifying the semiconductor structure.

[0055] In some embodiments, after the control chip 301 controls the storage chip 201 to initiate, the control chip 301 may further control the storage chip 201 to perform write, read, and erase operations. The control chip 301 may have a control circuit. The control circuit may be configured to control the storage chip 201 to initiate and control the storage chip 201 to perform write, read, and erase operations.

[0056] In some embodiments, the control chip 301 may have a heating circuit, configured to heat the storage chip 201. Before or after the control chip 301 heats the storage chip 201, the control chip may determine whether the temperature of the storage chip detected by the temperature detection unit reaches the specified threshold. If the temperature does not reach the specified threshold, the control chip may control the heating circuit to heat the storage chip. If the temperature reaches the specified threshold, the control chip may control the heating circuit to stop heating the storage chip. Therefore, the heating process may be accurately controlled, so that the temperature of the storage chip 201 can be kept near the specified threshold, thereby preventing the temperature of the storage chip 201 from being excessively high or low, and preventing the write time of the memory from being prolonged under undesirable temperatures.

[0057] This invention further presents a semiconductor structure preheating method. Referring to FIG. 8, the method may include the following steps S101 through S105.

[0058] In S101, a semiconductor structure may be provided. The semiconductor structure may include a storage chip, a control chip electrically connected to the storage chip, and a temperature detection unit.

[0059] In S102, the control chip may initiate.

[0060] In S103, before the storage chip initiates, the storage chip may be heated by the control chip.

[0061] In S104, the temperature of the storage chip may be detected by the temperature detection unit.

[0062] In S105, the control chip may determine whether the temperature detected by the temperature detection unit reaches a specified threshold, and, if the temperature reaches the specified threshold, control the storage chip to initiate.

[0063] In some embodiments, the number of temperature detection units may be 1 or greater than or equal to 2, and the number of storage chips may be 1 or greater than or equal to 2. When the number of storage chips is greater than or equal to 2, several storage chips may be sequentially stacked vertically.

[0064] In some embodiments, the number of temperature detection units may be 1. Upon determining that the temperature detected by the temperature detection unit reaches the specified threshold, the control chip may control all storage chips to initiate.

[0065] In some embodiments, the number of temperature detection units may be 1 and the number of storage chips may be greater than or equal to 2. Upon determining that the temperature detected by the temperature detection unit reaches the specified threshold, the control chip may first control the storage chip closest to the control chip to initiate, and then control other storage chips above the storage chip to sequentially initiate.

[0066] In some embodiments, the number of temperature detection units may be greater than or equal to 2 and the number of storage chips may be greater than or equal to 2. Each storage chip may have one temperature detection unit. The control chip may sequentially determine whether a respective temperature detected by each of the temperature detection units reaches the specified threshold, and, if the temperature detected by one of the temperature detection units reaches the specified threshold, control the storage chip corresponding to the temperature detection unit to initiate.

[0067] In some embodiments, after the control chip controls the storage chip to initiate, the control chip may further control the storage chip to perform write, read, and erase operations.

[0068] The limitation or description of the same or similar part in the embodiments of the method compared to the foregoing embodiments of the semiconductor structure will not be described repeatedly, the details of which may be referred to a corresponding part in the foregoing semiconductor structure embodiments.

[0069] Although the present disclosure has been disclosed above in the preferred embodiments, such preferred embodiments are not intended to limit the present disclosure. Any person skilled in the art may make a possible change and modification to the technical solutions of the present disclosure based on the foregoing dis-

closed method and technical content without departing from the spirit and scope of the present disclosure. Therefore, any simple alteration, equivalent change, and modification made to the foregoing embodiments based on the technical essence of the present disclosure without departing from the content of the technical solutions of the present disclosure fall within the protection scope of the technical solutions of the present disclosure.

Claims

1. A semiconductor structure, comprising:

a storage chip;
a temperature detection unit, configured to detect a temperature of the storage chip before the storage chip initiates; and
a control chip, configured to:

before the storage chip initiates, heat the storage chip,
determine whether the temperature detected by the temperature detection unit reaches a specified threshold, and,
in response to the temperature reaching the specified threshold, control the storage chip to initiate.

2. The semiconductor structure of claim 1, wherein the semiconductor structure comprises one or more storage chips, and, when the semiconductor structure comprises two or more storage chips, the two or more storage chips are sequentially stacked vertically.

3. The semiconductor structure of claim 2, wherein the one or more storage chips are located on the control chip and electrically connected to the control chip.

4. The semiconductor structure of claim 2, further comprising:
a line substrate comprising a connection line, the one or more storage chips and the control chip are both located on the line substrate, and the one or more storage chips and the control chip are connected through the connection line in the line substrate.

5. The semiconductor structure of claim 3 or 4, wherein the semiconductor structure comprises one or more temperature detection units electrically connected to the control chip, and the one or more temperature detection units are located:

in the control chip;
in the one or more storage chips; or
on the line substrate between the one or more storage chips and the control chip.

6. The semiconductor structure of claim 5, wherein, when the semiconductor structure comprises only one temperature detection unit, the control chip is configured to:
upon determining that the temperature detected by the temperature detection unit reaches the specified threshold, control all the one or more storage chips to initiate.

7. The semiconductor structure of claim 5, wherein, when the semiconductor structure comprises only one temperature detection unit and two or more storage chips, the control chip is configured to:
upon determining that the temperature detected by the temperature detection unit reaches the specified threshold, first control the storage chip closest to the control chip to initiate, and then control other storage chips on the storage chip to sequentially initiate.

8. The semiconductor structure of claim 5, wherein, when the semiconductor structure comprises two or more temperature detection units and two or more storage chips, each storage chip has one temperature detection unit, and wherein the control chip is configured to:

sequentially determine whether a respective temperature detected by each of the temperature detection units reaches the specified threshold; and
in response to the temperature detected by one of the temperature detection units reaching the specified threshold, control the storage chip corresponding to the temperature detection unit to initiate.

9. The semiconductor structure of claim 1, wherein the control chip is further configured to:
after the storage chip initiates, control the storage chip to perform write, read, and erase operations.

10. The semiconductor structure of claim 9, wherein the control chip initiates before the control chip heats the storage chip, and the control chip is configured to heat the storage chip using heat generated by the control chip after the control chip initiates.

11. The semiconductor structure of claim 1, wherein the control chip comprises a heating circuit configured to heat the storage chip.

12. The semiconductor structure of claim 11, wherein the control chip is configured to:

before or after the control chip heats the storage chip, determine whether the temperature of the storage chip detected by the temperature detection unit reaches the specified threshold; and

in response to the temperature not reaching the specified threshold, control the heating circuit to heat the storage chip; or
in response to the temperature reaching the specified threshold, control the heating circuit to stop heating the storage chip.

13. The semiconductor structure of claim 1, wherein the storage chip is a Dynamic Random Access Memory (DRAM) chip.

14. A semiconductor structure preheating method, comprising:

providing a semiconductor structure, wherein the semiconductor structure comprises a storage chip, a control chip electrically connected to the storage chip, and a temperature detection unit;
initiating the control chip;
heating, by the control chip and before the storage chip initiates, the storage chip;
detecting, by the temperature detection unit, a temperature of the storage chip;
determining, by the control chip, whether the temperature detected by the temperature detection unit reaches a specified threshold; and
in response to the temperature reaching the specified threshold, initiating the storage chip.

15. The preheating method of claim 14, wherein the semiconductor structure comprises one or more temperature detection units and one or more storage chips, and wherein when the semiconductor structure comprises two or more storage chips, the two or more storage chips are sequentially stacked vertically.

16. The preheating method of claim 15, wherein, when the semiconductor structure comprises only one temperature detection unit, the control chip is configured to:

upon determining that the temperature detected by the temperature detection unit reaches the specified threshold, control all the one or more storage chips to initiate.

17. The preheating method of claim 15, wherein, when the semiconductor structure comprises only one temperature detection unit and two or more storage chips, the control chip is configured to:
upon determining that the temperature detected by the temperature detection unit reaches the specified threshold, first control the storage chip closest to the control chip to initiate, and then controls other storage chips on the storage chip to sequentially initiate.

18. The preheating method of claim 15, wherein, when the semiconductor structure comprises two or more temperature detection units and two or more storage chips, each storage chip has one temperature detection unit, and wherein the control chip is configured to:

sequentially determine whether a respective temperature detected by each of the temperature detection units reaches the specified threshold; and
in response to the temperature detected by one of the temperature detection units reaching the specified threshold, control the storage chip corresponding to the temperature detection unit to initiate.

19. The preheating method of claim 14, wherein the control chip is further configured to:
after the storage chip initiates, control the storage chip to perform write, read, and erase operations.

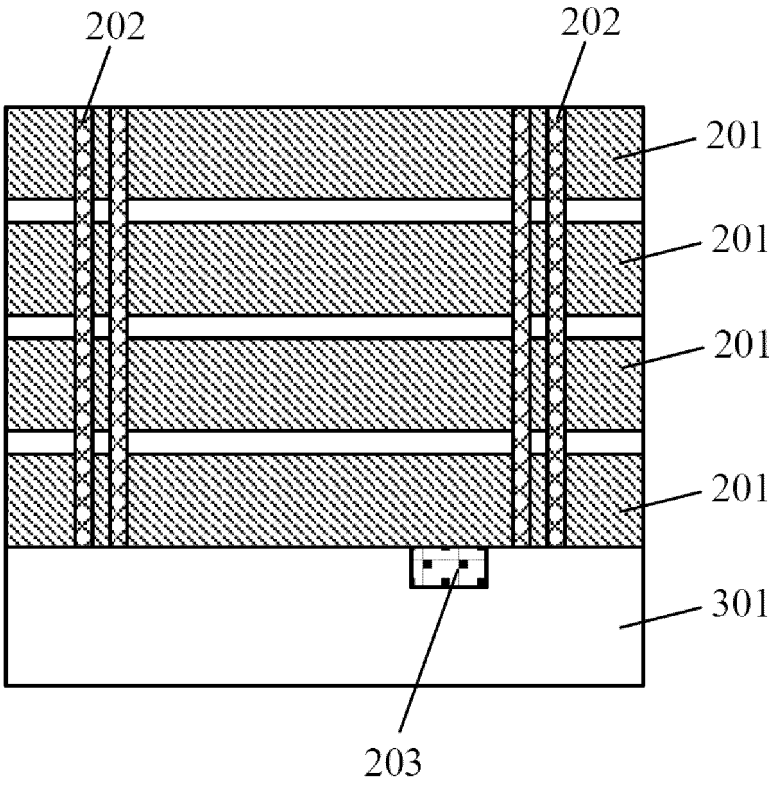

FIG. 1

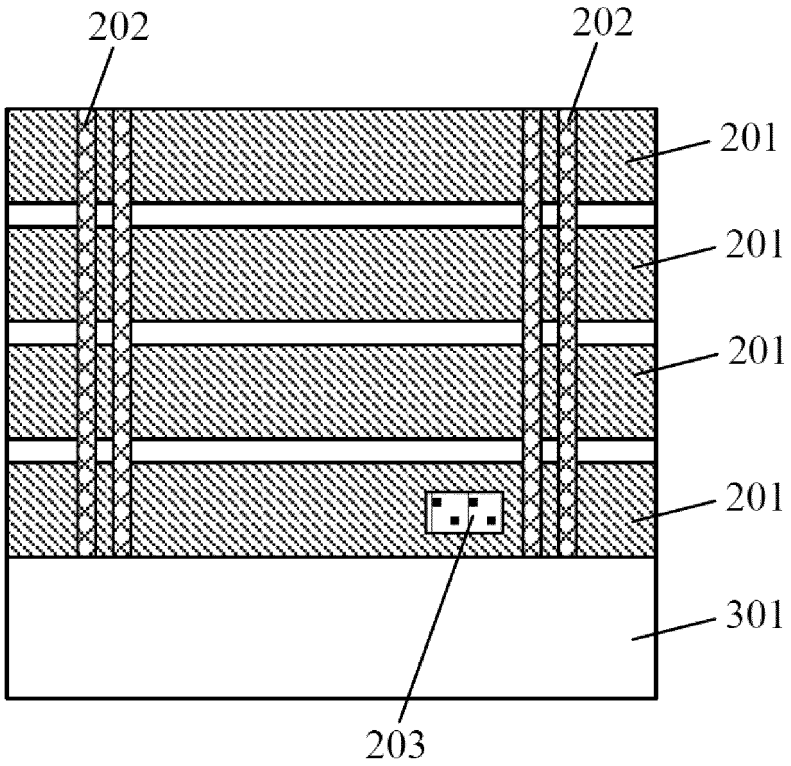

FIG. 2

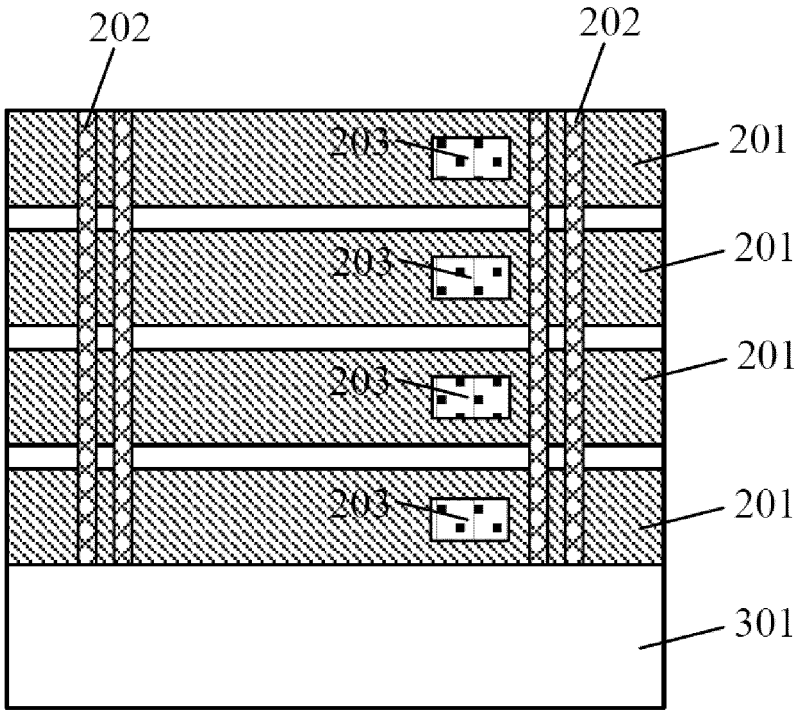

FIG. 3

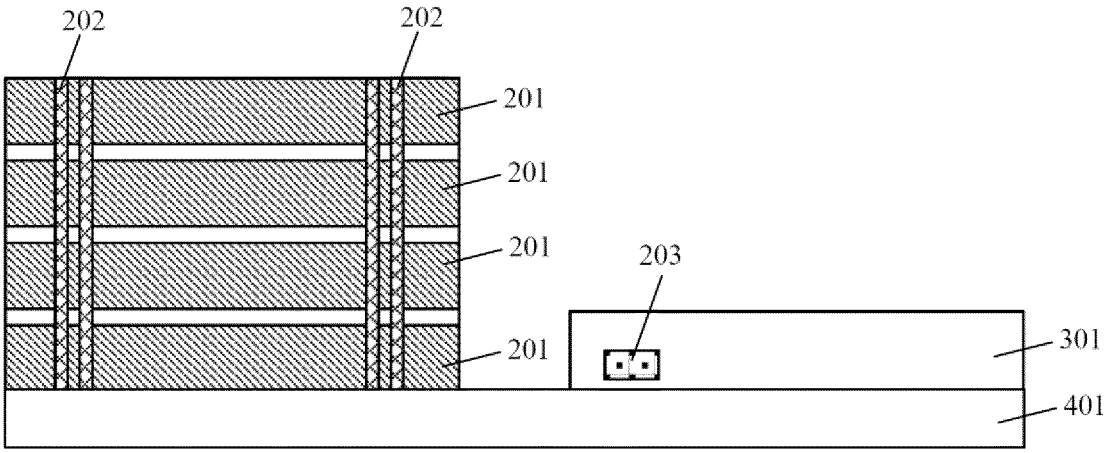

FIG. 4

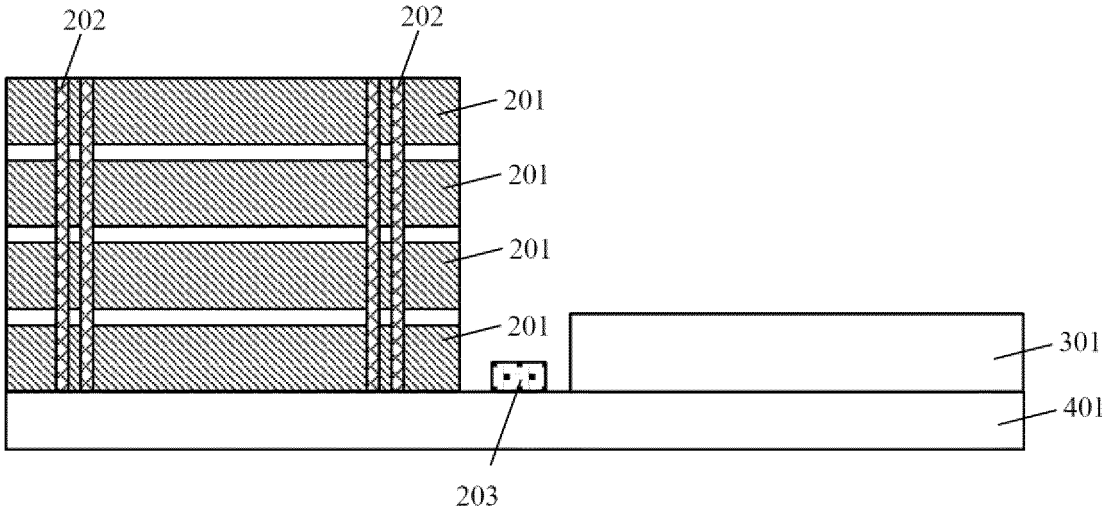

FIG. 5

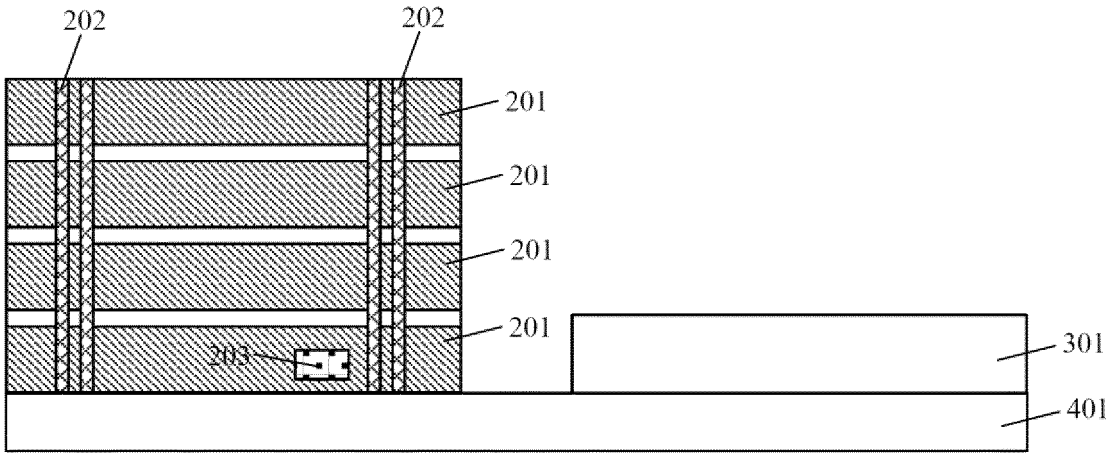

FIG. 6

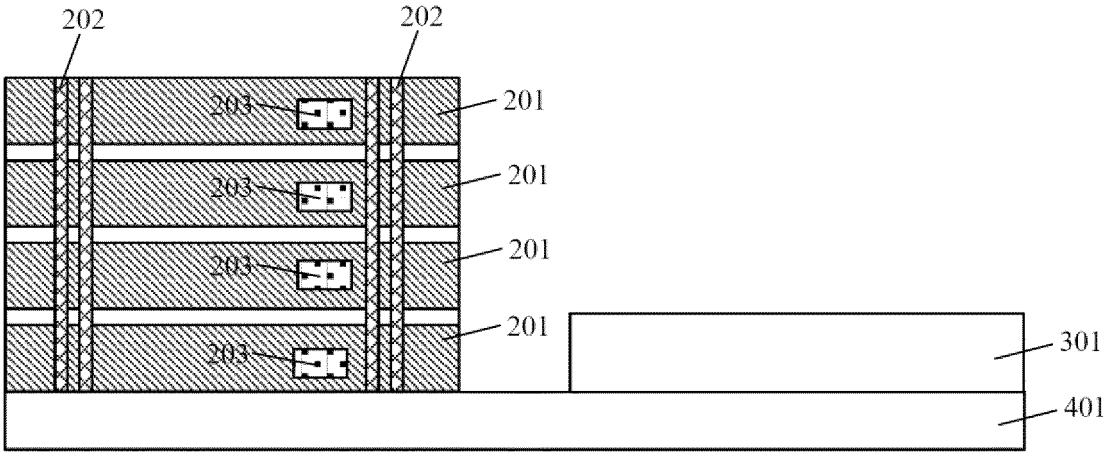

FIG. 7

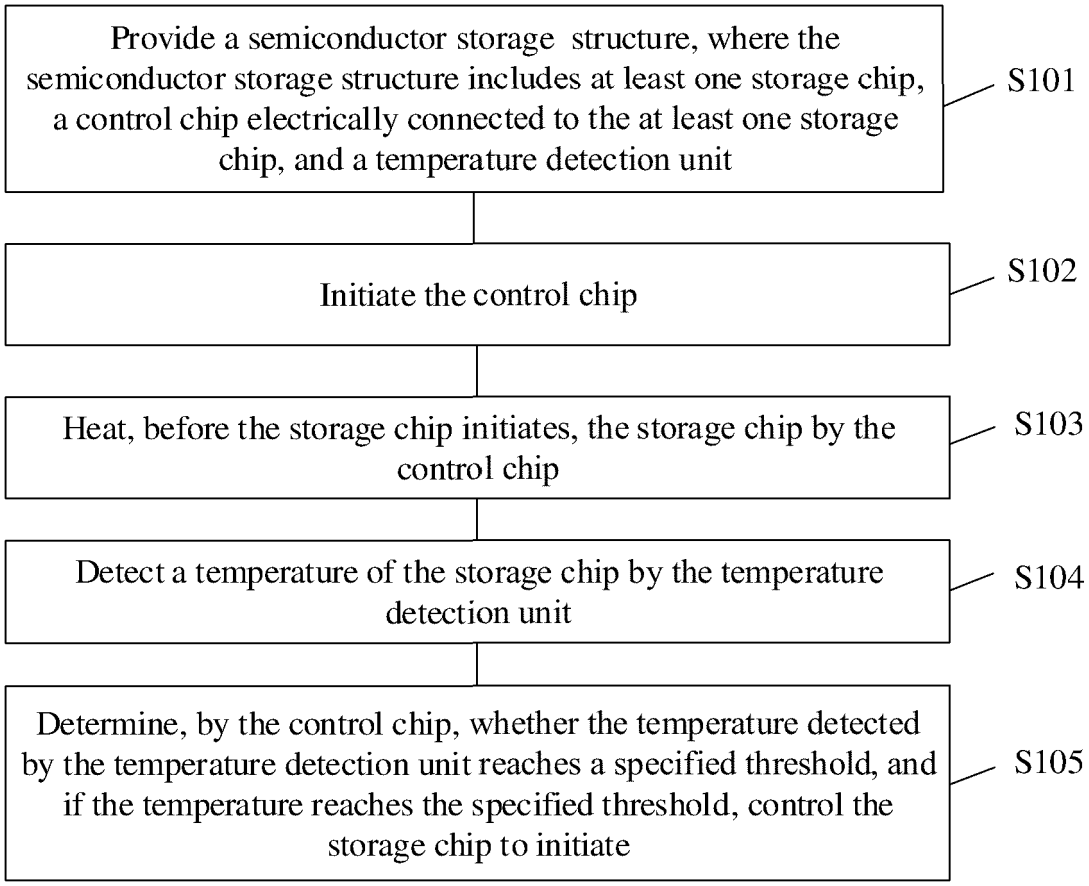
Provide a semiconductor storage structure, where the semiconductor storage structure includes at least one storage chip, a control chip electrically connected to the at least one storage chip, and a temperature detection unit
S101
Initiate the control chip
S102
Heat, before the storage chip initiates, the storage chip by the control chip
S103
Detect a temperature of the storage chip by the temperature detection unit
S104
Determine, by the control chip, whether the temperature detected by the temperature detection unit reaches a specified threshold, and if the temperature reaches the specified threshold, control the storage chip to initiate
S105

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2020/131414

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/108(2006.01)i; G11C 11/401(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L27/-;G11C11/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS; CNTXT; VEN; USTXT; EPTXT; WOTXT; CNKI: 加热, 预热, 温度, 检测, 感测, 传感器, 稳定, 低温, 存储, 动态随机存取存储器, heat, warm up, temperature, detect, sensor, stability, low temperature, memory, DRAM

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 211507637 U (CHANGXIN MEMORY TECHNOLOGIES, INC.) 15 September 2020 (2020-09-15) claims 1-13, description, paragraphs 35-62 and figures 1-8	1-19
E	CN 212303077 U (CHANGXIN MEMORY TECHNOLOGIES, INC.) 05 January 2021 (2021-01-05) description, paragraphs 1, 39-96	1-19
E	CN 212303079 U (CHANGXIN MEMORY TECHNOLOGIES, INC.) 05 January 2021 (2021-01-05) description, paragraphs 1, 38-89 and figures 1-6	1-19
E	CN 212303078 U (CHANGXIN MEMORY TECHNOLOGIES, INC.) 05 January 2021 (2021-01-05) description, paragraphs 1, 37-80 and figures 1-6	1-19
X	CN 107810530 A (WESTERN DIGITAL TECHNOLOGIES, INC.) 16 March 2018 (2018-03-16) claims 1-9, description, paragraphs 26-66 and figure 1	1-19

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 February 2021	**23 February 2021**
Name and mailing address of the ISA/CN **China National Intellectual Property Administration (ISA/CN)** **No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing 100088** **China** Facsimile No. **(86-10)62019451**	Authorized officer Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2020/131414

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	JP 2018097903 A (FUJITSU LTD.) 21 June 2018 (2018-06-21) entire document	1-19
A	CN 101866690 A (ACER INC.) 20 October 2010 (2010-10-20) entire document	1-19

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2020/131414

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
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CN	212303079	U	05 January 2021	None			
CN	212303078	U	05 January 2021	None			
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				CN	107810530	B	06 December 2019
				EP	3295458	B1	14 August 2019
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				US	9668337	B2	30 May 2017
				US	2017071056	A1	09 March 2017
				EP	3295458	A1	21 March 2018
				EP	3557578	A1	23 October 2019
				US	10021777	B2	10 July 2018
				WO	2017044339	A1	16 March 2017
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				JP	6756965	B2	16 September 2020
				US	10224078	B2	05 March 2019
CN	101866690	A	20 October 2010	CN	101866690	B	24 July 2013

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REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- CN 202010216794 **[0001]**