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(54) Silicon MOSFET doped with germanium to increase lifetime of operation.

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PATENT ABSTRACTS OF JAPAN vol. 11, no. 31 (E-475)(2478) 29 January 1987 ; & JP-A-61 198 681
PATENT ABSTRACTS OF JAPAN vol. 9, no. 61 (E-303)(1784) 19 March 1985 ; & JP-A-59 200 467

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Description

Technical Field

This invention relates to semiconductor devices and more particularly to transistor device structures in integrated circuits and to methods for making such structures.

Background of the Invention

It is known in the art that semiconductor devices, particularly both bipolar and MOS (metal oxide semiconductor) transistor devices, tend to degrade with use. That is, for example, the transconductances G_M of these devices undesirably continue to decrease after continued operation in the circuits. More specifically, for a given MOS transistor, a higher drain-to-source voltage V_{DS} causes a higher rate of undesirable reduction of G_M and hence a lower lifetime of useful operation (operational lifetime) of the transistor.

Each such device subject to this degradation is incorporated in a semiconductor body, typically silicon; and the device comprises a p-n junction, formed by the interface of two regions of the semiconductor body, one of the regions having a relatively high concentration of (conductivity-type determining) donor or acceptor impurities, the other having a relatively low concentration of acceptor or donor impurities, respectively—i.e., a p^+n or an n^+p junction, respectively. The p-n junction intersects the surface of the body at a location where the body is coated with an insulating layer. Degradation is believed to be caused by damage produced in the insulating layer by "hot" (fast-moving) charge carriers which are created in the region of relatively low impurity concentration, particularly in the neighborhood of the intersection of the p-n junction with the surface of the body. Accordingly, because of the higher electric fields which are ordinarily present in smaller sized devices and which cause a more severe hot charge carrier problem, smaller sized devices tend to have lower operational lifetimes.

In U.S. Patent No. 4,704,547 issued to H. Kirsch on November 3, 1987, entitled "IGFET Gating Circuit Having Reduced Electric Field Degradation," it was taught that the degradation of MOS transistors due to hot carriers could be alleviated in complementary transistor logic gates by the technique of inserting an extra (protective) transistor between the p-channel and n-channel transistors. However, the technique of that patent requires the added transistor, which may be undesirable from the standpoints of speed performance and of consuming precious semiconductor surface area, particularly in complex logic circuits; and the technique may not be convenient to use in the context of circuits other than complementary transistor logic gates and the like.

Another technique for reducing MOS transistor degradation is the lightly doped drain (LDD), in which the concentration of conductivity-type determining impurities is reduced in a neighborhood of the drain. However, in this technique unwanted added series resistance in the drain outside the transistor channel is unavoidable, whereby the switching speed of the transistor is undesirably reduced, especially when the added resistance is comparable to the resistance of the channel itself, as is the case where the channel length is approximately 0.5 micrometer or less.

Yet another technique for coping with the hot carrier problem is a reduction in drain-source operating voltages. This technique, however, entails not only loss of speed but also a reduction in tolerable noise margins. Moreover, in case the channel length goes to approximately 0.5 micrometer or less, the reduction in drain-source operating voltages would present a serious obstacle to the use of Bipolar Complementary MOS (BiCMOS) circuits because of the higher minimum operating voltage requirements of the bipolar transistors in such circuits.

It would therefore be desirable to have a technique for reducing the rate of degradation (increase the operational lifetime) of MOS transistors, which does not suffer from the aforementioned problems.

EP-A-0419256, which forms part of the state of the art by virtue of Article 54(3)EPC, discloses a MOSFET doped with carbon in the channel region at the interface with the gate oxide to suppress hot electron trapping. The concentration is in the range 10^{18} - $10^{20}cm^{-3}$.

Patent Abstracts of Japan, vol.11, no.31 (E-475) (2478) 29th January 1987 (JP-A-61-198681) discloses a MOS device with Ne, Ar, Kr or Xe implanted into the portions of the source and drain regions adjacent to the channel, to prevent hot electrons from being trapped in the gate oxide layer.

US-A-4837173 discloses implantation of Ge ions near the location of the source and drain regions at a dose of $10^{15}cm^{-2}$.

Summary of the Invention

The aforementioned problems in the prior art techniques for increasing the operating lifetime (reducing the rate of degradation) of a semiconductor device, incorporated in a semiconductor body at a major surface thereof and having a p-n junction which intersects the major surface, are alleviated in a transistor as set out in claim 1.

It is believed that this decrease in degradation is attributable--for example, in MOS transistors--to a prevention of the formation of hot charge carriers at or near the drain, or both, by virtue of scattering of the carriers by the germanium atoms. It is theorized that this scattering reduces the number of hot charge carriers that can penetrate to the insulating layer, where

the hot carriers damage the insulating layer and degrade device performance. Because they are neutral, moreover, the added germanium atoms apparently do not significantly reduce the desirable mobility of charge carriers in the channel. However, it should be understood that the successful results obtained in this invention do not depend upon the correctness of any theory.

Advantageously, in order to ensure p-n junctions that are shallow, any required relatively high temperature annealing of the neutral germanium region can be (but not necessarily) performed prior to implanting the conductivity-type determining impurity required to form the p-n junction (which thereafter generally requires a relatively low-temperature annealing).

Brief Description of the Drawing

FIG. 1 is a cross-section diagram of an MOS transistor device in accordance with a specific embodiment of the invention;

FIG. 2 is a cross-section diagram of an MOS transistor device in accordance with another specific embodiment of the invention; and

FIG. 3 is a cross-section diagram of an MOS transistor device in accordance with yet another specific embodiment of the invention.

Only for the sake of clarity, none of the drawings is to scale. Elements in different FIGURES which are substantially the same are denoted by the same reference numerals.

Detailed Description

As shown in FIG. 1 an n-channel MOS transistor device structure 100 includes a portion 10 of a p-type silicon semiconductor body. Upon a top major surface 10.5 of this body 10 are located a relatively thick field oxide layer 11 and a thin gate oxide layer 12. Typically this gate oxide layer 12 has a thickness of about 12 nanometer or less for a channel length (gate oxide length) of about 0.8 micrometer or less. Upon the gate oxide layer 12 is located an n^+ polycrystalline silicon gate electrode 13, as known in the art. Source and drain regions 14 and 15, respectively, are of n^+ type conductivity, typically as formed by ion implantation of 80 keV arsenic followed by annealing, typically at about 900 degrees C for about 10 minutes. Metal or metal silicide source and drain electrodes (not shown) are typically attached to the respective surfaces of the source and drain regions, to complete the transistor device 100 and to supply it with electrical access to the rest of the circuit (not shown) integrated in the silicon body.

As thus far described, the transistor device structure 100 is quite conventional. In accordance with this embodiment (FIG. 1) of the invention, however, the device structure 100 further comprises a neutral impurity region in the form of a germanium doped region 16 formed prior to definition or formation of the gate electrode 13 but subsequent to the formation and patterning of the field oxide 11. At that stage, the germanium region is formed, by example, by implantation with two doses of germanium ions, one having an energy of 25 keV and the other having an energy of 110 keV, using a standard source of germanium ions. Annealing is then performed at a temperature of about 950 degrees C, typically for approximately 30 to 60 minutes. Preferably, however, to ensure shallow source and drain junctions, this annealing of the germanium region, which is performed advantageously for a longer time or at a higher temperature (or both) than the annealing of the arsenic at the source and drain, is performed prior to formation--as by the arsenic implantation--of the source and drain region. Because of the relatively low diffusivity of germanium in silicon, this annealing does not significantly change the depth of the germanium doped region 16.

In another embodiment (FIG. 2) of the invention, an MOS transistor device structure 200 has a similar structure to that of the previously described transistor device 100 except the germanium is implanted subsequent to the formation of the gate, and either prior or subsequent to the formation of the source and drain regions 14 and 15; and, in addition to the 25 keV and 110 keV doses of germanium used for the previously described structure 100, a dose of 160 keV (or higher) germanium is implanted into the body 10 in order to ensure that a portion of the germanium region 26 extends outside the metallurgical p-n junction 25 of the drain region 15 laterally into and substantially all the way across the width of the channel (at the surface 10.5 underneath the gate oxide layer 12), where it can suppress hot charge carrier formation. Again, an annealing of the germanium region preferably is performed prior to source and drain implantation.

In yet another embodiment (FIG. 3) of the invention an MOS transistor device structure 300 has a similar structure to that of the previously described device structure 200 except for the presence of a side-wall oxide (or other insulator) layer 32. The implantation of arsenic to form the source and drain regions is performed subsequent to side-wall oxide formation; whereas the implantation of the germanium to form the germanium doped region 36 is performed prior to side-wall oxide layer formation, in order to ensure that a portion of the germanium region 36 extends outside the drain region 15 laterally into (and across) the channel. In view of the offset of the drain region 15 relative to the germanium doped region 36 caused by the side-wall oxide formation, there is no need for a 160 keV germanium dose in addition to the 25 and 110 keV doses. Again, preferably an annealing of the germanium region is performed prior to the implantation of the source and drain regions.

Transistor devices of the kind shown in FIGS. 1,2,

and 3 have been fabricated and successfully tested, and the implantations of germanium to concentration in the approximate range of $3x10^{17}$ to $1x10^{20}$ (3E17 to 1E20) per cubic centimeter have resulted in significant improvements (reductions) in the rate of degradation of the transconductance. More specifically, to obtain the germanium concentration of 3E17 per cubic centimeter, a dose of 1E12 per square centimeter of 25 keV germanium ions plus a dose of 3E12 per square centimeter of 110 keV germanium ions (plus a dose of 3E12 per square centimeter of 160 keV germanium ions in the case of the structure 200) can be used. To obtain the germanium concentration of 1E20 per cubic centimeter, a dose of 3E14 per square centimeter of 25 keV germanium ions plus a dose of 1E15 per square centimeter of 110 keV germanium ions can be used. It should be noted that doses of germanium in an amount above about 3E19 per cubic centimeter produce amorphous silicon; doses below that amount produce damaged silicon. Higher germanium concentration than 1E20 per cubic centimeter may prove to be useful in conjunction with higher annealing temperatures. It should be noted, however, that experiments performed thus far on structures of the kind shown in FIG. 1 have indicated that the germanium concentration in this kind of structure (but not in structures like 200 and 300) should be limited to not more than 1E19 per cubic centimeter.

Although the invention has been described in terms of specific embodiments, various modifications can be made without departing from the scope of the invention. For example, the polysilicon gate can be a p^+ polysilicon or a metal gate, instead of a n^+ polysilicon gate. Moreover, in addition to n-channel transistors, p-channel silicon MOS transistors similarly can benefit from neutral germanium regions in the neighborhood of the drain junction. Also both p-channel and n-channel transistor devices can be interconnected and integrated in the same silicon body, as known in the complementary MOS (CMOS) integrated circuit art, with either or both of these types of devices having the neutral germanium impurity regions described above, to reduce the rate of device degradation. In addition, MOS transistor devices of this invention can be interconnected and integrated with bipolar transistors in the same semiconductor body.

Also, a single annealing step can be used to repair simultaneously both the germanium and the arsenic damage at a temperature and for a time sufficient for repairing the damage due to the germanium implantation. However, in the case of fabricating a device of the kind shown in FIG. 2, the parameters of such a single annealing step must be carefully adjusted to ensure that in the device 200 the germanium region 26 extends beyond the metallurgical p-n junction 25 into the p-type silicon body 10 everywhere in a neighborhood of at least one-half the intersection of the metallurgical p-n junction 25 with the surface 10.5, such neighborhood thus extending laterally beyond the junction into the channel for a distance advantageously equal to at least approximately 0.01 micrometer.

Instead of ion implantation, other methods can be used for obtaining a germanium region in silicon, such as epitaxially growing germanium-doped-silicon (silicon doped with germanium). Finally instead of silicon MOS transistors, other semiconductor devices, such as bipolar transistors, or diodes that suffer from hot carrier degradation can be used in conjunction with the neutral impurity regions of this invention. In the case of such bipolar transistors or diodes, advantageously the neutral impurity region encompasses the regions of the devices where detrimental hot carriers are formed, particularly at or near (or both) an intersection of a p-n junction with a semiconductor surface.

Claims

1. A MOS transistor formed in a device region of a first conductivity type in a silicon substrate, said transistor comprising a drain region (15) in a surface region of said device region forming a pn-junction with the device region and having a higher impurity concentration than the device region, a channel contiguous with the drain region, a portion (16, 26, 36) of the device region containing germanium atoms, the concentration of germanium atoms in the portion being at least 3×10^{17} atoms/cm^3 and also being at least as high as the impurity concentration of the device region at the intersection of the pn-junction with the surface of the substrate, the portion being contiguous with at least one-half the intersection of said pn-junction with the surface (10.5) of the substrate, said portion extending laterally beyond the drain region into the channel for a distance of at least 0.01 µm.

2. The transistor of claim 1 in which an insulating layer (11, 12) overlies the surface of the substrate where the pn-junction intersects it.

3. An integrated circuit comprising the transistor recited in in claim 1 or 2.

Patentansprüche

1. MOS-Transistor, der in einem Bauteilbereich eines ersten Leitfähigkeitstyps in einem Siliciumsubstrat ausgebildet ist, wobei der Transistor einen Drain-Bereich (15) in einer Oberfläche des Bauteilbereichs umfaßt, welcher einen p-n-Übergang mit dem Bauteilbereich bildet und eine hö-

here Verunreinigungskonzentration hat als der Bauteilbereich, einen Kanal, der mit dem Drain-Bereich zusammenhängend ist, einen Abschnitt (16, 26, 36) des Bauteilbereichs, der Germaniumatome enthält, wobei die Konzentration der Germaniumatome in dem Abschnitt wenigstens 3 x 10^{17} Atome/cm^3 beträgt und ebenfalls wenigstens so hoch wie die Verunreinigungskonzentration des Bauteilbereichs am Schnittbereich des p-n-Übergangs mit der Oberfläche des Substrates ist, wobei der Abschnitt mit wenigstens einer Hälfte des Schnittbereichs des p-n-Übergangs mit der Oberfläche (10.5) des Substrates zusammenhängend ist, wobei sich der Abschnitt seitlich über den Drain-Bereich in den Kanal über einen Abstand von wenigstens 0,01 µm erstreckt.

2. Transistor nach Anspruch 1, bei welchem eine Isolierschicht (11, 12) über der Oberfläche des Substrats liegt, wo der p-n-Übergang diese schneidet.

3. Integrierte Schaltung umfassend den in Anspruch 1 oder 2 erwähnten Transistor.

Revendications

1. Un transistor MOS formé dans une région de dispositif d'un premier type de conductivité d'un substrat en silicium, ce transistor comprenant une région de drain (15) dans une région de surface de la région de dispositif, formant une jonction p-n avec la région de dispositif et ayant une concentration en impuretés supérieure à celle de la région de dispositif, un canal contigu à la région de drain, une partie (16, 26, 36) de la région de dispositif contenant des atomes de germanium, la concentration d'atomes de germanium dans cette partie étant au moins de 3 x 10^{17} atomes/cm^3 et étant également au moins aussi élevée que la concentration en impuretés de la région de dispositif à l'intersection de la jonction p-n avec la surface du substrat, la partie précitée étant contiguë à au moins la moitié de l'intersection de la jonction p-n avec la surface (10.5) du substrat, et cette partie s'étendant latéralement au-delà de la région de drain et à l'intérieur du canal sur une distance d'au moins 0,01 µm.

2. Le transistor de la revendication 1, dans lequel une couche isolante (11, 12) recouvre la surface du substrat à l'endroit auquel la jonction p-n la rencontre.

3. Un circuit intégré comprenant le transistor spécifié dans la revendication 1 ou 2.

FIG. 1

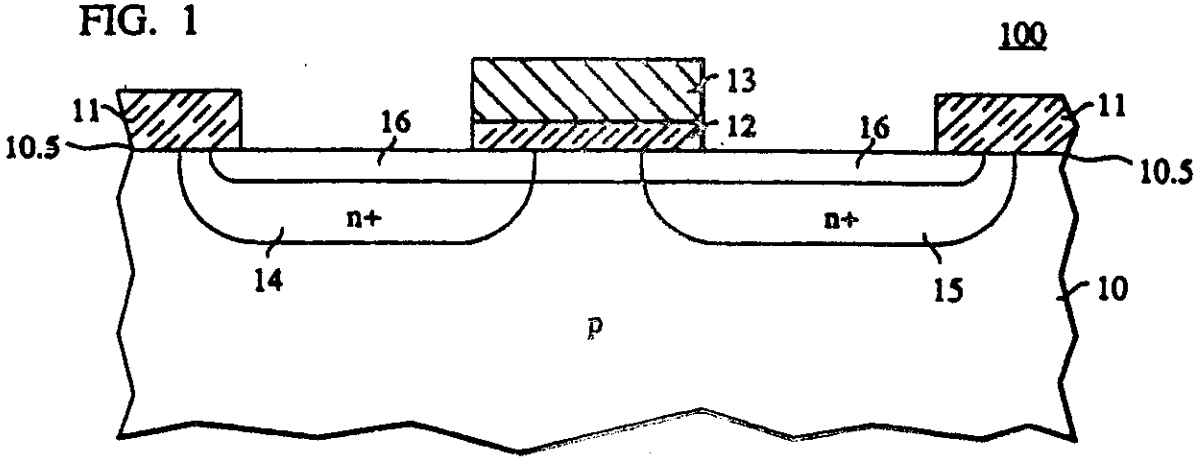


FIG. 2

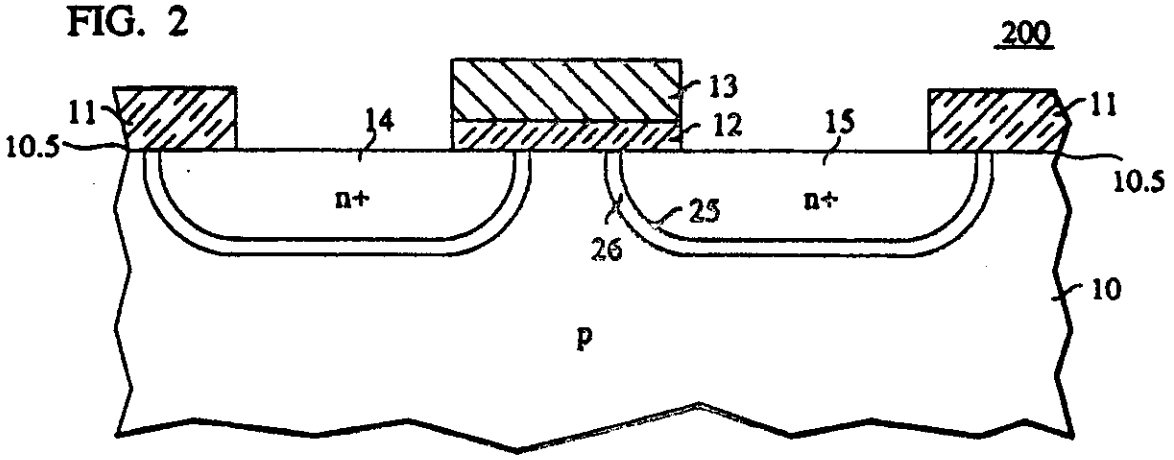
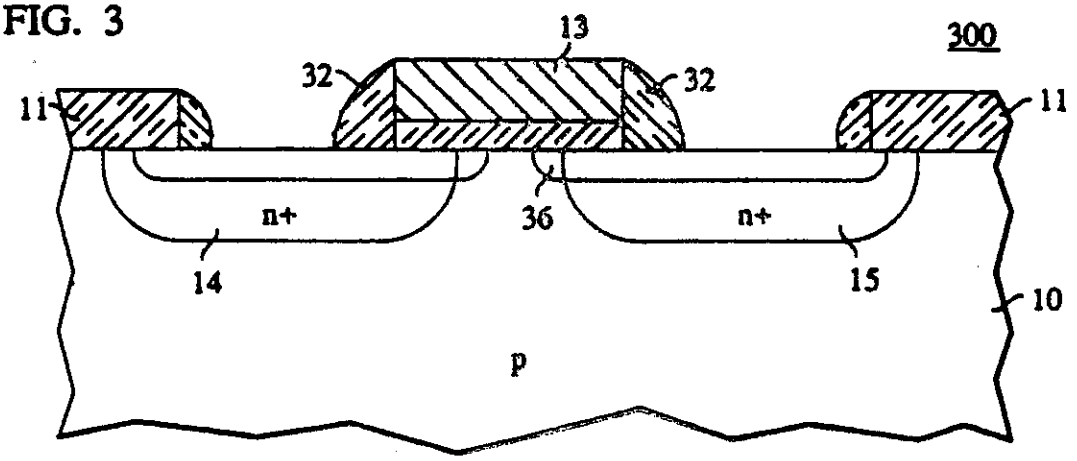


FIG. 3



REGISTER ENTRY FOR EP0419128

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Title NEUTRAL IMPURITIES TO INCREASE LIFETIME OF OPERATION OF SEMICONDUCTOR DEVICES.

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