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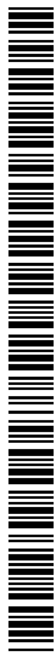

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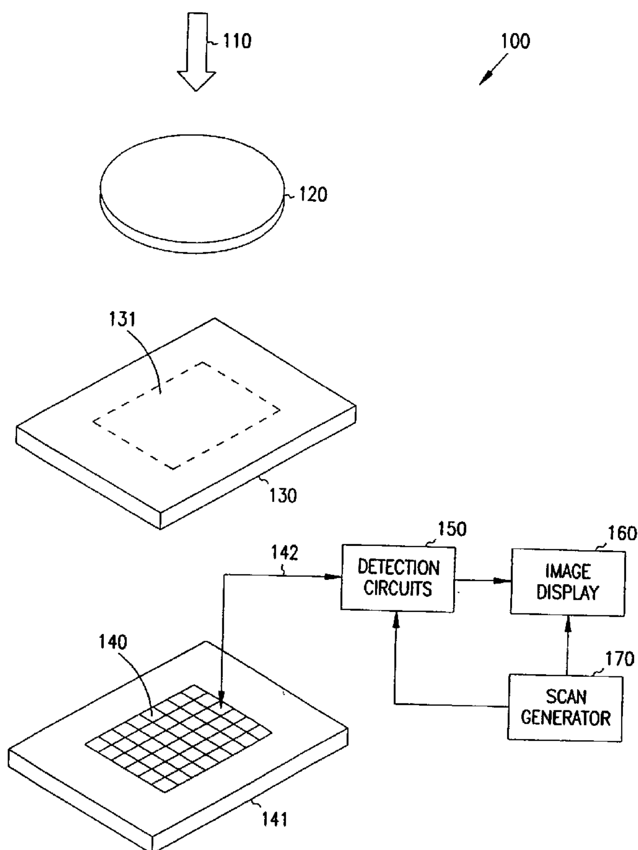

(57) Abstract: An infrared detector has a window in a cover having a cavity for exposing detector pixels to incident radiation. The window has an antireflective element formed within the cavity as a field of posts. The field of post structures is formed in a cavity by etching the posts in a desired pattern first, and forming the cavity by a general etch over the whole field afterward.

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INFRARED DETECTOR PACKAGED WITH IMPROVED ANTIREFLECTION ELEMENT

Technical Field

The present invention concerns thermal imaging, and more specifically concerns structures and methods for packaging arrays of infrared detectors.

Background

Night vision and related applications can be realized by receiving the infrared radiation emitted by warm bodies in an array of uncooled bolometer pixels or other detector whose electrical output signals are converted into a visible image.

An array of uncooled bolometers or similar detector on a semiconductor substrate must be packaged so as to protect the detector pixels from contamination and degradation. Many conventional integrated-circuit packaging techniques are not suitable because the face of the array must be exposed to incident radiation.

A package cover can be fabricated from a material that transmits infrared, such as silicon, to provide a window for a detector array. A cavity can be micromachined into the cover so that the cover can be sealed to a substrate holding the array. Evacuating the sealed cavity produces a vacuum that protects the array pixels and their circuitry on the substrate.

The high indices of refraction of infrared optical components causes large insertion losses. Many conventional infrared-detector packages employ antireflection layers or coatings for reducing insertion losses to a more acceptable level. However, when the optical element is a window is formed in a cavity, applying an effective antireflective element within the cavity is difficult. In addition to the performance degradation from the high temperatures required for many such coatings, it is difficult to achieve uniformity in a depressed surface such as a cavity.

Summary

An infrared detector according to the invention has a window in a cover having a cavity for exposing one or more detector pixels to incident radiation. The window has an antireflective element formed within the cavity as a field of posts having a height, spacing, and fill factor for achieving the desired optical effect in a wavelength range of interest.

In another aspect, the invention concerns fabricating an infrared optical element. A field of post structures is formed in a cavity by etching the posts in a desired pattern and forming the cavity by a general etch over the area of the field.

Drawing

Fig. 1 shows an infrared detector having a package according to the invention.

Fig. 2 is an isometric view of one of the pixels of Fig. 1.

Fig. 3 is a cross section of the package of Fig. 1, taken along line 3-3' in Fig. 1.

Fig. 4 is a flowchart of a method for making a detector package according to the invention.

Fig. 5 is a graph of the transmittance of the window of Figs. 1 and 3 over a range of wavelengths.

Detailed Description

Fig. 1 is a stylized exploded view of a representative infrared imaging detector 100 according to the invention. Arrow 110 represents infrared radiation produced by a warm body and transmitted to infrared imaging optics 120 of conventional design. Package cover 130 has a window area 131 transparent to infrared wavelengths for transmitting radiation 110. Sealing package 130 and evacuating the atmosphere therefrom is desirable in many applications to increase sensitivity and inter-pixel isolation, and to reduce contamination and degradation.

Bolometer array 140 within package 130 is fabricated on a substrate 141 of silicon or similar material having appropriate electrical and micromachining properties. (Alternatively, array 140 can be mounted upon a separate substrate 141.) Individual

pixels such as 200 are commonly disposed in rows and columns of a rectangular matrix, although a single line and other configurations are also employed. In many applications, array 140 operates at ambient temperatures, e.g., in the approximate range of -40°C to +100°C. It is possible, however, to operate the array at much lower temperatures, e.g., below about 2K to 20K, either by cooling the array or by operating it in an environment such as space. Row and column wiring 142 reads out the electrical signals representing the temperature of each individual pixel such as 200, and may also introduce scanning signals for time-multiplexing the pixel signals.

Detection circuits 150 process an image signal from detector 140, performing functions such as amplifying and demultiplexing the pixel signals. Unit 160 receives the processed signals and presents a visible image to a viewer. In other embodiments, unit 160 might be replaced or augmented by a recorder or other device for storing signals representing one or more successive images, or for other processing of the signals; the term "display" will be taken broadly to include any or all of these functions. Scan generator 170 can be included for multiplexing the pixel signals and/or for controlling the display or processing of images on unit 160. System 100 represents an example environment for the present invention; others are possible.

Fig. 2 details a typical pixel 200 of array 140, Fig. 1. A thermally isolated platform 210 absorbs incident radiation. Resistor 220 has a high coefficient of resistance change with temperature and is in thermal contact with platform 210, so that its resistance indicates the temperature rise caused by the radiation. Conductors 230 carry voltages and signals. For example, conductors 231 and 232 provide supply and return current to resistor 220. Address line 233 activates the pixel to output a signal from resistor 220 that represents the temperature increase of the pixel caused by the incident radiation. Pixel design can vary considerably; the invention is also useful with other types of infrared detectors, such as pyrometers. A typical array 140 might have 120×160 detectors.

Fig. 3 is a cross section of package cover 130 assembled to detector array 140. In this example, elements 130 and 140 are silicon wafers about 10cm square and 0.5mm thick, although other suitable materials and dimensions can be employed. Window area 131 is indicated by arrows in Fig. 3; silicon transmits long-wave infrared (LWIR) well.

The depth of cavity 134 can vary; in this example it is about 100μm. An acceptable range extends from nearly 500μm to 0μm; that is, in some configurations it is possible to eliminate the cavity altogrther. A conventional perimeter seal 132 hermetically joins cover 130 to substrate 141. Port 133 allows cavity 134 to be evacuated so as to protect array 140 against atmospheric contamination and degradation, and, most importantly, to minimize signal loss from air conductance. Seal 135 maintains the vacuum in cavity 134. The top outside surface of cover 130 has an antireflection coating or layer 136 to prevent reflection of incident radiation 110 from . The material and thickness of coating 136 depends upon the wavelengths desired to be affected; for long-wave infrared, the embodiment of Fig. 3 uses a multilayer film having a thickness of more than 1μm. Contact pads 143 couple array 140 to external wiring 142, Fig. 1.

Recessed interior cavity surface 137 of package cover 130 also has an antireflection element, indicated generally at 300, extending at least over the area above the detector array, and preferably over a greater area of cavity surface 137. Element 300 is a field 310 of upstanding posts 320 extending from a ground 330 below the level of surface 137. Posts 320 are shown as right circular cylinders, and are arranged in a rectangular matrix of rows and columns in field 310. The dimensions and spacing (periodicity) of posts 320 depends upon the refraction index of the window material and the wavelength band of the incident radiation 110 desired to be detected. To approximate a quarter-wavelength antireflective layer, the height of the posts is about $h=\lambda/(4n)$, where λ is the approximate center of the wavelength band of interest, and n is the effective index of refraction of field 310. Post height is typically in the range of 0.2μm to 4μm, corresponding to band centers from 3 to 60μm. To avoid reflection at surface 137, it is desirable to make $n=\sqrt{n_w}$, where n_w is the index of the solid window material. Because posts 320 are arranged in a pattern having symmetry in two orthogonal directions, n is anisotropic. The antireflective properties of field 310 are then the same for all polarizations of radiation 110. The pattern could also have other shapes; for example, hexagonal posts permit higher packing density within field 310.

In this example, the tops of the posts are flush with interior surface 137 of the cavity, and their bottoms, the ground level, lie below that surface. Alternatively, the

posts can be fabricated as holes extending below interior surface 137, having substantially the same cross-sectional area as the posts. The term "posts" will be em[ployed herein to denote both upstanding posts and depressed holes. The shapes of the posts (or holes) can be round, square, rectangular, or have any other convenient cross section. It is also possible to fabricate posts (or holes) having a non-vertical sidewalls; that is, the posts can be shaped to provide a varying cross section along their height,such as substantially pyramidal or conical, including frustum and other variations of these shapes where the cross section decreases along the height of the posts (or, equivalently, depth of holes). Although more difficult to fabricate, such posts offer enhanced antireflection performance over a wider range of wavelengths.

A desired effective index n of field 310 depends upon n_w and upon the fill factor or relative area $A=A_p/A_f$ of the posts A_p to the total field A_f. In "Antireflection Surfaces in Silicon Using Binary Optics Technology" (APPLIED OPTICS, Vol. 31, No. 2, 1 August 1992), Motamedi et al. derive an approximate relation for the effective index as:

$$n = \left(\frac{[1 - A + An_w^2][A + (1 - A)n_w^2] + n_w^2}{2[A + (1 - A)n_w^2]} \right)^{1/2}$$

For round pillars of diameter d and center-to-center spacing s, $A=(\pi/4)(d/s)^2$. The relative area of other shapes is easily calculated. For silicon, the fill factor can range from about 20% to about 60%, being about 40% in this example. Post spacing or periodicity should be less than any wavelength in the desired band to avoid diffraction and scatter; for a rectangular array, this is also the spacing between adjacent rows and columns. The lowest spacing is determined by process limitations rather than by optical considerations. For a silicon cover 130 and a detector 140 operating in the wave band of about 6-12μm, square posts of side 1.5μm can be spaced 2.3μm apart.

Fig. 4 shows the method 400 of forming the package cover 130 of Figs. 1 and 3. In block 410, a mask having the pattern of field 310 is applied to a surface of a flat wafer.

In the example described, the wafer is made of silicon and is about 0.5mm thick. The pattern is aligned so as to produce areas of resist having the shape or cross-section of posts 320 in the desired region of window 132.

Block 420 forms the field of posts by etching. The term "etching" is employed here in a broad sense of material removal. Reactive ion etching (RIE) is typically desirable, because the ions can form relatively tall structures of small cross section. In this example, the posts are about 0.7μm deep ($\lambda/4n$ at 9μm wavelength), and pitch is about 2.3μm. Typically, pitch/height ratio is in the range of 2 to 20, ratios toward the smaller endof the range being preferable.

Block 430 applies a mask having the shape of the entire cavity 134 to the wafer surface that was etched in block 420. This mask has resist only in the perimeter region of cover 130, such as the area where seal 132 is placed in Fig. 1. The purpose of this mask is to define the boundary of cavity 137.

Block 440 etches the entire area of cavity 134, including the field 310 containing posts 320. A typical cavity depth is about 100μm. Again, an RIE process allows the cavity to form without significantly undercutting or otherwise degrading the shapes of the posts. Because the tops of the posts and the ground surface of the field are etched substantially equally, the effect is to sink field 310 of posts 320 into a cavity, rather than to etch it at the bottom of an already formed cavity. This is advantageous because it is easier to form fine features such as posts (or holes) on a planar surface without a cavity. After this etching operation, the tops of the posts 320 lie approximately even with the bottom surface 137 of cavity 134.

Block 450 applies antireflection coating 136 to the other (top) surface of package cover 130. In the applications envisaged by this example embodiment, coating 136 may be a 1μm layer of Y_2O_3, or a multilayer coating. Alternatively, however, antireflection element 136 can be a further field of posts of the same kind as field 310, formed in the same manner, but upon the top surface of cover 130, in the area of window 131. In this case, operations 410 and 420 are repeated within block 450 upon the top surface of cover 130.

In block 460, package cover 130 is sealed to substrate 141, Fig. 1. Solder,

indium, or indium-lead can be employed as an airtight seal. In block 470, the ambient atmosphere is evacuated from cavity 134, and a vacuum-deposited plug 135 seals port 133. A residual pressure typically less than about 1mTorr in the cavity is sufficient to prevent signal loss and to protect detector array 140.

Many arrays can be fabricated and sealed together at the same time. The wafer then contains multiple patterns, and the substrate contains a corresponding number of detector arrays. Theses can be sealed together and evacuated as a single unit. Block 480 then dices such a wafer into indicvidual packages each containing a single array. This lowers handling effort and costs.

Fig. 5 is a graph 500 showing transmittance normalized relative over the band of 6μm to 12μm in the near infrared. Curve 510 depicts the transmittance of window __ constructed according to the invention. Curve 520 shows the same window, but without an antireflective coating on the interior surface of cavity 134. Without any interior antireflection element, the window has only about 65% of the transmittance obtainable with the invention. The post structure causes response to vary less than 5% over the wavelengths of interest.

Conclusion

The invention present an infrared optical device having a cavity structure. An antireflection structure having a pattern of posts significantly enhances the transmissivity of the device. The field of posts is formed prior to formation of the cavity itself.

Claims

1. A package cover having a cavity for receiving an infrared detector and a window area for transmitting infrared radiation to the detector, an interior surface of the window area within the cavity having a field of posts shaped and spaced so as to form an antireflection element for infrared radiation transmitted through the window area.

2. The cover of claim 1 where the posts are upstanding from a ground level below the bottom surfce of the cavity.

3. The cover of claim 2 where the tops of the posts are flush with the bottom surface of the cavity.

4. The cover of claim 1 where the posts are holes depressed below the bottom surface of the cavity.

5. The cover of claim 1 where the cover is a silicon wafer.

6. The cover of claim 5 where the cavity is about 0-500μm deep.

7.The cover of claim 6 where the cavity is about 10-100μm deep.

8. The cover of claim 5 where the cavity is surrounded by a perimeter area.

9. The cover of claim 1 where the posts form a pattern having two orthogonal directions of symmetry.

10. The cover of claim 1 where the posts are square.

11. The cover of claim 1 where the posts are right circular cylinders.

12. The cover of claim 11 where the posts have a diameter in the approximate range of 1μm to 10μm.

13. The cover of claim 12 where the posts have a spacing less than about 6μm.

14. The cover of claim 1 where the posts have non-vertical sidewalls.

15. The cover of claim 14 where the posts are substantially pyramidal.

16. The cover of claim 14 where the posts are substantially conical.

17. The cover of claim 1 where the posts are between about 0.2μm and about 4μm high.

18. The cover of claim 1 where the posts are equally spaced rows and columns.

19. The cover of claim 18 where the rows and columns are spaced less than about 6μm apart.

20. The cover of claim 1 where an exterior surface of the cover has an antireflective coating in the window area.

21. The cover of claim 20 where the antireflective layer comprises a further field of posts shaped and spaced so as to form an antireflection element.

22. An infrared detector, comprising:

an array of pixels for producing an electrical signal in response to incident infrared radiation;

a substrate for holding the array;

a package cover having a window in a cavity for transmitting the radiation to the

array;

a field of spaced posts for reducing reflections of the infrared radiation in the window.

23. The detector of claim 22 further comprising a seal for joining a perimeter area of the cover to the substrate.

24. The detector of claim 23 where the cavity is evacuated.

25. The detector of claim22 where the tops of the posts are substantially flush with a surface of the cavity.

26. The detector of claim 22 where the bottoms of the posts lie below the level of a surface of the cavity.

27. The detector of claim 22 where the array of pixels is a rectangular array of bolometers.

28. The detector of claim 22 further comprising detection circuits for processing an image signal from the detector.

29. The detector of claim 28 further comprising scanning circuits coupled to the detector.

30. The detector of claim 28 further comprising a display coupled to the detection circuits.

31. The detector of claim 30 further comprising scanning circuits coupled to both the detector and the display.

32. A method for fabricating an infrared optical element from a wafer of material capable of transmitting infrared radiation therethrough, comprising, in the order listed:

masking a surface of the wafer with a pattern defining a cross section of a field of posts;

etching the wafer surface so as to form the field of posts to a desired depth;

masking the field of posts with a shape defining a cavity in the surface of the wafer;

etching the wafer surface including the field of posts so as to form a cavity in the wafer.

33. The method of claim 32 where the second etching operation is performed such that the tops of the posts lie below the surface of the cavity.

34. The method of claim 32 where the second etching operation is performed such that tops of the posts are approximately flush with a bottom surface of the cavity.

35. The method of claim 32 where the second etching operation is performed such that bottoms of the posts lie below a bottom surface of the cavity.

36. The method of claim 32 where the cross section of the posts varies along their height.

37. The method of claim 36 where the cross section decreases along the height.

38. The method of claim 32 where the first etching operation is a reactive ion etch.

39. The method of claim 38 where the second etching operation is a reactive ion etch.

40. The method of claim 32 where the height of the posts after the second etching operation is in the approximate range of 0.5μm to 4μm.

41. The method of claim 32 further comprising applying an antireflection layer to a side of the wafer opposite the cavity.

42. The method of claim 32 further comprising mounting an infrared detector to the wafer so as to receive incident infrared radiation through the wafer.

43. The method of claim 42 where the infrared detector is an array of bolometer pixels.

44. The method of claim 42 further comprising mounting the detector to the wafer.

45. The method of claim 44 wherein the detector is hermetically sealed to the wafer.

46. The method of claim 44 further comprising evacuating the cavity.

47. A method for fabricating an infrared optical device, comprising:

masking a surface of awafer of material capable of transmitting infrared radiation therethrough with a pattern defining a field of posts;

etching the wafer surface so as to form the field of posts to a desired height;

applying an antireflection element to the other surace of the wafer;

sealing the wafer to a substrate containing an array of bolometers.

48. The method of claim 47 further comprising evacuating a space between the wafer and the substrate.

49. The method of claim 47 where the posts have varying cross section along their height.

50. The method of claim 47 further comprising:

performing the above operations for a plurality of infrared optical devices on the same wafer;

dicing the wafer after sealing it to the substrate containing multiple arrays of

bolometrs;

therefater, dicing the wafer and the substrate to separate individual ones of the devices.

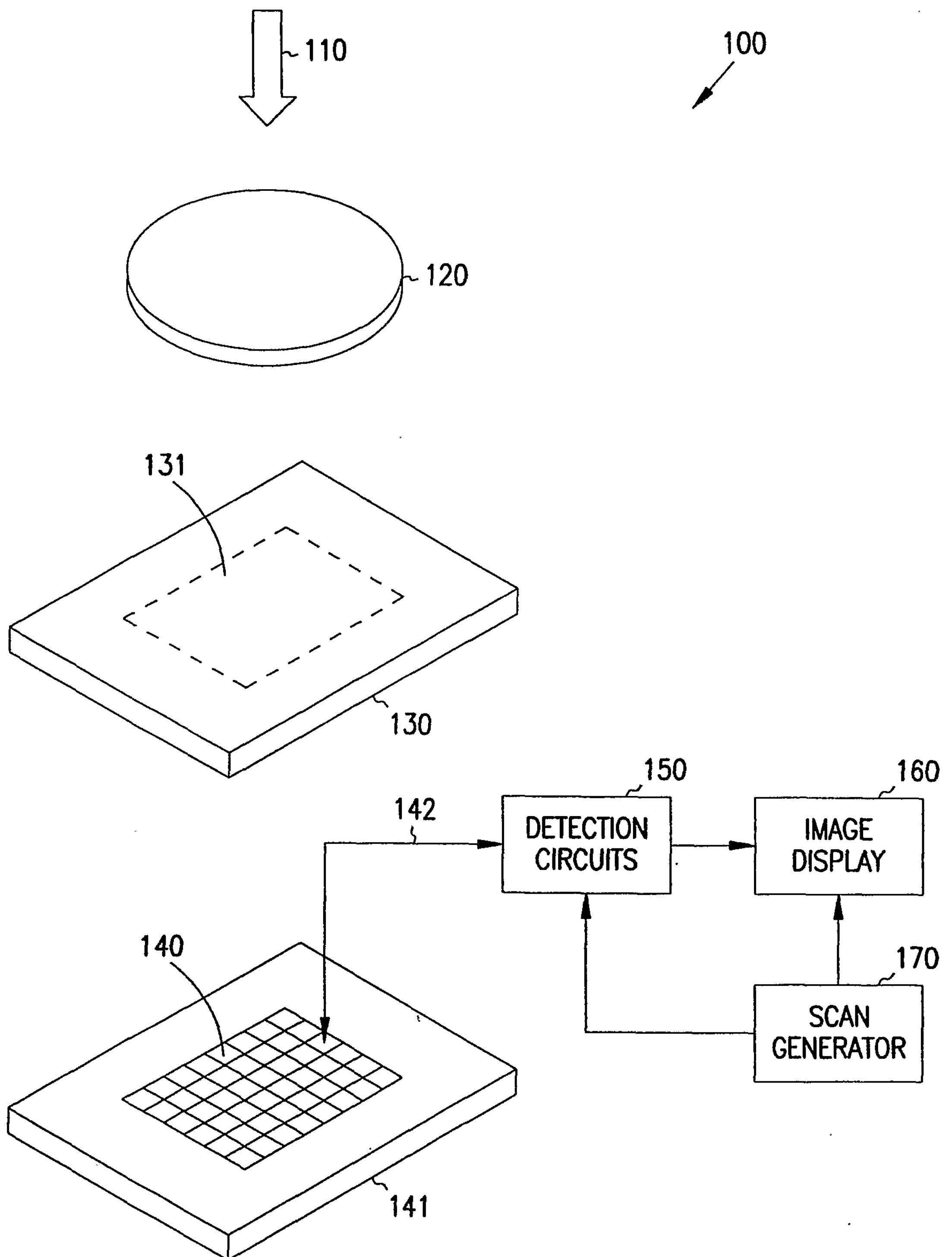

FIG. 1

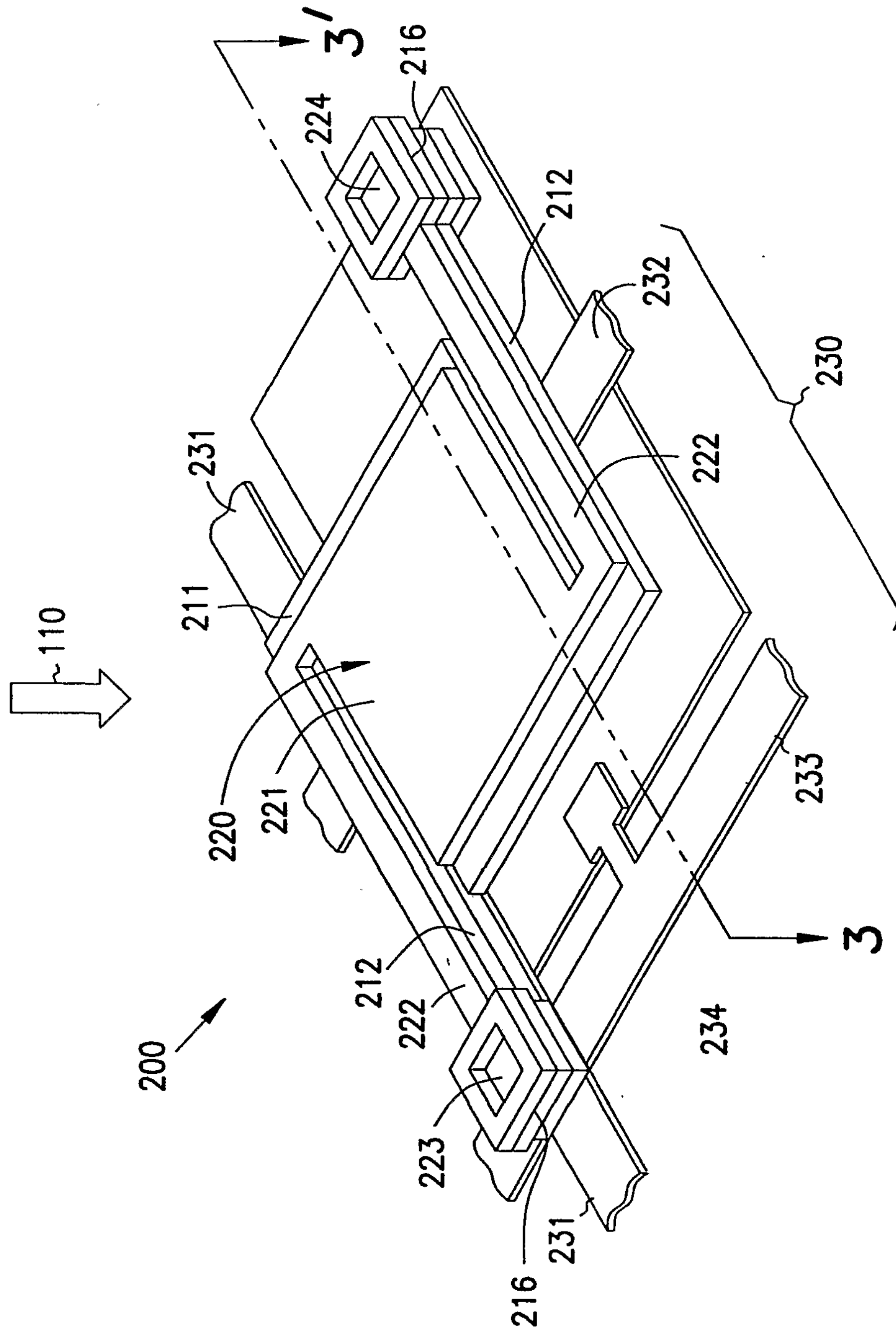

FIG. 2

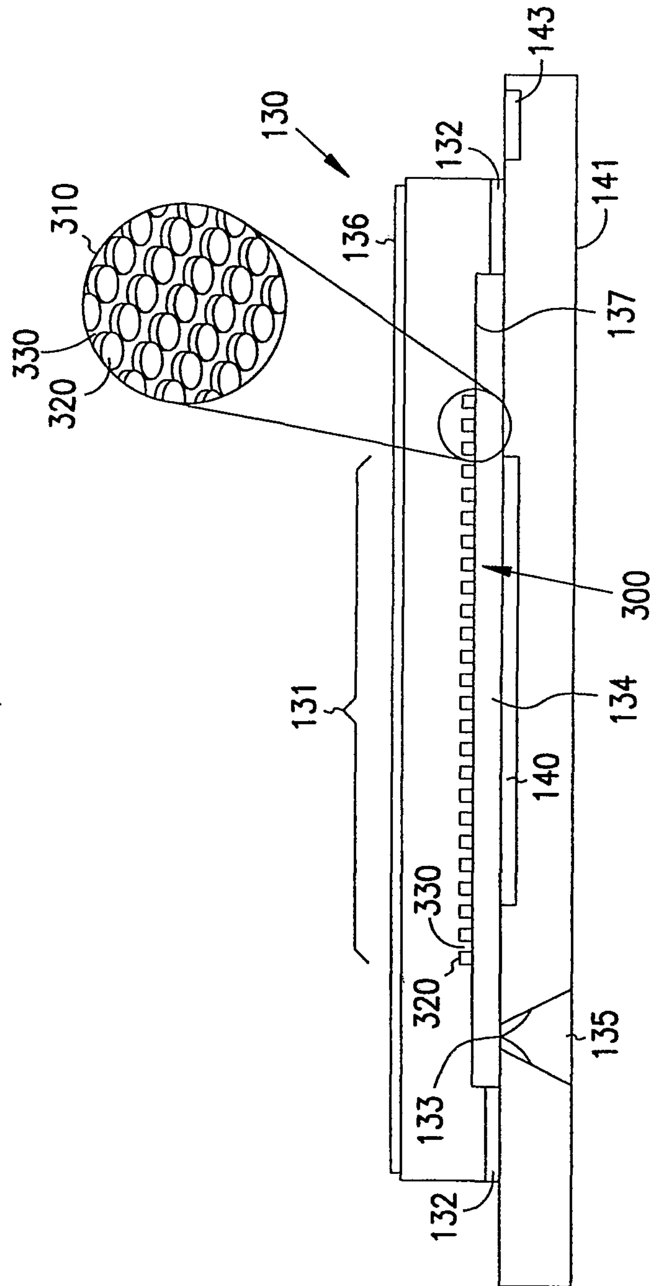

FIG. 3

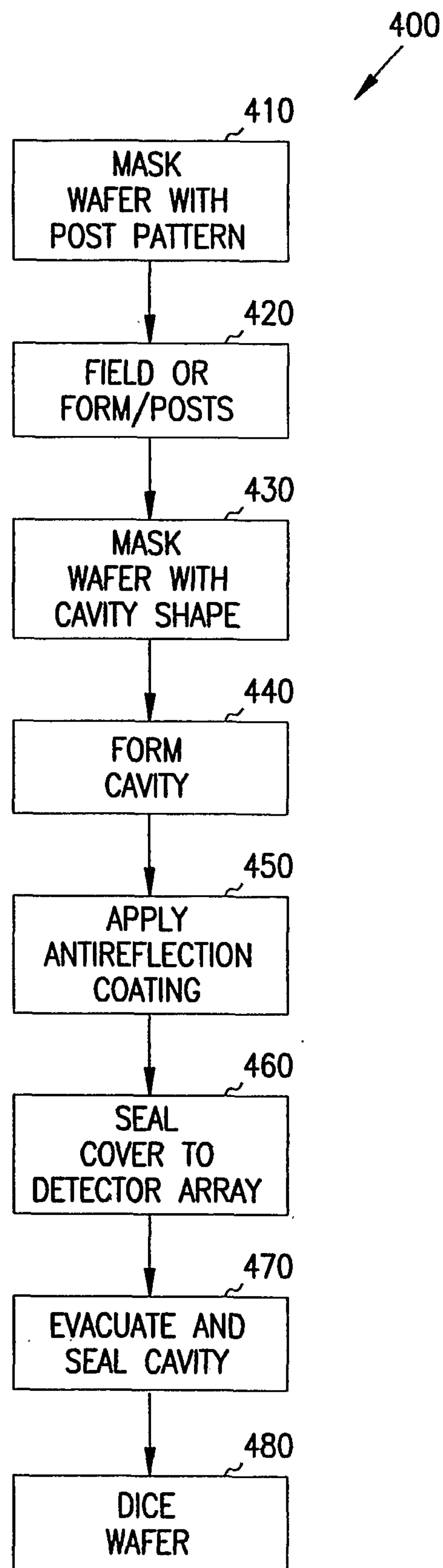

FIG. 4

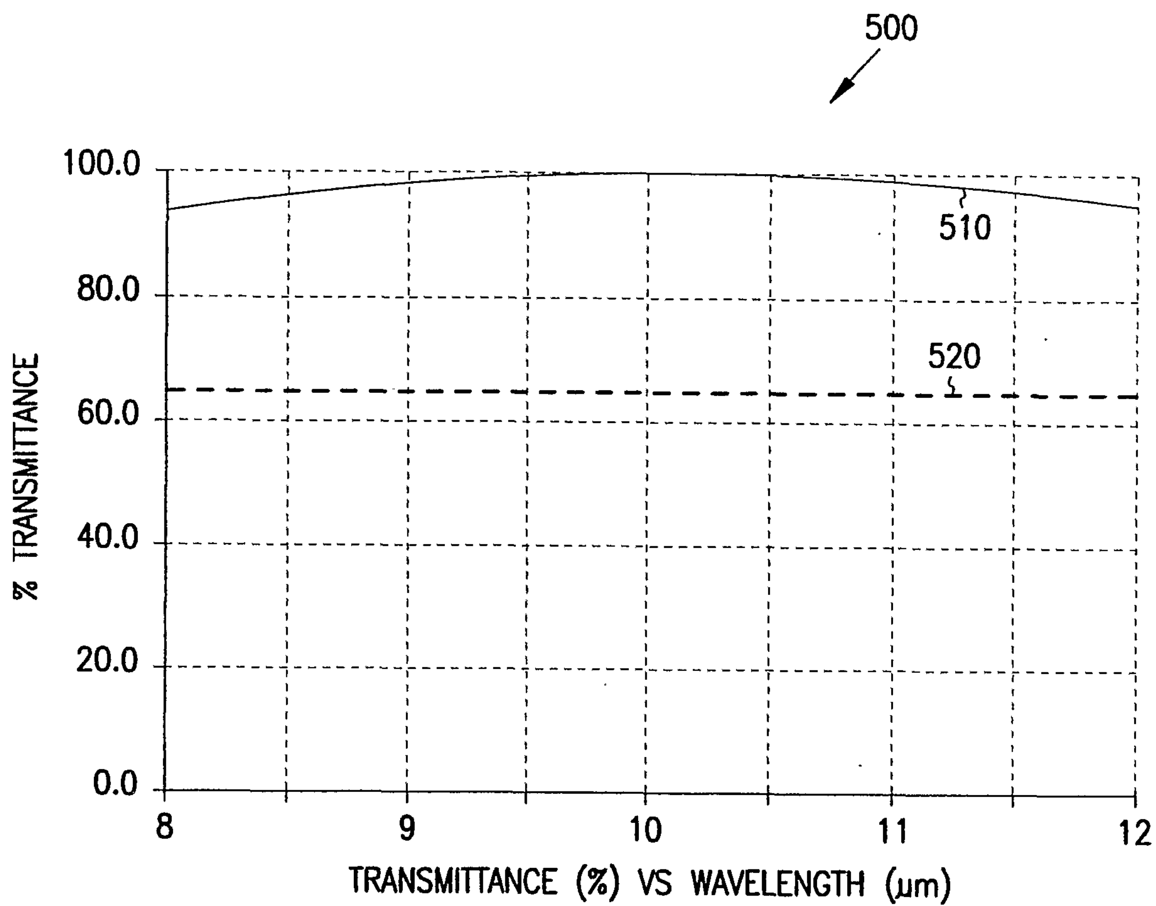

FIG. 5