(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
5 April 2007 (05.04.2007)

PCT

(10) International Publication Number
WO 2007/038575 A2

(51) International Patent Classification:
H01L 21/8234 (2006.01) *H01L 29/10* (2006.01)
H01L 21/336 (2006.01)

(21) International Application Number:
PCT/US2006/037634

(22) International Filing Date:
26 September 2006 (26.09.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/238,444 28 September 2005 (28.09.2005) US

(71) Applicant (*for all designated States except US*): **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): **KAVALIEROS, Jack** [US/US]; 14260 NW Belle Court, Portland, Oregon 97229 (US). **BRASK, Justin** [US/US]; 12748 NW Bayonne Lane, Portland, Oregon 97229 (US). **DOYLE, Brian** [IE/US]; 11156 NW Montreux Lane, Portland, Oregon 97229 (US). **SHAH, Uday** [NP/US]; 13409 NW Keeton Park Ln, Portland, Oregon 97229 (US). **DATTA, Suman** [IN/US]; 16659 NW Talkingstick Way, Beaverton, Oregon 97006 (US). **DOCZY, Mark** [US/US]; 2922 NW Norwalk Place, Beaverton, Oregon 97006 (US). **METZ, Matthew** [US/US]; 3136 NE 13th Ave, Hillsboro, OR 97124 (US). **CHAU, Robert** [US/US]; 8875 SW 171st Avenue, Beaverton, Oregon 97007 (US).

(74) Agents: **VINCENT, Lester J.** et al.; BLAKELY SOKOLOFF TAYLOR & ZAFMAN, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 (US).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: PROCESS FOR INTEGRATING PLANAR AND NON-PLANAR CMOS TRANSISTORS ON A BULK SUBSTRATE AND ARTICLE MADE THEREBY

(57) Abstract: A process capable of integrating both planar and non-planar transistors onto a bulk semiconductor substrate, wherein the channel of all transistors is definable over a continuous range of widths.

WO 2007/038575 A2

PROCESS FOR INTEGRATING PLANAR AND NON-PLANAR CMOS TRANSISTORS ON A BULK SUBSTRATE AND ARTICLE MADE THEREBY

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

[0001] The present invention relates to the field of semiconductor integrated circuit manufacturing, and more particularly to methods of integrating non-planar transistors with variable channel widths into a bulk semiconductor CMOS process.

2. DISCUSSION OF RELATED ART

[0002] For decades, planar transistors have been fabricated on bulk semiconductor substrates. Transistor 100, as shown in Figure 1A, is such a planar device. An active region, having opposite sidewalls 106 and 107, and a top surface 108, is formed between isolation regions 110 on bulk semiconductor substrate 101. The isolation regions 110 substantially cover the opposite sidewalls 106 and 107. The top semiconductor surface 108 is apportioned into, a source region 116, a drain region 117, and a channel region covered by a gate insulator 112 and a gate electrode 113. In the planar transistor design, the device is typically controlled or gated via the capacitive coupling between the top semiconductor surface 108 and the gate electrode 113. Because the channel is gated by a single gate electrode-semiconductor interface, the planar transistor is frequently called a single-gate device.

[0003] More recently, non-planar transistors have been under development to address the short channel effect (SCE) afflicting planar nano-scale transistors. A non-planar transistor is a transistor where the semiconductor channel is non-planar and the gate electrode couples to the channel through more than one surface plane, typically through sidewall portions formed by the non-planarity. Transistor 150, as shown in Figure 1B, is such a non-planar device. An active semiconductor region, having opposite sidewalls 106 and 107, and a top surface 108, is formed over a substrate comprised of an isolation region 103 on a carrier 102. The top surface 108 and the opposite sidewalls 106 and 107 are apportioned into a source region 116, and a drain region 117, and a channel region covered

by a gate insulator 112 and a gate electrode 113. In this transistor design, the device can be gated by the opposite sidewalls 106 and 107, as well as the top surface 108 of the device, reducing the SCE. Because the channel is gated by multiple gate electrode-semiconductor interfaces, the non-planar transistor is frequently called a multi-gate device.

[0004] Non-planar, or multi-gate, devices have been typically been formed upon substrates comprising an insulating layer, commonly called semiconductor-on-insulator (SOI). While there are many advantages to non-planar devices formed on SOI, there are also many disadvantages. For example, the channel width of a non-planar transistor on SOI is limited by the final thickness of the active silicon layer formed on the insulator layer of the SOI substrate. Thus, circuit designers are limited to a fundamental width and multiples of that width for all transistors of a circuit formed on the substrate. As shown in Figure 1C, multiple non-planar bodies, each having a source 116 and drain 117 region are coupled by a common gate electrode 113 through a gate insulator 112 in an electrically parallel fashion to form device 175. Device 175 limits circuit design flexibility because the current carrying width must be incremented discretely, not continuously. Also, because of lithographic pitch limitations, non-planar transistors like device 175 shown in Figure 1C incur a layout penalty relative to traditional planar transistors. Another disadvantage of devices formed on SOI is the commonly known "floating body" effect due to the buried insulator layer, which results in the loss of a ground plane for the transistors. Furthermore, non-planar transistors formed on SOI substrates suffer from poorer thermal conductivity and a higher overall cost than devices formed on bulk substrates.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] **Figures 1A and 1B** are illustrations of a perspective view of a conventional planar, single-gate transistor on a bulk semiconductor substrate and a conventional non-planar, multi-gate transistor on an SOI substrate, respectively.

[0006] **Figure 2** is an illustration of a perspective view of a circuit device having a planar transistor and non-planar transistors in accordance with an embodiment of the present invention.

[0007] Figures 3A-3G are illustrations of perspective views of a method of fabricating a device with both planar and non-planar transistors in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0008] A novel CMOS device structure and its method of fabrication are described. In the following description, numerous specific details are set forth, such as specific materials, dimensions and processes, etc. in order to provide a thorough understanding of the present invention. In other instances, well-known semiconductor processes and manufacturing techniques have not been described in particular detail in order to not unnecessarily obscure the present invention.

[0009] In accordance with an embodiment of the present invention, as illustrated in Figure 2, three transistors, a planar device 10, a non-planar device 20 having a first channel width and a non-planar device 30 having a second channel are formed on a single "bulk semiconductor" substrate 201. Transistors 10, 20, and 30 are each coupled to the semiconductor substrate (preventing the floating-body effect) and both planar and non-planar transistor designs have a channel width that can be independently defined to be any value (rather than merely discrete values). By utilizing a method enabling the non-planar transistors 20 and 30 to have various sidewall heights, various channel widths can be specified and the performance requirements of individual portions of a single device can be individually satisfied with any combination of planar transistors (having baseline SCE) and non-planar transistors (having reduced SCE). In a specific embodiment of the present invention, a microprocessor core, comprising logic regions, is made up of planar transistors, while a microprocessor cache, comprising memory, such as SRAM, is made up of non-planar transistors. In another particular embodiment of the present invention, a portion of a circuit, such as a driver, requiring a large total current is made up of planar transistors having a larger current carrying channel width than the non-planar transistors used in other portions of the circuit.

[0010] Embodiments of the non-planar transistor of the present invention include, but are not limited to, dual-gate, FinFET, tri-gate, pi-gate or omega-gate designs. In some embodiments, all non-planar transistors are a "tri-gate" design having a top gate, while in other embodiments all non-planar transistors are a "dual-gate" design having only sidewall gates.

[0011] Substrate 201 is comprised of a "bulk semiconductor", such as, but not limited to, a monocrystalline silicon substrate or a gallium arsenide substrate. In a further embodiment of the present invention the substrate 201 is a bulk silicon semiconductor having a doped epitaxial silicon layer with either p-type or n-type conductivity at an impurity concentration level between $1x10^{16}$-$1x10^{19}$ atoms/cm^3. In another embodiment of the present invention, the substrate 201 is a bulk silicon semiconductor substrate having an undoped, or intrinsic epitaxial silicon layer. In a "bulk semiconductor" substrate, unlike a silicon-on-insulator (SOI) substrate, there is no "buried" insulating layer between semiconductor portion used to fabricate the active devices and the semiconductor portion used for handling.

[0012] Transistors 10, 20 and 30, as shown in Figure 2, are comprised of active regions 204, 224 and 244 on the bulk semiconductor substrate. The distance between the isolation regions 210 defines an individual transistor active area width. The active regions 204, 224, 244 have top surfaces, 218, 238, 258 and bottom planes 208, 228, 248, respectively. The bottom planes 208, 228 and 248 are defined to be substantially level with the bottom surface of isolation regions 210, as shown in Figure 2. For simplicity, semiconductor active regions of Figure 2 are referred to as "on" the substrate, wherein the substrate is the semiconductor portion below the reference planes 208, 228, and 248. However, the active regions could also be considered "in" the substrate if a different reference plane is chosen. The portion of the active region sidewalls exposed to the gate insulator and control gate electrode is referred as the "gate-coupled sidewall." As shown in Figure 2, the isolation regions 210 substantially cover the sidewalls 206 and 207 of the active region 204 of transistor 10. Therefore, the planar, single-gate transistor 10 does not have gate-coupled sidewalls because the distance between the top surface 218 and the bottom plane 208 is roughly equal to the thickness of the bordering isolation regions 210. As such, the active region of transistor 10 has primarily only the top surface 218 coupled to the control gate 213 and the channel width is equal to the width of the top surface 218. For non-planar device 20 however, the portion of the pair sidewalls 226 and 227 extending above the top surface of the adjacent isolation regions 210 is "gate-coupled" and this portion contributes to the total channel width of device 20. As shown in Figure 2, the "gate-coupled sidewall" height of transistor 20 is equal to the distance between the top surface 238 and the bottom plane 228 minus the thickness of the adjacent isolation regions 210. In an embodiment of the present invention, the height of the gate-coupled sidewalls is substantially equal to the

width of the active area top surface 258, as shown in transistor 30 of Figure 2. In another embodiment of the present invention, the gate-coupled sidewall height of the non-planar transistors is between half the active area width and twice the active area width. In a particular embodiment of the present invention, the non-planar transistors have an active area width and gate-coupled sidewall height less than 30 nanometers, and more particularly, less than 20 nanometers.

[0013] The current carrying width of a non-planar transistor in accordance with an embodiment of the present invention can be continuously and individually set to virtually any desired value by varying the height of the gate-coupled sidewall. As pictured in Figure 2, sidewalls 226 and 227 of transistor 20 have a first gate-coupled sidewall height and sidewalls 246 and 247 of transistor 30 have a second, different gate-coupled sidewall height. Therefore, transistor 20 has a first current carrying channel width and transistor 30 has a second, different, current carrying channel width. Because the current carrying channel width of a non-planar transistor increases as the gate-coupled sidewall height increases, in the embodiment shown in Figure 2, transistor 20 has a greater channel width than transistor 30. Thus, embodiments of the present invention have non-planar transistors with continuously variable channel widths and thereby provide circuit design flexibility previously unavailable to non-planar transistors.

[0014] In embodiments of the present invention no layout efficiency penalty is incurred for non-planar transistors having a channel width greater than a minimum width. Layout efficiency is a ratio of the absolute current carrying width of a non-planar device layout over that of the typical planar device occupying the same layout width. In embodiments of the present invention, the gate-coupled sidewall height of a single non-planar transistor is scaled to provide a desired total current carrying width. Thus, scaling the current carrying width does not rely on incrementing the number of parallel non-planar devices having a discrete channel width. Because the channel width increases with sidewall height rather than top surface area, no additional layout width is required to increase the channel width of a non-planar transistor fabricated in accordance with particular embodiments of the present invention. As such, these particular embodiments improve the packing density of the devices and can have layout efficiencies greater than unity.

[0015] As shown in Figure 2, transistors 10, 20, and 30 have a gate insulator layer 212. In the depicted non-planar embodiments, gate insulator 212 surrounds the active regions, in contact with the exposed semiconductor surfaces. In such embodiments, gate dielectric

layer 212 is in contact with the sidewalls as well as the top surfaces of the active regions of transistors 20 and 30, as shown in Figure 2. In other embodiments, such as in particular FinFET or dual-gate designs, the gate dielectric layer is only in contact with the sidewalls of the active regions, and not the top surfaces 238 and 258 of the non-planar devices. In planar transistor embodiments, such as transistor 10 in Figure 2, the gate insulator is formed only on the top surface 218. Gate insulator 212 can be of any commonly known dielectric material compatible with the semiconductor surface and the gate electrode 213. In an embodiment of the present invention, the gate dielectric layer is a silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y) or a silicon nitride (Si_3N_4) dielectric layer. In one particular embodiment of the present invention, the gate dielectric layer 212 is a silicon oxynitride film formed to a thickness of between 5-20 Å. In another embodiment of the present invention, gate dielectric layer 212 is a high K gate dielectric layer, such as a metal oxide dielectric, such as but not limited to tantalum oxide, titanium oxide, hafnium oxide, zirconium oxide, and aluminum oxide. Gate dielectric layer 212 can be other types of high K dielectric, such as, but not limited to, lead zirconium titanate (PZT).

[0016] The transistors 10, 20, and 30 have a gate electrode 213, as shown in Figure 2. In certain embodiments, gate electrode 213 is in contact with gate dielectric layer 212 formed on sidewalls of each of the non-planar transistors 20 and 30. In planar embodiments, such as transistor 10, the gate electrode 213 is in contact with the gate dielectric layer over the top surface 218. Gate electrode 213 has a pair of laterally opposite sidewalls separated by a distance, defining the gate length (L_g) of transistor 10, 20, and 30. In an embodiment of the present invention, L_g of planar transistor 10 and non-planar transistors 20 and 30 are between about 20 nm and about 30 nm. Gate electrode 213 has an effective width equal to the current carrying width of the semiconductor channel controlled by gate electrode 213. In an embodiment of the present invention, effective current carrying width of a non-planar device is greater than the effective width of the planar device. In a particular embodiment, as shown in Figure 2, the gate-coupled sidewall height of each the sidewalls 226 and 227 is greater than the width of the top surface 218. In this manner, the effective gate electrode width of transistor 20 is greater than the effective gate electrode width of transistor 10. In another embodiment, the effective width of the gate electrode of transistor 10 is greater than that of transistor 20. In still another embodiment of the present invention, the gate electrode physically connects, or is continuous between, a

planar device and a non-planar device, multiple planar devices, or multiple non-planar devices.

[0017] Gate electrode 213 of Figure 2 can be formed of any suitable gate electrode material having the appropriate work function. In an embodiment of the present invention, the gate electrode is comprised of polycrystalline silicon. In another embodiment, the gate electrode is comprised of a metal, such as tungsten, tantalum nitride, titanium nitride or titanium silicide, nickel silicide, or cobalt silicide. It should also be appreciated that the gate electrode 213 need not necessarily be a single material, but rather can also be a composite stack of thin films such as a metal/polycrystalline silicon electrode.

[0018] Transistors 10, 20 and 30, as shown in Figure 2, each have source regions 216 and drain regions 217. Source regions 216 and drain regions 217 are formed in the active regions on opposite sides of gate electrode 213. The source region 216 and the drain region 217 are formed of the same conductivity type, such as n-type or p-type conductivity, depending on the transistor being an nMOS device or a pMOS device. In an embodiment of the present invention, source region 216 and drain region 217 have a doping concentration of $1x10^{19}$-$1x10^{21}$ atoms/cm^3. Source region 216 and drain region 217 can be formed of uniform concentration or can include subregions of different concentrations or doping profiles such as tip regions (e.g., source/drain extensions).

[0019] As shown in Figure 2, transistors 10, 20, and 30 each have a channel region below the gate electrode 213 in the active area located between source regions 216 and drain regions 217. The channel regions of transistors 10, 20, and 30 can be independently doped to an impurity level appropriate for the particular device geometry, gate stack, and performance requirements. When the channel region is doped, it is typically doped to the opposite conductivity type of the source region 216 and the drain region 217. For example, the nMOS device 205 has source and drain regions which are n-type conductivity while the channel region is doped to p-type conductivity. In certain embodiments of the present invention, the channel regions of the non-planar devices 20 and 30 are intrinsic or undoped while the channel region of the planar devices is doped. In an embodiment of the present invention, the channel regions of transistors 10, 20 30 are all doped. When a channel region is doped, it can be doped to a conductivity level of $1x10^{16}$-$1x10^{19}$ atoms/cm^3.

[0020] A method of fabricating a CMOS device on a bulk substrate in accordance with an embodiment of the present invention as shown in Figure 2 is illustrated in Figures 3A-3G.

In a particular embodiment, the fabrication begins with a "bulk" silicon monocrystalline substrate 201. In certain embodiments of the present invention, the substrate 201 is a silicon semiconductor having a doped epitaxial region with either p-type or n-type conductivity with an impurity concentration level of $1x10^{16}$-$1x10^{19}$ atoms/cm^3. In another embodiment of the present invention the substrate 201 is a silicon semiconductor having an undoped, or intrinsic epitaxial silicon region. In other embodiments, the bulk substrate 201 is any other well-known semiconductor material, such as gallium arsenide (GaAs), indium antimonide (InSb), gallium antimonide (GaSb), gallium phosphide (GaP), indium phosphide (InP), or carbon nanotubes (CNT).

[0021] A mask is used to define the active regions of the transistors. The mask can be any well-known material suitable for defining the semiconductor substrate. As shown in Figure 3A, in an embodiment of the present invention, mask 310 is formed of a dielectric material that has been lithographically defined and etched. In another embodiment, mask 310 is itself a photo-definable material. In a particular embodiment, as shown in Figure 3A, masking layer 310 can be a composite stack of materials, such as an oxide/nitride stack. If masking layer 310 is a dielectric material, commonly known techniques, such as chemical vapor deposition (CVD), low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), or even spin on processes may be used to deposit the mask material while commonly known lithography and etching process may be used to define the mask. In an embodiment of the present invention, the minimum lithographic dimension is used to define the width of the mask 310. In another embodiment, the minimum width of the mask 310 is sub-lithographic, formed by commonly known techniques such as dry develop, oxidation/strip, or spacer-based processes. In a particular embodiment of the present invention, the width of mask 310 is less than 30 nanometers, and more particularly, less than 20 nanometers.

[0022] As shown in Figure 3B, once masking layer 310 has been defined, a portion of the semiconductor on bulk substrate 201 is etched using commonly known methods to form recesses or trenches 320 on the substrate in alignment with mask 310. The isolation etch defining the active regions has sufficient depth to isolate individual devices from one another and form a gate-coupled sidewall of adequate height to achieve the maximum desired channel width of the non-planar transistors. In a particular embodiment of the present invention, trenches 320 are etched to a depth equal to the maximum desired non-planar transistor channel width plus about 100 Å to about 500 Å to accommodate a

dielectric isolation region. In still another embodiment, the trenches 320 are etched to a depth of approximately 1500 Å to 3000 Å.

[0023] As shown in Figure Fig 3C, the trenches 320 are then filled with a dielectric to form shallow trench isolation (STI) regions 210 on substrate 201. In an embodiment of the present invention, a liner of oxide or nitride on the bottom and sidewalls of the trenches 320 is formed by commonly known methods, such as thermal oxidation or nitridation. Next, the trenches 320 are filled by blanket depositing an oxide over the liner by, for example, a high-density plasma (HDP) chemical vapor deposition process. The deposition process will also form dielectric on the top surfaces of the mask 310. The fill dielectric layer can then be removed from the top of mask 310 by chemical, mechanical, or electrochemical, polishing techniques. The polishing is continued until the mask 310 is revealed, forming isolation regions 210, as shown in Figure 3C. In a particular embodiment of the present invention, commonly known methods are used to selectively remove the mask 310. In another embodiment, as shown in Figure 3C, a portion of mask 310 is retained.

[0024] If desired, wells can then be selectively formed for pMOS and nMOS transistors. Wells can be formed using any commonly known technique to dope the active regions to a desired impurity concentration. In embodiments of the present invention, active regions 204, 224, and 244 are selectively doped to p-type or n-type conductivity with a concentration level of about $1x10^{16}$-$1x10^{19}$ atoms/cm^3 using commonly known masking and ion implantation techniques. In a particular embodiment, the well regions extend into the semiconductor about 500 Å deeper than the bottom planes 208, 228 and 248 of the active regions, shown in Figure 3C. In embodiments of the present invention, after the selective well implant and mask strip, a commonly known clean, such as HF, removes either the mask 310 or native oxides from the active region top surfaces 218, 238 and 258. In a further embodiment of the present invention, commonly known techniques are then used to either grow or deposit a sacrificial oxide over the top surfaces 218, 238 and 258.

[0025] The isolation regions can then be selectively protected with a masking material to allow selective definition of the non-planar devices. In an embodiment, as shown in Figure 3D, mask 330 is formed in a manner similar to that described above with reference to Figure 3A. Mask 330 can be either a photo-definable material or a commonly known "hard" mask material that was patterned with common lithography and etch techniques. In the embodiment depicted in Figure 3D, mask 330 is a photo-definable material, a photo

resist. As shown in Figure 3D, mask 330 is used to protect isolation regions 210 bordering the active region 204 of planar device 10 and active region 224. If desired, additional mask layers may be utilized to selectively protect various other isolation regions.

[0026] Next, the isolation regions not protected by a mask are etched back, or recessed, to expose the sidewalls of the active area of the non-planar transistors. As shown in Figure 3E, isolation regions 210 not protected by mask 330 are etched back without significantly etching the semiconductor active area 224, exposing at least a portion of semiconductor sidewalls 226 and 227. In embodiments where semiconductor active areas are silicon, isolation regions 210 can be recessed with an etchant comprising a fluorine ion, such as HF. In some embodiments, isolation regions 210 are recessed using a commonly known anisotropic etch, such as a plasma or RIE process using an etchant gas such as, but not limited to, C2F6. In a further embodiment, an anisotropic etch can be followed by an isotropic etch, such as a commonly known dry process using a gas such as NF3, or a commonly known wet process such as HF, to completely remove the isolation dielectric from at least a portion of the semiconductor active region sidewalls. In some embodiments, only a portion of the unprotected isolation regions is removed during the recess etch. In a particular embodiment (not pictured), the recess etch is selective to the isolation liner material over the isolation fill material, such that the isolation recess etch is deeper along the liner region immediately adjacent to the active region than in the isolation fill region. In this manner, the width of the recess etch can then be very tightly controlled by the width of the liner, enabling a high transistor packing density.

[0027] The isolation regions are selectively recessed by an amount which, when added to a subsequent amount of unselective, or blanket recess etching, achieves the desired final gate-coupled sidewall height for the designed non-planar transistor channel width. A transistor's final gate-coupled sidewall height is determined by the cumulative amount, or depth, the adjacent isolation region is recessed. The isolation recess depth is limited by the demands of device isolation and moderate aspect ratios. For example, subsequent processing can result in inadvertent spacer artifacts if the isolation recess produces aspects ratios that are too aggressive. In a particular embodiment of the present invention, a portion of the isolation region is recessed so that the final isolation thickness is about 200 Å to about 300 Å. In other embodiments, the final isolation thickness is significantly more than about 300 Å. In an embodiment of the present invention, isolation regions 210 are recessed by approximately the same amount as the width dimension of the top surface 238

of the semiconductor active region 224. In other embodiments, the isolation regions 210 are recessed by a significantly larger amount than the width dimension of the top surface 238.

[0028] In an embodiment of the present invention, as shown in Figure 3F, the mask 330 is then removed by commonly known means and a second mask 340 is formed in a fashion similar as that previously discussed in reference to Figure 3D. Mask 340 protects the active region 224 while the isolation regions 210 surrounding active region 244 are recessed as described above in reference to Figure 3E. In this embodiment, a different sidewall height can be achieved for 244 than that of 224, thereby forming a non-planar transistor 30 having a different channel width than non-planar transistor 20. It should be appreciated that the process of selectively masking a portion of the isolation regions and recess etching the isolation regions by a specific amount can be repeated a number of times and in a number of ways to achieve a menu of gate-coupled sidewall heights, corresponding to a menu of non-planar transistor channel widths, in accordance with the present invention.

[0029] Once the selective isolation recess etches are completed, all isolation masks are removed with commonly known techniques. If desired, a final clean, such as HF, may then be performed on all active regions, further recessing all isolation regions. In a particular embodiment of the present invention, additional sacrificial oxidation and blanket oxide etches or cleans are performed to both improve the semiconductor surface quality and further tailor the shape of the active regions through corner rounding, feature shrinking, etc.

[0030] A gate dielectric can then be formed over the active regions in a manner dependent on the type of non-planar device (dual-gate, tri-gate, etc.). In a tri-gate embodiment of the present invention, as shown in Figure 3G, a gate dielectric layer 212 is formed on the top surface of each of the active regions 204, 224 and 224, as well as on, or adjacent to, the exposed sidewalls 226, 227 and 246, 247 of the non-planar devices. In certain embodiments, such as dual-gate embodiments, the gate dielectric is not formed on the top surfaces of the non-planar active regions. The gate dielectric can be a deposited dielectric or a grown dielectric. In an embodiment of the present invention, the gate dielectric layer 212 is a silicon dioxide dielectric film grown with a dry/wet oxidation process. In an embodiment of the present invention, the gate dielectric film 212 is a deposited high dielectric constant (high-K) metal oxide dielectric, such as tantalum pentaoxide, titanium

oxide, hafnium oxide, zirconium oxide, aluminum oxide, or another high-K dielectric, such as barium strontium titanate (BST). A high-K film can be formed by well-known techniques, such as chemical vapor deposition (CVD) and atomic layer deposition (ALD).

[0031] A gate electrode is then formed over each active region. In an embodiment of the present invention, the gate electrode 213, as shown in Figure 3G, is formed on the gate dielectric layer 212 over the top surfaces 218, 238, 258 and is formed on or adjacent to the gate dielectric 212 along the sidewalls 226, 227 and 246, 247. The gate electrode can be formed to a thickness between 200-3000 Å. In particular embodiments, the thickness of the gate electrode material is constrained by the depth of the isolation region recess etch because the gate electrode material will tend to form a conductive spacer along the topography generated by the recess etch. For such embodiments, over-etching of the gate electrode material can prevent such spacer artifacts if the isolation recess depth is less than the thickness of the gate electrode material. In an embodiment, the gate electrode has a thickness of at least three times the gate-coupled sidewall height (previously defined as the exposed portion of the active area sidewall). In an embodiment of the present invention, the gate electrode is comprised of polycrystalline silicon. In some embodiments of the present invention, the gate material is metal such as, but not limited to, tungsten, tantalum nitride, titanium nitride or titanium silicide, nickel silicide, or cobalt silicide. In still other embodiments, the electrode is formed from a composite of poly-silicon and metal. In an embodiment of the present invention, gate electrode 213 is formed by well-known techniques, such as blanket depositing a gate electrode material over the substrate and then patterning the gate electrode material. In other embodiments of the present invention, the gate electrode is formed using "replacement gate" methods. In such embodiments, the gate electrode utilizes a fill and polish technique similar to those commonly employed in damascene metallization technology, whereby the recessed isolation regions may be completely filled with gate electrode material.

[0032] In an embodiment of the present invention, source regions 216 and drain regions 217 for transistors 10, 20, and 30 are formed in the active regions on opposite sides of gate electrode 213, as shown in Figure 3G. For a pMOS transistor, the active region is doped to p-type conductivity and to a concentration of 1×10^{19}-1×10^{21} atoms/cm^3. For an nMOS transistor, the active is doped with n-type conductivity ions to a concentration of 1×10^{19}-1×10^{21} atoms/cm^3. At this point the CMOS transistor of the present invention is substantially complete and only device interconnection remains.

[0033] Although the invention has been described in language specific to structural features and/or methodological acts, it is to be understood that the invention defined in the appended claims is not necessarily limited to the specific features or acts described. Rather, the specific features and acts are disclosed as particularly graceful implementations of the claimed invention.

IN THE CLAIMS

We claim:

1. A device comprising:

a planar transistor and a non-planar transistor on a bulk semiconductor substrate.

2. The device of claim 1, wherein said planar transistor is in a microprocessor core and said non-planar transistor is in a microprocessor SRAM region.

3. The device of claim 1, wherein said planar transistor has a smaller channel width than that of said non-planar transistor.

4. A semiconductor device comprising:

a first active region having sidewalls substantially covered by an adjacent isolation region on a bulk semiconductor substrate;

a second active region having sidewalls extending above a top surface of an adjacent isolation region on said bulk semiconductor substrate;

a first gate insulator on a top surface of said first active region and a second gate insulator adjacent to at least a portion of said sidewalls of said second active region;

a first gate electrode on said first gate insulator and a second gate electrode adjacent to said second gate insulator; and

a first pair of source/drain regions on opposite sides of said first gate electrode and a second pair of source/drain regions on opposite sides of said second gate electrode.

5. The device of claim 4, wherein said second gate insulator is on a top surface of said second active region and said second gate electrode is on said second gate insulator.

6. The device of claim 4, wherein said first gate electrode and said second gate electrode are physically connected.

7. A device comprising:

a first multi-gate transistor having a first channel width and a second multi-gate transistor having a second channel width on a bulk semiconductor substrate, wherein said first channel width is different than said second channel width.

8. The device of claim 7, wherein said first multi-gate transistor has a first gate-coupled sidewall height and said second multi-gate transistor has a second gate-coupled sidewall height different than said first gate coupled sidewall height.

9. The device of claim 7, further comprising a single-gate transistor on said bulk semiconductor substrate.

10. A method of forming planar and non-planar transistors comprising:

forming a first active region having sidewalls adjacent to a first isolation region on a bulk semiconductor substrate;

forming a second active region having sidewalls adjacent to a second isolation region on said bulk semiconductor substrate;

exposing at least a portion of said sidewalls of said second active region by recessing a top surface of said second isolation region;

forming a first gate insulator on said top surface of said first active region;

forming a second gate insulator adjacent to at least a portion of said sidewalls of said second active region;

forming a first gate electrode on said first gate insulator;

forming a second gate electrode adjacent to said second gate insulator; and

forming a first pair of source/drain regions on opposite sides of said first gate electrode and a second pair of source/drain regions on opposite sides of said second gate electrode in said first active region and said second active region.

11. The method of claim 10, wherein an etchant comprising a fluoride ion is used to recess said top surface of said second isolation region.

12. The method of claim 10, wherein an anisotropic etch is used to recess said top surface of said second isolation region.

13. The method of claim 10, wherein a liner region of said isolation region is recessed by an amount greater than an adjacent fill region of said isolation region.

14. The method of claim 10, further comprising lithographically defining said second isolation region to be recessed.

15. The method of claim 10, wherein a sacrificial oxide is formed on the top surface of said first and said second active region prior to recessing said top surface of said second isolation region.

16. The method of claim 10, wherein forming said first and said second gate electrode comprises a replacement gate process.

17. The method of claim 10, wherein defining said first and said second gate electrode includes etching said gate electrode material to substantially remove said gate electrode from said sidewalls of said second active region.

18. A method of forming non-planar transistors comprising:

forming a first active region having sidewalls adjacent to a first isolation region on a bulk semiconductor substrate;

forming a second active region having sidewalls adjacent to a second isolation region on said bulk semiconductor substrate;

recessing a top surface of said first isolation region by a first amount to expose at least a portion of said sidewalls of said first active region;

recessing a top surface of said second isolation region to by a second amount to expose at least a portion of said sidewalls of said second active region, said second amount of recess being different than said first amount of recess;

forming a first gate insulator adjacent to at least a portion of said sidewalls of said first active region and forming a second gate insulator adjacent to at least a portion of said sidewalls of said second active region;

forming a first gate electrode adjacent to said first gate insulator and forming a second gate electrode adjacent to said second gate insulator; and

forming a first pair of source/drain regions on opposite sides of said first gate electrode and a second pair of source/drain regions on opposite sides of said second gate electrode.

19. The method of claim 18 further comprising:

forming a first gate insulator and first gate electrode on a top surface of said first active region; and

forming a second gate insulator and second gate electrode on a top surface of said second active region.

20. The method of claim 18, further comprising blanket etching a sacrificial oxide prior to forming said first insulator and said second gate insulator.

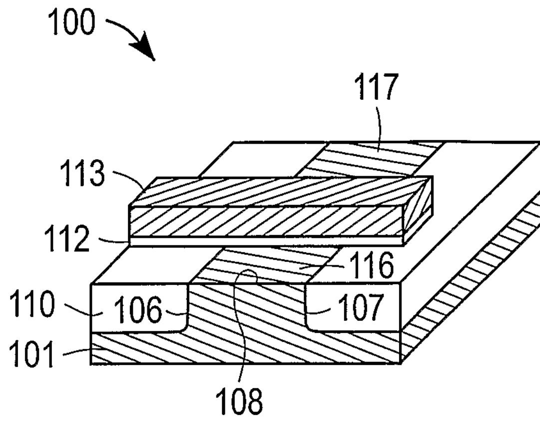

FIG. 1A
(PRIOR ART)

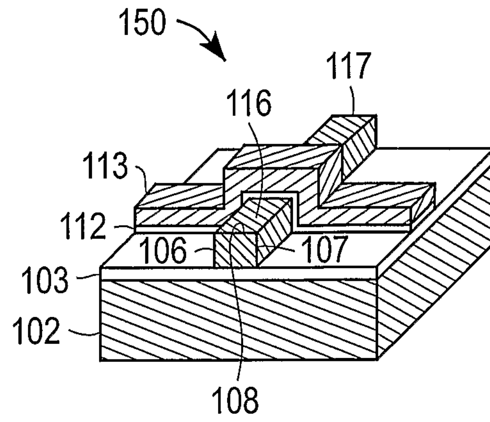

FIG. 1B
(PRIOR ART)

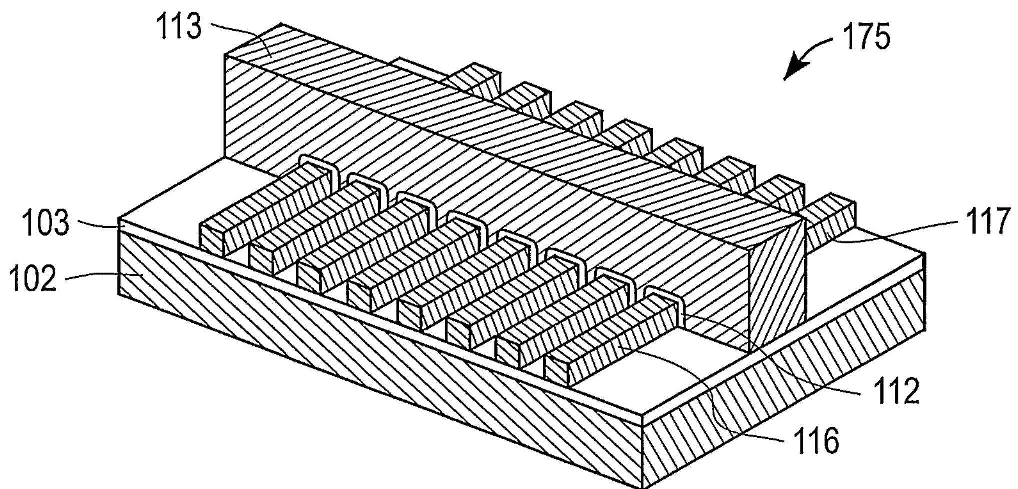

FIG. 1C
(PRIOR ART)

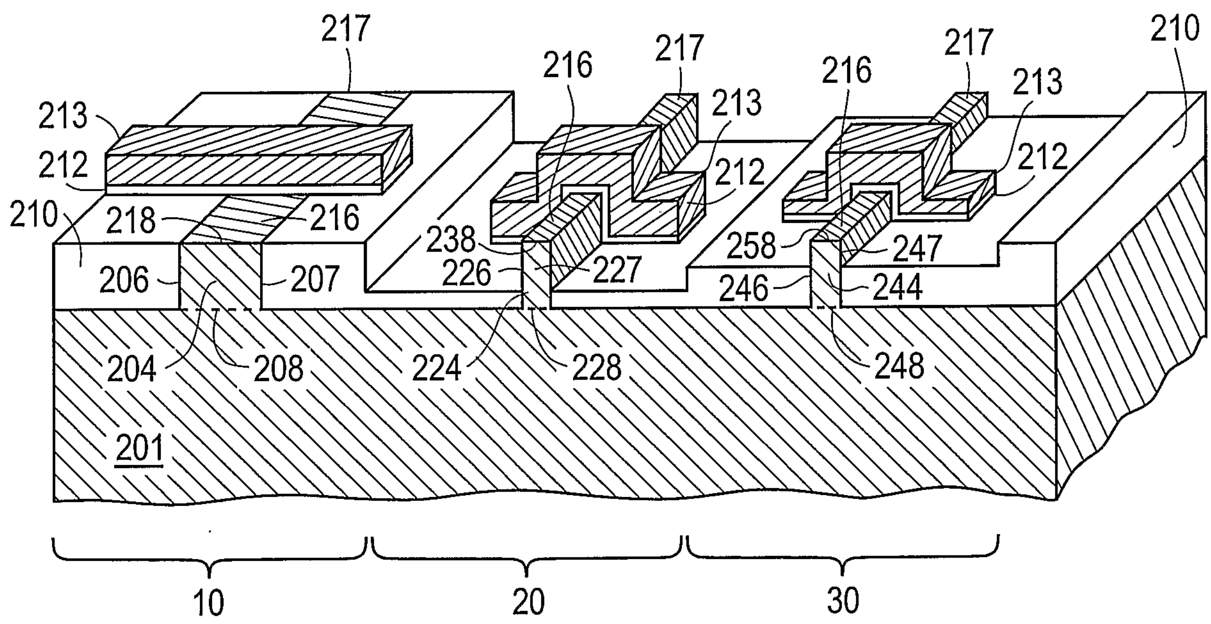

FIG. 2

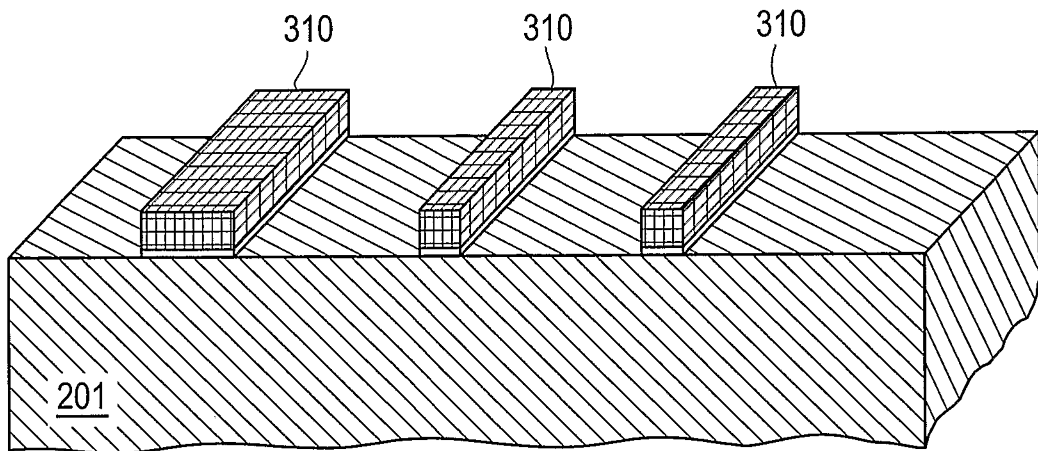

FIG. 3A

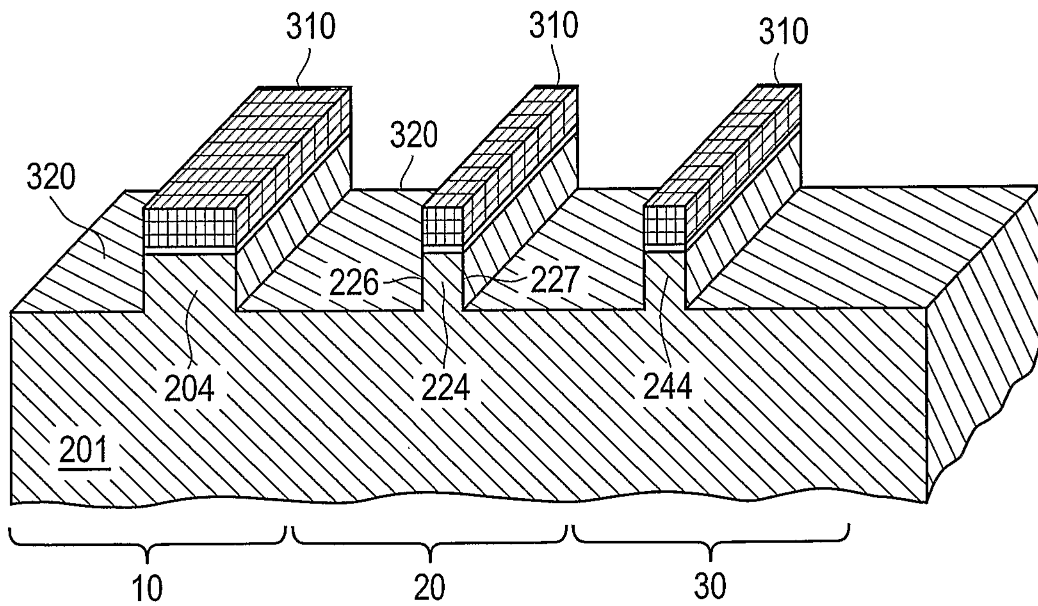

FIG. 3B

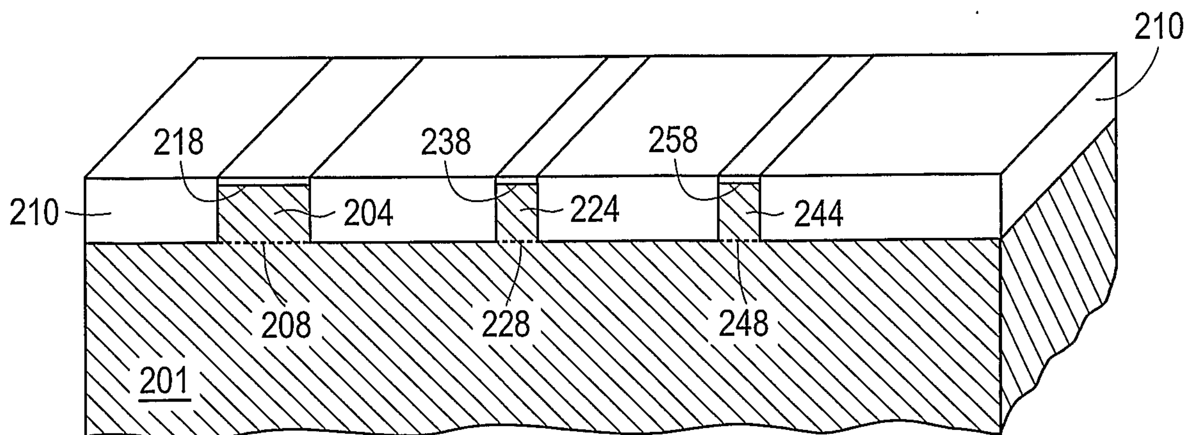

FIG. 3C

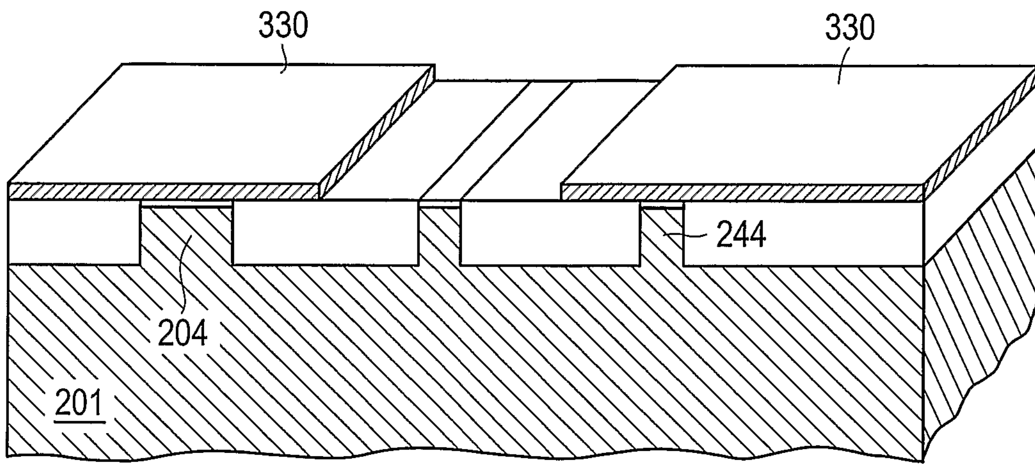

FIG. 3D

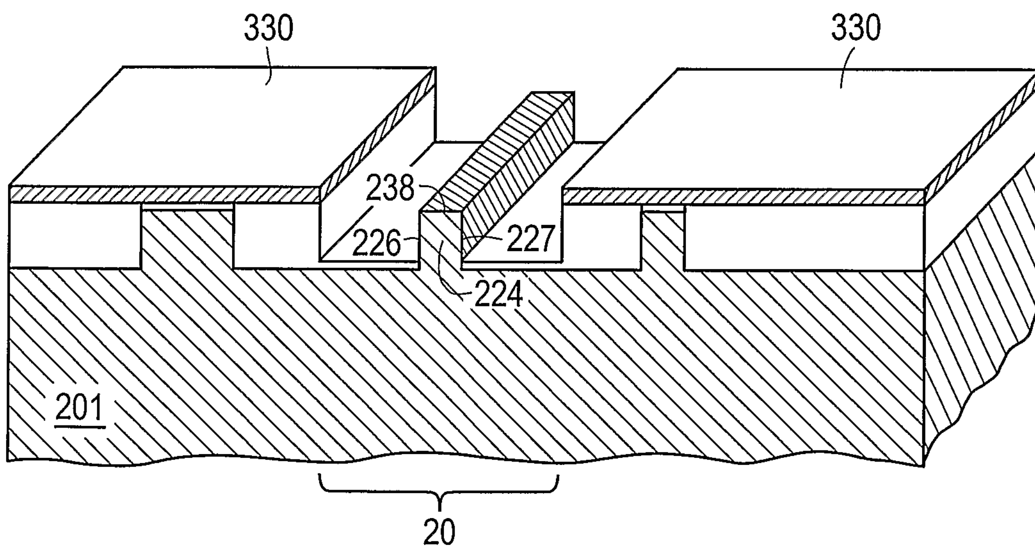

FIG. 3E

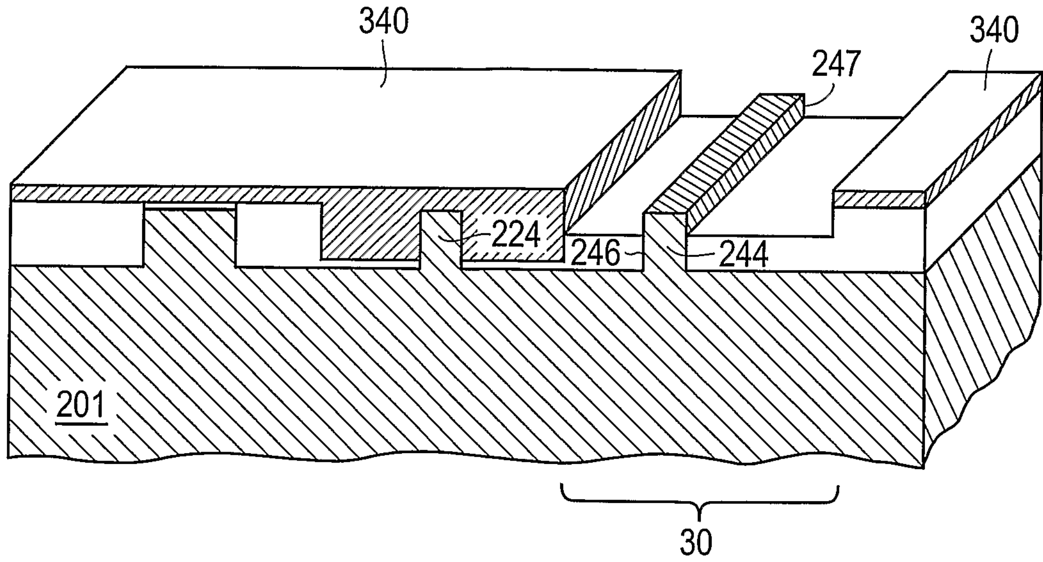

FIG. 3F

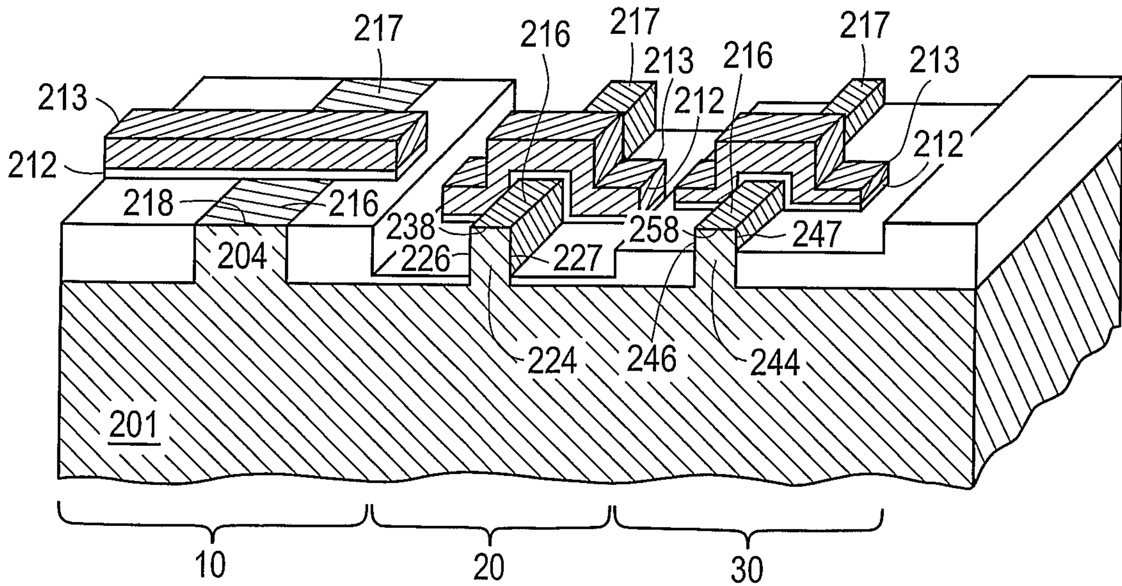

FIG. 3G