March 11, 1969 E. I. SCHWARTZ 3,432,754

MATCHED SIGNAL TRANSMITTER-RECEIVER ARRANGEMENT

Filed Nov. 13, 1964 Sheet 1 of 13

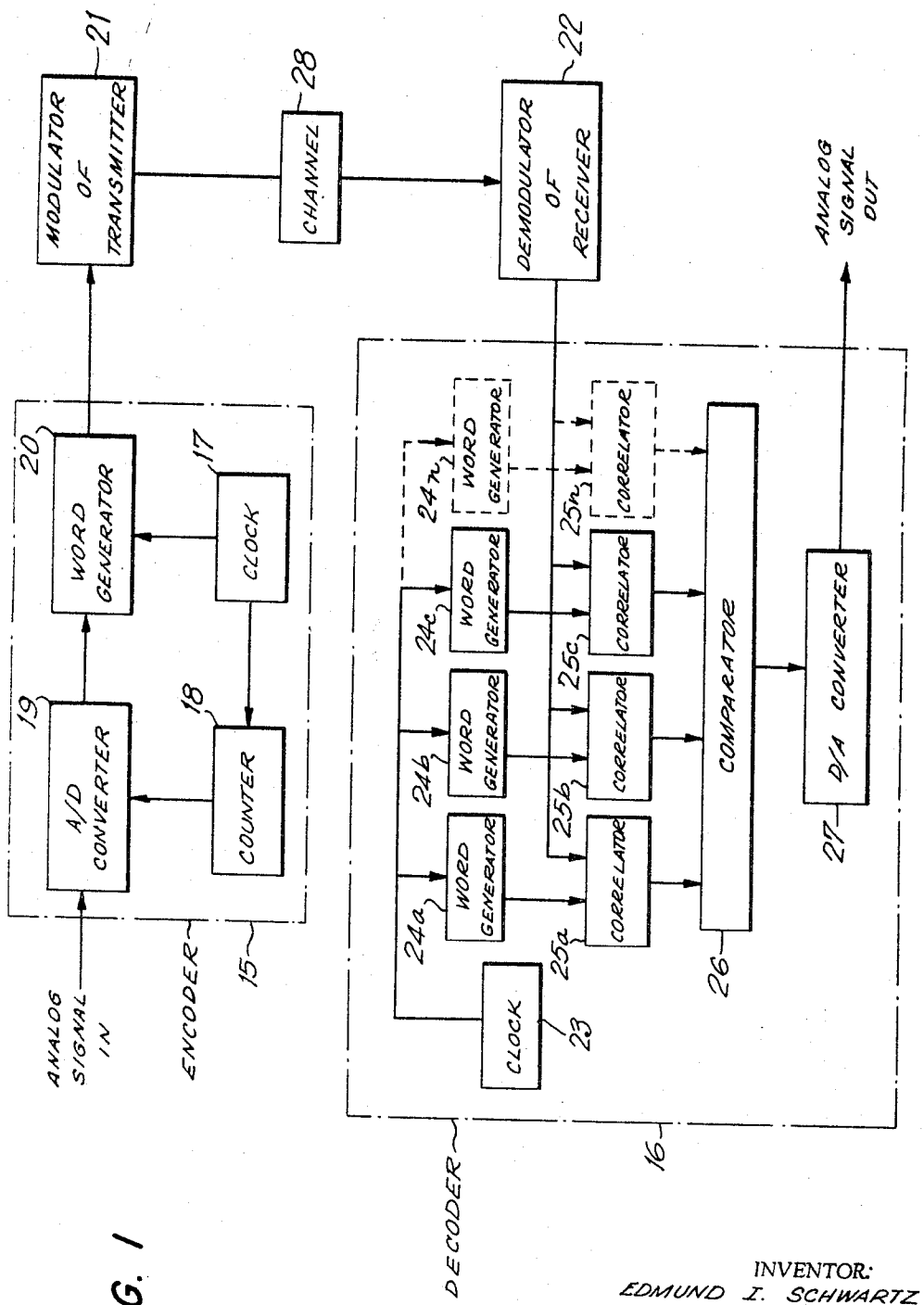


FIG. 1

INVENTOR:
EDMUND I. SCHWARTZ

BY
Breitenfeld & Levine
ATTORNEYS

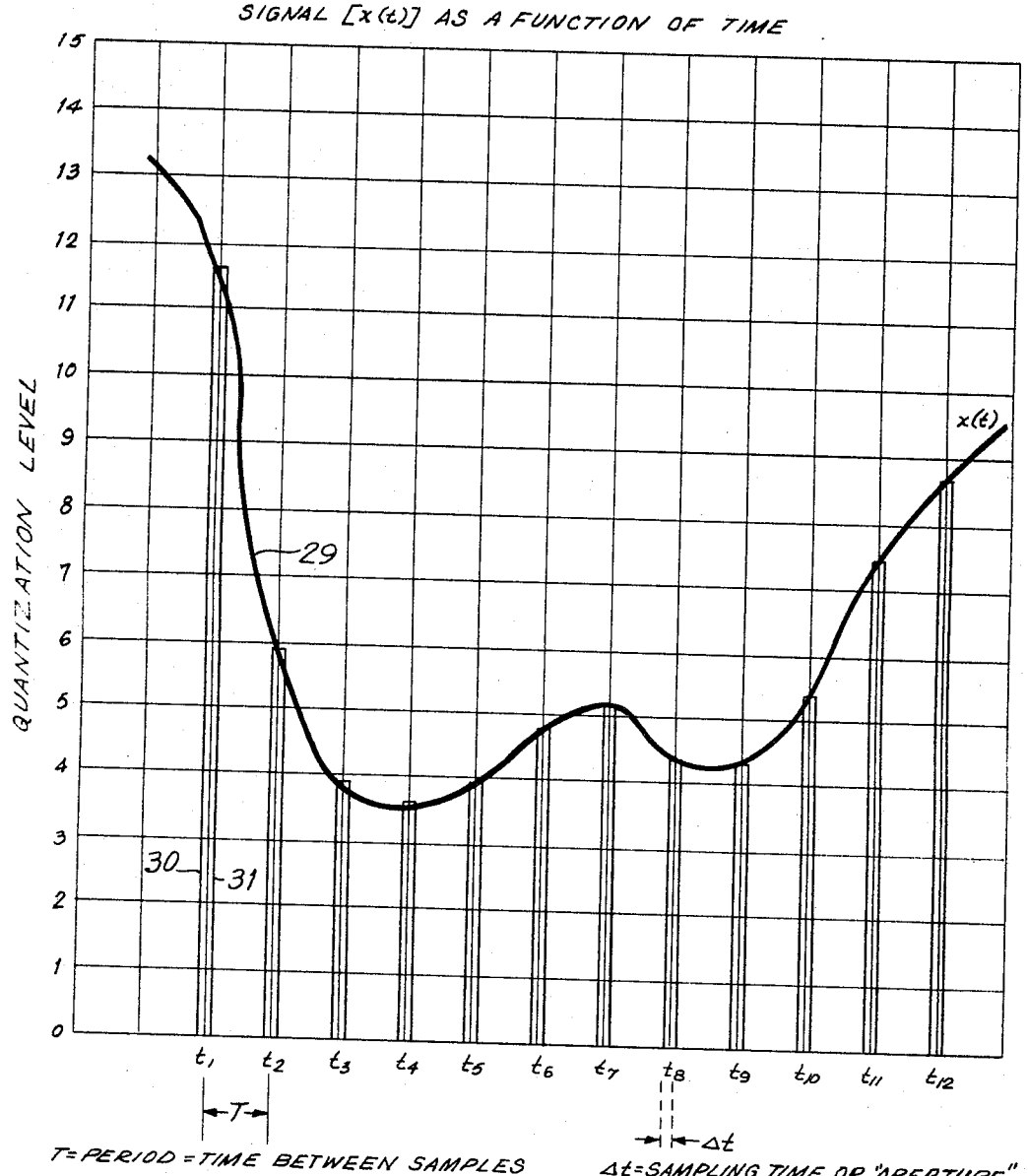
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MATCHED SIGNAL TRANSMITTER-RECEIVER ARRANGEMENT

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FIG. 2



INVENTOR:
EDMUND I. SCHWARTZ

BY
Breitenfeld & Levine
ATTORNEYS

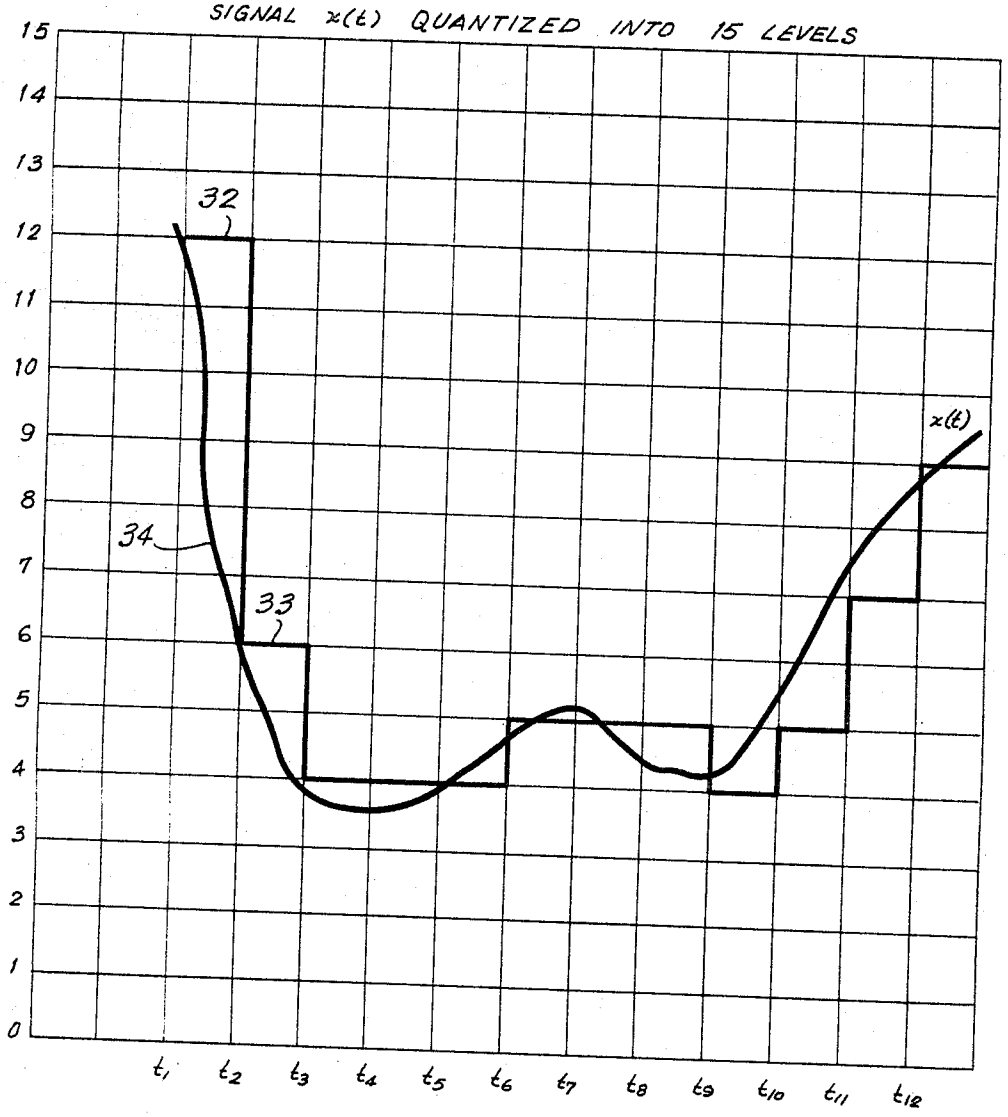
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FIG. 3



INVENTOR:
EDMUND I. SCHWARTZ

BY:
Brattenfeld & Levine
ATTORNEYS

FIG. 4

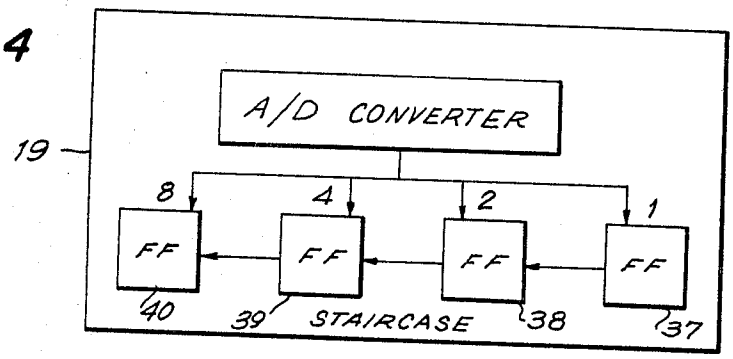


FIG. 5

TABLE A

STAIRCASE SETTINGS FOR $x(t)$

SAMPLING TIME	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}
QUANTIZATION LEVEL	12	6	4	4	4	5	5	5	4	5	7	9

TABLE B

FLIP-FLOP STATE

SAMPLING TIME	#40	#39	#38	#37
t_1	1 (ON)	1 (ON)	0 (OFF)	0 (OFF)
t_2	0	1	1	0
t_3	0	1	0	0
t_4	0	1	0	0
t_5	0	1	0	0
t_6	0	1	0	1
t_7	0	1	0	1
t_8	0	1	0	1
t_9	0	1	0	0
t_{10}	0	1	0	1
t_{11}	0	1	1	1
t_{12}	1	0	0	1

INVENTOR:
EDMUND I. SCHWARTZ
BY
Breitenfeld & Levine
ATTORNEYS

FIG. 6

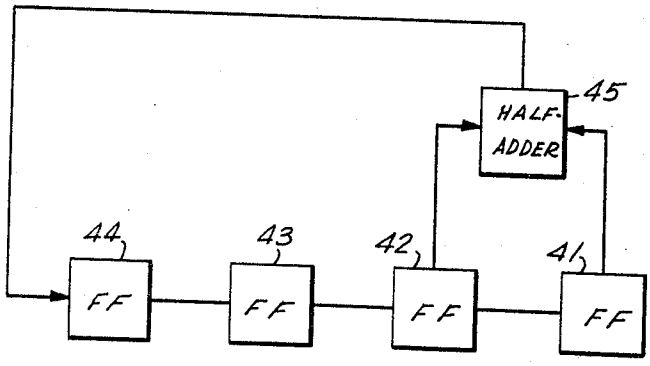


FIG. 7

PULSE NO.	FLIP-FLOP STATE 44	43	42	41	QUANTIZATION LEVEL
1	1	1	1	1	15
2	0	1	1	1	7
3	0	0	1	1	3
4	0	0	0	1	1
5	1	0	0	0	8
6	0	1	0	0	4
7	0	0	1	0	2
8	1	0	0	1	9
9	1	1	0	0	12
10	0	1	1	0	6
11	1	0	1	1	11
12	0	1	0	1	5
13	1	0	1	0	10
14	1	1	0	1	13
15	1	1	1	0	14
16	1	1	1	1	
17	0	1	1	1	
18	0	0	1	1	

INVENTOR:
EDMUND I. SCHWARTZ
BY Breitenfeld & Levine
ATTORNEYS

MATCHED SIGNAL TRANSMITTER-RECEIVER ARRANGEMENT

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	44	43	42	41	44'	43'	42'	41'
t_1	1	1	0	0				
$t_1 + T/15$	0	1	1	0				
$t_1 + 2T/15$	1	0	1	1				
$t_1 + 3T/15$	0	1	0	1				
$t_1 + 4T/15$	1	0	1	0				
$t_1 + 5T/15$	1	1	0	1				
$t_1 + 6T/15$	1	1	1	0				
$t_1 + 7T/15$	1	1	1	1				
$t_1 + 8T/15$	0	1	1	1				
$t_1 + 9T/15$	0	0	1	1				
$t_1 + 10T/15$	0	0	0	1				
$t_1 + 11T/15$	1	0	0	0				
$t_1 + 12T/15$	0	1	0	0				
$t_1 + 13T/15$	0	0	1	0				
$t_1 + 14T/15$	1	0	0	1				
$t_1 + 15T/15 = t_2$								
$t_2 + T/15$								
$t_3 + 2T/15$								
					0	1	1	0
					1	0	1	1
					0	1	0	1
					1	0	1	0
					1	1	0	1
					1	1	1	0
					1	1	1	1
					0	1	1	1
					0	0	1	1
					0	0	0	1
					1	0	0	0
					0	1	0	0
					0	0	1	0
					1	0	0	1
					1	1	0	0
t_3	0	1	0	0				
$t_3 + T/15$	0	0	1	0				
$t_3 + 2T/15$	1	0	0	1				
	1	1	0	0				
	0	1	1	0				
	1	0	1	1				
	0	1	0	1				
	1	0	1	0				
	1	1	0	1				
	1	1	1	0				
	1	1	1	1				
	0	1	1	1				
	0	0	1	1				
	0	0	0	1				
	1	0	0	0				
t_4								
$t_4 + T/15$								
					0	1	0	0
					0	0	1	0
					1	0	0	1
					1	1	0	0
					0	1	1	0
					1	0	1	1
					0	1	0	1
					1	0	1	0
					1	1	0	1
					1	1	1	0
					1	1	1	1
					0	1	1	1
					0	0	1	1

FIG. 8

INVENTOR:
EDMUND I. SCHWARTZ
BY.
Breitenfeld & Levine
ATTORNEYS

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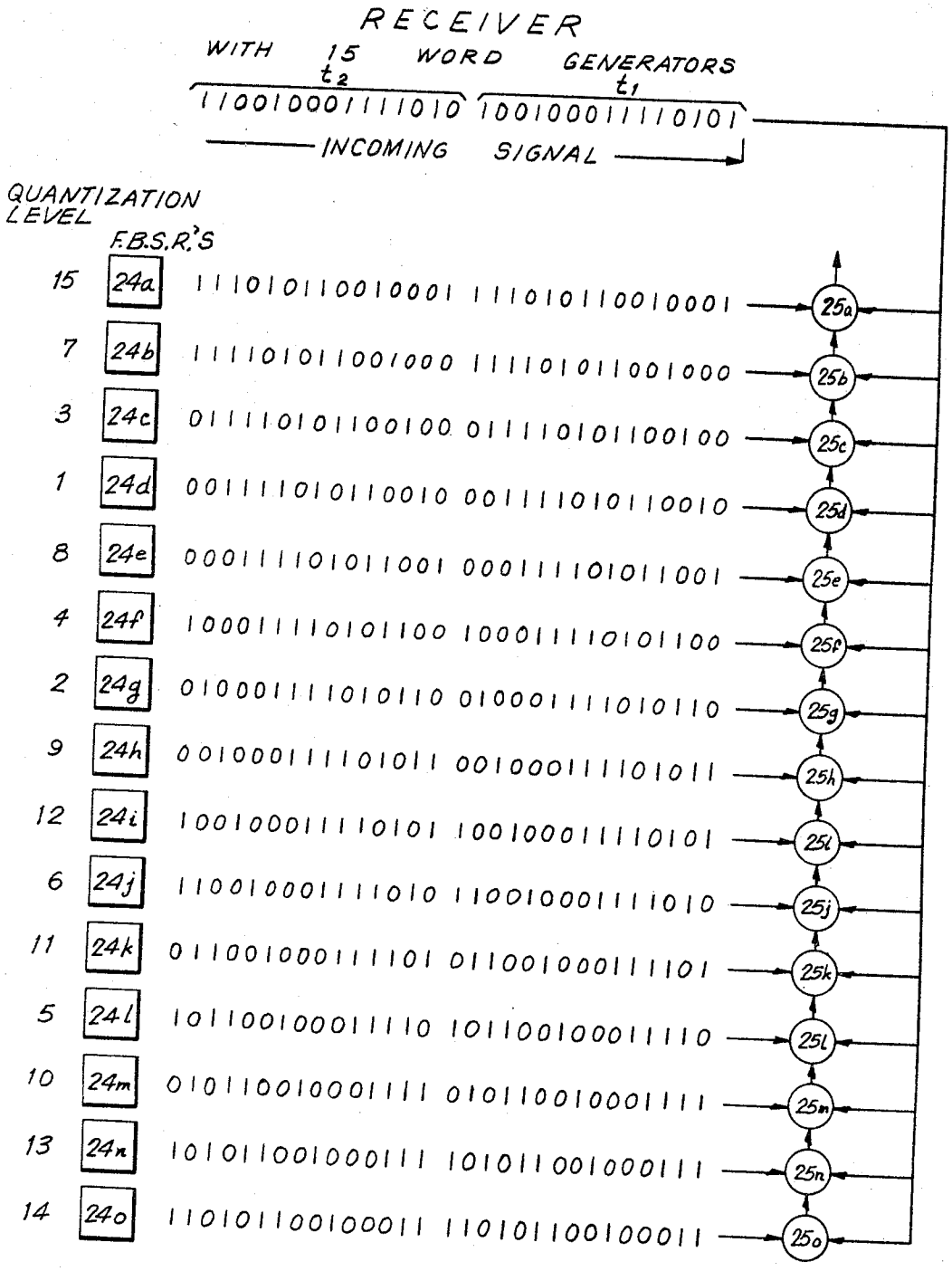


FIG. 9

INVENTOR:
EDMUND I. SCHWARTZ
BY Pretenfeld & Levine
ATTORNEYS

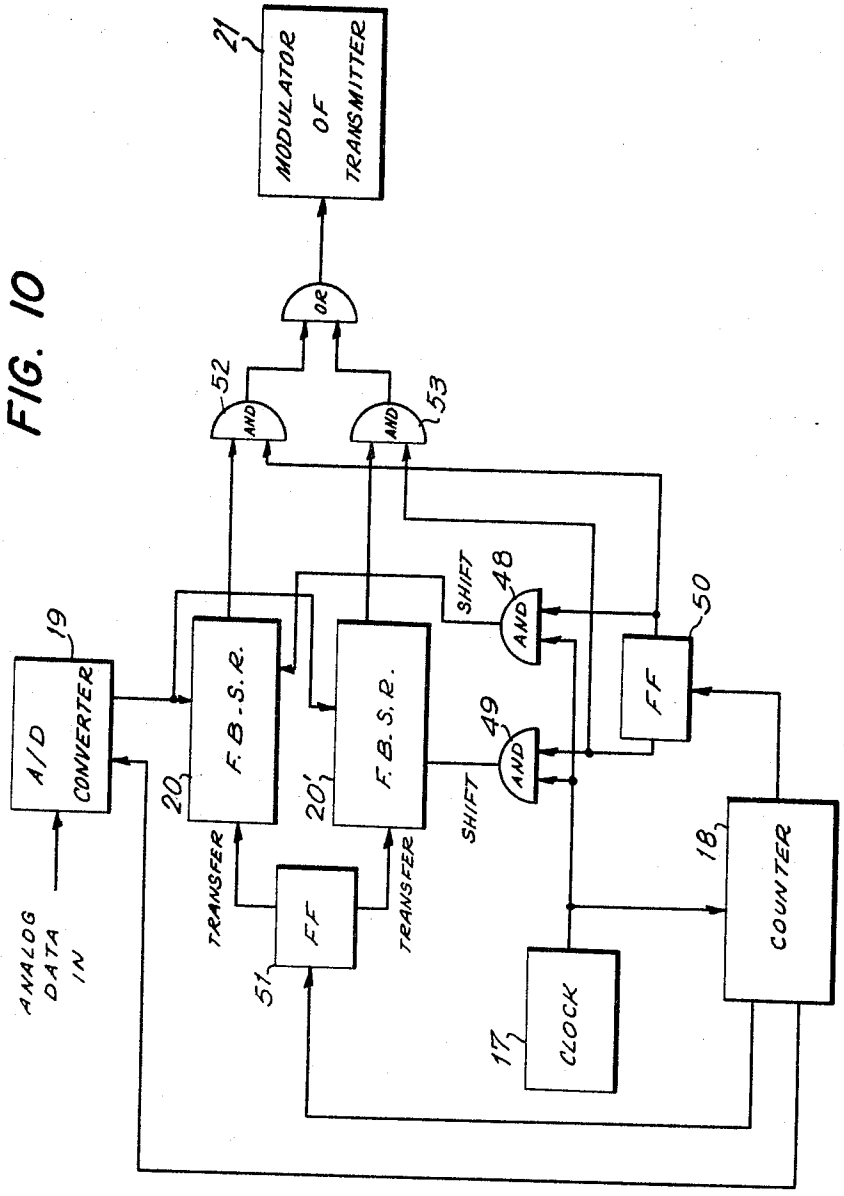
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FIG. 10



INVENTOR:
EDMUND I. SCHWARTZ

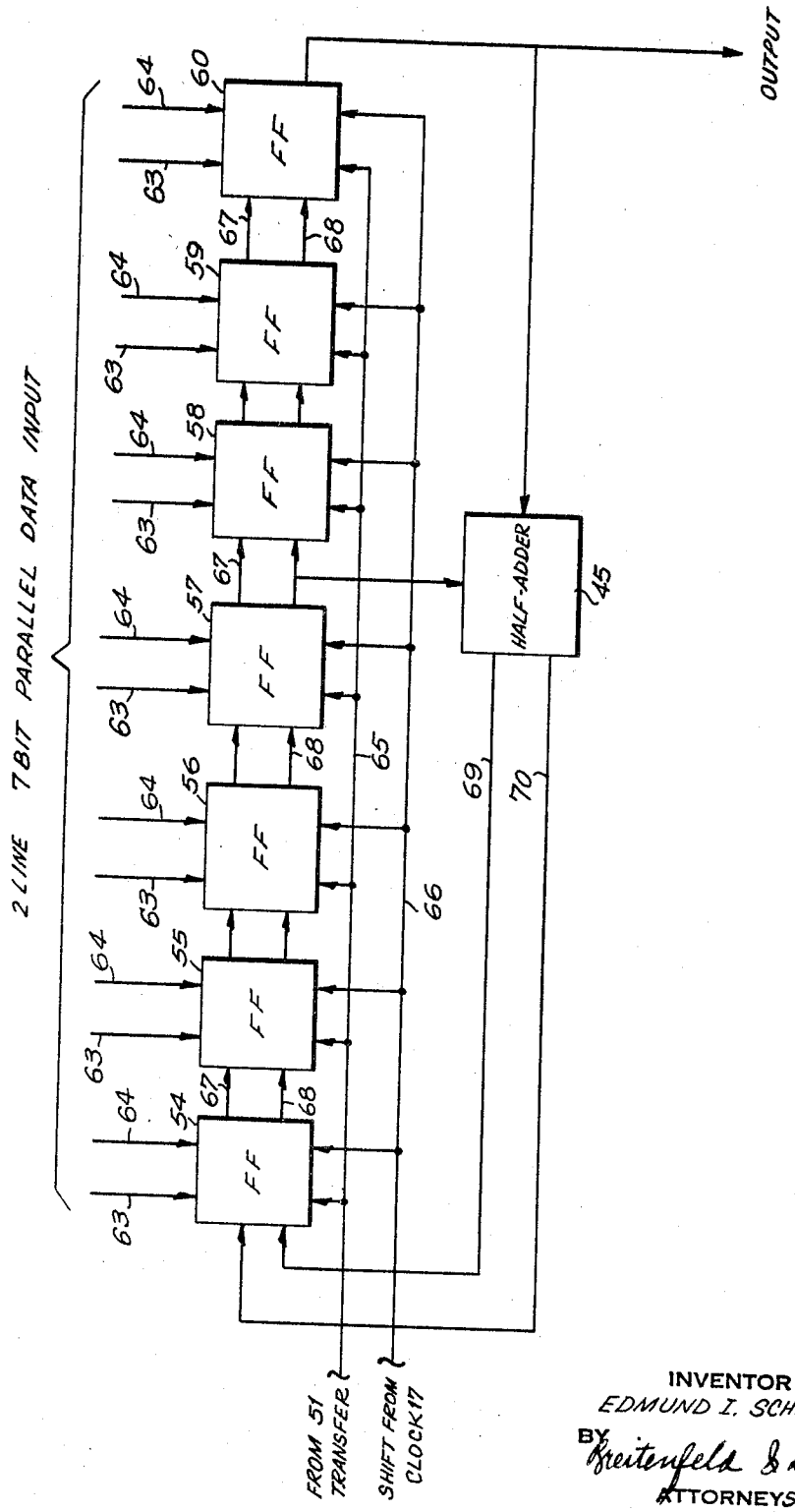
BY Breitenfeld & Levine
ATTORNEYS

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FIG. 11



INVENTOR:
EDMUND I. SCHWARTZ
BY Breitenfeld & Levine
ATTORNEYS

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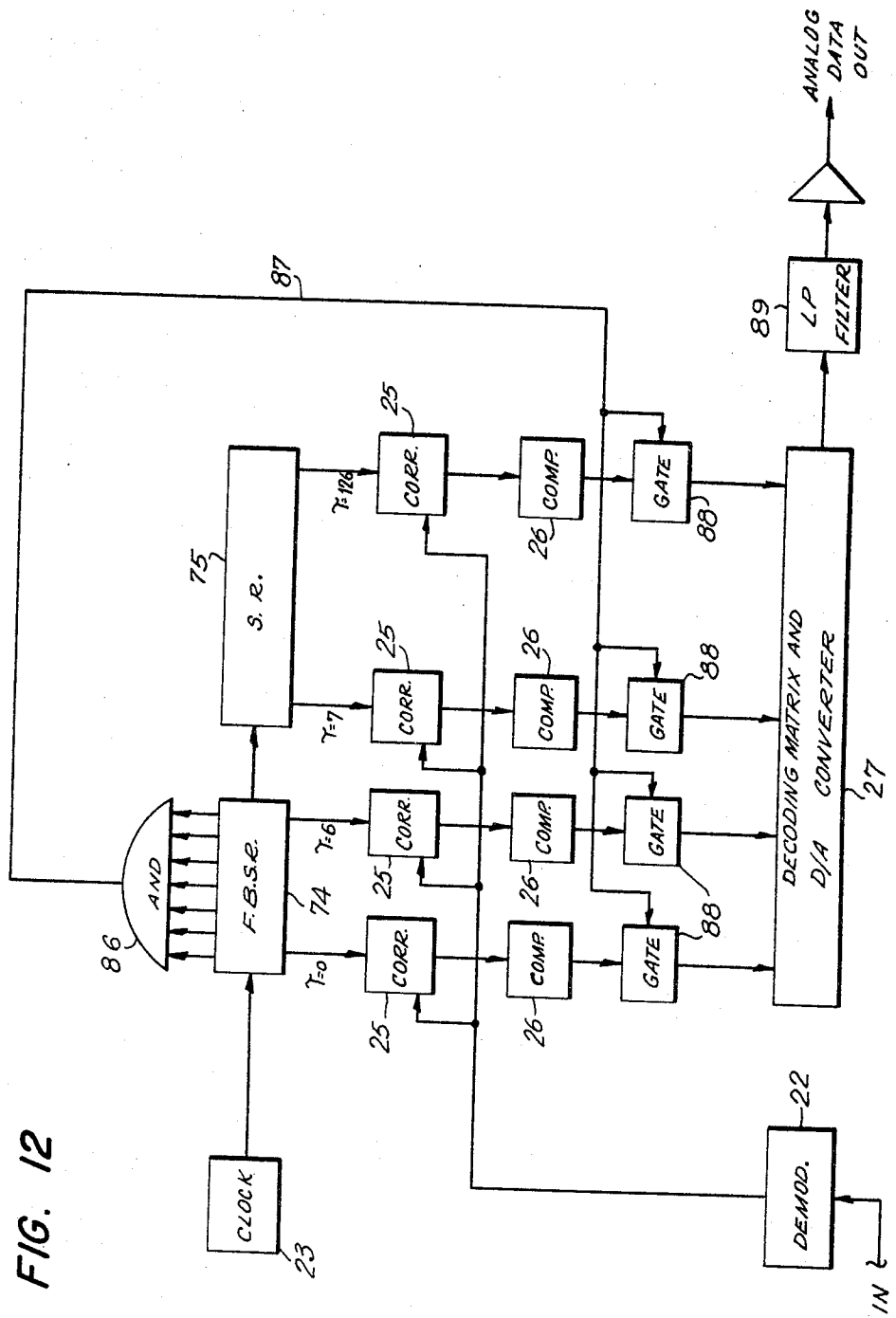


FIG. 12

INVENTOR:
EDMUND I. SCHWARTZ
BY
Brustenfeld & Levine
ATTORNEYS

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FIG. 13

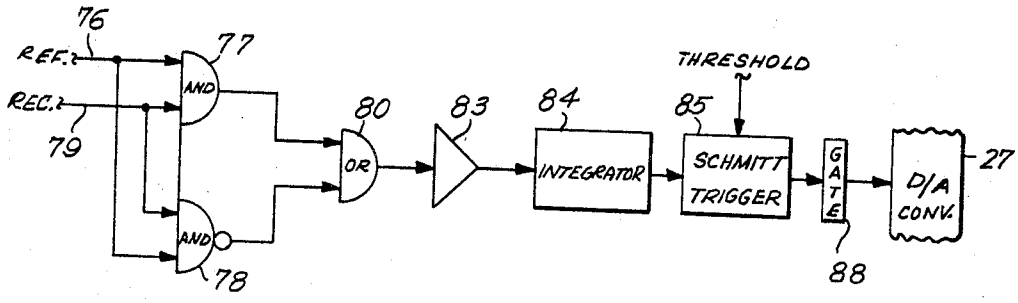
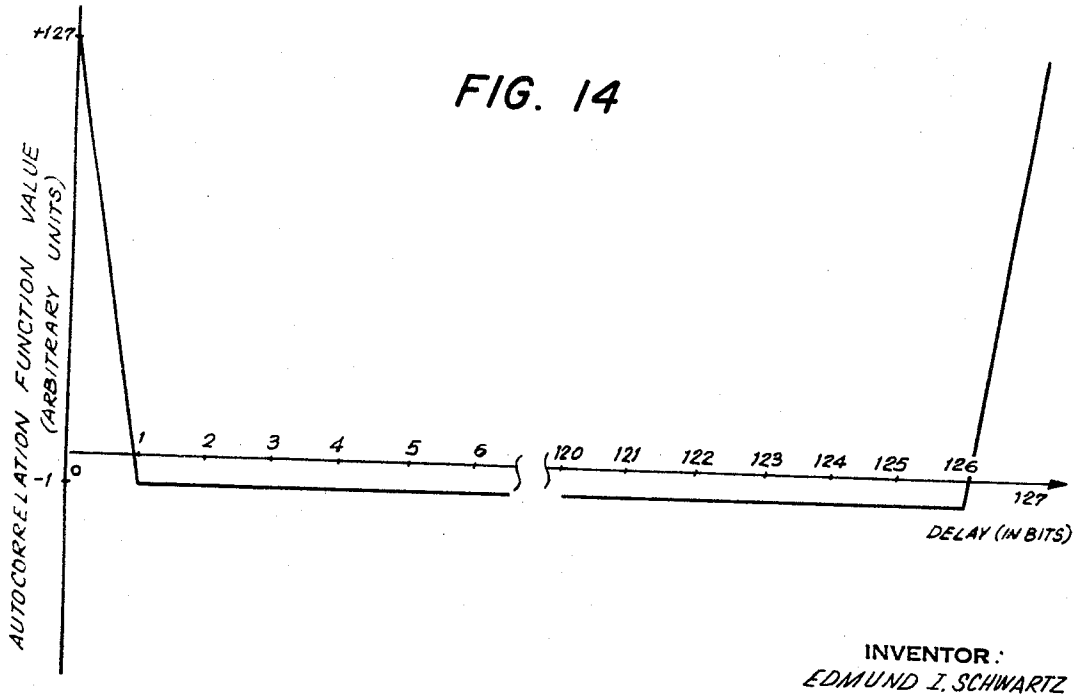


FIG. 14



INVENTOR:
EDMUND I. SCHWARTZ
BY
Breitenfeld & Levine
ATTORNEYS

FIG. 15

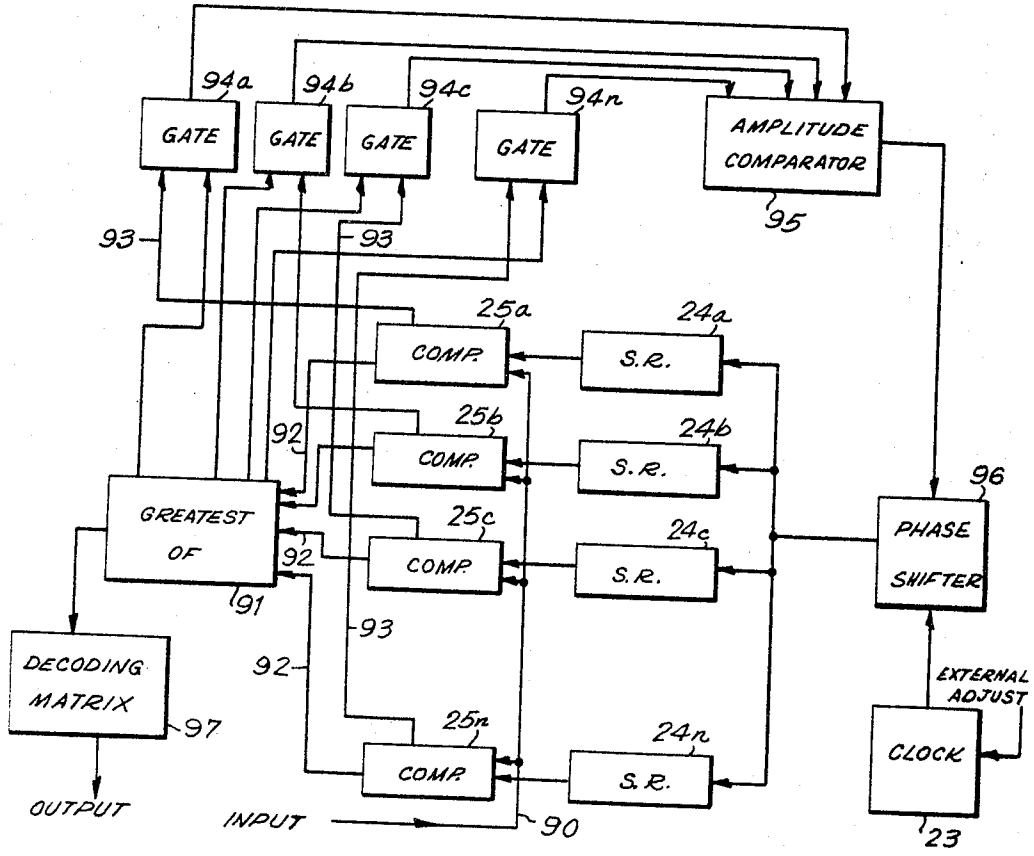
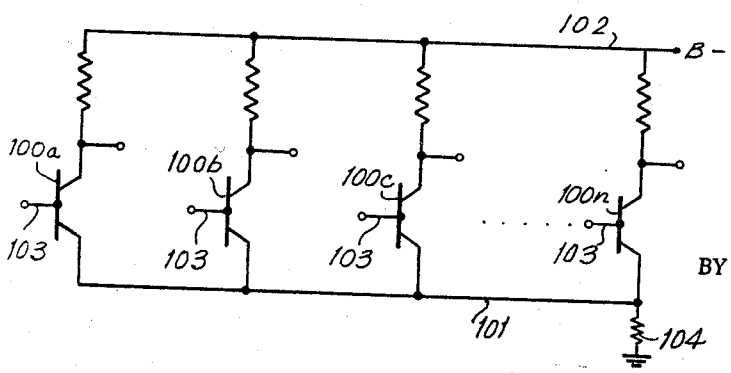


FIG. 16



INVENTOR:
EDMUND I. SCHWARTZ
BY Brutenfeld & Levine
ATTORNEYS

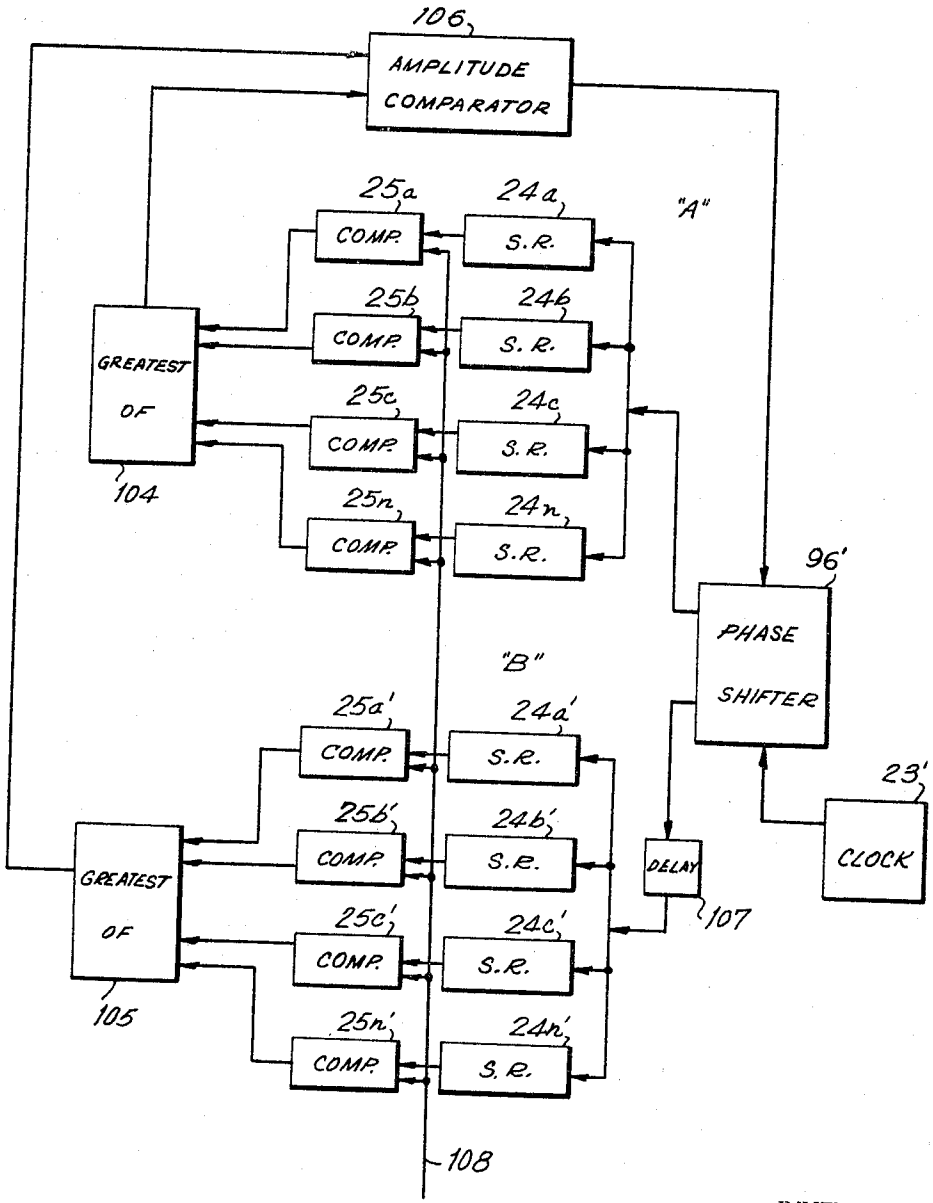
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FIG. 17



INVENTOR:
EDMUND I. SCHWARTZ

BY Brustenfeld & Levine

ATTORNEYS

United States Patent Office 3,432,754
Patented Mar. 11, 1969

3,432,754

MATCHED SIGNAL TRANSMITTER-RECEIVER ARRANGEMENT

Edmund I. Schwartz, Fair Lawn, N.J., assignor to Devenco Incorporated, New York, N.Y., a corporation of New York

Filed Nov. 13, 1964, Ser. No. 411,058
U.S. Cl. 325—38 13 Claims
Int. Cl. H04b 1/06, 1/16; H03k 13/00

ABSTRACT OF THE DISCLOSURE

Arbitrary signal quantized at regular intervals into a predetermined number of levels, and a different pseudo-random binary word transmitted for each level. Every possible word simultaneously produced in receiver, and comparison with transmitted word yields signal at quantization level of sampled signal. Sampling may be done by analog-to-digital converter (A/DC) adapted to initially set a shift register which produces the pseudo-random binary words. Receiver may include shift register for producing words, correlators for determining identity of transmitted word, comparator for producing a signal corresponding to output of sampling A/DC, and digital-to-analog converter for producing signal whose amplitude matches that of sampled signal.

This invention relates to a transmission system for electromagnetic signals having arbitrary amplitude variations with respect to time, and more particularly to such a system employing a correlation type receiver and transmitter.

Correlation type receivers, otherwise known as matched-filter receivers, are well known. They are usually employed in transmission systems in which the signal transmitted and to be received has a predetermined pattern of amplitude variation with respect to time. An example of such a system is a radar system, wherein a signal of known characteristics is transmitted, and upon reflection, received by the receiver of the system. For systems such as these, a matched filter receiver may readily be built because the manner in which the amplitude of the signal varies is known in advance. A matched filter receiver is one so designed that its output, in response to the transmitted signal to which it is matched, will be least disturbed by the inherent noise in the receiver system, i.e., the output signal-to-noise ratio of the receiver will be a maximum when it receives the signal to which it is matched. As a result, a correlation type or matched filter receiver offers a maximum probability of detection of the transmitted signal for any particular power input, distance between transmitter and receiver, and false alarm rate (number of instances per unit time that noise is interpreted by the receiver as a transmitted signal).

In the case of communications systems, and in particular, systems for transmitting speech, the amplitudes of the modulating signals vary in no predetermined fashion. As a result, it has not been possible to build a receiver matched to the transmitted signal, and consequently all the advantages of matched transmitter-receiver systems have not been obtainable.

It is therefore the primary object of the present invention to provide a matched transmitter-receiver system for use in transmitting signals having arbitrary amplitude variations with respect to time.

It is another object of the invention to provide a technique for transmitting and receiving speech, and like information, over greater distances than heretofore possible for a given power input and quality of reception.

To accomplish these objectives, I have conceived of the idea of fragmentizing or quantizing the information

to be transmitted into a perdetermined number of states or levels, and providing means for generating a different discrete signal having a special property, corresponding to each level. The same predetermined number of receivers are employed, each one matched to one of the discrete signals. The particular discrete signals employed are characterized by the fact that each produces a relatively large output when applied to the receiver which is matched to it, and an insignificant output when applied to all the other receivers. Thus, the chances of misinterpreting the discrete signals, as by mistaking one for another, are greatly diminished. Since any arbitrary signal can be broken into the various proposed amplitude levels, any signal can be transmitted by means of the predetermined, and hence known, discrete signals. Thus, it is possible to build a receiver, or more correctly an assembly of receivers, matched to the signals which will be transmitted, regardless of the nature of the information to be transmitted.

A feature of the invention is its ability to yield any desired quality of reproduction of the original information signal at the receiver. The quality of reproduction is a function of the number of levels into which the original signal is quantized. Thus, the greater the number of levels, the higher the quality of reproduction.

Another feature of the invention is its ability to quickly transform the amplitude of the original information signal at any instant of time to a particular one of a predetermined number of code signals, and transmit the code signal to a receiver adapted to receive the code signal and reconvert it to a signal having an amplitude level corresponding to the level of the original signal at the instant it was sampled. This ability to transform any amplitude level to a particular code signal is achieved by utilizing the technique of generating a predetermined number of pseudo-random binary words, and controlling the operation of the binary word generator by a means which samples the information signal and thereby determines the particular binary word to be generated. The predetermined number of different words which the word generator is capable of producing equals the number of levels into which the original signal is quantized, whereby one particular pseudo-random binary word can correspond to each quantized level.

As used herein, the term "pseudo-random binary word" is intended to mean a word comprising n bits, wherein any sequence of a particular number of successive bits is non-repetitive until after the "nth" bit has been generated, the particular number being equal to the number of bits in the preliminary word initially inserted into the word generator.

In its preferred form, the invention employs an analog-to-digital converter for sampling the original information-bearing signal and producing a digital ouptut, or preliminary word, corresponding to the amplitude level of the signal at the instant of sampling. The preliminary word is inserted as an initial setting into a word generator, which may be a shift register employing the standard technique of feed-back with half-adding, thereby determining the particular pseudo-random binary word which will be produced by the generator. This particular word corresponds to the amplitude level of the original signal at the time of sampling by the analog-to-digital converter, and this same word will be generated each time the amplitude of the original signal is at the particular level to which the word corresponds. The binary or code word may be transmitted to the receiver by any standard technique, such as by modulating a radio wave.

In the receiver are a number of word generators equal to the number of different words which can be produced by the word generator at the transmitter end of the system. Each of the receiver word generators continuously

and repeatedly produces a reference word identical to one of the possible words which can be produced by the transmitter word generator. Correlator means in the receiver compare the code word transmitted with all the reference words, and upon sensing correlation between the code word and one of the reference words causes a signal to be engendered having an amplitude corresponding to the amplitude level of the original signal sample which led to the generation of the particular transmitted code word.

The present invention employs a very special type of code and reference words exhibiting a property which enables the invention to perform an autocorrelation function. When a code word of the type employed is correlated with the reference word identical to it, the correlator means produces a relatively large positive output. However, all other correlators comparing that code word with their respective reference words will produce negative outputs. Thus, the output of the correlator corresponding to the transmitted code word can easily be distinguished from the outputs of the other correlators, even under extremely adverse conditions, e.g. noise in the system.

It will be appreciated that the desired behavior of the present invention is dependent upon the code words at the transmitter end of the system being generated at the same rate as each reference word at the receiver end of the system, so that there is no changing time delay between generation of each code word and generation of a series of reference words with which it is to be compared. It is therefore a feature of the invention to provide means for synchronizing, and maintaining synchronization of, all the word generators in the system by means of the signal carrying the code words from the transmitter to the receiver, i.e., without the need for a separate synchronization signal. Obviously, if desired, a separate synchronization signal could be employed.

Another feature of the invention is the provision of two word generators at the transmission end of the system operating in "leap-frog" fashion, i.e., while a preliminary word is inserted into one of the word generators, the other is in operation producing a code word. In this way, a continuous stream of encoded information is produced, without interruption, at the transmitter end of the system.

Other features and advantages of the invention will be apparent from the following description in which reference is made to the accompanying drawings.

In the drawings:

FIG. 1 is a simplifide block diagram of an encoder and decoder according to this invention;

FIG. 2 is a diagram showing a arbitrary information-bearing signal being sampled;

FIG. 3 is a diagram showing the signal of FIG. 2 as reproduced by an encoder and decoder according to this invention;

FIG. 4 is a simplified diagram of an analog-to-digital converter;

FIG. 5 is a table indicating the conditions of the flip-flop circuits of the analog-to-digital converter as a result of sampling the signal of FIG. 2;

FIG. 6 is a simplified diagram of a feed-back shift register;

FIG. 7 is a table indicating the pseudo-random words which may be produced by the shift register of FIG. 6;

FIG. 8 is a table indicating which particular pseudo-random words are produced by the first four samplings of the signal of FIG. 2;

FIG. 9 is a diagram showing the pseudo-random words entering the decoder, and the reference words produced in the decoder;

FIG. 10 is a more detailed block diagram of an encoder according to this invention;

FIG. 11 is a block diagram of one of the shift registers of FIG. 10;

FIG. 12 is a more detailed block diagram of a decoder according to this invention;

FIG. 13 is a block diagram of one of the correlators of FIG. 12;

FIG. 14 is a diagram indicating the autocorrelation function of a pseudo-random binary word;

FIG. 15 is a block diagram of means for maintaining synchronization between the encoder and decoder;

FIG. 16 is a schematic diagram of the "greatest of" circuit of FIG. 15; and

FIG. 17 is a block diagram of another means for maintaining synchronization between the encoder and decoder.

The general mode of operation of an illustrative embodiment of the invention will be described with reference to FIG. 1. An encoder for transforming successive samples of an information-bearing signal into code words for transmission to a distant receiver is defined by the upper dot-dash rectangle **15**, and a decoder for retransforming the transmitted code words into signals having amplitudes corresponding to the amplitudes of the successive signal samples is defined by the lower dot-dash rectangle **16**. The signal samples entering the encoder **15** are labeled "analog signal in," and the reconstituted signals leaving the decoder **16** are labeled "analog signal out."

The encoder **15** includes a clock **17** running continuously at a predtermined rate. The clock causes actuation of a counter **18** which in turn controls the operation of an analog-to-digital converter **19** (sometimes referred to hereinafter as "A/DC"). The clock also actuates a word generator **20**. At a predetermined count of the counter **18**, the A/DC **19** samples the information-bearing signal, and produces a digital output corresponding to the amplitude level of the information signal at the time of sampling. The A/DC **19** is capable of producing a predetermined number of different digital outputs, and consequently is capable of quantizing the information signal, or dividing it, into the same predetermined number of quantized amplitude levels, each of the possible digital outputs corresponding to a differnt quantized level of the amplitude of the information signal. The digital output of the A/DC **19** is inserted into the word generator **20**, thereby conditioning the word generator to produce a particular code word. The word generator is capable of producing a predetermined number of differnet code words equal to the number of different digital outputs capable of being produced by the A/DC. The particular code word produced by the word generator **20** is determined by the particular digital signal it receives from the A/DC **19**, and any particular code word produced, therefore, corresponds to the quantized level of the information signal amplitude at the time of sampling by the A/DC. Once the digital output of the A/DC has been inserted into the word generator, the clock **17** activates the latter causing it to produce a code word.

The code word may be transmitted to a receiver by means of any standard technique, and the manner in which this is done forms no part of the present invention. For example, the code word may be applied to the modulator **21** of a radio transmitter. The output of the transmitter is applied through an appropriate channel **28** to the demodulator **22** of a receiver, and the code word is thus delivered to the decoder **16**.

The decoder includes a clock **23** running continuously at a rate equal to the rate of the clock **17** in the encoder. The clock pulses are applied to a series of word generators **24***a*, **24***b*, **24***c*, and **24***n* activating them and causing them to produce code words simultaneously. The number of word generators present in the decoder equals the number of different code words capable of being produced by the word generator **20** in the encoder. Furthermore, each of the word generators **24***a–n* is arranged to continuously and repeatedly produce a different one of the possible code words which may be produced by the word generator **20**. Consequently, each time a code

word is transmitted from the encoder **15** to the decoder **16**, the transmitted code word will be identical to one of the code words produced by the word generators **24***a–n* of the decoder, and will differ from the code word produced by every other word generator in the decoder. Associated with each of the word generators **24***a–n* is a correlator which receives the code word produced by the word generator. Thus, the word produced by the word geneator **24***a* is applied to correlator **25***a*, the word produced by the word generator **24***b* is applied to correlator **25***b*, and so forth. The code word received from the encoder is also applied to all the correlators **25***a–n*, simultaneously.

The correlators compare the code word transmitted from the encoder with the words received from their respective word generators, and all but one correlator produce a small negative output, because the transmitted word does not match the words received by these correlators from their respective word generators. However, since the transmitted word will always be identical to one of the words produced by the word generators **24***a–n*, one of the correlators will sense agreement between the transmitted word and the word received from its respective word generator. As a result, the output of this correlator will be relatively large and positive. For example, if the transmitted code word is identical to the word produced by the word generator **24***c*, the correlator **25***c* will have a relatively large positive output and each of the other correlators will have a small negative output. The outputs of all the correlators **25***a–n* are applied to a comparator **26**. The comparator responds to the relatively large output of one of the correlators by causing a signal, corresponding to the digital output of the analog-to-digital converter **19** which determined the code word to be produced by the word generator **20**, to be applied to a digital-to-analog converter (D/AC) **27**. In response, the D/AC produces an output signal having an amplitude which matches the quantized level of the information-bearing signal at the time is was sampled. Thus, sampling of the information/bearing signal at successive time intervals causes a signal to be produced by the D/AC which approximates the amplitude of the information signal at the time of the sample, and combining the successive outputs of the D/AC produces a signal approximating the information-bearing signal.

The relationship between an original information-bearing signal and the approximate signal produced by means in accordance with this invention can be seen by comparing FIGS. 2 and 3. The curve **29** of FIG. 2 represents a portion of the original signal, such as speech, the amplitude of which varies arbitrarily with respect to time. Sampling of the signal **29** by the A/DC **19** takes place at intervals t_1, t_2, etc., shown along the horizontal axis, the time T between samples being determined by the counter **18**. Since the sampling time Δt extends for some finite period, each sampling time is defined by two vertical lines, such as the lines **30** and **31** of sampling time t_1, spaced apart along the horizontal or "time" axis. In the specific example to be described below, the A/DC is capable of producing 15 different digital outputs. Hence, FIG. 2 illustrates, along the vertical axis, 15 possible quantization levels of amplitude.

At sampling time t_1, the amplitude of signal **29** is closest to the twelfth quantization level, i.e, the portion of the signal between the lines **30** and **31** is closest to the twelfth quantization level. As a result of this sampling, the decoder **16** produces a signal **32**, beginning at time t_1 in FIG. 3, having an amplitude at the twelfth quantization level. The signal **32** maintains this amplitude level until the next succeeding sampling period. By sampling time t_2 (FIG. 2), the amplitude of signal **29** has dropped to a point closest to the sixth quantization level. Consequently, the decoder **16** produces a new output signal **33** (FIG. 3), beginning at time t_2, having an amplitude at the sixth quantization level. Further comparison of FIGS. 2 and 3 indicates that the amplitude of each decoder output signal approximates the amplitude of the original signal **29** at the time of taking the sample to which the decoder signal corresponds. Suitable means of any well known variety can be employed to "smooth out" the reconstructed signal created by the decoder. The smoothed out reconstructed signal, which approximates the original signal, is indicated by the curve **34**. It is apparent that the greater the number of quantization levels and the shorter the intervals T between samplings, the more faithfully will the original signal be reproduced, i.e., the closer will the reconstructed signal **34** conform to the original signal **29**.

As mentioned above, the successive samples of the original signal are translated into code words by encoder **15** for transmission to the receiver. It has been found advantageous to use a pseudo-random sequence of binary words as the code words because such binary words offer the autocorrelation feature mentioned above and to be discussed in more detail below. However, the invention is not limited to the use of pseudo-random binary words, and any series of words offering the advantages presented by these binary words may be employed. Pseudo-random binary words may be generated by a shift register employing feedback with half addition. According to this technique, a shift register having n stages or flip-flop circuits is capable of producing a maximum of 2^n-1 different pseudo-random words, each word containing 2^n-1 bits. Thus, a shift register having three stages will produce seven different pseudo-random words each containing seven bits; a shift register having four stages will produce fifteen different pseudo-random words, each containing fifteen bits, and so forth. The particular binary word produced by the shift register, during any cycle, depends upon the initial setting of the shift register stages at the beginning of the cycle. Setting the shift register stages is accomplished, according to this invention by the analog-to-digital converter **19**.

The A/DC **19** shown schematically in FIG. 4 has a four stage staircase generator including flip-flop circuits **37**, **38**, **39**, and **40**. This A/DC is capable of setting the stages of a four stage shift register which, when actuated, will produce a fifteen bit binary word. Each flip-flop of the A/DC has, of course, two possible states: "on" or "off," these states being sometimes referred to hereinafter as 1 or 0. By means of any suitable well known arrangement, not shown, the A/DC is able to sample the original information-bearing signal **29** (FIG. 2), and the flip-flops **37–40** will thereupon flip until the output of the staircase generator approximates the amplitude of the signal **29** at the moment of sampling. In well-known fashion, the flip-flop **37** is arranged when "on" to produce an output equal to one unit of the maximum fifteen unit output of the staircase generator, the flip-flop **38** is arranged to produce an output of two units, the flip-flop 39 four units, and the flip-flop 40 eight units. The value of the output produced by each flip-flop is shown above each in FIG. 4. Thus, by appropriate switching of the four flip-flops between their on and off states, any output from one unit to fifteen units can be achieved. Each different output level of the A/DC corresponds to one of the quantization levels, shown in FIG. 2, into which the original signal can be divided.

FIG. 5 shows in Table A the quantization level of the signal **29** at each sampling time shown in FIG. 2, and in Table B the state each of the flip-flops **37–40** assumes as a consequence of each of the samplings. During the first sampling interval t_1, the signal **29** is near the twelfth quantization level. Thus, the staircase generator runs until its output equals twelve units. At this point, the flip-flops **39** and **40** will be on, and the flip-flops **37** and **38** will be off. This setting of the flip-flops will be inserted into the shift register (to be discussed next) and thereby cause the latter to generate a unique fifteen bit pseudo-random binary word. At sampling time t_2, the staircase

generator will run until the flip-flops **38** and **39** are on and flip-flops **37** and **40** are off, thereby yielding an output of six units which corresponds to the sixth quantization level near which the signal **29** exists at time t_2. This new setting of the flip-flops will be inserted into the shift register in order to cause another unique fifteen bit word to be generated. Further reference to FIG. 4 will indicate the setting of the four flip-flops **37–40** at each successive sampling time shown in FIG. 2.

In the present example, the word generator **20** is a feed-back shift register (sometimes referred to hereinafter as "FBSR") shown diagrammatically in FIG. 6. The FBSR includes four stages or flip-flop circuits **41, 42, 43,** and **44,** and the feed-back loop includes a half-adder **45.** Each of the flip-flops **41–44** has two possible states: "on" or "off" ("1" or "0"). When pulses from the clock **17** are applied to the FBSR, the latter steps and produces a fifteen bit pseudo-random binary word. The particular word produced depends upon the initial setting of each of the flip-flops **41–44,** i.e., "on" or "off", at the beginning of the fifteen bit cycle, and the particular feed-back arrangement employed. Just as there are fifteen different possible combinations of states of the four flip-flops **37–40** of the A/DC **19,** there are fifteen different possible combinations of states of the four flip-flops **41–44** of the shift register. Since each initial setting of the flip-flops **41–44** causes a unique fifteen bit pseudo-random binary word to be produced when pulses from clock **17** are applied to the shift register, the shift register is capable of producing fifteen different pseudo-random binary words with any particular feed-back arrangement. It follows, therefore, that each fifteen bit binary word produced by the shift register of FIG. 6 corresponds to one of the fifteen levels into which the original signal can be quantized. This is because the particular binary word produced depends upon the initial setting of the flip-flops **41–44,** and this setting is the same as the setting of the flip-flops **37–40** of the A/DC **19** after the latter samples the original signal and its staircase generator steps to produce an output approximating the amplitude level of the original signal at the time of sampling. When the appropriate output is reached, the states of the flip-flops **41–44** are caused, by suitable well-known means, to assume the states of the flip-flops **37–40,** respectively.

The discussion above mentions that the four flip-flops **37–40** and the flip-flops **41–44** yield fifteen different possible combinations of states, and fifteen different binary words. Actually, of course, there are sixteen possible combinations of states, the combination ignored above being the one in which all flip-flops are "off." The reason that this combination is not considered is that when the initial setting of each of the flip-flops **41–44** is "off", the shift register when stepped will produce nothing more than a series of "0" bits. Such a series is not actually a pseudo-random binary word, and therefore is not treated as one within the context of the present invention. It should be noted, however, that when apparatus according to this invention is in operation during a period in which the original signal **29** discontinues, i.e., falls to the zero quantization level in FIG. 2, the settings of all the flip-flops of the A/DC will be "off" and therefore the flip-flops **41–44** of the shift register will be similarly set, and hence a series of "0" bits will be generated and applied to the modulator **21.** None of the correlators **25***a–n* will sense correlation between this transmitted "word" and its respective reference word, and so there will be no analog output signal from the decoder. Consequently the series of "0" bits is capable of transmitting the information that the original signal has been discontinued.

FIG. 7 illustrates the manner in which the states of the flip-flops **41–44** of the shift register of FIG. 6 change as the shift register steps. For the sake of illustration, assume that all the flip-flops are initially set "on." Thus, a "1" appears under each of the flip-flop reference numerals. As each pulse from clock **17** is applied to the shift register, the state of each flip-flop shifts one flip-flop to the right, i.e., each flip-flop assumes the on or off state previously existing in the flip-flop to its left, and the state of the leftward most flip-flop, **44,** is determined by the feed-back loop including the half-adder **45.** The operation of the feed-back loop is as follows: if both flip-flops **41** and **42** are on (1) or off (0), the flip-flop **44** will be turned off (0); however, if one of the flip-flops **41** and **42** is on and the other is off, the flip-flop **44** will be turned on. When the first pulse is applied to the shift register (the successive pulses are indicated at the left in FIG. 7) the feed-back loop turns flip-flop **44** off, because flip-flops **41** and **42** are both on, and the "on" state of each flip-flop shifts one flip-flop to the right. Thus, all flip-flops remain on except flip-flop **44.** After the second pulse, flip-flop **44** remains off and the flip-flop **43** to its right turns off. With the third pulse, the flip-flop **44** remains off, and the off state shifts to flip-flop **42** as well as flip-flop **43.** Now the states of flip-flops **41** and **42** differ. Hence, when the fourth pulse is applied to the shift register, the feed-back loop causes flip-flop **44** to be turned on. The states of the four flip-flops continue to change in this way throughout the fifteen pulse cycle, and it should be noted that in the course of the fifteen pulse cycle, every possible combination of states of the flip-flops appears (with the exception of all flip-flops "off"). Upon application of the sixteenth pulse, which is the first pulse of the succeeding cycle, the initial state, in which all flip-flops were "on," returns.

The fifteen successive states of the flip-flop **44,** outlined in FIG. 7, represent a pseudo-random binary word. The fifteen bits of this word are applied to the modulator **21** for transmission to the receiver and decoder. The particular word outlined in FIG. 7 corresponds to the fifteenth quantization level of FIG. 2, because it was generated from an initial setting in which all flip-flops **41–44** were "on." It can be seen with reference to FIG. 4 that all flip-flops of the A/DC **19** are "on" when the A/DC samples a signal near the fifteenth quantization level. A quantization level is indicated to the right of each combination of states of the flip-flops **41–44,** in FIG. 7. Upon sampling a signal at any particular quantization level, the A/DC would initially set the flip-flops **41–44** to the states shown corresponding to that quantization level. From that starting point, the successive states of flip-flop **44** would represent a unique fifteen bit binary word.

FIG. 8 shows the fifteen successive combinations of states of the flip-flops **41–44** as they would actually appear as a result of the first four samples indicated in FIG. 2. The combinations resulting from every other sampling are offset for the sake of clarity. At the sample time t_1, the signal **29** is closest to quantization level **12.** FIG. 7 indicates that the initial setting of the flip-flops **44–41** corresponding to the twelfth quantization level is "1", "1", "0", "0", respectively. Hence, this combination is shown opposite time t_1 in FIG. 8. The series of times shown at the left in FIG. 8 indicate the times, after the sampling step, that each successive clock pulse is applied to the shift register. The pseudo-random binary word appearing beneath the reference numeral **44** is the code word corresponding to the twelfth quantization level. At the time of the second sampe, t_2, the signal **29** is closest to the sixth quantization level. Hence, the initial setting of the flip-flops **41–44** is as shown opposite time t_2 in FIG. 8. The pseudo-random binary word shown beneath reference numeral **44'** (the use of the "prime" appendage to this reference numeral will be explained hereinafter) is the code word corresponding to the sixth quantization level. The remaining combinations shown for sampling times t_3 and t_4 will, it is believed, be readily understood in view of the above discussion.

FIG. 9 shows, at the top, the code words transmitted to the receiver as a result of the samplings of signal **29** at times t_1 and t_2. These words should be read from right

to left and are identical to the two code words just discussed with reference to FIG. 8. Below these incoming words are illustrated fifteen word generators or feed-back shift registers **24***a–o*, and fifteen correlators **25***a–o*, within the decoder **16**. Each of the FBSR's **24***a–o* continuously and repeatedly generates a different one of the fifteen possible binary words which can be produced by the FBSR in the encoder **15**, and applies it to its corresponding correlator. The specific binary words are shown extending between the FBSRs and the correlators in FIG. 9. The quantization level corresponding to each of the code words is indicated to the left of the FBSR's. Although each of the FBSR's **24***a–o* continuously reproduces its assigned word, without interruption between repetitions, a space is shown between the repetitions in FIG. 9 for the sake of clarity. The words transmitted to the decoder are applied to each of the correlators **25***a–o*. It will be seen that the first word, resulting from the sampling at time t_1, is identical to only one of the reference words produced by the FBSR's **24***a–o*, namely the word produced by FBSR **24***i* (all words in FIG. 9 are to be read from right to left), and the code word produced by this FBSR corresponds to quantization level **12**. Thus, correlator **25***i* will sense correlation between the incoming word and the reference word applied to it. All the other correlators will sense that the incoming word differs from the reference words applied to them. The outputs of the correlators are used as described above with reference to FIG. 1 and to be described below in more detail.

FIG. 10 illustrates in more detail the operation of the encoder **15**, particularly, the manner in which the various operations of the encoder are controlled. In practice, two word generators or shift registers **20** and **20′** are employed, rather than one as shown in FIG. 1. If only one shift register is used, a delay must necessarily exist between the generation of the last bit of one word and the generation of the first bit of the next succeeding word. The delay is a result of the time required for the A/DC **19** to reset the flip-flops of the shift register, after completion of one code word, in order to determine the next code word which will be generated by the shift register. On the other hand, if two shift registers are employed, the flip-flops of one can be set to condition the shift register to produce an appropriate word, during the time that the other shift register is actually generating a word. In this way, it is possible to obtain a continuous stream of bits from the encoder without any delay whatsoever between the last bit of one word and the first bit of the next succeeding word. In this situation, the time T between samplings (see FIG. 2) will equal the time required to generate one code word. Furthermore, the stream of bits from the encoder remains continuous even during pauses between words or sentences, when speech is being transmitted, since as mentioned above when the amplitude of the original signal drops to zero, the shift register produces a series of "0" bits.

The A/DC **19** of FIG. 10 samples the original signal and sets the flip-flops of one of the shift registers, say the register **20**. Pulses from the clock **17** are applied to the shift registers **20** and **20′** through AND circuits **48** and **49**, respectively. The AND circuits operate alternatively to transmit the clock pulses under control of a flip-flop circuit **50** which is in turn controlled by the counter **18**. In the present example, the AND circuit **48** transmits pulses to the FBSR **20**, whereby the latter generates a code word. The outputs of the FBSR's are passed to the modulator **21** of the transmitter by AND circuits **52** and **53**, respectively, and OR circuit **47**. The AND circuits operate alternatively under control of the flip-flop circuit **50**. In the present example, the AND circuit **52** passes the output of FBSR **20** to modulator **21**. While the FBSR is generating a word, the counter **18**, which is continuously actuated by clock **17**, sends a pulse to the A/DC **19** commanding it to sample the original information-bearing signal. Conversion of the analog value of the original signal to a digital response ordinarily takes about 20–40 microseconds, and after conversion is complete, i.e., after the flip-flops of the A/DC have reached a setting which produces a digital output approximating the amplitude value of the original signal at the time of sampling, a pulse from the counter **18** is applied to a flip-flop circuit **51**. This flip-flop, as a result, produces a pulse which causes the inactive FBSR, in this case register **20′**, to accept an initial setting from the A/DC **19**. When the fifteenth pulse is transmitted from clock **17** through AND circuit **48** to FBSR **20**, assuming that the code words employed are each fifteen bits long, the counter **18** sends a pulse to flip-flop **50**, which in turn causes the AND circuit **49** to start transmitting clock pulses to FBSR **20′** and the AND circuit **48** to cease transmitting clock pulses to the FBSR **20**. At the same time, the flip-flop **50** causes the AND circuit **52** to discontinue passing the output from the FBSR **20** to the modulator **21** of the transmitter, and causes the AND circuit **53** to begin passing the output from the FBSR **20′** to the modulator. Operation of the encoder **15** as just described is continuous. The two FBSR's operate in "leap frog" fashion to produce a continuous stream of encoded information without gaps or breaks of any kind. It will now be appreciated that the combinations of flip-flop states appearing on the left in FIG. 8 illustrate the states of flip-flops **41–44** of FBSR **20**, and the combinations appearing on the right illustrate the states of flip-flops **41′–44′** of FBSR **20′**.

In a practical system, according to this invention, for transmitting, say, a five kilocycle band of speech, the A/DC should convert each analog sample to a digital output at a 20 kilocycle per second rate, which is greater than twice the Nyquist rate to insure high fidelity. Furthermore, it is thought that a practical system requires an A/DC and a shift register each having a minimum of seven stages, whereby each code word will comprise 127 bits and the original information-bearing signal can be quantized into 127 levels. In such a system, the cycling rate required to produce a continuous stream of bits from the encoder is 127×20,000 cycles, or 2.54 megacycles per second. Thus, the clock **17** would generate pulses at the rate of 2.54 megacycles per second.

FIG. 11 illustrates a seven stage shift register of the type which may be used in the arrangement of FIG. 10, two such shift registers being shown in FIG. 10. Each of the flip-flops **54–60** receives signals from its respective flip-flop of the A/DC, via a pair of conductors **63** and **64**, for the purpose of initially setting the state of the flip-flops **54–60**. Another conductor **65** carries the pulses from the flip-flop **51** (FIG. 10) to each of the flip-flops **54–60** commanding the latter to accept the settings from the A/DC via the conductors **63** and **64**. Thereafter, pulses from clock **17** are applied to each of the flip-flops **54–60** via conductor **66**. In response to each clock pulse, the state of each flip-flop is shifted one stage to the right by means of conductors **67** and **68** between each two adjacent flip-flops. The outputs of flip-flops **57** and **60** are added in a half-adder **45**, and the sum is fed-back to the first stage flip-flop **54** via conductors **69** and **70**. This is a standard technique referred to as "half-adding" or "exclusive OR combining." The output of the last stage or flip-flop **60** represents the code word output of the shift register. The particular stage used to generate the code word is immaterial, and it will be noted that in FIGS. 6 and 7 the output of the first stage was treated as the code word.

The decoder **16** is shown in more detail in FIG. 12. The signal from the transmitter is applied to the demodulator **22** of the receiver. The receiver sequence of bits, or binary code word, is applied to each of **127** correlators **25**. Also applied to each correlator is a reference word, as described above. These reference words could be supplied by **127** individual seven stage feed-back shift

registers. However, the same result can be achieved in a simpler fashion. A seven stage FBSR **74** identical to the FBSR of FIG. 11 is provided, and receives pulses from the clock **23**. The output of each stage of this FBSR is used as a reference word. Thus, the FBSR **74** produces seven reference words, making it necessary to provide additional means for producing the remaining **120** reference words. The additional means may be a delay register **75** consisting of 120 stages or flip-flops identical to those in the shift register **74**, but containing no feed-back loops. The output of each stage of the register **75** is the same as the sequence generated by the FBSR **74**, but delayed by a time dependent upon the number of stages between it and the FBSR. Thus, the 127 reference words are produced by using only 127 individual flip-flops.

The correlators and comparator will be described in more detail with reference to FIGS. 12 and 13. Each of the 127 correlators is designed to produce a positive pulse each time a bit of the transmitted code word matches a bit of the reference word applied to the correlator, and no output when the transmitted bit and reference bit do not match. This is achieved by introducing the reference word and the transmitted word into a pair of parallel connected AND and NAND circuits. Thus, the reference word is introduced, via conductor **76** into AND circuit **77** and NAND circuit **78**, and the transmitted code word is introduced into circuits **77** and **78** via conductor **79**. The AND circuit **77** produces a positive pulse each time a "1" of the reference word matches a "1" of the transmitted word, but no output when any other combination of bits is applied to it. The NAND circuit **78** produces a positive pulse each time a "0" of the reference word matches a "0" of the transmitted word, but no output when any other combination of bits is applied to it. The outputs of both circuits **77** and **78** are applied to a single OR circuit **80**. Thus, it will be seen that the OR circuit receives a positive pulse each time two "0" bits or two "1" bits are simultaneously applied to the circuits **77** and **78**. The output of the OR circuit **80** is applied to a capacitor **84** through an amplifier **83**. In the correlator receiving the reference word identical to the transmitted word, each pair of bits applied to the circuits **77** and **78** will produce a positive pulse, since they will always match. These pulses, after inversion by amplifier **83** will serve to charge the capacitor **84** highly negative. In all the other correlators, the capacitor will contain approximately zero charge, for a reason to be discussed below with reference to FIG. 14.

The negative charge on capacitor **84** is applied to a Schmitt trigger **85**, which also has a threshold voltage applied to it. The Schmitt triggers serve as comparators **26**. When the negative charge becomes large enough to counteract the threshold voltage, the Schmitt trigger switches. It should be noted that for each transmitted code word, the Schmitt trigger is connected to only one correlator, i.e., the correlator corresponding to the transmitted word, will switch. The Schmitt triggers connected to all the other correlators will remain unaffected. This is because the threshold voltage applied to each Schmitt trigger is adjusted so that the capacitors in the correlators not corresponding to the transmitted word never receive enough charge to counteract the threshold voltage. On the other hand, the threshold voltage need not necessarily be so high that the capacitor must receive 127 pulses before it is charged sufficiently to overcome the threshold voltage. In general, the more intense the noise in the system, the higher the threshold voltage will have to be in order to avoid an inordinate number of false alarms.

When the 127th bit of the transmitted word and each of the reference words have been applied to the correlators, the FBSR **74** sends a pulse, through an AND circuit **86** and conductor **87**, to a series of gates **88**, one of which follows each Schmitt trigger **85**. The gate following the Schmitt trigger which has switched will thereupon produce an output pulse, but the other gates will have no output. The amplitude of the output pulse produced by each gate, when its corresponding Schmitt trigger has switched, is always the same, and equal to the output pulse produced by every other gate. The output of the gate corresponding to the Schmitt trigger which has switched is applied to a decoding matrix (within the box identified by reference numeral **27** in FIG. 12), and the latter sets the flip-flops of the D/AC, the particular setting depending upon which gate transmits the pulse to the matrix. As a result of this setting, the D/AC produces a signal whose amplitude approximately equals the amplitude of the original signal at the time of the sample which led to generation of the code word which caused the particular output pulse. The output of the D/AC is smoothed by a low-pass filter **89**.

FIG. 14 is intended to illustrate the autocorrelation function of the pseudo-random binary words employed in the present invention. As mentioned above, if a particular transmitted code word is correlated with an identical reference word, a positive pulse from OR circuit **80** (FIG. 13) will result as each of the 127 bits in the code word is matched with its corresponding bit in the reference word. Consequently, in the absence of inversion by amplifier **83**, a positive charge equal to 127 positive pulse units would build up on an integrator **84**, which may be a capacitor. This charge is indicated on the vertical axis of FIG. 14. The point of intersection between the two axes indicates not only zero charge, but zero time delay between the code word and its corresponding reference word. The horizontal axis represents time delay, in bits, between the code word and the same reference word just mentioned. Obviously, however, any such time delay is equivalent to a change in the reference word. Thus 126 time delays at one bit intervals actually represent the other 126 reference words. It will be seen that correlation of the code word with each of the reference words which do not match it produces, after comparison of all 127 bits of the code word, a negative charge of one unit. Thus, there is no chance of any Schmitt trigger **85** switching except the one corresponding to the reference word which matches the transmitted word.

From the above it will be apparent that the successful operation of the present invention depends upon the clock **17** in the encoder running at exactly the same rate as the clock **23** in the decoder. Any difference in clock rates will, of course, cause a time delay between generation of the transmitted code word and generation of the reference word to which it should correspond with the result that the transmitted word and reference word will not match as they should. Even if the two clocks are operating at the same rate, the same disadvantageous result will occur if there is relative motion between the transmitter and receiver, since the transmitted signal will appear to the receiver to have slipped some number of bits.

Synchronization of the word generator in the encoder and the word generators in the decoder can be accomplished by sending an independent synchronization signal to the receiver at the time transmission of a new code word commences. However, the present invention offers the advantage of achieving initial synchronization; and thereafter maintaining synchronization without resort to a separate synchronization signal. Initial synchronization between the word generators of the encoder and decoder can be achieved by repeatedly sending a known code word corresponding to a certain quantization level. In the absence of synchronization, the output of the decoder will be at some other quantization level. The decoder is adjusted by prohibiting one pulse at a time produced by clock **23** from reaching the word generators **24***a–n*. This can be accomplished by means of a gate or a phase shifter between the clock and word generators. This procedure is continued until the output of the decoder is at the same quantization level as the quantization level corresponding to the transmitted word.

FIG. 15 illustrates means for maintaining the synchronization of the encoder and decoder word generators despite variations which may occur between the rates of clocks **17** and **23** and despite relative movement between the receiver and transmitter. The word generators or shift registers **24***a–n* and correlators **25***a–n* are comparable to those illustrated in FIG. 1. The transmitted code word is applied to each correlator via conductor **90**. The output of each correlator is applied to both a "greatest-of" circuit **91**, via conductors **92**, and to a gate, via conductors **93**. The gates are indicated by reference numerals **94***a–n*, and there is one gate associated with each correlator. An output from the greatest-of circuit **91** is also applied to each of the gates **94***a–n*. Outputs from all the gates are applied to an amplitude comparator **95**, of any well known kind, and the output of the amplitude comparator is in turn applied to a phase shifter **96**, through which pulses from clock **23** are applied to the shift registers **24***a–n*.

As described above, when a transmitted code word is decoded, only one of the correlators **25***a–n* will produce an output of any significance. This assumes, however, that the encoder and decoder word generators are synchronized. The greatest-of circuit **91** responds to asignal from the correlator corresponding to the transmitted word by turning on the two gates associated with the correlators on either side of the correlator applying the signal to the greatest-of circuit. Thus, if the correlator **25***b* corresponds to the transmitted word, the greatest-of circuit will turn on gates **94***a* and **94***c*. Consequently, the ouputs of correlaors **25***a* and **25***c* will be applied, through these gates, to the amplitude comparator **95**. If synchronization exists, the outputs of correlators **25***a* and **25***c* will be equal and negligible, and therefore there will be no output from comparator **95**. However, if the word generators in the encoder and decoder are not perfectly synchronized, the output of correlator **25***b* will be reduced, since the AND circuit **77** (FIG. 13) will conduct for only a fraction of the time it would conduct if synchronization were present. Hence, the output of the OR circuit **80** will similarly be reduced, and the positive charge which builds up on integrator **84** will no longer be equal to 127 positive pulse units, but rather to some lesser value. For the same reason, in the absence of synchronization, the output of one of the correlators adjacent to the correlator **25***b*, say correlator **25***a*, will be correspondingly increased, because the charge which builds up on the integrator corresponding to the correlator **25***a* will increase and no longer be equal to the charge on the integrator corresponding to the correlator **25***c*. The comparator **95** will sense the difference between the outputs of correlators **25***a* and **25***c*, and will activate the phase shifter **96** to alter the transmission of pulses from clock **23** to the word generators **24***a–n* in order to resynchronize those word generators with the word generator of the encoder. The amplitude comparator **95** continues to adjust the phase shifter until it no longer senses any difference in the outputs of the correlators **25***a* and **25***c*. The "sense" or direction of the error in synchronization is revealed by noting which of the outputs of the correlatros **25***a* and **25***c* exceeds the other. Thus, if the output of correlator **25***a*, which corresponds to a lower quantization level than correlator **25***c*, is greater than the output of correlator **25***c*, the phase shifter is adjusted to speed up the application of pulses from clock **23** to the word generators.

It should be noted in passing that FIG. 15 illustrates an alternative to the comparators **84**, Schmitt triggers **85**, and gates **88** of FIG. 13. The outputs of the greatest-of circuit **91** can be applied to a decoding matrix **97**; instead of the outputs of gates **88**. The matrix **97** in turn feeds a register comprising seven flip-flops, the setting of which depends upon the value of the output of the matrix. The output of the matrix depends upon the correlator providing the pulse to the greatest-of circuit. For each different matrix output, a unique seven bit binary word will be produced by the register. The register is connected to a binary-weighted resistive adder having 127 possible output amplitude levels. Consequently, a signal approximating the amplitude level of the original signal sample can be produced.

The greatest-of circuit **91** is shown in detail in FIG. 16. A series of transistors **100***a–n*, equal in number to the number of correlators **25***a–n* (FIG. 15) are arranged with their emitters connected to a single junction by conductor **101**, and with their collectors connected to another junction by conductor **102**. The output of each correlator is applied to the base **103** of its respective transistor. In such an arrangement, when the base of one transistor receives a signal larger than that applied to any other transistor, the collector voltage of that transistor will drop whereas the collector circuits of the other transistors remain at a relatively high potential. Since all the transistors are connected by conductor **101** to a common emitter load resistor **104**, the voltage drop across this resistor will equal that of the largest input signal to all the transistors. Consequently, all the transistors will assume a non-conducting condition except the one receiving the largest input signal, and therefore the latter transistor will conduct.

FIG. 17 illustrates an alternative arrangement for synchronizing the encoder and decoder. In this arrangement, two banks of shift registers and correlators, A and B are provided instead of one. In other words, twice as many shift registers and correlators are present as there are quantization levels. All the shift registers are actuated by a clock **23′** through a phase shifter **96′**. However, a delay circuit **107** is located between the phase shifter **96′** and the bank of shift registers **24***a′–n′*. The circuit **107** has the effect of delaying the application of the clock pulses by some predetermined interval. The delay might be one-half bit delay, i.e., a time delay equal to one half the time required to generate a bit. The transmitted code word is applied to each of the correlators **25***a–n* and **25***a′–n′* via conductor **108**. The outputs of correlators **25***a–n* are applied to a greatest-of circuit **104**, and the outputs of correlators **25***a′–n′* are applied to another greatest-of circuit **105**. The output of the greatest-of circuits are applied to an amplitude comparator **106**, which in turn controls the phase shifter **96′**.

Assuming that the encoder word generator and the word generators **24***a–n* are synchronized, one of the correlators **24***a–n*, say correlator **24***b*, corresponding to the transmitted code word will produce a maximum output signal, i.e., a signal equal to 127 units. On the other hand, since there is a one-half bit time delay between the encoder word generator and the word generators **24***a′–n′*, the correlators **25***a′* and **25***b′* will each produce an input signal equal to one-half the maximum output signal of correlator **24***b*. These outputs are transmitted to the amplitude comparator **106** by greatest-of circuits **104** and **105**, and under these conditions, the comparator **106** will produce no output. Assume now that the output of correlator **25***b′* becomes larger than the output of correlator **25***a′*, e.g., the output of correlator **25***b′* rises to 75% of the maximum output and the output of correlator **25***a′* falls to 25% of the maximum output. In response to this circumstance, the amplitude comparator **106** will adjust the phase shifter **96′** in order to delay the transmission of the clock pulses to the shift registers. Adjustment of the phase shifter **96′** continues until the synchronized condition described above returns.

In order to initially achieve synchronization between a transmitter and receiver having a very high velocity in relation to each other, means are provided for rapidly varying the rate of the clock, which may be an oscillator, until some output is produced by the correlators. Fine synchronization can then be achieved by the means described above.

The invention has been shown and described in preferred form only and by way of example, and many changes may be made in the embodiment disclosed without necessarily

departing from the spirit and scope of the invention. It is understood, therefore, that the invention is not limited to any specific form or embodiment except insofar as such limitations appear in the appended claims.

What is claimed is:

1. A transmission system for a signal having amplitude variations with respect to time, comprising

(a) means for sampling the signal at predetermined intervals and producing one of a predetermined number of discrete signals corresponding to quantized levels of the amplitute of the original signal,

(b) means responsive to the signal produced by said sampling means at each sampling interval for generating one of a predetermined number of different code words,

(c) the number of said different code words and the number of said discrete signals being equal, and each code word corresponding to one of said discrete signals so that a particular discrete signal always causes the same code word to be generated,

(d) means for transmitting said code words,

(e) means for receiving said code words,

(f) means for continuously and repeatedly producing all the code words capable of being produced by means (b),

(g) means for comparing each transmitted code word received by means (e) with the words produced by means (f), and

(h) means responsive to said comparing means (g) when the latter senses agreement between a transmitted word and one of the words produced by means (f) for producing a signal having an amplitude corresponding to the quantized amplitude level of the original signal sample with which the word corresponds,

whereby a composite singal resembling the original sampled signal is produced.

2. A transmission system as defined in claim 1 wherein said means (f) is a shift register.

3. A transmission system as defined in claim 1 wherein said means (h) is a digital-to-analog converter.

4. A transmission system for an electromagnetic signal comprising:

(a) an analog-to-digital converter capable of producing a predetermined number of preliminary binary words,

(b) means for commanding said converter to sample said signal at selected time intervals and to produce a preliminary word corresponding to the quantized level of the amplitude of said signal,

(c) a word generator,

(d) means for introducing said preliminary word into said word generator,

(e) means for activating said word generator to produce a distinct binary code word corresponding to the preliminary word introduced into it,

(f) means for transmitting said code word,

(g) receiver means including a number of word generators equal to said predetermined number of preliminary words, each of said receiver word generators continuously and repeatedly generating a reference word identical to one of said code words;

(h) means for comparing the transmitted code word with said reference words, and producing a signal corresponding to the reference word which agrees with said code word, and

(i) a digital-to-analog converter responsive to the signal from said comparator for producing a signal having an amplitude corresponding to the quantized amplitude level of the original signal sample with which said code word corresponds.

5. A transmission system as defined in claim 4 including means for operating said command means (b) and said activating means (e) in timed relationship.

6. A transmission system as defined in claim 4 including means for operating said command means (b) once during the generation of each code word.

7. A transmission system as defined in claim 4 including two word generators, said means (d) being arranged to introduce preliminary words alternately into said word generators, and said means (e) being arranged to activate and deactivate said word generators alternately.

8. A transmission system according to claim 7 wherein said means (b) is arranged to command said converter to sample said signal once during the generation of each code word, and said means (d) is arranged to introduce the preliminary word produced by said converter into the inactive one of said word generators.

9. A transmission system as defined in claim 8 including a single counter forming part of said command means (b), introducing means (d), and activating means (e) for controlling the timing of the signal sampling, the word introduction into said generator, and the word generation.

10. A transmission system as defined in claim 9 including a clock for controlling the speed of operation of said counter, and a clock in said receiver for controlling the speed of operation of said word generators, said clocks operating at the same rate.

11. A transmission system as defined in claim 4 including a clock for controlling the speed of operation of said word generator (c), another clock in said receiving means for controlling the speed of operation of said word generators, said clocks operating at the same rate, and means for altering the transmission of pulses produced by said receiver clock to said word generators for the purpose of synchronizing said word generator (c) and said receiver word generator.

12. A transmission system as defined in claim 11 wherein said altering means is a phase shifter, and including means controlled by the output of said comparing means (h) for adjusting the phase shifter in order to vary the timing of the application of said clock pulses to said word generators.

13. A transmission system as defined in claim 11 wherein said altering means includes a phase shifter, at least one additional word generator continuously and repeatedly generating a word identical to one of the reference words produced by one of said first-mentioned word generators, the word produced by said additional word generator being out-of-phase with the word produced by its corresponding one of said first-mentioned word generators, and means for comparing the output of said additional word generator with the output of its corresponding one of said first-mentioned word generators and controlling said phase shifter accordingly in order to vary the timing of the application of said clock pulses to said word generators.

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ROBERT L. GRIFFIN, *Primary Examiner.*

W. S. FROMMER, *Assistant Examiner.*

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