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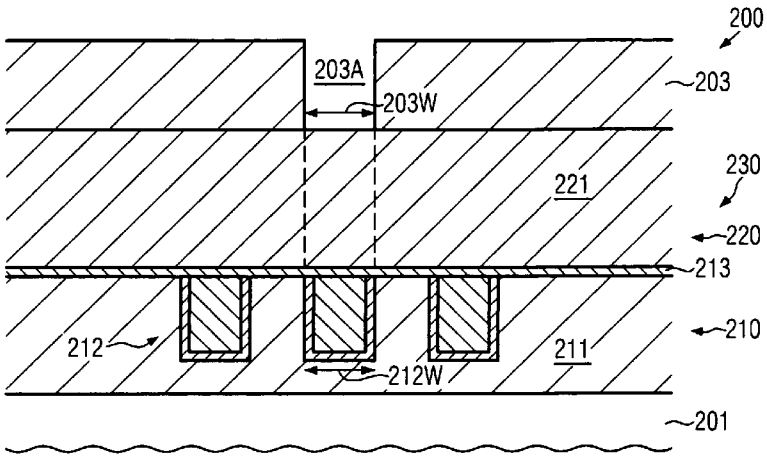

FIG. 2a

(57) Abstract: In a metallization system of a semiconductor device a transition via may be provided with an increased degree of tapering by modifying a corresponding etch sequence. For example, the resist mask for forming the via opening may once, or several times be eroded in order to increase the lateral size of the corresponding mask opening. Due to the pronounced degree of tapering, enhanced deposition conditions may be accomplished during the subsequent electrochemical deposition process for commonly filling the via opening and a wide trench connected thereto.

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A METALLIZATION SYSTEM OF A SEMICONDUCTOR DEVICE COMPRISING EXTRA-TAPERED TRANSITION VIAS

FIELD OF THE PRESENT DISCLOSURE

Generally, the present disclosure relates to microstructures, such as advanced integrated circuits, and more particularly to conductive structures, such as copper based metallization layers, comprising wide metal lines connected to closely spaced narrow metal lines by transition vias.

DESCRIPTION OF THE PRIOR ART

In the fabrication of modern microstructures, such as integrated circuits, there is a continuous drive to steadily reduce the feature sizes of microstructure elements, thereby enhancing the functionality of these structures. For instance, in modern integrated circuits, minimum feature sizes, such as the channel length of field effect transistors, have reached the deep sub-micron range, thereby increasing performance of these circuits in terms of speed and/or power consumption and/or diversity of functions. As the size of individual circuit elements is reduced with every new circuit generation, thereby improving, for example, the switching speed of the transistor elements, the available floor space for interconnect lines electrically connecting the individual circuit elements is also decreased. Consequently, the dimensions of these interconnect lines are also reduced to compensate for a reduced amount of available floor space and for an increased number of circuit elements provided per unit die area as typically the number of interconnections required increases more rapidly than the number of circuit elements. Thus, usually a plurality of stacked "wiring" layers, also referred to as metallization layers, is provided, wherein individual metal lines of one metallization layer are connected to individual metal lines of an overlying or underlying metallization layer by so-called vias. Despite of the provision of a plurality of metallization layers reduced dimensions of the interconnect lines are necessary to comply with the enormous complexity of, for instance modern CPUs, memory chips, ASICs (application specific ICs) and the like.

Advanced integrated circuits, including transistor elements having a critical dimension of 0.05μm and even less, may, therefore, typically be operated at significantly increased current densities of up to several kA per cm^2 in the individual interconnect structures despite the provision of a relatively large number of metallization layers owing to the significant number of circuit elements per unit area. Consequently, well-established materials, such as aluminum are being replaced by copper and copper alloys, a material with significantly lower electrical resistivity and improved resistance to electromigration even at considerably higher current densities compared to aluminum. The introduction of copper into the fabrication of microstructures and integrated circuits comes along with a plurality of severe problems residing in copper's characteristic to readily diffuse in silicon dioxide and a plurality of low-k dielectric materials, which are typically used in combination with copper in order to reduce the parasitic capacitance within complex metallization layers. In order to provide the necessary adhesion and to avoid the undesired diffusion of copper atoms into sensitive device regions, it is, therefore, usually necessary to provide a barrier layer between the copper and the dielectric material in which the copper based interconnect structures are embedded. Although silicon nitride is a dielectric material that effectively prevents the diffusion of copper atoms, selecting silicon nitride as an interlayer dielectric material is less then desirable, since silicon nitride exhibits a moderately high permittivity, thereby increasing the parasitic capacitance of neighbouring copper lines, which may result in non-tolerable signal propagation delays. Hence, a thin conductive barrier layer that also imparts the required mechanical stability to the copper is usually formed so as to separate the bulk copper from the surrounding dielectric material, thereby reducing copper diffusion into the dielectric materials and also reducing the diffusion of unwanted species, such as oxygen, fluorine, and the like, into the copper. Furthermore, the conductive barrier layers may also provide highly stable interfaces with the copper, thereby reducing the probability for significant material transport at the interface, which is typically a critical region in view of increased diffusion paths that may facilitate current induced material diffusion. Currently, tantalum, titanium, tungsten and their compounds with nitrogen and silicon and the like, are preferred candidates for a conductive barrier layer, wherein the barrier layer may comprise two or more sub-layers of different composition so as to meet the requirements in terms of diffusion suppressing and adhesion properties.

Another characteristic of copper significantly distinguishing it from aluminum is the fact that copper may not readily be deposited in larger amounts by chemical and physical vapor deposition techniques, thereby requiring a process strategy that is commonly referred to as the damascene or inlaid technique. In the damascene process, first a dielectric layer is formed which is then patterned to include trenches and/or vias which are subsequently filled with copper, wherein, as previously noted, prior to filling in the copper, a conductive barrier layer is formed on sidewalls of the trenches and vias. The deposition of the bulk copper material into the trenches and vias is usually accomplished by wet chemical deposition processes, such as electroplating and electroless plating, thereby requiring the reliable filling of vias with an aspect ratio of 5 and more with a diameter of 0.3 μm or even less in combination with trenches having a width ranging from 0.1μm to several μm. Electrochemical deposition processes for copper are well established in the field of electronic circuit board fabrication. However, for the dimensions of the metal regions in semiconductor devices the void free filling of high aspect ratio vias is an extremely complex and challenging task, wherein the characteristics of the finally obtained copper based interconnect structure significantly depend on process parameters, materials and geometry of the structure of interest. Since the basic geometry of interconnect structures is substantially determined by the design requirements and may, therefore, not be significantly altered for a given microstructure, it is of great importance to estimate and control the impact of materials, such as conductive and nonconductive barrier layers, of the copper microstructure and their mutual interaction on the characteristics of the interconnect structure so as to insure both high yield and the required product reliability.

In addition to achieve high production yield and superior reliability of the metallization system, it is also important achieve production yield and reliability on the basis of a high overall throughput of the manufacturing process under consideration. For instance, the so-called dual damascene process is frequently used, in which a via opening and a corresponding trench are filled in a common deposition sequence, thereby providing for superior process efficiency. Due to a complex layout of sophisticated metallization systems, the metal lines of two adjacent metallization layers may have a very different lateral size, since metal lines of one layer may have to be adapted to a moderately high packing density of corresponding interconnect structures, while the trenches in the adjacent

metallization layer may have to provide a high current drive capability. In this case, the vertical interconnection between a metal line with an increased width to a metal line having a significantly smaller width may have to be established on the basis of a via that corresponds to the trench having the significantly reduced width. A manufacturing regime according to the dual damascene strategy may, however, result in significant irregularities during the deposition of the copper material due to the significant different in lateral width of the corresponding trench and the via, as will be explained in more detail with reference to figures 1A and 1B.

Figure 1A schematically illustrates a cross-sectional view of a semiconductor device 100 at a manufacturing stage, in which a complex metallization system 130 is to be formed above a substrate 101. It should be appreciated that the substrate 101 may comprise a plurality of circuit elements, such as transistors, and the like, which may be formed on the basis of design dimensions of approximately 50 nm and less, if sophisticated applications are considered. For convenience, any such circuit elements are not shown in figure 1A. The metallization system 130 comprises a metallization layer 110, which may represent any of a plurality of metallization layers, wherein the number of corresponding metallization layers may depend on the complexity of the circuit layout of the device 100. For instance, the metallization layer 110 comprises a dielectric material 111, which may include a low-k dielectric material in order to reduce the parasitic capacitance between adjacent metal lines 112, which, at least in the portion shown in figure 1A, may represent closely spaced metal lines as may be required by the overall circuit layout. For instance, the metal lines 112 may have a width 112W of approximately 100 nm and less and similarly the distance between adjacent two of the metal lines 112 may be of a similar order of magnitude. As previously discussed, the metal lines may be formed on the basis of a copper material in combination with a conductive barrier material 112B in order to provide for the required copper confinement and the electromigration behaviour, as discussed above. Furthermore, an electric cap or etch stop layer 113 is typically provided on the dielectric material 111 and the metal lines 112, wherein the cap layer 113 may, depending on the overall process strategy, also provide for copper confinement and superior interface characteristics with the metal lines 112. Furthermore, a metallization layer 120 is formed above the layer 110 and comprises a trench 121T and a via opening 121V

formed in a corresponding dielectric material 121. For example, the dielectric material 121 may represent a low-k dielectric material or any other dielectric material, depending on requirements with respect to parasitic capacitance, and the like. The trench 121T may have a significantly greater width 121W in order to provide for a sufficient current drive capability, which may be required in the metallization layer 120. On the other hand, the wire opening 121V may connect to one of the metal lines 112 so that a corresponding width 121U substantially corresponds to the width 112W of the metal lines 112 in the metallization layer 110. The semiconductor device 100 as illustrated in figure 1A may be formed on the basis of well established manufacturing techniques. For example, after providing any circuit elements in the device level of the device 100 (not shown) an appropriate contact structure may be provided so as to connect to the circuit elements and provide a platform for forming thereon the metallization system 130. Thereafter, one or more metallization layers may be formed on the basis of process techniques, as will be described with reference to the metallization layer 120. Thus, after forming the metallization layer 110 and depositing the cap layer 110 on the basis of well established deposition techniques, such as CVD (chemical vapor deposition) and the like, in order to provide one or more materials, such as silicon carbide, nitrogen containing silicon carbide, and the like, the dielectric material is deposited. For this purpose, any appropriate deposition technique may be used, depending on the composition of the material 121. Thereafter, various process strategies are typically used in order to form the via opening 121U and the trench 121T according to the design dimensions. For example, in a so-called "via first-trench last" approach, the via opening 121V may be formed by providing etch mask, such as a resist mask, and etching the dielectric material 121 down to a specified depth or down to the etch stop layer 113. Next, a corresponding etch mask for the trench may be formed on the basis of sophisticated lithography techniques, wherein if required, a corresponding planarization material may be deposited first in order to at least partially fill the via opening 121V, when extending down to the etch stop layer 113. Thereafter, a further etch process is performed so as to obtain the trench 121T and the etch mask be removed, while also the etch stop layer 113 is opened so that the via opening 121V may extend into the metal line 112. Thereafter, any required manufacturing processes may be performed for preparing the device 100 by the deposition of a conductive barrier material. For example, a

barrier material 122B is deposited, for instance in the form of a tantalum/ tantalum nitride layer stack on the basis of strata deposition, and the like. Moreover, a seed material (not shown) may be deposited in order to enhance a subsequent electrochemical deposition process for filling in the copper material into the trench 121T and the via 121V. It should be appreciated that due to the sophisticated device geometries caused by the wide trench 121T and the narrow via 121V, corresponding deposition parameters may have to be appropriately selected in order to reliably cover the exposed portions within the trench 121T and the via 121V with the barrier material 122B.

Figure 1B schematically illustrates the semiconductor device 100 when subjected to an electrochemical deposition process for depositing copper material. As previously explained, in view of superior process efficiency, the trench 121T and the via 121V may be formed in an interrelated patterning process and the filling thereof may be accomplished on the basis of the common deposition process 102. However, the sophisticated device topography caused by the per se very complex electrochemical deposition of the copper material may result in deposition irregularities, such as voids 122C, thereby contributing to significantly yield losses and reduced reliability of the resulting metallization system 130. That is, the electrochemical deposition of the copper material 122A may be based on highly complex electrolyte solutions including sophisticated additives in order to obtain, in combination with an appropriate pulse reverse regime in electroplating techniques, a bottom to top fill behaviour. However, due to the significant difference in lateral dimensions of the trench 121T and the via 121V, a premature "closure" of the via opening 121B may result in a corresponding irregularity 122C.

In some conventional strategies, the probability of creating the deposition related irregularities 122C may be reduced by redesigning the layout of the metallization layer 110 so that increased areas are provided at certain portions of the metal lines 112 so as to provide for an increased lateral size of the "landing area" of the via 121V. However, a corresponding redesign may generally reduce overall packing density in the metallization system 130.

In view of the situation described above, the present disclosure relates to techniques and semiconductor devices, in which metal lines provided in adjacent metallization layers of very different widths may be connected, while avoiding or at least reducing the effects of one or more of the problem identified above.

SUMMARY OF THE DISCLOSURE

Generally, present disclosure provides techniques and semiconductor devices, in which the surface topography of a wide trench and a via opening connecting to a metal line of reduced lateral size may be "relaxed" by introducing a pronounced degree of tapering such that a desired reduced lateral width of the via opening may be obtained in the vicinity of the metal line of reduced lateral dimension, while the width of the opening may readily increase. Consequently, any constraints imposed on a common deposition process for filling the via opening having the pronounced tapering and the wide trench may significantly be reduced, without requiring dedicated design strategies, which may conventionally result in a reduced packing density. In some illustrative aspects disclosed herein, the pronounced tapering of the via may be accomplished by modifying the etch sequence for forming the via opening in the dielectric material by increasing a corresponding mask opening in a resist mask at least once during the patterning sequence. For instance, the resist material may be "eroded" after performing a first etch step and thereafter a further etch step may be performed on the basis of an increased lateral width of the mask opening. If required, further etch steps may be performed with preceding mask erosion processes in order to obtain a substantially gradual tapering of the resulting via opening. In other illustrative aspects disclosed herein, the etch process for forming the via opening may be performed on the basis of an appropriately designed initial etch mask for forming a first portion of the via opening, while a remaining depth of the via opening may be obtained on the basis of a spacer element, which may also result in a pronounced tapering of the finally obtained via opening.

One illustrative method disclosed herein comprises forming an etch mask above a dielectric material of a first metallization layer of a semiconductor device, wherein

the etch mask comprises a mask opening having a first lateral size that corresponds to a target lateral size at a bottom of a via to be formed in the dielectric material. The method further comprises forming a via opening on the basis of the mask opening having the first lateral size in order to form the via opening so as to extend to the first depth in the dielectric material. Thereafter, the mask opening is increased to obtain a second lateral size thereof and a via opening is increased on the basis of the mask opening having the second lateral size so as to extend to a second depth. The method further comprises forming a trench above the via opening in the dielectric material so as to connect to the via opening. Finally, the method comprises commonly filling the via opening and the trench with a metal containing material, wherein the via opening extends to a metal region of a second metallization layer located below the first metallization layer.

A further illustrative method disclosed herein comprises forming a via opening in a dielectric material of a first metallization layer of a semiconductor device, wherein the via opening extends to a first depth and has a first lateral size. Additionally, a spacer element is formed on sidewalls of the via opening and a depth of the via opening is increased so as to extend to a metal region of a second metallization layer that is formed below the first metallization layer.

One illustrative semiconductor device disclosed herein comprises a first metallization layer formed above a substrate, wherein the first metallization layer comprises a metal line having a first width. The semiconductor device further comprises a second metallization layer formed below the first metallization layer and comprising a second metal line having a second width that is less than the first width. Additionally, the semiconductor device comprises a via extending from the first metal line to the second metal line, wherein the via has a first lateral dimension at the first metal line and has a second lateral dimension at the second metal line, wherein the second lateral dimension is approximately 60% or less of the first lateral dimension.

BRIEF DESCRIPTION OF THE DRAWINGS

Further embodiments of the subject matter disclosed herein are defined in the appended claims and will become more apparent with the following detailed description when taken with reference to the accompanying drawings, in which:

Figures 1A and 1B schematically illustrate cross-sectional views of a sophisticated semiconductor device during various manufacturing stages in forming a metallization system on the basis of conventional process strategies.

Figures 2A to 2F schematically illustrates cross-sectional views of a semiconductor device during various manufacturing stages in forming a metallization system, in which a via having a pronounced tapering connects a narrow metal line to a wide metal line according to illustrative embodiments; and

Figures 2G to 2I schematically illustrates cross-sectional views of the semiconductor device during various manufacturing stages, in which a pronounced tapering of a via opening may be accomplished by providing an additional spacer element in the patterning sequence according to still further illustrative embodiments.

DETAILED DESCRIPTION

While the subject matter disclosed herein is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the present disclosure to the particular illustrative embodiments disclosed, but rather the described illustrative

embodiments merely exemplify the various aspects of the present disclosure, the scope of which is defined by the appended claims.

Generally, the present disclosure relates to manufacturing techniques and corresponding semiconductor devices, in which interconnections between narrow metal lines and wide metal lines of adjacent metallization layers may be accomplished on the basis of vias having a pronounced tapering so that a bottom width thereof may be adapted to a design width of the narrow metal line, while the top of the via may have a significantly increased lateral dimension in order to provide for an enhanced device geometry during a common deposition process for filling the via opening and the corresponding trench of the metal line with a reduced probability of creating deposition related irregularities. Consequently, corresponding vias of a pronounced tapering, which may also be referred to a transition vias, may be provided without requiring specifically provided increased "landing" areas connected to the narrow metal lines, thereby providing for enhanced packing density and superior design flexibility in providing complex metallization systems. In some illustrative embodiments, the pronounced tapering of the transition vias may be accomplished by performing the etch sequence for patterning the via opening on the basis of a resist mask, which may intermittently be modified, for instance, by performing one or more material removal processes, so that an initial lateral size of a mask opening may be increased during the further advance of the overall etch sequence. In other illustrative embodiments, the etch sequence for forming the via opening in the dielectric material may be started with a desired lateral size at the top of the via opening and a desired reduced target dimension for the via bottom may be obtained on the basis of a spacer element, which may be formed at an intermediate phase of the overall patterning sequence. Consequently, during the further patterning process, the spacer element may also be removed, so that a corresponding configuration of the spacers may be transferred into the dielectric material, which may thus result in a corresponding tapered configuration. Consequently, a superior device geometry may be provided prior to the common deposition process by not unduly contributing to the overall process complexity, while also avoiding specifically designed contact areas of increased lateral dimensions for the narrow metal lines. Hence, metal lines having a width of several hundred nanometers and even more may reliably be connected

to metal lines of a lower lying metallization layer having a width of approximately 100 nm and significantly less in sophisticated applications on the basis of a electrochemical deposition process. It should be appreciated, however, that although the present disclosure is particularly advantageous in the context of sophisticated metallization systems with metal lines having dimensions in the above specified range, the principles disclosed herein may nevertheless be applied to any other less critical metallization systems. Consequently, the present disclosure should not be considered as being restricted to any specific device dimensions, unless such restrictions are explicitly set forth in a specification or the appended claims.

With reference to figures 2A to 2I, further illustrative embodiments will now be described in more detail, wherein also reference may be made to figures 1A and 1B if appropriate.

Figure 2A schematically illustrates a cross-sectional view of a semiconductor device 200 comprising a substrate 201, above which may be formed a metallization system 230. The metallization system 230 may comprise any number of metallization layers wherein, for convenience, a first metallization layer 220 and a second metallization layer 210 are illustrated in figure 2A. For example, in some illustrative embodiments, the metallization system 230 may represent an interconnect structure of a sophisticated semiconductor device, in which circuit elements (not shown) may have critical dimensions of approximately 50 nm and less. As previously explained with reference to the semiconductor device 100, corresponding circuit elements may be formed in an above an appropriate semiconductor material that may be positioned below the metallization system 230. Moreover, the metallization layers 210, 220 may have a similar configuration, as is discussed above with reference to the layers 110, 120 of the device 100 described with reference to figures 1A and 1B. For instance, the metallization layer 210 may comprise a dielectric material 211, such as a low-k dielectric material, and the like, in which may be embedded metal lines 212, which may represent, at least in the device portion illustrated in figure 2A, metal lines of "narrow pitch". That is, the metal lines 212 may have a width 212W which may represent a critical dimension of the metallization layer 210, which may be approximately 100 nm and less in

sophisticated applications. It should be appreciated, however, that in other illustrative embodiments, metal lines 212 may have a greater width depending on the overall design rules and the metallization level under consideration. Moreover, an etch stop layer 213, such a silicon nitride layer, a silicon carbide, a nitrogen enriched silicon carbide layer or any other appropriate material may be provided with appropriate etch stop capabilities and, if required, responding copper confinement characteristics, as previously explained. In the manufacturing stage shown, the metallization layer 220 may be provided in the form of a non-patterned dielectric material 221, which may have any appropriate composition as required for forming therein a wide metal line, at least above the closely spaced metal lines 212. Furthermore, in the manufacturing stage shown, an etch mask 230, for instance in the form of a resist mask, is provided above the dielectric material 221 and comprises a mask opening 203A having a lateral dimension 203W that corresponds to a target lateral dimension of a via opening to be formed in the dielectric material 221. That is, the width 203W may substantially correspond to the width of a corresponding via opening at the bottom thereof, so as to enable a reliable connection to one of the metal lines 212, as indicated by the dashed lines, without interfering with any adjacent metal lines 212. For example, the width 203W may be substantially equal to or less than the corresponding width 202W of the metal line 212.

The semiconductor device 200 as illustrated in figure 2A may be formed on the basis of process techniques, as are also described above with reference to the semiconductor device 100. Thus, in some illustrative embodiments, a high degree of compatibility with conventional process techniques may be accomplished. For example, the etch mask 203 may be formed on the basis of well established process techniques, wherein the mask opening 203 may, however, be designed so as to correspond with the width 212W without requiring additional layers of increased lateral size, which may frequently be used in order to oppress any deposition related irregularities, such as the irregularities 122C as illustrated in figure 1B.

Figure 2B schematically illustrates a semiconductor device 200 when exposed to an etch ambient 204, which may represent an etch ambient created on the basis of

well established etch recipes. Consequently, during the etch process 204, material of the layer 212 may be removed in a highly anisotropic manner, thereby obtaining via opening 212V having a lateral size that substantially corresponds to the lateral size 203W of the mask opening 203A. In some illustrative embodiments, the etch process 204 may be controlled so that the depth 221D of the via opening 221V may be approximately one third or less of a final depth of the via opening 221V, that is, a thickness of the dielectric material 221. A corresponding control of the etch process 204 may readily be accomplished by determining a removal rate for the material 221 and appropriately adjusting the process time of the etch process 204.

Figure 2C schematically illustrates the semiconductor device 200 during a material removal process 205A, which is designed so as to remove material of the etch mask 203. For example, the process 205A may be performed as a plasma assisted process using an oxygen species, while in other cases, any other appropriate plasma assisted etch ambient may be used, in which organic material may be removed without removing significant portions of the dielectric material 221. In still other illustrative embodiments, the process 205A may include a wet chemical resist removal process that may be performed on the basis of well established selective etch chemistries. Consequently, during the process 205A the initial etch mask 203 may be eroded, thereby increasing the lateral size of the opening 203A, as is indicated by the width 203E. It should be appreciated that the increased lateral width 203E may efficiently be adjusted by determining the removal rate of the material of the etch mask 203 in the etch ambient of the process 205A and controlling the etch time. Due to the selectivity of the etch process 205A with respect to the dielectric material 221, the initial lateral width of the via opening 221V may substantially be maintained, at least at the bottom thereof.

Figure 2D schematically illustrates the semiconductor device 200 during a further etch step 204B, which may be performed on the basis of the same etch recipe as the process 204A (cf figure 2B) so that material of the layer 221 may be removed selectively to the etch mask 203. Due to the increased width 203E, also a width of the via opening 221V may be increased at the top thereof, while also increasing a depth, as indicated by 221E, wherein, however, a bottom width may substantially correspond to the initial width 203W (cf. figure 2C). In some illustrative

embodiments, the anisotropic nature of the etch process 204B may be less pronounced compared to the process 204A, thereby obtaining a significant "rounding" of a corner or step caused by the different lateral widths 203W and 203E (cf. figure 2C), thereby obtaining more or less tapered configuration, as illustrated in figure 2D.

Figure 2E schematically illustrates the semiconductor device 200 according to further illustrative embodiments, in which an even more pronounced degree of tapering may be accomplished by repeating the processes 205A, 204B of figures 2C and 2D one or more times, depending on the degree of graduation and the degree of tapering required. For example, as illustrated, the device 200 may be exposed to a further resist erosion process 205B, thereby obtaining a further increased lateral size 203F of the mask opening 203A. For this purpose, the same or similar process recipes may be used, as described above for the process 205A (cf. figure 2C).

Figure 2F schematically illustrates the semiconductor device 200 when exposed to a further etch process 204C so as to further increase the depth of the via 221V, wherein in the embodiment shown, the via 221V may extend down to the etch stop layer 213. It should be appreciated, however, that any other depth of the via 221V may be selected, depending on the overall process strategy. If, for instance, a trench is to be formed in an upper portion of the dielectric material 221, the final etch step for forming the via opening 221B may be performed commonly with a corresponding etch step for obtaining the corresponding trench. After forming a desired amber of resist erosion/etch cycles and achieving the desired depth of the via opening 221V, the further processing may be continued by removing the etch mask 203, which may be accomplished by well established recipes, and thereafter a further etch mask may be formed so as to define the lateral size of a wide trench to be formed above the via opening 221V. For this purpose, in some cases, a corresponding film material may be deposited so as to planarize the surface topography and a corresponding etch mask may be formed on the basis of the planarized surface topography using well established lithography techniques. Thereafter, the via opening 221V and the corresponding wide trench may be filled

in a common deposition sequence, as is, for instance, also described with reference to the semiconductor device 100.

Figure 2G schematically illustrates the semiconductor device 200 according to further illustrative embodiments, in which a pronounced tapering of a via opening may be obtained on the basis of spacer elements. As illustrated, the via opening 221V may be formed in the dielectric material 221 so as to have an initial width 221I and having a first depth 221D, which may for instance, represent approximately 40% to 60% of the final depth of the via opening 221V. Furthermore, in the manufacturing stage shown, spacer elements 206A may be formed on the sidewalls of the via opening 221V, wherein in some illustrative embodiments, the spacer element 206A may be comprised of a material having a similar etch behaviour as the dielectric material 221. That is, the removal rate during an etch process designed so as to remove material of the layer 221 may be within approximately plus-minus 10% for the material of the spacer elements 206A compared to the dielectric material 221. In one illustrative embodiment, the spacer element 206A may be formed on the basis of substantially the same material composition as the dielectric material 221. In this manner a substantially identical etch behaviour may be accomplished during the further patterning of the via opening 221V. Furthermore, in the embodiment shown, an etch stop liner 206B such as a silicon dioxide material, a silicon nitride material, and the like may be provided, if required, with a thickness of several nanometers to approximately ten or more nanometers, depending on overall process requirements.

The semiconductor device 200 as illustrated in figure 2G may be formed on the basis of the following processes. After depositing the dielectric material 221, an appropriate etch mask, such as a resist mask, may be formed, which may comprise an opening having the lateral dimensions corresponding to the initial width 221I of the via opening 221V. Next, an anisotropic etch process may be performed on the basis of well established recipes, as also previously discussed, so as to obtain the via opening 221V extending to the first depth 221D. Thereafter, the resist mask may be removed and a spacer layer (not shown) may be deposited, possibly in combination with the etch stop liner 206B, which may be accomplished by well established deposition techniques. Next, the spacer material may be etched on the

basis of, for instance, similar etch recipes as may also be used for forming the via opening 221V, due to the similarity of the etch behaviour of the spacer material compared to the dielectric material 221. Consequently, the material of the spacer layer may be removed from horizontal device portions and from the centre of the via opening 221V, wherein the advance of the etch front may reliably be stopped at or within the etch stop liner 206B, if provided. In this case, a certain degree of "over etching" may be applied so as to obtain the pronounced rounding of the spacer elements 206A at the top of the via opening 221V. Thereafter, in some illustrative embodiments, exposed portions of the etch stop liner 206B may be removed, for instance by appropriate selected wet chemical etch recipes, plasma assisted etch processes and the like. In other illustrative embodiments, the etch stop liner 206B may be maintained and a corresponding trench etch mask may be formed on the liner 206B.

Figure 2H schematically illustrates the semiconductor device 200 in a further advanced manufacturing stage. As illustrated, an etch mask 207 may be formed above the dielectric material 221 and may comprise an opening 207A so as to define the position and lateral size of a trench 221T formed in an upper portion of the dielectric material 221. For instance, the trench 221T may represent a wide metal line having a width 221W that may be significantly greater than the width 212W of the metal lines 212. In some illustrative embodiments, the width 221W may be twice or more the width of 212W, thereby providing for increased current drive capability, as previously explained.

The etch mask 207 may be formed on the basis of well-established process strategies, in which the surface topography may be planarized, if required, by an appropriate film material and performing a lithography process for patterning a resist material in accordance with the lateral position and size of the trench 221T. It should be appreciated that the via opening 221V (figure 2T) may not necessarily be centered in the middle of the trench 221T so that any appropriate configuration, i.e. spatial relation between the via opening 221V and the trench 221T may be accomplished. Thereafter, the semiconductor device 200 may be exposed to an etch sequence, for instance for removing an exposed portion of any planarization material, if provided, and also etching through exposed portions of the etch stop

liner 206B (cf. Figure 2G). Thereafter, an anisotropic etch process 204D may be performed so as to remove material of the layer 221 on the basis of the etch mask 207, wherein also the via opening 221V is "transferred" into the lower portion of the dielectric material 221. Due to the presence of the spacer elements 206A, a pronounced tapering of the via opening 221V may be accomplished so that a reduced width 221B at the bottom of the via opening 221V may be adapted dto the width 212W of the metal line 212. On the other hand, the via opening 221V may terminate into the trench 221T with a significantly increased width, which may initially be defined by the width 221I, wherein it should be appreciated, that additional corner rounding may occur during the etch process 204D, thereby even further increasing the finally obtained width at the top of the via opening 221V. It should be appreciated that during the etch process 204D, also the etch stop liner 206B may be removed, since during the etch process 204D etch stop material 206B may be attacked from both sides, i.e. the material may be exposed by increasingly removing the spacer 206A and further removing the exposed portion of the material 221 at the opposite side of the layer 206B. After the etch process 204D, the mask 207 may be removed and also the etch stop 213 may be removed in the via opening 221V in order to expose surface portion of the metal line 212.

Consequently, also in this case, a pronounced tapering of the via opening 212V may be accomplished, thereby providing for a significantly enhanced surface topography for the subsequent process sequence for forming a conductive barrier layer and filling in copper or any other highly conductive material on the basis of an electrochemical deposition process.

Figure 2I schematically illustrates the semiconductor device 200 in a further advanced manufacturing stage. As illustrated, the wide metal line 222L is formed above a tapered via 222V, which connects the wide metal line 222L with one of the metal lines 212 of the lower lying metallization layer 210. As previously shown, a width 222W of the wide metal line 222L, may significantly be greater than the width 212W, thereby providing for the high drive current capability of the metal line 222L. Similarly, a width 222B of the via 222V may substantially correspond to the width 212W of the metal line 212, thereby enabling a reliable electrical connection without requiring additional contact areas of increased lateral size. On the other hand, the

width 222T at the top of the via 222V may be significantly greater than the bottom width 222B, thereby providing for the enhanced surface conditions during the filling process, as previously explained. In some illustrative embodiments, the bottom width 222B is approximately 60% or less of the top width 222T.

The semiconductor device 200 as illustrated in figure 2I may be formed on the basis of well established process techniques for forming a conductive barrier material 222A, wherein also the enhanced surface topography provided by the pronounced tapering of the corresponding via opening may enhance overall process uniformity and reliability. Thereafter, copper material or any other highly conductive metal may be filled in by electrochemical deposition, as previously explained with reference to the device 100, wherein a reliable bottom to top fill behavior may be accomplished irrespective of the significantly increased lateral dimension 222W compared to the bottom width 222B. Thereafter, any excess material may be removed, for instance by CMP and the further processing may be continued by forming a cap material on the metal line 222L and the dielectric material 221. Subsequently, any further metallization layers may be formed, if required.

As a result, the present disclosure provides techniques and semiconductor devices, in which a pronounced tapering of transition vias may be accomplished by modifying an etch sequence, for instance by intermittently eroding a resist mask as to form two or more etch steps on the basis of a different lateral size of a corresponding mask opening. In other cases, the etch process may start with the "maximum" lateral size of the via opening, which may reduce during the further advance of the etch process on the basis of appropriately dimensioned spacer elements.

Further modifications and variations of the present disclosure will be apparent to those skilled in the art in view of this description. Accordingly, the description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the principles disclosed herein. It is to be

understood that the forms shown and described herein are to be taken as the presently preferred embodiments.

CLAIMS

1. A method comprising:

forming an etch mask above a dielectric material of a first metallization layer of a semiconductor device, said etch mask comprising a mask opening having a first lateral size corresponding to a target lateral size at a bottom of a via to be formed in said dielectric material;

forming a via opening on the basis of said mask opening having said first lateral size so as to extend to a first depth in said dielectric material;

increasing said mask opening such that the mask opening has a second lateral size;

increasing said via opening on the basis of said mask opening having said second lateral size so as to extend to a second depth;

forming a trench above said via opening in said dielectric material so as to connect to said via opening; and

commonly filling said via opening and said trench with a metal containing material, said via opening extending to a metal region of a second metallization layer located below said first metallization layer.

2. The method of claim 1, further comprising increasing said mask opening such that the mask opening has a third lateral size and increasing said via opening on the basis of said mask opening having said third lateral size so as to extend to a third depth.

3. The method of claim 1, wherein increasing the lateral size of said mask opening comprises providing said etch mask as a resist mask and performing a resist removal process.

4. The method of claim 1, wherein forming said trench comprises forming a trench etch mask above said dielectric material and said via opening extending at least to said second depth and performing an etch process to obtain said trench and increase a depth of said via opening.

5. The method of claim 1, wherein increasing said via opening further comprises performing an etch process on the basis of said etch mask and controlling said etch process by using an etch layer formed below said dielectric material.

6. The method of claim 1, wherein said target lateral size is approximately equal to or less than a width of said metal region.

7. The method of claim 1, wherein said via opening extending to said first depth is formed prior to forming said trench.

8. The method of claim 1, wherein said trench is formed prior to forming said via opening.

9. The method of claim 1, wherein said first depth is approximately 30 percent of a final depth of said via opening.

10. The method of claim 1, wherein said target lateral size is approximately 100 nanometer or less.

11. A method comprising:

forming a via opening in a dielectric material of a first metallization layer of a semiconductor device, said via opening extending to a first depth and having a first lateral size;

forming a spacer element on sidewalls of said via opening; and

increasing a depth of said via opening so as to extend to a metal region of a second metallization layer that is formed below said first metallization layer.

12. The method of claim 11, wherein forming said via opening comprises forming an etch mask having a mask opening, etching said into said dielectric material on the basis of said etch mask and removing said etch mask .

13. The method of claim 12, wherein forming said spacer element comprises depositing a spacer layer and etching said spacer layer so as to define a target width of a bottom of said via opening.

14. The method of claim 13, further comprising forming an etch stop layer prior to depositing said spacer layer.

15. The method of claim 11, wherein increasing the depth of said via opening comprises removing material of said spacer element and said dielectric material with a similar removal rate.

16. The method of claim 11, further comprising forming a trench in said dielectric material above said via opening, wherein said via opening connects to said trench.

17. The method of claim 16, wherein said trench is formed while increasing the depth of said via opening.

18. A semiconductor device comprising:

a first metallization layer formed above a substrate, said first metallization layer comprising a metal line having a first width;

a second metallization layer formed below said first metallization layer and comprising a second metal line having a second width that is less than said first width; and

a via extending from said first metal line to said second metal line, said via having a first lateral dimension at said first metal line and a second lateral dimension at said second metal line, said second lateral dimension being approximately 60 percent or less of said first lateral dimension.

19. The semiconductor device of claim 18, wherein said second lateral dimension is approximately 100 nanometer (nm) or less.

20. The semiconductor device of claim 18, wherein said second lateral dimension is approximately 40 percent or less of the said first lateral dimension.

21. The semiconductor device of claim 18, wherein said first width is at least twice said second width.

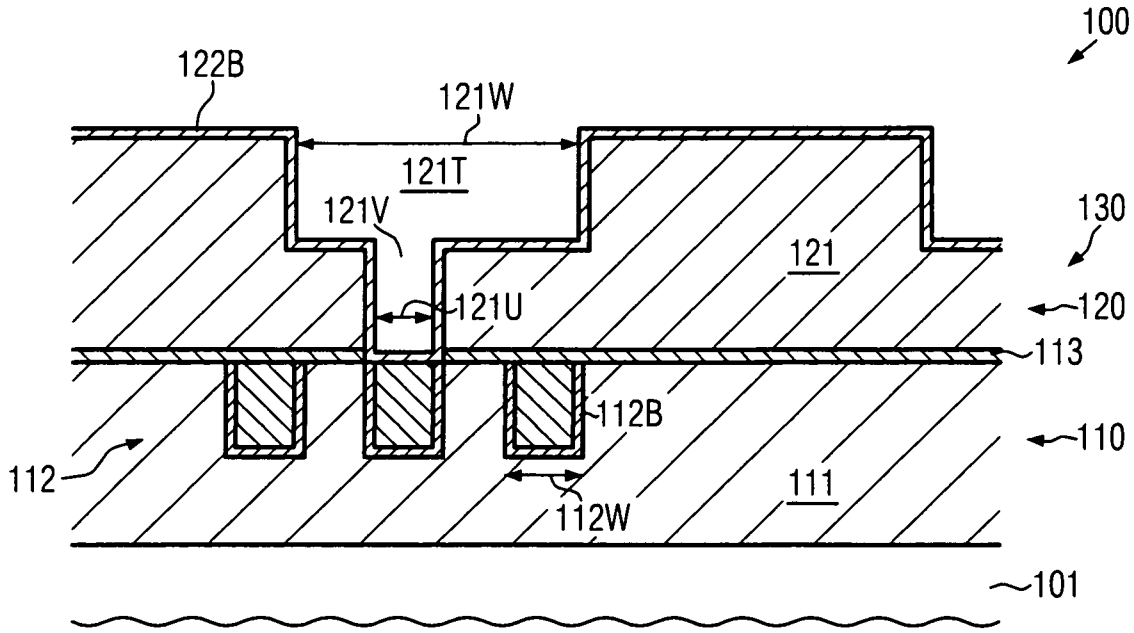


FIG. 1a
(prior art)

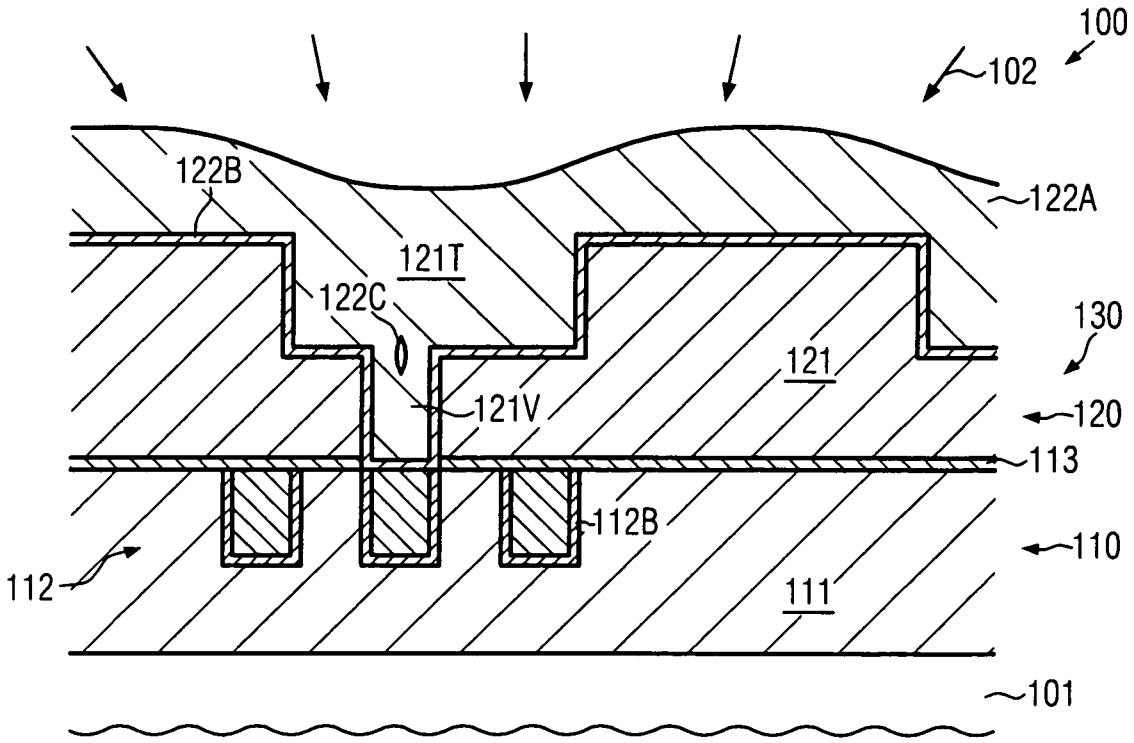


FIG. 1b
(prior art)

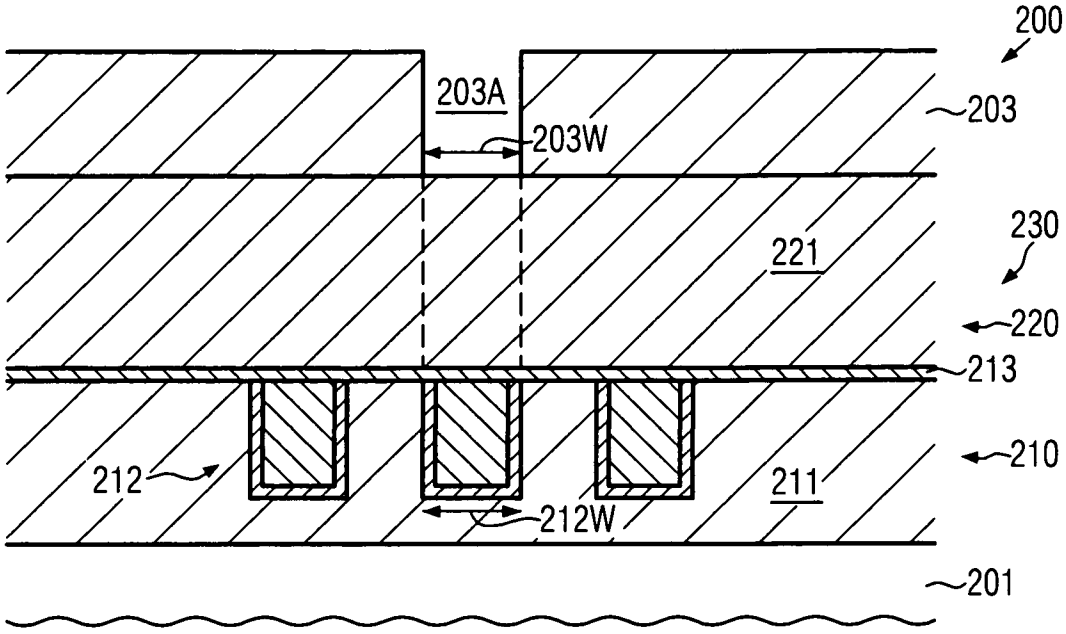

200
203A
203W
203
230
221
220
213
212
211
210
212W
201

FIG. 2a

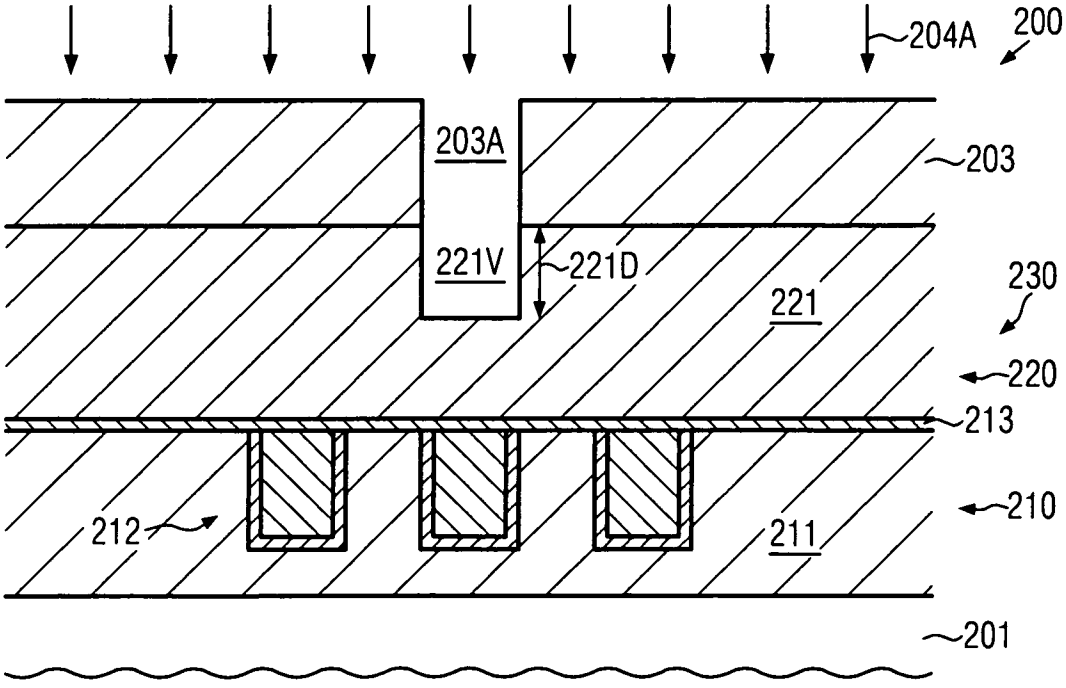
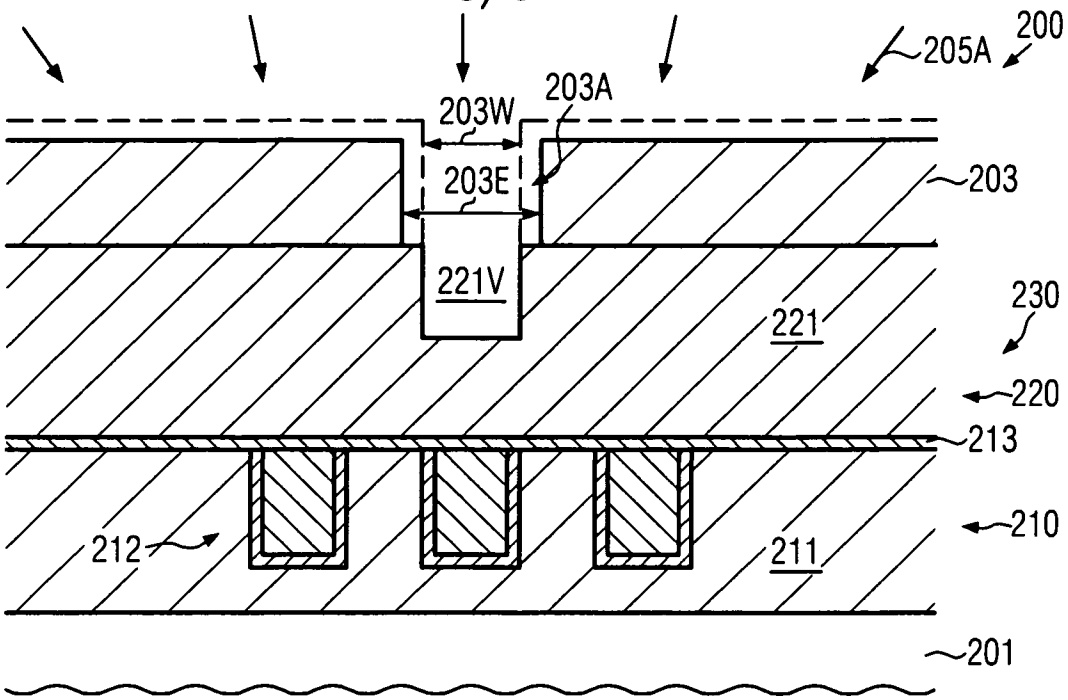

204A
200
203A
203
221V
221D
230
221
220
213
212
211
210
201

FIG. 2b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205A
203A
203W
203E
203
221V
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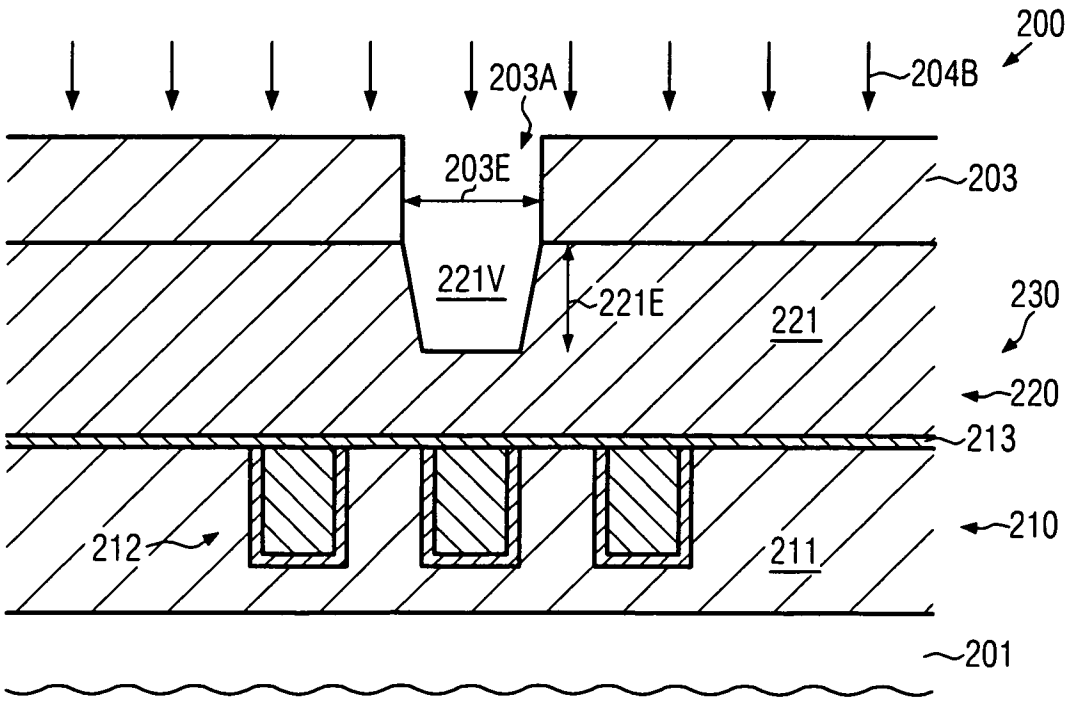
230
220
213
210
212
211
201

FIG. 2c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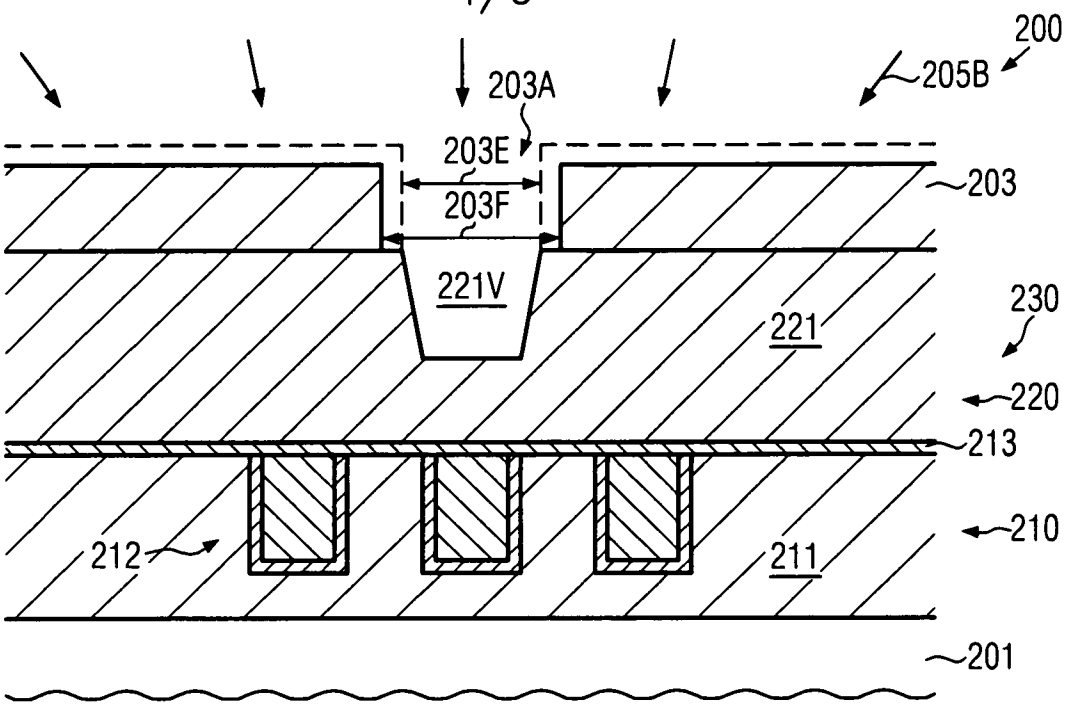
204B
203A
203E
203
221V
221E
221
230
220
213
210
212
211
201

FIG. 2d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203E
203F
203
221V
221
230
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213
210
212
211
201

FIG. 2e

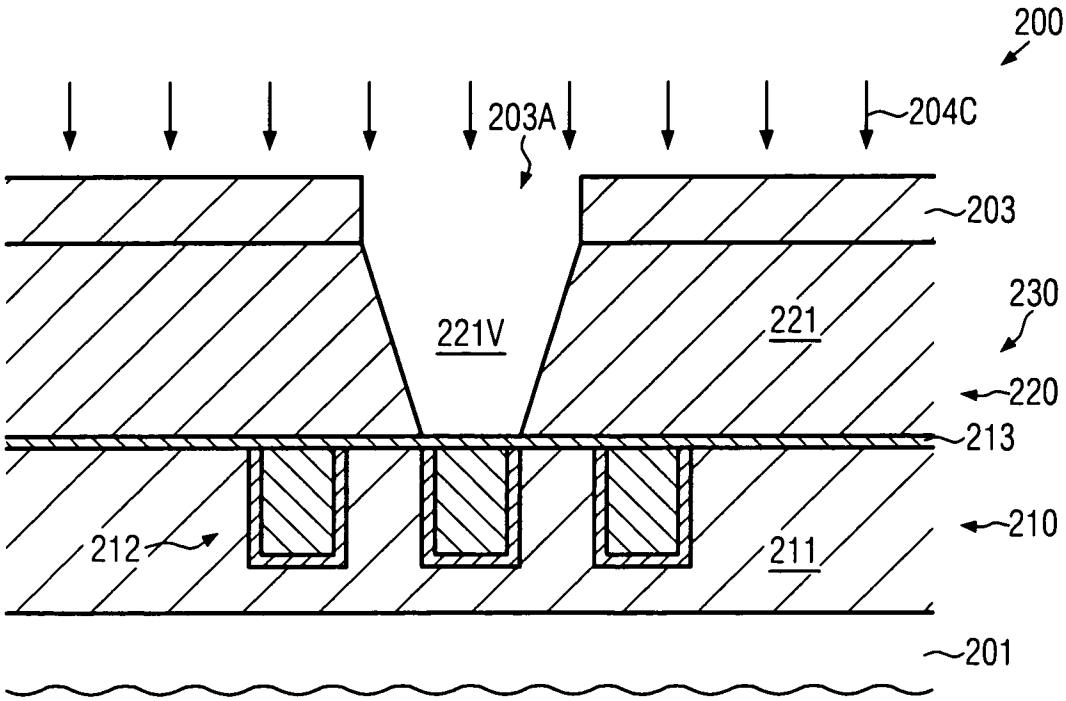
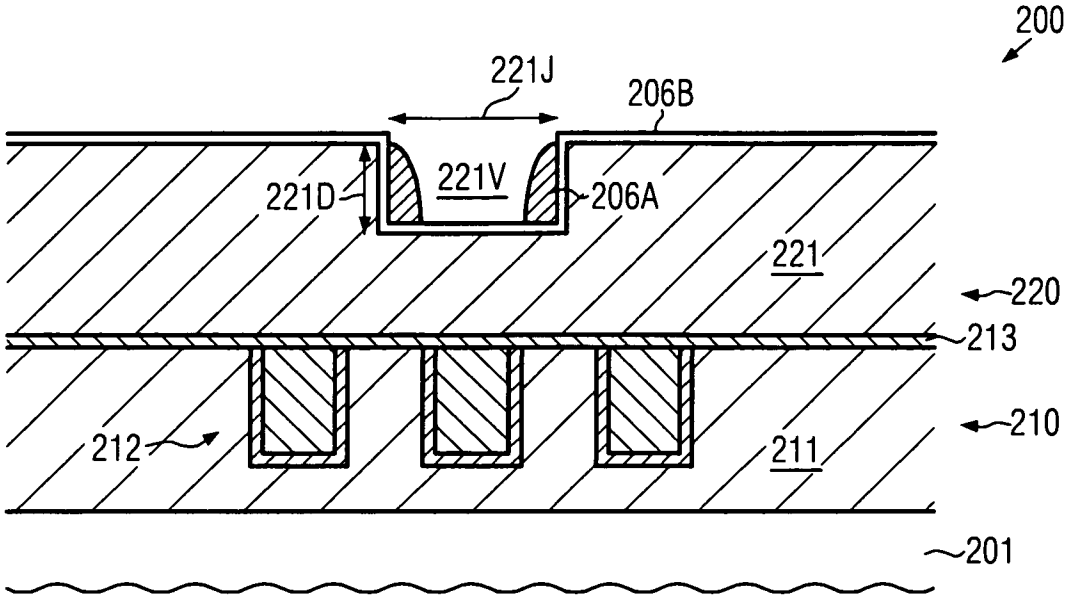

200
204C
203A
203
221V
221
230
220
213
210
212
211
201

FIG. 2f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221J
206B
221D
221V
206A
221
220
213
210
212
211
201

FIG. 2g

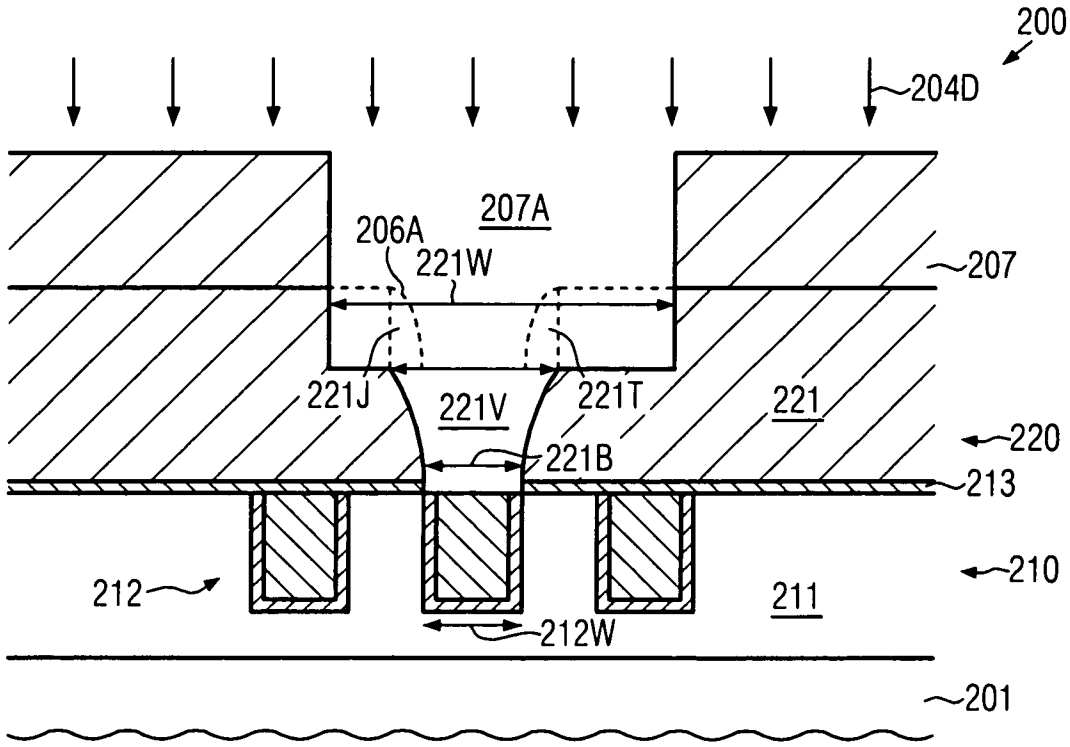
200
204D
207A
206A
221W
207
221J
221V
221T
221
220
221B
213
210
212
211
212W
201

FIG. 2h

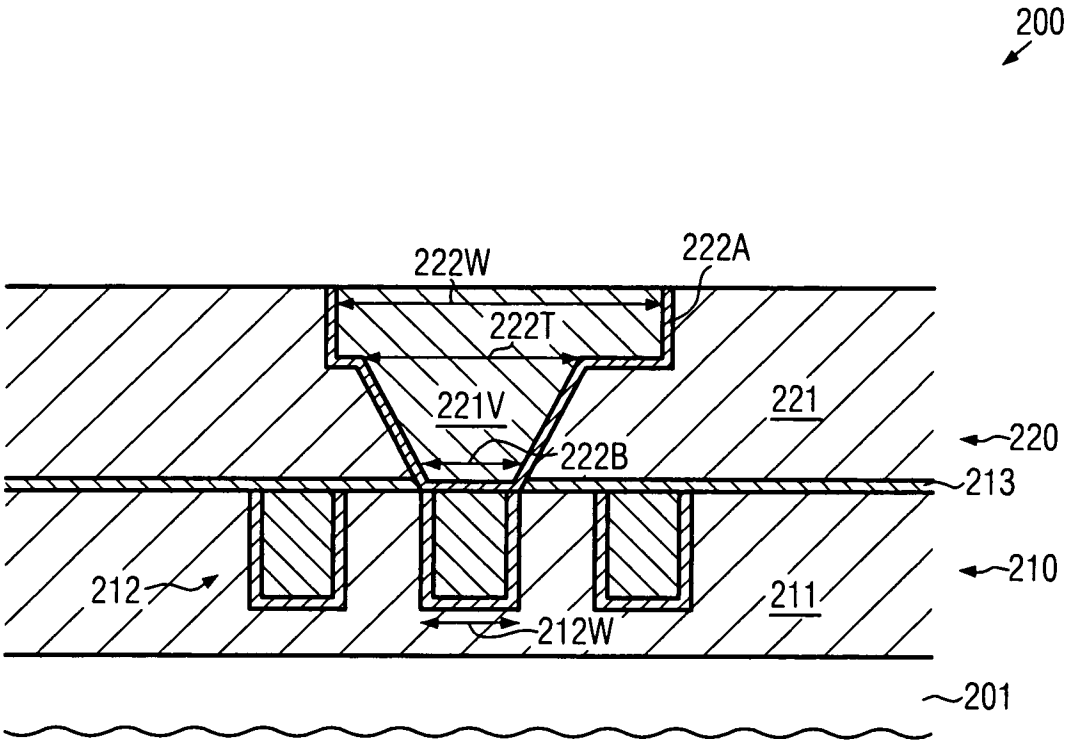

FIG. 2i

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/009308

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/768
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2006/270214 A1 (IBA YOSHIHISA [JP]) 30 November 2006 (2006-11-30) page 1, paragraph 6 - page 4, paragraph 50; figures 1-8	1-10, 18-21
A	US 4 698 128 A (BERGLUND ROBERT K [US] ET AL) 6 October 1987 (1987-10-06) column 4, line 7 - column 5, line 2; figures 1-6	2,3
A	JP 08 191062 A (SONY CORP) 23 July 1996 (1996-07-23) the whole document	1-10, 18-21
A	US 6 403 471 B1 (LOU CHINE-GIE [TW]) 11 June 2002 (2002-06-11) column 2, line 25 - column 4, line 44; figure 2	1-10, 18-21

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
1 June 2010	09/06/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Fax: (+31–70) 340–3016	Lyons, Christopher

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/009308

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 440 847 B1 (LOU CHINE-GIE [TW]) 27 August 2002 (2002-08-27) column 3, line 15 - column 4, line 6; figures 1-7	11-13, 16,17
X	US 2001/039114 A1 (NAKAMURA RYOICHI [JP]) 8 November 2001 (2001-11-08) page 2, paragraph 31 - page 3, paragraph 42; figures 2-10	11-14,16
X	US 4 472 240 A (KAMEYAMA SHUICHI [JP]) 18 September 1984 (1984-09-18) column 6, line 60 - column 8, line 20; figures 8-9	11-14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2009/009308

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-10, 18-21

directed to a method of forming an interconnect comprising a via opening with an etch mask whose opening is increased in size between two via etch steps and a device fabricated by this method.

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2. claims: 11-17

directed to a method of forming a via opening in two etch steps with a spacer formed in the via between the two etch steps.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2009/009308

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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