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(54) **Title:** ELECTROCHEMICAL DEPOSITION PROCESSES FOR SEMICONDUCTOR WAFERS

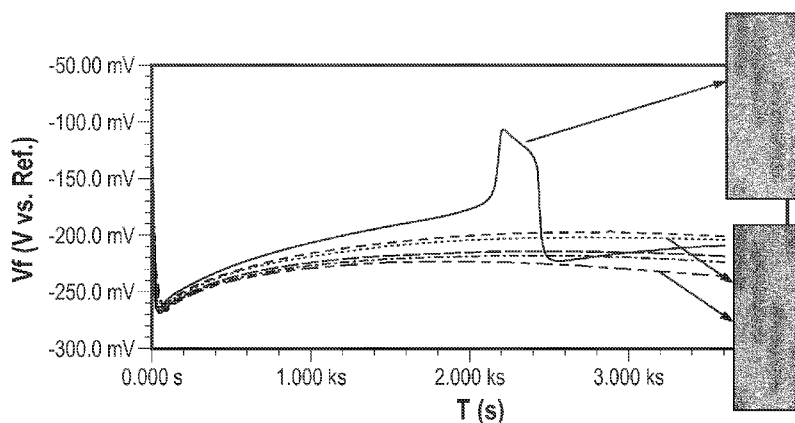


FIG. 1

(57) **Abstract:** A method for electroplating a wafer detects plating bath failure based on a voltage change. The method is useful in plating wafers having TSV features. Voltage of each anode of a plating processor may be monitored. An abrupt drop in voltage signals a bath failure resulting from conversion of an accelerator such as SPS to it's by products MPS. Bath failure is delayed or avoided by current pulsing or current ramping. An improved plating bath has a catholyte with a very low acid concentration.

ELECTROCHEMICAL DEPOSITION PROCESSES FOR SEMICONDUCTOR WAFERS

TECHNICAL FIELD

[0001] The invention relates to processors, systems, and methods for
5 electroplating substrates such as semiconductor material wafers. More specifically the
invention provides improved techniques especially useful with wafers having through
silicon vias (TSV) or similar features.

BACKGROUND OF THE INVENTION

[0002] Microelectronic devices such as semiconductor devices are generally
10 fabricated on and/or in substrates or wafers. In a typical fabrication process, one or
more layers of metal or other conductive materials are formed on a wafer in an
electroplating processor. The processor may have a bath of electrolyte held in vessel or
bowl, with one or more anodes in the bowl. The wafer itself may be held in a rotor in a
head movable into the bowl for processing and away from the bowl for loading and
15 unloading. A contact ring on the rotor generally has a large number of contact fingers
that make electrical contact with the wafer.

[0003] Many advanced microelectronic devices have through silicon vias (TSV).
A TSV is a vertical electrical interconnection usually passing completely through the
wafer or die, which may or may not actually be silicon. TSV's are used to create three
20 dimensional electronic structures and packages. Use of TSV's allows for very high
density integrated circuits. The electrical characteristics of the interconnections are also
improved because generally TSV's are shorter than alternative interconnections. This

results in faster device operation and reduced effects from undesirable inductive or capacitive characteristics of the interconnections.

[0004] TSV's tend to have high aspect ratios, as they are essentially tall narrow micro-scale columns of metal, generally copper, formed in a hole in silicon or other substrate material. TSV's may be formed by electroplating copper from the bottom up. Achieving proper fill of the TSV is technically challenging for several reasons, including the micro-scale dimensions of the TSV, high aspect ratios, and other factors.

[0005] Historically, the processes and chemistries used for plating fill of TSV have exhibited uncommon instability as the plating bath ages, which directly affects the microelectronic manufacturing process. Since the plating bath is generally still within specification at failure, the reason for bath failure has not been well understood. Improved techniques and understanding of plating TSV features are needed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] In the drawings, the same element number indicates the same element in each of the views.

[0007] Fig. 1 is a graph of data of chronopotentiometric measurements (voltage vs. time) for a fresh plating bath and a failed plating bath, with corresponding X-ray images of wafers plated using the baths.

[0008] Fig. 2 is a graph of data of chronopotentiometric measurements for a bath having a chemical makeup different from the graphs of Fig. 1.

[0009] Fig. 3 is a graph of data similar to Fig. 2 but with the bath injected with MPS and with current ramping.

[0010] Fig. 4A is a graph of voltage for a control bath of fresh electrolyte.

- [0011] Fig. 4B is a graph of voltage for a bath that failed after about 30 minutes.
- [0012] Fig. 4C is a graph of voltage for a bath recovered after 70 hours of idle time.
- [0013] Fig. 5A is a plot of voltage for a fresh bath vs. a bath after 10 runs.
- 5 [0014] Fig. 5B are graphs of voltage from of bench scale chronopotentiometry aging trial.
- [0015] Figs. 6A-6F are X-ray images of TSV's on wafers processed as described.
- [0016] Fig. 6G is a graph of voltage from chronopotentiometry aging trials.
- [0017] Fig. 7 is a graph of chronopotentiometry vs. wafer rotation speed.
- 10 [0018] Figs. 8A and 8B show X-ray images of wafers processed as described.
- [0019] Fig. 9 is a graph of chronopotentiometry vs. bath age.
- [0020] Fig. 10 is a comparison table of prior art electrolyte to a new electrolyte.
- [0021] Fig. 11 is a perspective view of a Raider M processor as used running tests reflected in the data shown in the Figs. above.
- 15 [0022] Fig. 12 is a section view of the processor shown in Fig. 11.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

I. DETECTION OF BATH FAILURE

A. Bench Scale Detection of Bath Failure

- [0023] Detection of bath failure has been a challenge in a TSV plating baths. The
- 20 bath failure can be defined by under fill deposition, seam voids and pinch off voids in the features. There is a common trend that fresh bath performs well, but with continued reductive plating (to 0.45 A Hr/L) the bath fails.

[0024] The conventional way to detect bath failure is to plate a wafer in the tool and do X-ray imaging/ cross section imaging using focused ion beam (FIB) to detect voids. However wafer availability for imaging is usually limited. This is expensive and time consuming process. Until now there has been no real and practical method
5 available to detect bath failure.

[0025] As described below, a chronopotentiometric method has now been invented for detecting bath failure. The inventors have now determined that the reason for this is that the bath becomes accelerator dominated and loses suppression with over plating time. This leads to conformal growth and voids in the vias or trenches.

10 **[0026]** This method may be practiced in a bench top electrochemical setup, or in a tool or system level setup.

[0027] In one form of a bench top method, a chronopotentiometric measurement with long time scale (3600 seconds) is used to detect bath failure. Referring to Fig. 1, a one hour time scale allows adsorption kinetics for organic additives during the plating
15 step to be fully accounted for. In general, plating in TSV lasts between 10-180 minutes (e.g., for 3x 50 to SOx 150 features). As shown in Fig. 1, a fresh bath is highly suppressive immediately after immersion of the Cu-plated Pt electrode with a final potential at 3600s, around -240 mV.

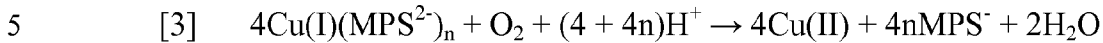
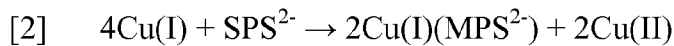
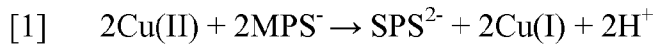
[0028] Organic additives are conventionally included in the plating bath to
20 improve results in TSV plating. A suppressor additive, (usually a high-molecular-weight polyalkene glycol such as PEG) adsorbs strongly on the Cu cathode surface, in the presence of chloride ions, to form a film that sharply increases the over-potential for Cu deposition. An accelerator additive counters the suppressive effect of the suppressor to

provide the accelerated deposition within trenches and vias needed for bottom up filling. SPS (sodiumsulfopropyl disulfide) has been used as an accelerator. MPS (3-mercaptopropylsulfonic acid) is a known bi-product or breakdown product of SPS. A leveler additive, such as amine and heterocyclic compounds, is also used in TSV plating. The leveler is also a strong suppressor.

[0029] The chronopotentiometric measurements of the bath samples in Fig. 1 demonstrate quick adsorption of suppressor and leveler to the electrode surface, followed by replacement of the suppressor and leveler by the accelerator. With continuous reductive plating, up to 0.347 A Hr/L, the bath becomes less suppressive (about 25 mV less) than the fresh bath. This results because the SPS (accelerator) is reduced to MPS or Cu (I) thiolate, which facilitates Cu deposition. When the bath is aged to 0.45 A Hr/L, test data shows an increased rate of displacement of suppressor and leveler by accelerator and also competitive adsorption or oscillation behavior. This oscillation behavior correlates directly with failure of the bath.

[0030] Fig. 1 shows that fresh bath at 0 Amp Hr./L is highly suppressor dominated and becomes less suppressor dominated with reductive plating over time. The bottom X-ray image in Fig. 1 is from a wafer plated in a processor at 0.34 Amp Hr./L and shows no voids. The top X-ray image in Fig. 1 is from a wafer plated at 0.45 Amp Hr./L and shows the voids at the light gray areas towards the top of the vias. At around -110 mV, either formed Cu(I) thiolate incorporates into the copper film or it detaches from the copper surface. The bath then becomes suppressor dominated again. The potential oscillation and failure mode in a bench top test were confirmed in a tool scale test.

[0031] The key chemical reactions describing the oxidative thiol-disulfide relationship at the root of the instability are:



[0032] In a bench method, a bath sample of 200 ml was taken from the bath of processor having a total electrolyte volume of about 80 L. A three-electrode potentiostat was used to pass a constant current through the sample, while monitoring potential over time. Referring to the top trace in Fig. 1, the potential gradually rose from about -250 mV to about -180 mV until about 2000 seconds when the potential spiked up to about -110 mV and then dropped rapidly back down to about -250 mV at about 2400 seconds. A TSV test wafer plated with this bath after 2400 seconds showed voids.

B. Tool or System Scale Detection of Bath Failure

[0033] In existing plating processors designed for TSV applications, the plating process tends to be unstable, with under-filled and/or voids in TSV's occurring after running even a relatively small number of wafers in a fresh bath. The inventors have determined that the instability is linked to accelerator SPS and its by-product MPS, leading to field depolarization or loss of suppression, with electrical current shifted from the vias or trenches to the field or top surface of the wafer. Suppression refers to the combined suppressing effect of the suppressor and the leveler.

[0034] In a tool or system scale set up, a test wafer having a copper blanket seed layer may be loaded into the processor. The potential of each anode in the processor may be monitored to sense changes in the bath chemistry and the onset of voids or

under fill can be detected. An oscillation or drop in cell voltage will occur when surface suppression is lost or reduced. If this occurs while a TSV feature is still filling, voiding or under fill will result. Voiding is the primary failure mode. Overfill and under fill may occur as lesser failure modes, especially if the failure occurs near the end of the process
5 when the feature is already largely completed. In this case, slight under fill may occur.

[0035] Smaller features fill faster than larger feature. The number of wafers that may be plated before a predicted bath failure may be influenced by the plating time for each wafer, which is determined at least in part by feature size. Cumulative plating time is identified as a key factor in predicting bath failure, as opposed to number of wafers
10 plated.

[0036] Figs. 4A-4C show voltage plots for a processor having four anodes (an Applied Materials Raider S plating processor). The voltage measurement for each of the anodes are labeled A1, A2, A3 and A4, with A1 being the inner anode and A4 the outer anode. The TSV is 10 μm X 100 μm . Fig. 4A shows data for a fresh bath with stable
15 performance, as expected. The S-ray image in Fig. 4A shows no voids in the TSV feature. Fig. 4B shows a bath failure at 30 minutes, with the failure indicated by the abrupt change in potential. The X-ray image of Fig. 4B shows voids at the light gray area at the bottom end of the TSV feature. Fig. 4C shows voltage plots after 70 hours of idle time. Comparing Fig. 4A with Fig. 4C shows that idle time recovery can restore the
20 bath to its original fresh condition, although only after a long recovery period.

[0037] Fig. 5A shows data from a tool or processor scale test (an Applied Materials Raptor-M processor) using a blanket copper seed layer 300 mm wafer run at 2 mA/cm² for 60 minutes. The lower trace is run No. 1 using a fresh bath. The upper

trace is run No. 10. The sudden drop of the upper trace (about 95 mV) at 30 minutes indicates bath failure.

[0038] Fig. 5B shows similar data from a corresponding bench or beaker scale test.

5 **[0039]** Figs. 6A-6G show test data with varying dissolved oxygen (DO) concentrations in the bath. Existing processors generally operate with baths having 7-8 ppm of dissolved oxygen, which is the saturation level. Reducing dissolved oxygen in the bath to 3-5 ppm can extend the effective bath life. The following were observed:

[0040] A.] 15-20mV depolarization between 0 and 0.5Ahr/L bath age.

10 **[0041]** B.] Solid 10x100 fill performance out to 2.6 A Hr/L

[0042] C.] Stable (+/-5mV) suppression between 0.5 and 2.5Ahr/L.

[0043] D.] Slight under-fill at center of wafer together with additional loss of suppression and voltage oscillation at 3.2Ahr/L.

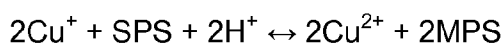
[0044] E.] Effective B&F from sampling is <3%

15 **[0045]** F.] By operating at lower DO concentration (3-5ppm vs saturation) bath life can be extended by >300%

[0046] Fig. 7 is a chronopotentiometry graph with the plot on the left using a wafer rotation speed of 1500 rpm and the plot on the right using 500 rpm, again with the Raptor M processor. All other parameters were the same. The higher rpm provides
20 higher mass transfer, and is also shown as having earlier bath failure. Reducing mass transfer may prolong bath life. This test was run on a 200 ml sample at 2 mA/cm² and 3.2 A Hr./L.

[0047] The results discussed above apply generally to all types of processors. Some processors use a membrane that separates the anodes from the wafer, with the electrolyte above the membrane referred to as catholyte, and the electrolyte below the membrane referred to as anolyte. Figs. 8A and 8B show results from bench testing of a low acid and low accelerator catholyte compared to a moderate acid and moderate accelerator catholyte. Fig. 8A shows X-ray images from wafers plated using a low acid (10g/L sulfuric acid) and low accelerator (5 ml/L) at 0, 5, 10 and 15 A Hr/L, with no voids present. Fig. 8B shows X-ray images from wafers plated using a moderate acid (50g/L sulfuric acid) and moderate accelerator (10 ml/L) at 0 and 1 A Hr/L with a void present at 1 A Hr/L.

[0048] Fig. 9 shows chronopotentiometry plots of bench top data of baths that provided the results shown in Fig. 8A. No potential oscillations were observed on bath samples aged to 24 A Hr/L with low acid and low accelerator concentrations. By reducing sulfuric acid concentration, H⁺ ion availability is reduced. This may affect the SPS breakdown rate. By reducing both the H⁺ availability and the SPS, the equilibrium concentration of MPS is effectively reduced via the chemical reaction:



[0049] Fig. 10 compares a new electrolyte for plating copper TSV wafers in a membrane processor, in comparison to existing designs. The catholyte VMS of 63.5/10/80 is 63.5 grams/liter copper, 10 gm/liter of sulfuric acid, and 80 ppm of chloride concentration. The bath life is extended from less than 2.5 A Hr/L to over 20 A Hr/L. The new parameters listed in Fig. 10 were determined experimentally. Initially theories of improvement were generated. The theories were then tested via screening of variables.

This identified the key variables of bath stability as sulfuric acid concentration, accelerator concentration, and plating process design. From this optimized set points were determined. Production simulations were then conducted which demonstrated the results shown in Fig. 10. Reducing the acid content is a major contributor to the longer bath life.

II. RECOVERY FROM BATH FAILURE

[0050] Instability of the bath correlates with formation of MPS, a strong accelerator, during reductive plating. This results in poor bottom up fill, poor suppression in the field and in the trenches. It is difficult or impossible to maintain a constant concentration of MPS throughout the plating process. However, MPS may be mitigated in several ways.

[0051] MPS can be minimized with bleed and feed (30 %), where the bath is constantly being refreshed. This removes MPS from the bath continuously, so that the MPS concentration remains generally stable. Bleed and feed however adds cost and complications to the plating process.

[0052] MPS may also be controlled by idle time recovery. By allowing the bath to sit idle, MPS will oxidize or convert back to SPS. However, this can take hours or days. It is highly time consuming and of course delays processing.

[0053] Purging the bath also removes MPS. This may be performed by bubbling clean dry air up through the bath. Deplating or running the plating process with reverse polarity also removes MPS. These techniques are generally inefficient and time consuming as well.

A. Current Pulsing

[0054] An improved technique for delaying or avoiding bath failure resulting from MPS is current pulsing. In standard plating processes current is continuous. This results in continuous formation of MPS or Cu(I) thiolate, a complexing group, by combining
5 Cu(I) ions with MPS thiolate group. This causes the bath to become highly accelerator dominated over time, resulting in under fill due to decreased suppression on the fields.

[0055] By pulsing the current during the plating process, using short pulses or long pulses, formation of MPS is controlled. The pulsing may be negative, that is current may be pulsed to negative current from a positive or plating current, or the pulsing may
10 be positive, that is pulsing of plating current or going to an open circuit potential. Cross-over pulsing may also be used via pulsing with constant current and constant voltage. The pulsing may be done at regular intervals in a POR process. This may help to maintain bath stability by knocking MPS off of the copper surface and increasing bath suppression.

15 **[0056]** Pulsing may also be performed with no wafer present.

B. Current Ramping

[0057] Current density ramping may be used to reduce the effect of MPS and restore bath stability. Fig. 2 shows chronopotentiometric measurements of a fresh JCU bath (63/50/80-10/5/15) and a fresh JCU bath (63/50/80-10/5/15) injected with 0.02 ppm
20 MPS at a constant current density of -2 mA/sq.cm and rotation at 500 rpm. As shown in the plots, the bath that was injected with 0.02 ppm MPS demonstrates a potential oscillation which is associated with a failed bath. This behavior was also observed on

tool scale experiments in which under-fill and/or voids were associated with potential oscillations.

[0058] Figure 3 shows a chronopotentiometric measurement of a fresh JCU (63/50/80-10/5/15) bath injected with 0.02 ppm MPS at an increasing current density from 2 to 3.2 mA/sq.cm over 3600 seconds with rotation at 500 rpm. The potential oscillation observed under a constant current density was mitigated and some of the bath suppression was restored. The ramping current density increases bath suppression and stabilizes the bath, either due to increasing chloride coverage on the copper surface or suppressor/leveler adsorption dependency with negative current density.

III. PROCESSOR AND SYSTEMS

[0059] Figs. 11-12 show an example of a processor 20 which may be provided with a bath failure detection system. In this example the processor 20 has a rotor 24 in a head 22. The head may be lowered to position a wafer 40 on the rotor 24 into contact with catholyte in the bowl 26 above a membrane 32. Anolyte and one or more anodes 28 are in the bowl 26 below the membrane 32. An agitator or paddle 36 may optionally be provided in or at the top of the bowl 26.

[0060] In this design, the processor controller 50 monitors the voltage of each anode 28. Upon detection of an abrupt change in voltage, the controller determines that a bath failure has occurred. The controller may then sound an alert or alarm, and optionally shut down. Generally, most processors of this type already have the electrical connections needed to perform this function, so that this function may be added to the

processor via software used in programming the controller. The methods described above may be used in processors with or without a membrane.

[0061] As described, an electroplating system for processing a wafer having TSV features may include a bowl for holding a bath of electrolyte and one or more anodes in the bowl. A wafer holder has a contact ring making electrical contact with the wafer, with a cathode electrically connected to the contact ring. A voltage monitor monitors voltage between one or more of the anodes and the contact ring. A controller is linked to the voltage monitor, with the controller detecting a bath failure based on a change in voltage.

CLAIMS:

1. A method for electroplating a wafer, comprising:
placing the wafer into contact with a bath of electrolyte having an
accelerator, a leveler and a suppressor;
5 passing electrical current from one or more anodes through the electrolyte
and through a conductive layer on the wafer;
 monitoring the voltage of the one or more anodes;
 detecting a failure of the bath from a change of the voltage.
2. The method of claim 1 further comprising detecting a failure of the bath on
10 the basis of a drop in voltage of at least 100 mV.
3. The method of claim 1 wherein the wafer has TSV features.
4. A method for electroplating a wafer, comprising:
 placing the wafer into contact with a bath of electrolyte having an
accelerator and a suppressor;
15 passing electrical current from one or more anodes through the electrolyte
and through a conductive layer on the wafer; and
 pulsing the electrical current to control formation of MPS in the bath.
5. The method of claim 4 further including monitoring the voltage of the one
or more anodes to detect a failure of the bath based on a drop or an oscillation of the
20 voltage.
6. The method of claim 4 wherein the wafer has TSV features.

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7. A method for electroplating a wafer, comprising:

placing the wafer into contact with a bath of electrolyte having an accelerator and a suppressor;

passing electrical current from one or more anodes through the electrolyte

5 and through a conductive layer on the wafer; and

ramping the electrical current to control formation of MPS in the bath.

8. The method of claim 7 further including monitoring the voltage of the one or more anodes to detect a failure of the bath based on a drop or an oscillation of the voltage.

10 9. The method of claim 7 wherein the wafer has TSV features.

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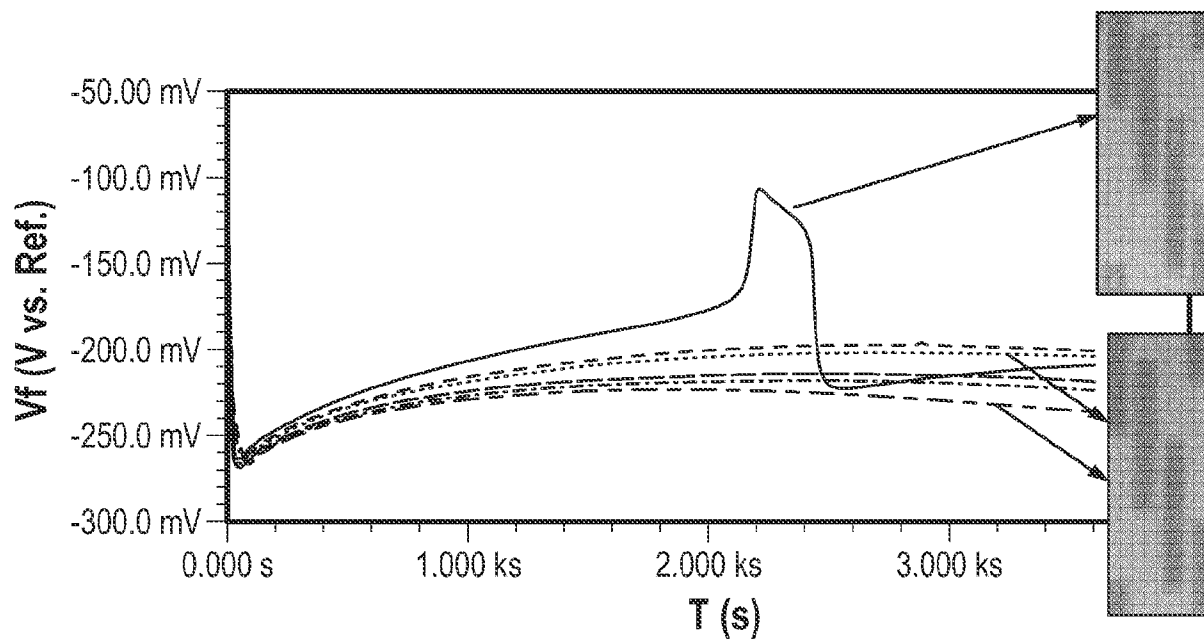


FIG. 1

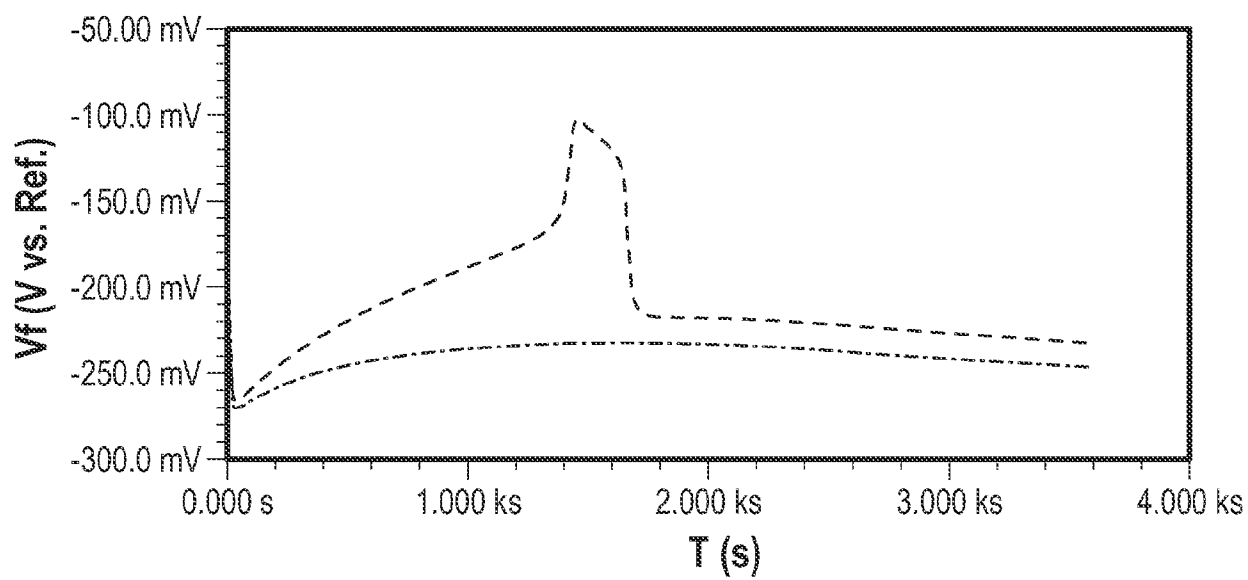


FIG. 2

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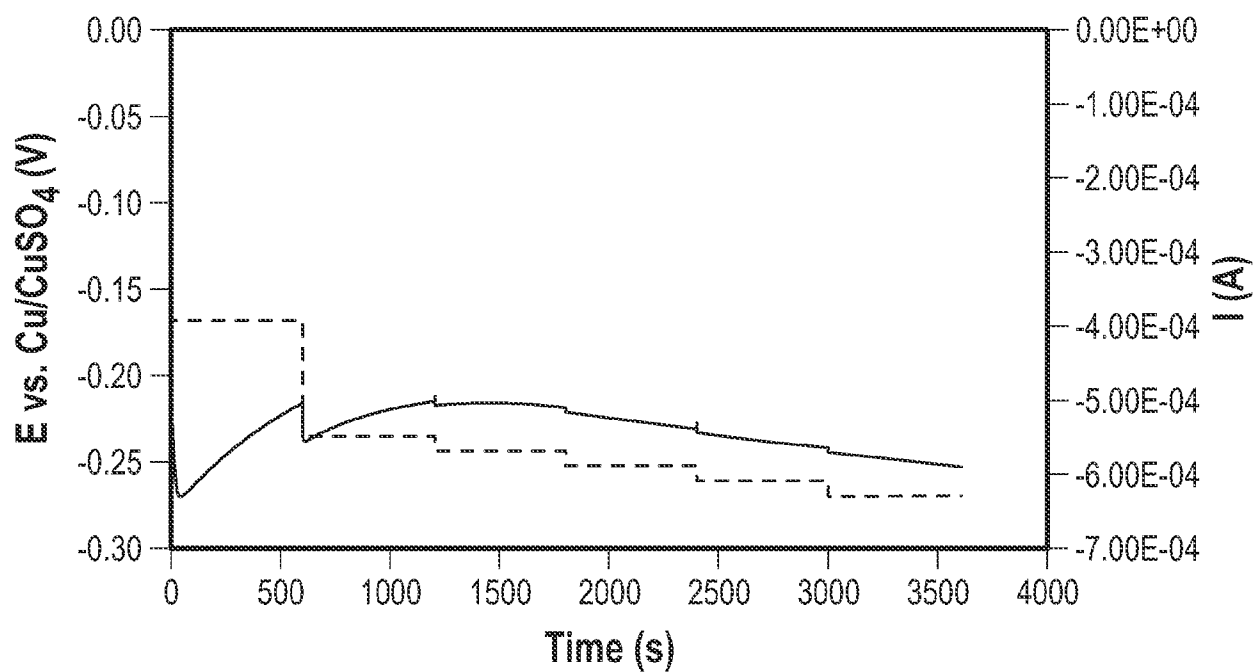


FIG. 3

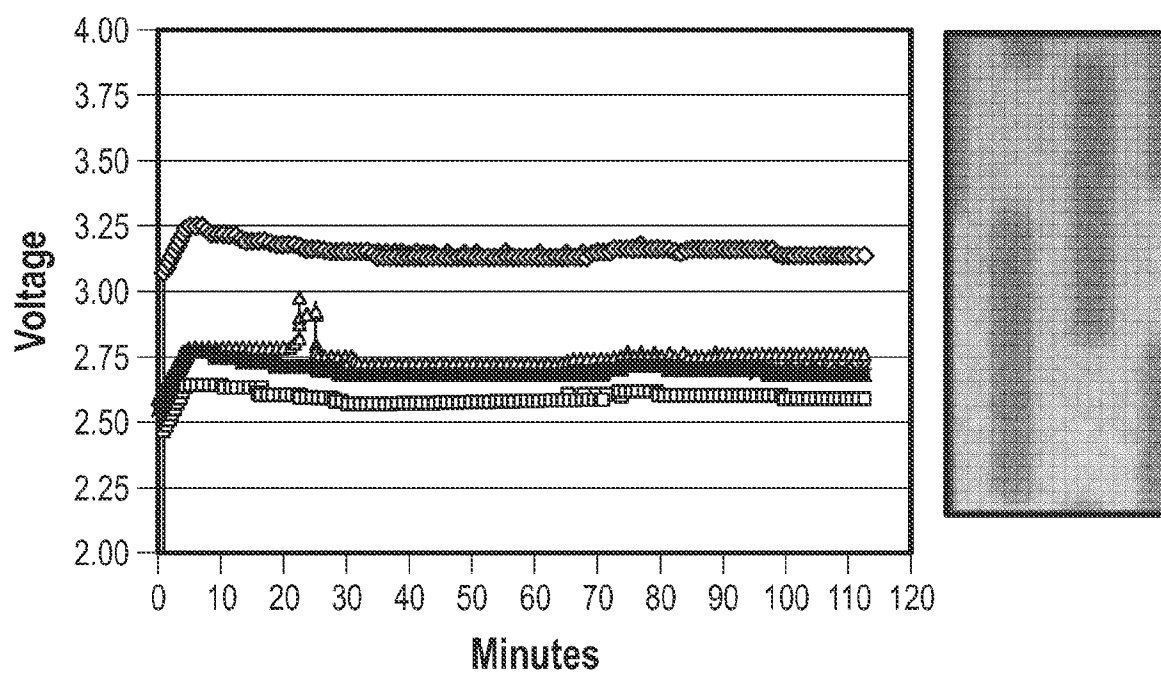


FIG. 4A

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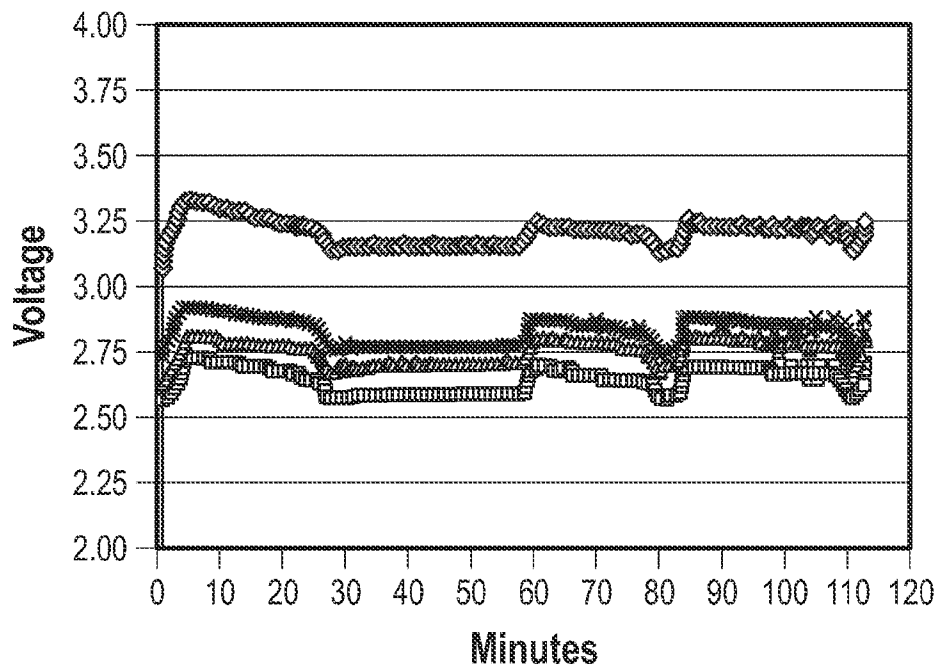


FIG. 4B

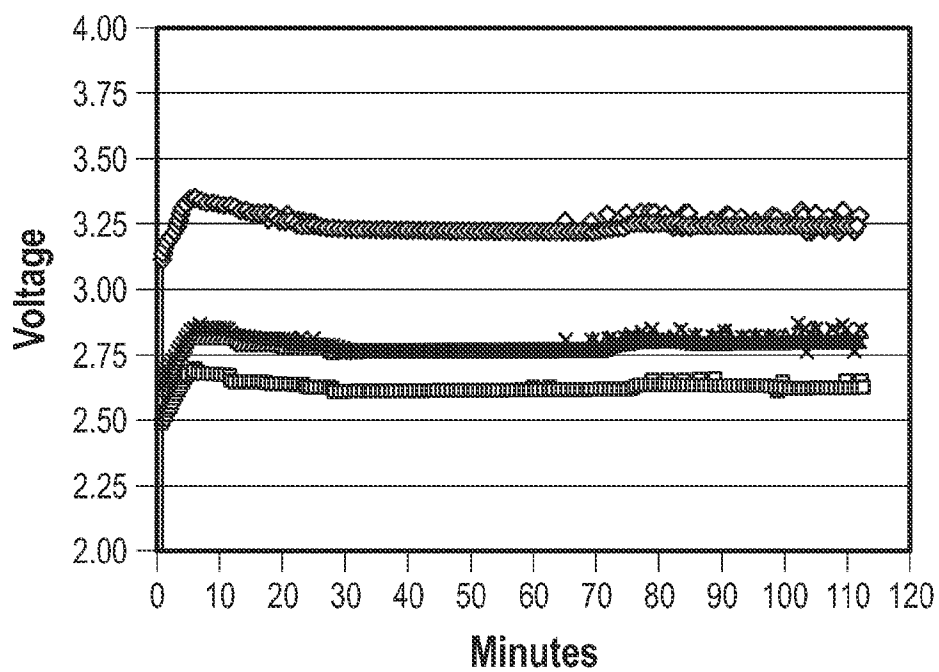


FIG. 4C

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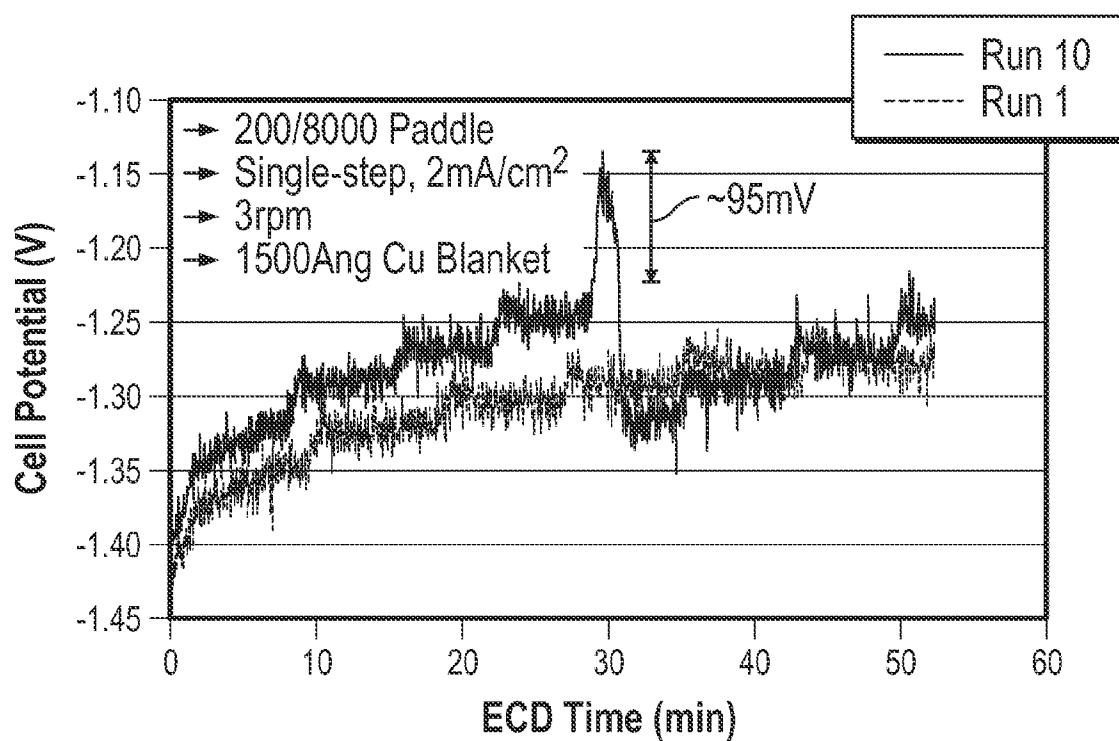


FIG. 5A

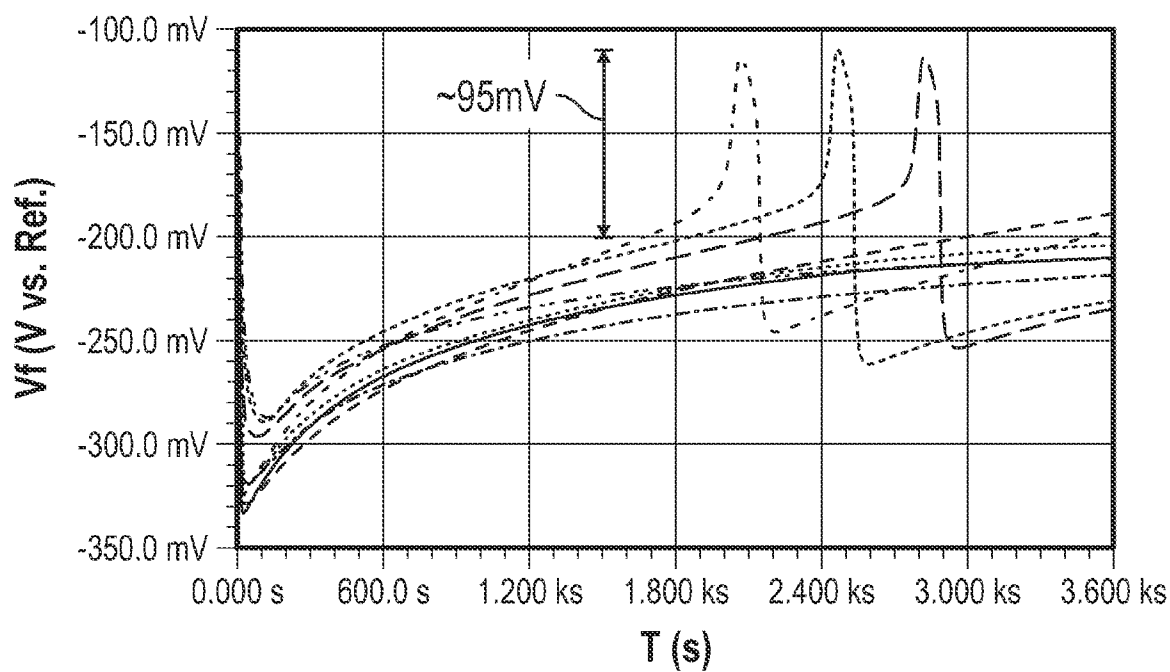


FIG. 5B

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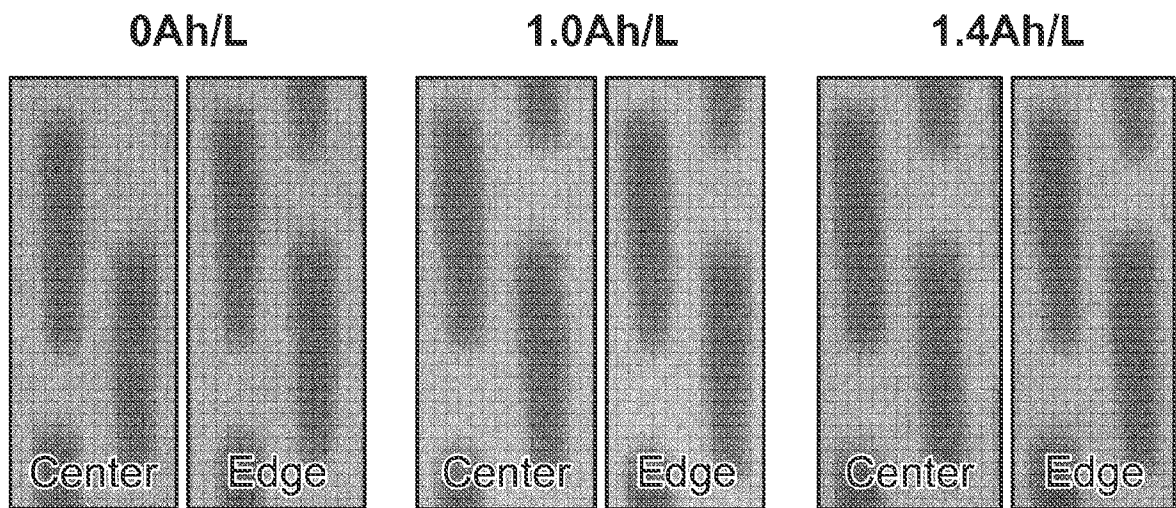


FIG. 6A

FIG. 6B

FIG. 6C

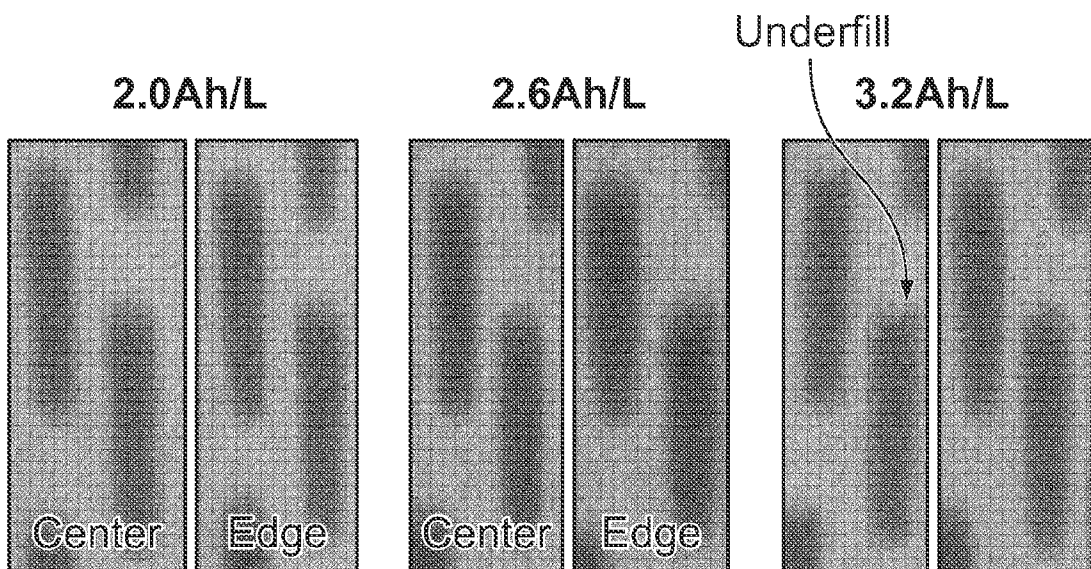


FIG. 6D

FIG. 6E

FIG. 6F

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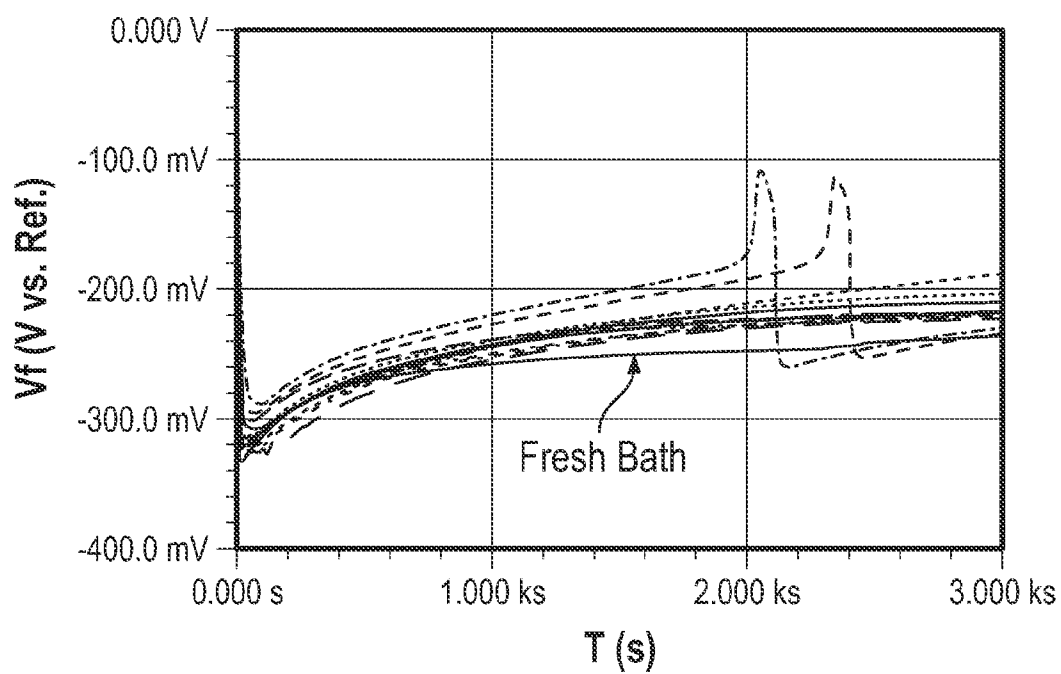


FIG. 6G

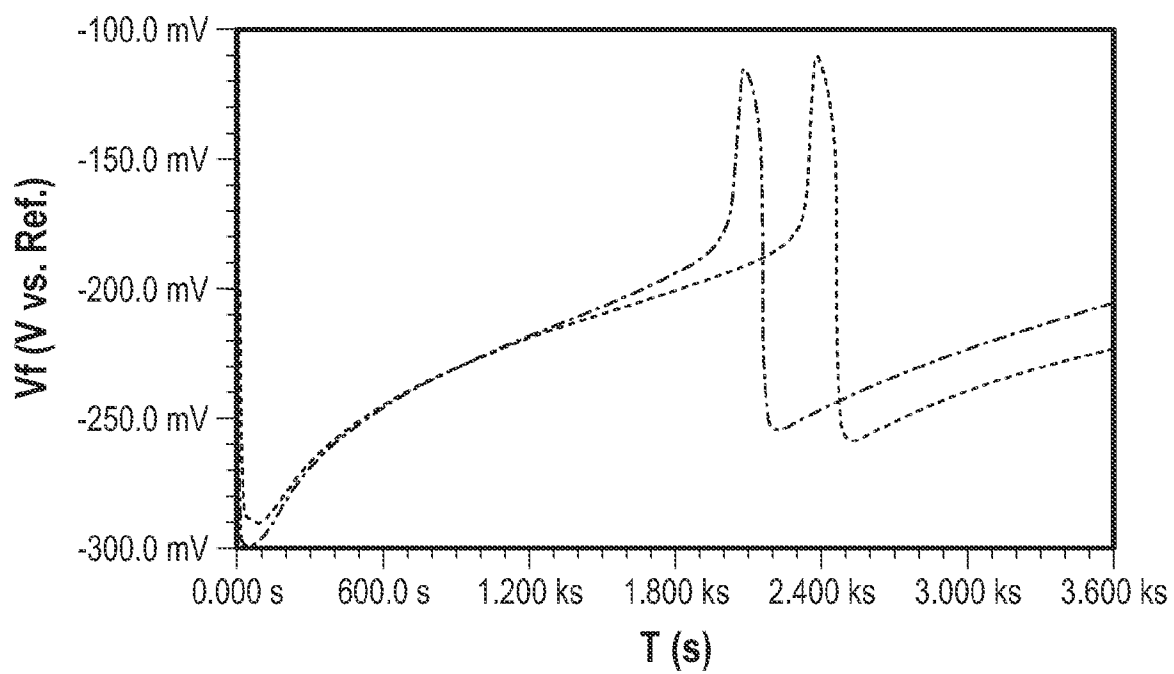


FIG. 7

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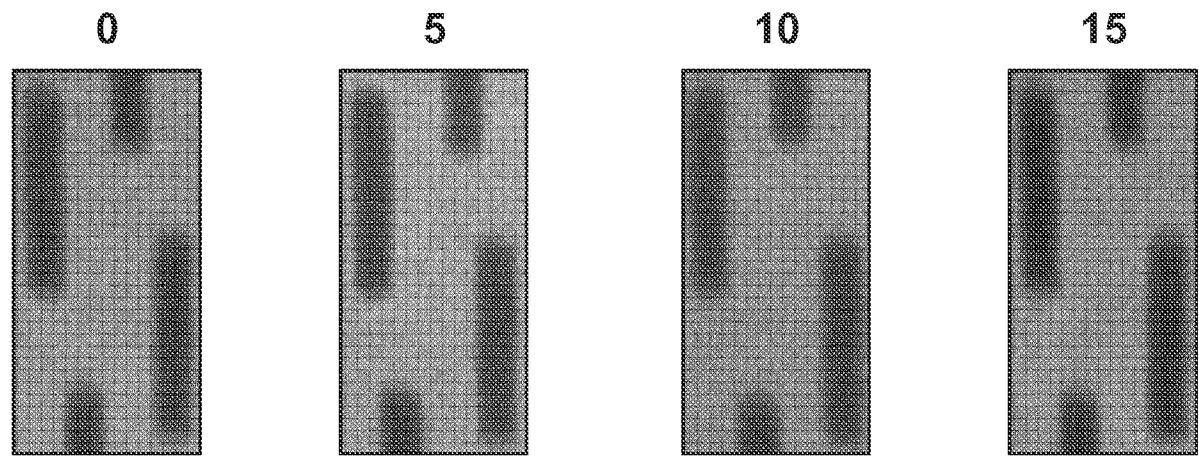


FIG. 8A

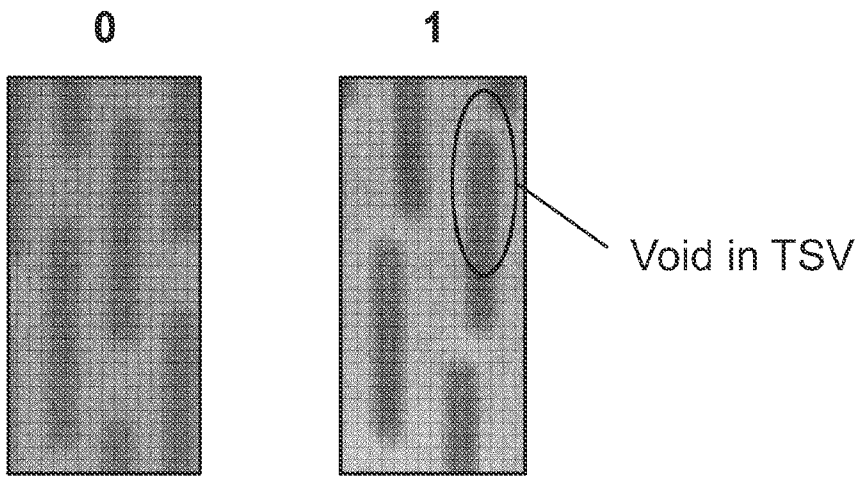


FIG. 8B

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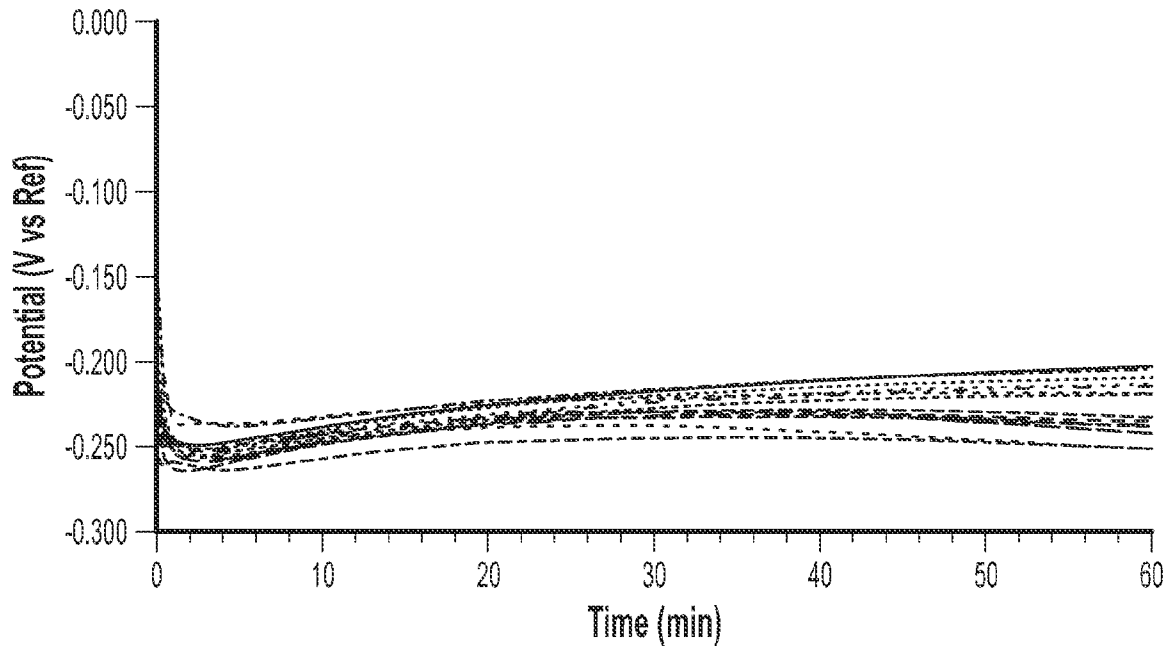


FIG. 9

Parameter	Old BKM	New BKM	Reasoning
Catholyte VMS	63.5/50/80	63.5/10/80	Improved Bath Stability
Anolyte VMS	63.5/pH=2/80		
Suppressor (A)	10 ml/L		
Accelerator (B)	5 ml/L	4 ml/L	Improved Accelerator Stability
Leveler (C3)	15 ml/L	7 ml/L	Lower Leveler = Reduced Fill Time
Temperature	25 C		
10x100 Recipe	68 min, 8-steps 114.8 amp-min	73 min, 14-steps 123.4 amp-min	Slight Decrease in Fill Rate Stabilized Field Suppression
Bleed and Feed	10% Daily		
Analysis Method	Onboard RTA		
Dosing	Feed Forward & Feed Back		
Consumption Rates	A: ~0.001 ml/min B: ~0.17 ml/A-min C3: ~0.30 ml/min	A: ~0.001 ml/min B: ~0.17 ml/A-min C3: ~0.30 ml/min	Improve Accelerator Stability 10x
Bath Life	<2.5 Ahr/L	>20.0 Ahr/L	Improved Stability
Chemistry Cost (85% util., 8 ECD Chambers)	~\$24.07/wafer	~\$4.99/wafer	Bath Life, Throughput, Accelerator Consumption

FIG. 10

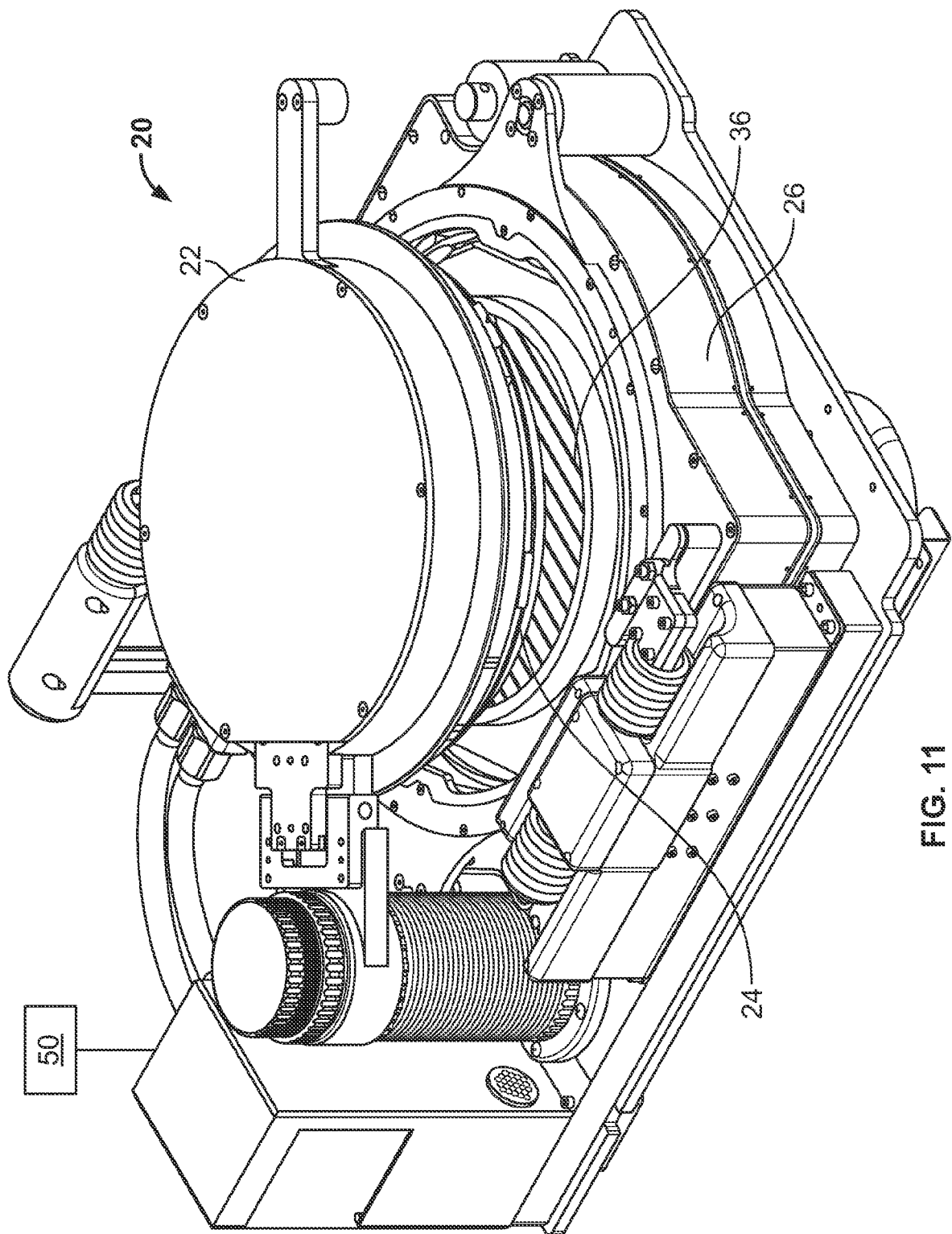
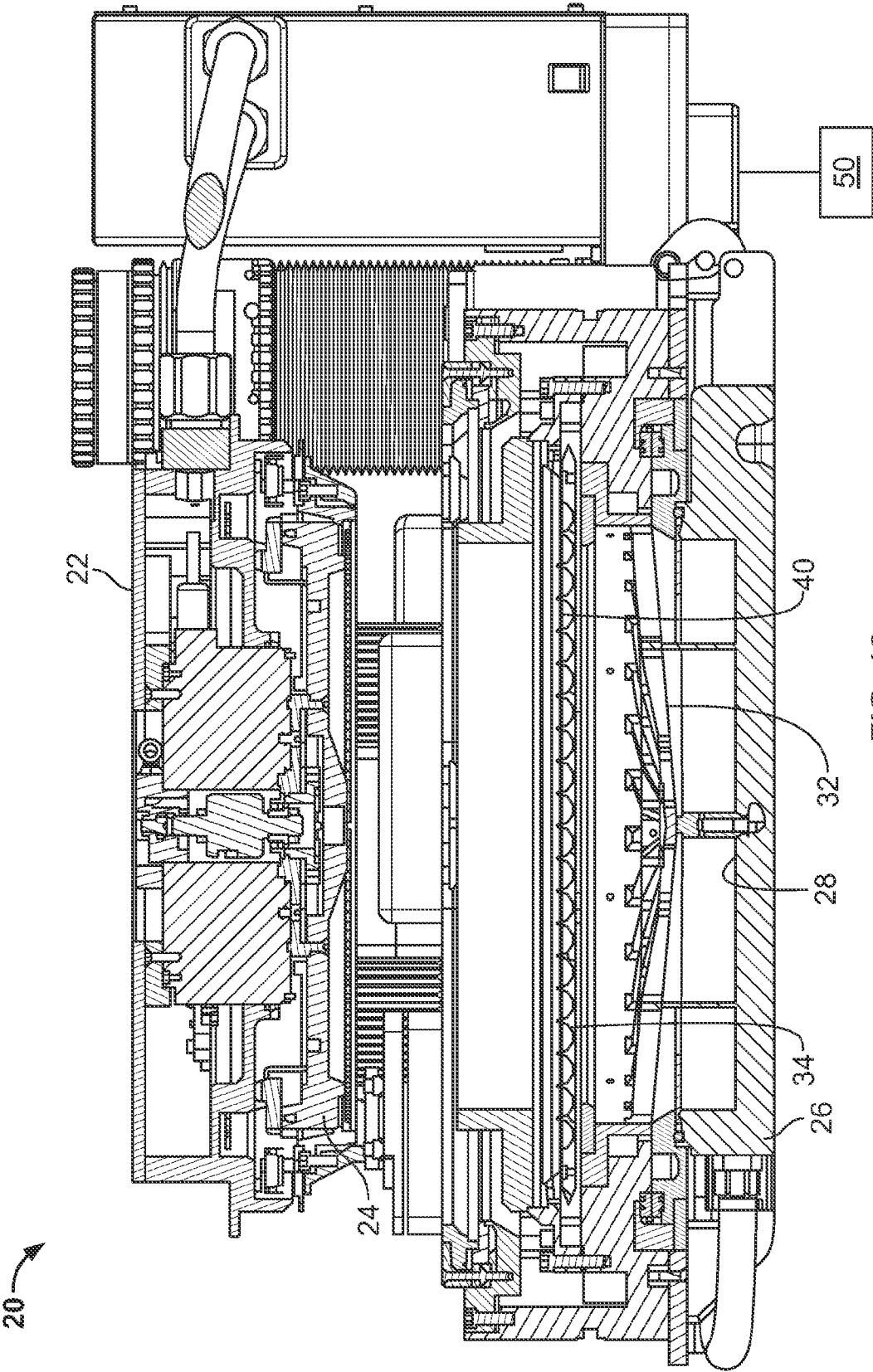


FIG. 11



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/015876**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/288(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/288; C25B 9/00; C25D 3/38; H01L 21/445; C25D 21/12; G01N 27/26; C25D 5/02; C25D 21/00; C25D 19/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: electroplating, failure, MPS, pulsing, ramping, current

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011-0284386 A1 (MARK J. WILLEY et al.) 24 November 2011 See paragraphs [0024], [0027], [0060]-[0067], [0084]-[0117], [0164]-[0183] and figures 1A-1C, 3A, 8	1-9
Y	WO 03-095715 A1 (UNIVERSITY OF SOUTHERN CALIFORNIA) 20 November 2003 See abstract, page 16, line 11 - page 18, lines 22 and figures 6(a), 6(c), 7(a).	1-3,5,8
Y	US 2003-0015433 A1 (HIDEKI TSUCHIDA et al.) 23 January 2003 See abstract, paragraphs [0067], [0087]-[0110] and figures 1-3.	4-9
A	US 2012-0024713 A1 (ROBERT F. PREISSER) 02 February 2012 See paragraphs [0033]-[0034], [0047]-[0073], [0179]-[0210] and figures 1-3.	1-9
A	US 2005-0247577 A1 (MICHAEL PAVLOV et al.) 10 November 2005 See abstract, paragraphs [0045]-[0052] and figures 1-4.	1-9
A	US 2007-0261963 A1 (JIANWEN HAN et al.) 15 November 2007 See abstract, paragraphs [0077]-[0114] and figures 1A-5.	1-9



Further documents are listed in the continuation of Box C.



See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search

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Information on patent family members

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