(19) **United States**
(12) **Patent Application Publication**
AKIMOTO

(10) **Pub. No.: US 2015/0340508 A1**
(43) **Pub. Date: Nov. 26, 2015**

(54) **SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME**

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(21) Appl. No.: **14/816,112**

(22) Filed: **Aug. 3, 2015**

Related U.S. Application Data

(62) Division of application No. 12/893,513, filed on Sep. 29, 2010, now Pat. No. 9,130,043.

(30) **Foreign Application Priority Data**

Oct. 1, 2009 (JP) 2009-229323

Publication Classification

(51) **Int. Cl.**

H01L 29/786	(2006.01)
H01L 29/423	(2006.01)
H01L 29/417	(2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/7869*** (2013.01); ***H01L 29/78603*** (2013.01); ***H01L 29/41733*** (2013.01); ***H01L 29/42384*** (2013.01)

(57) **ABSTRACT**

An object is to provide a method for manufacturing a highly reliable semiconductor device which includes a thin film transistor using an oxide semiconductor and having stable electric characteristics. In manufacture of a semiconductor device in which an oxide semiconductor is used for a channel formation region, after an oxide semiconductor film is formed, a conductive film including a metal, a metal compound, or an alloy that can absorb or adsorb moisture, a hydroxy group, or hydrogen is formed to overlap with the oxide semiconductor film with an insulating film provided therebetween. Then, heat treatment is performed in the state where the conductive film is exposed; in such a manner, activation treatment for removing moisture, oxygen, hydrogen, or the like adsorbed onto a surface of or in the conductive film is performed.

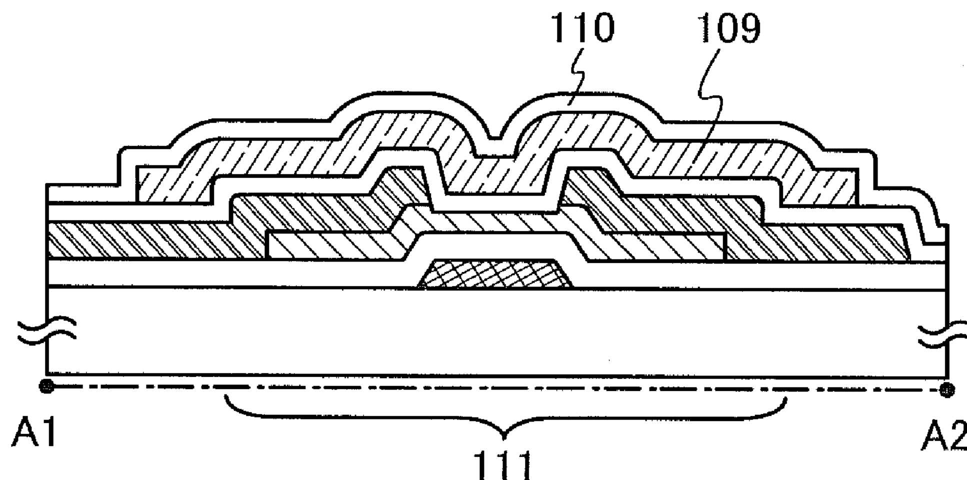


FIG. 1A

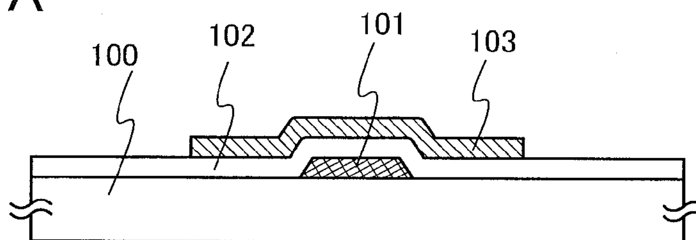


FIG. 1B

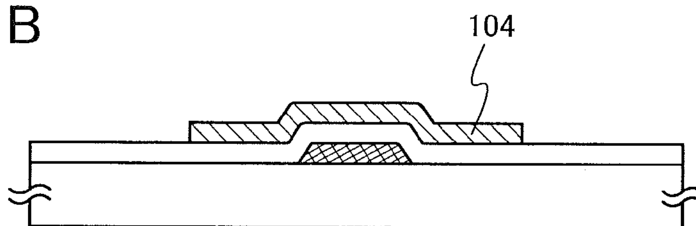


FIG. 1C

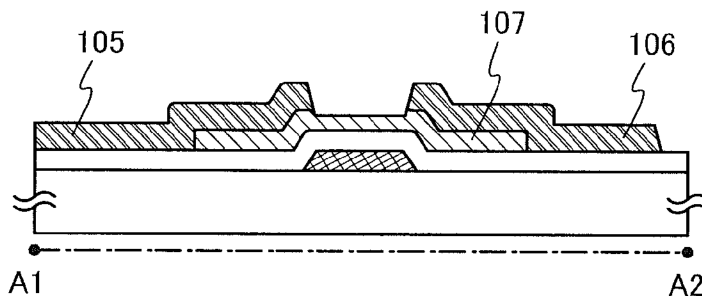


FIG. 1D

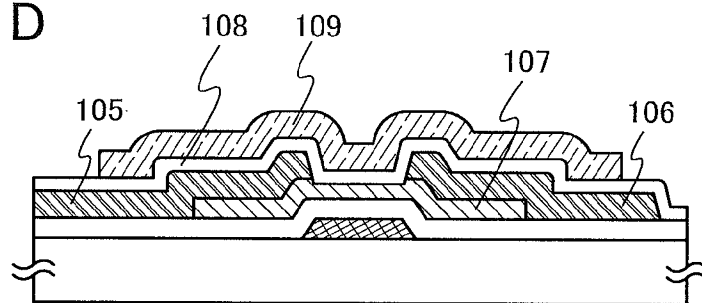


FIG. 1E

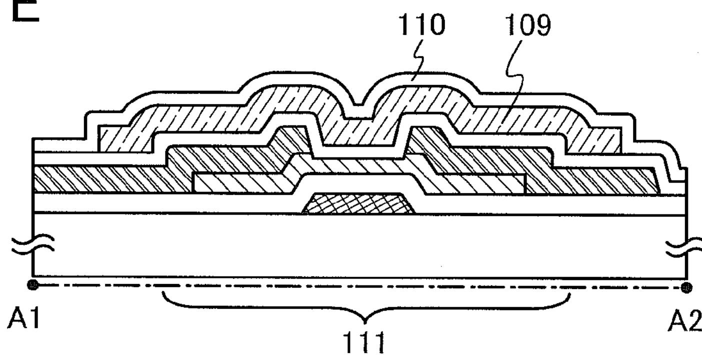


FIG. 2A

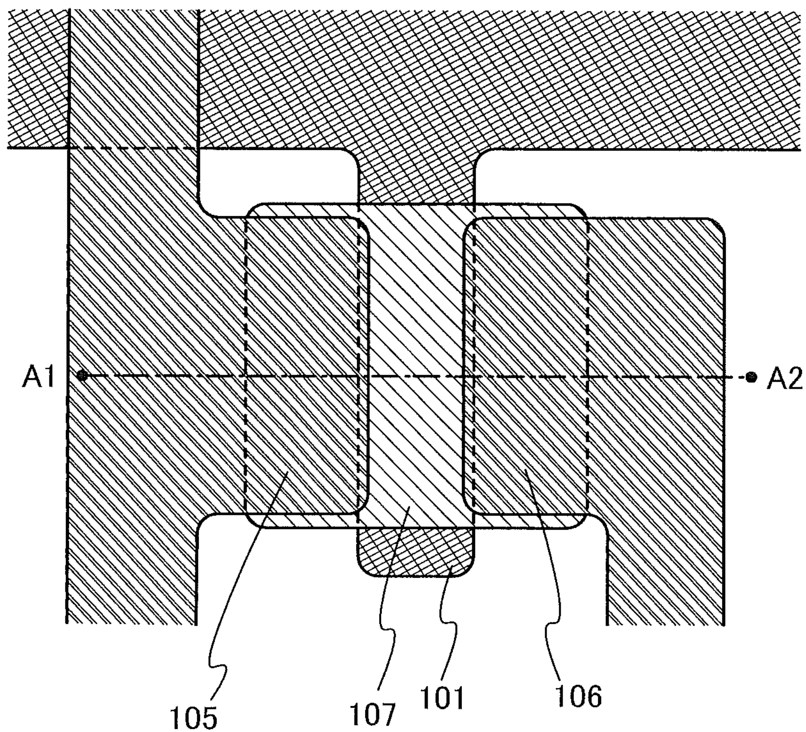


FIG. 2B

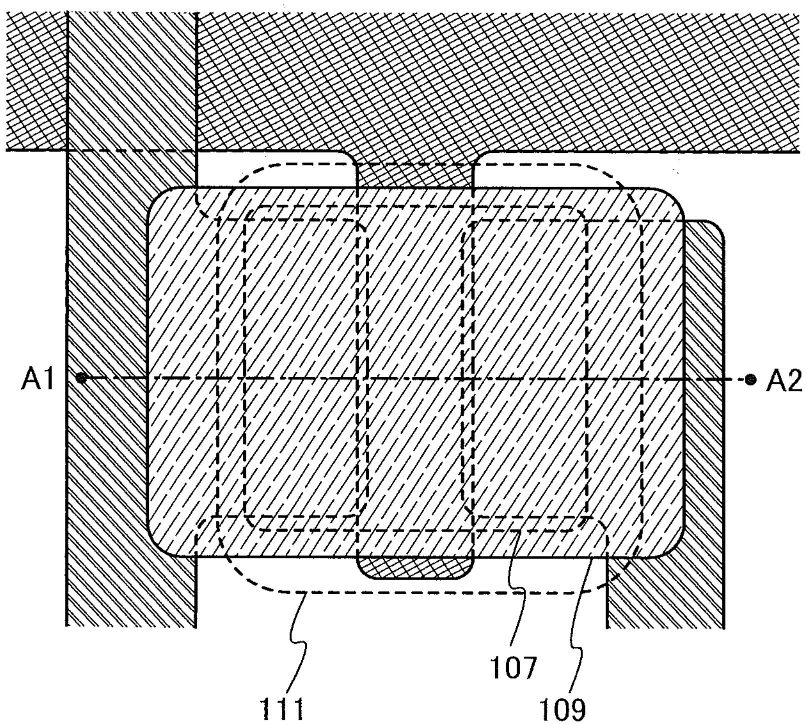


FIG. 3A

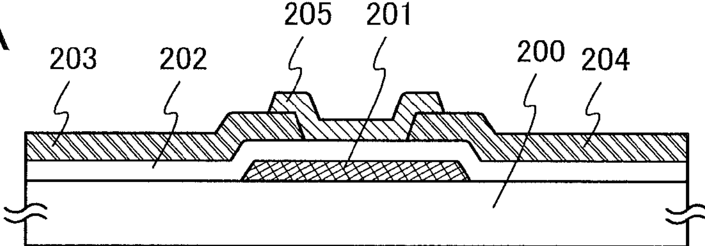


FIG. 3B

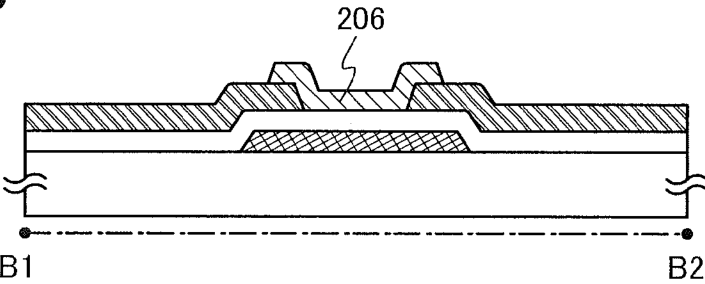


FIG. 3C

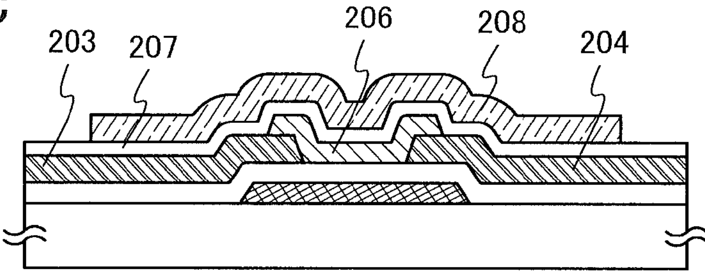


FIG. 3D

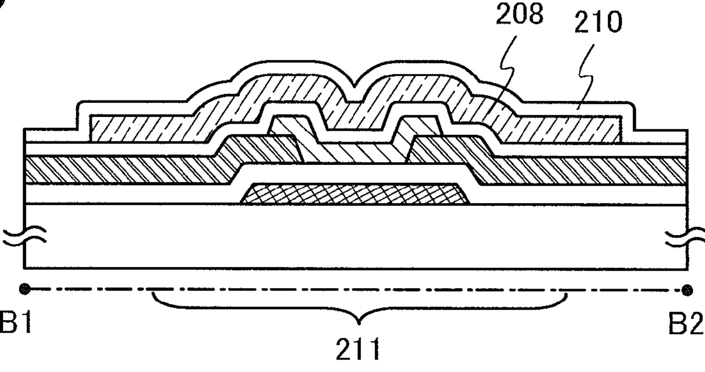


FIG. 4A

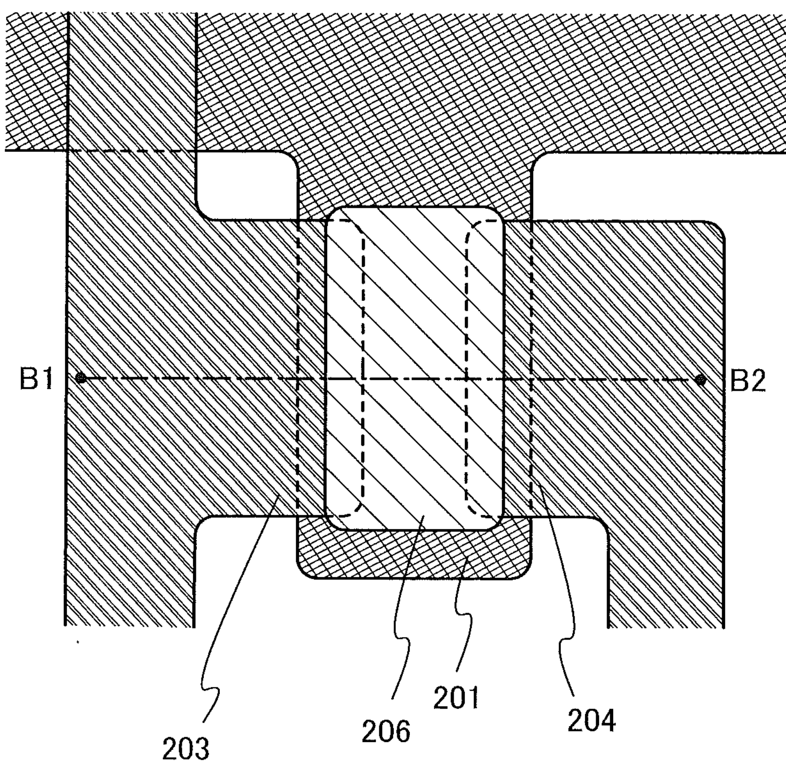


FIG. 4B

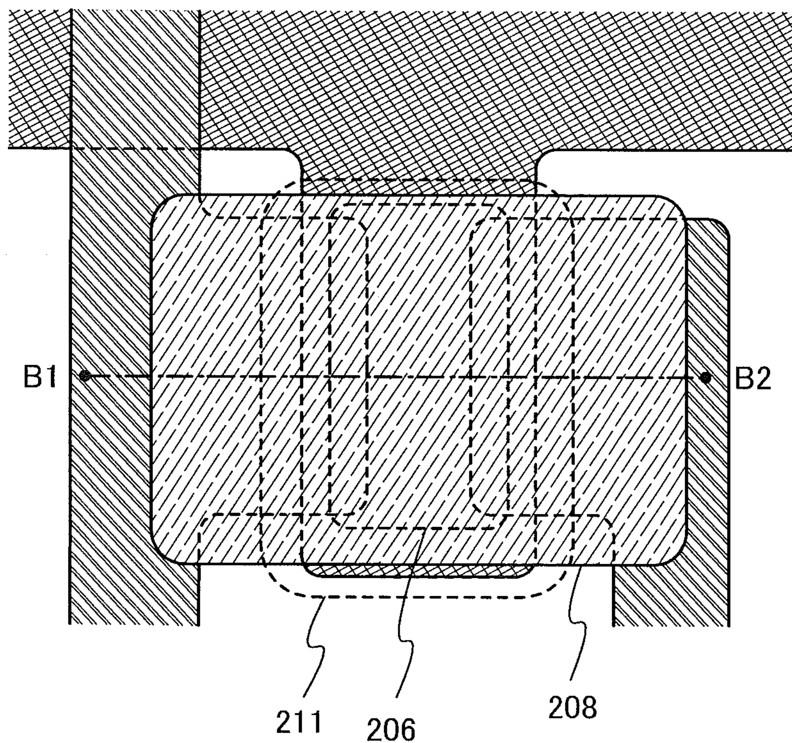


FIG. 5A

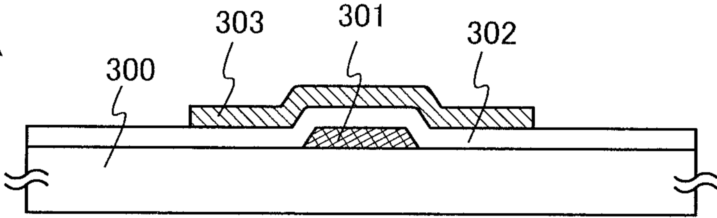


FIG. 5B

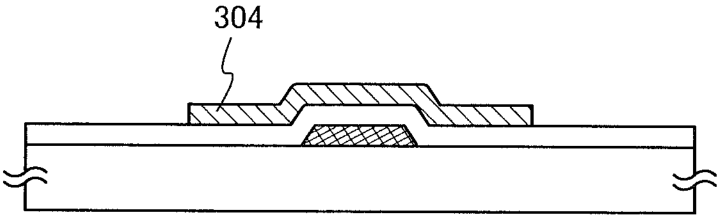


FIG. 5C

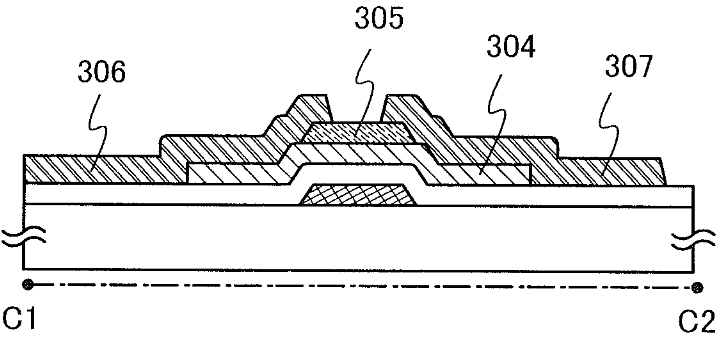


FIG. 5D

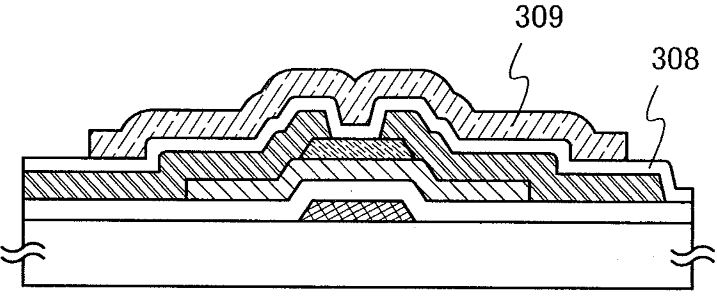


FIG. 5E

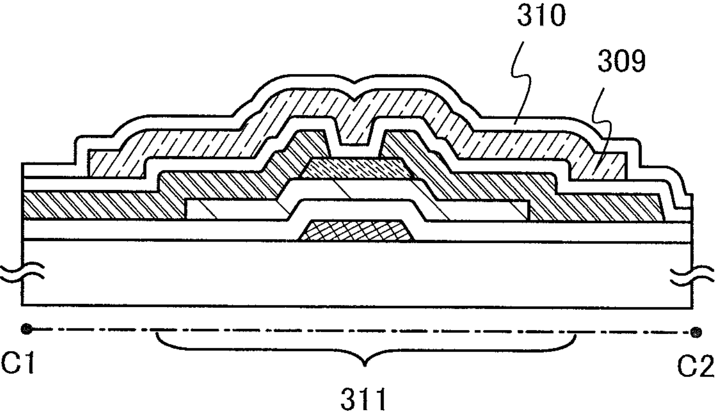


FIG. 6A

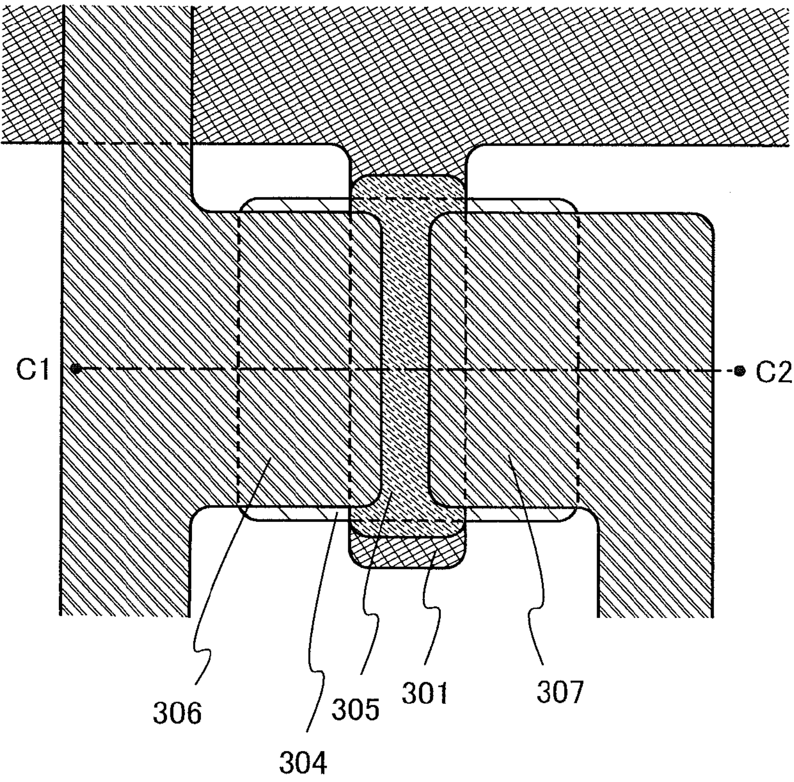
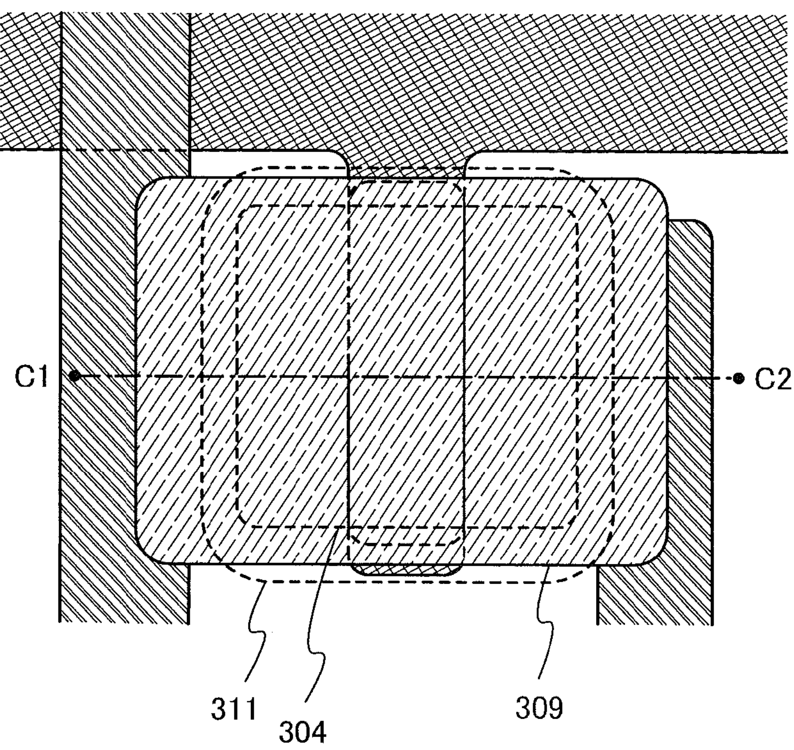


FIG. 6B



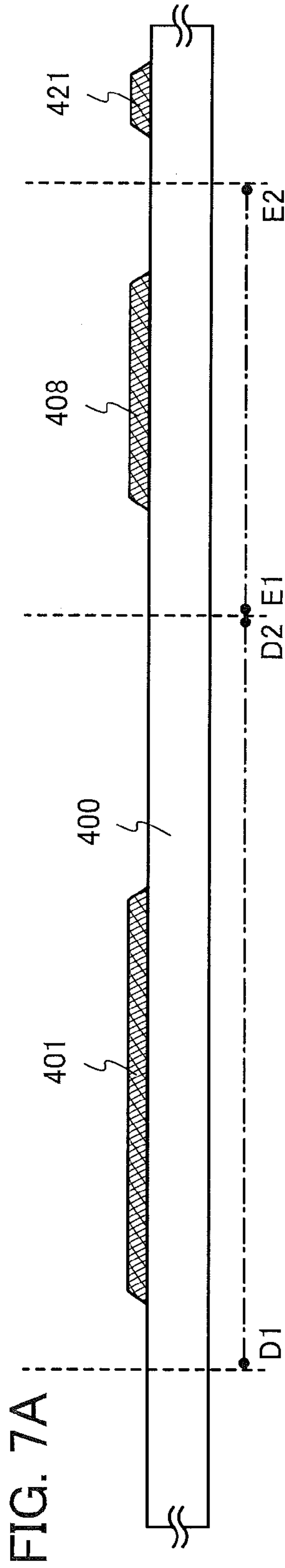


FIG. 7A
421
408
400
401
D1
D2
E1
E2

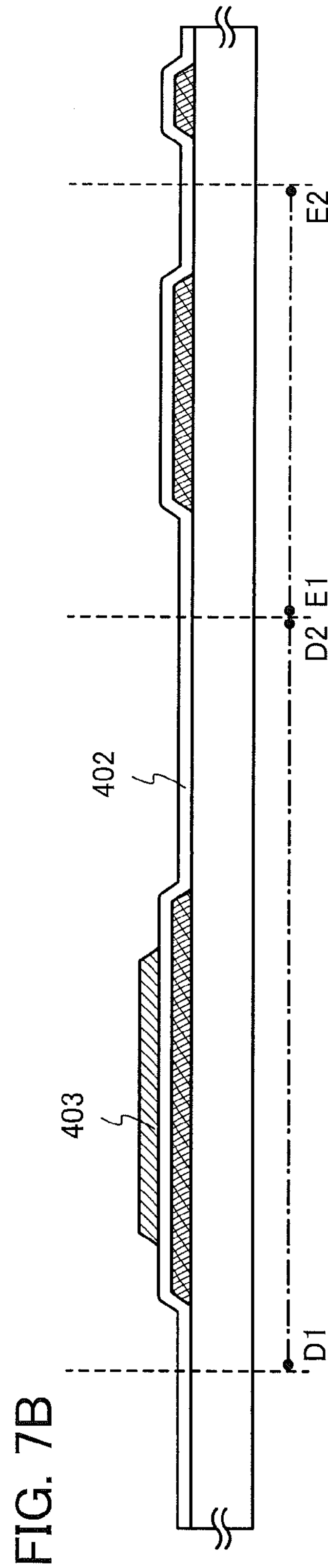


FIG. 7B
402
403
D1
D2
E1
E2

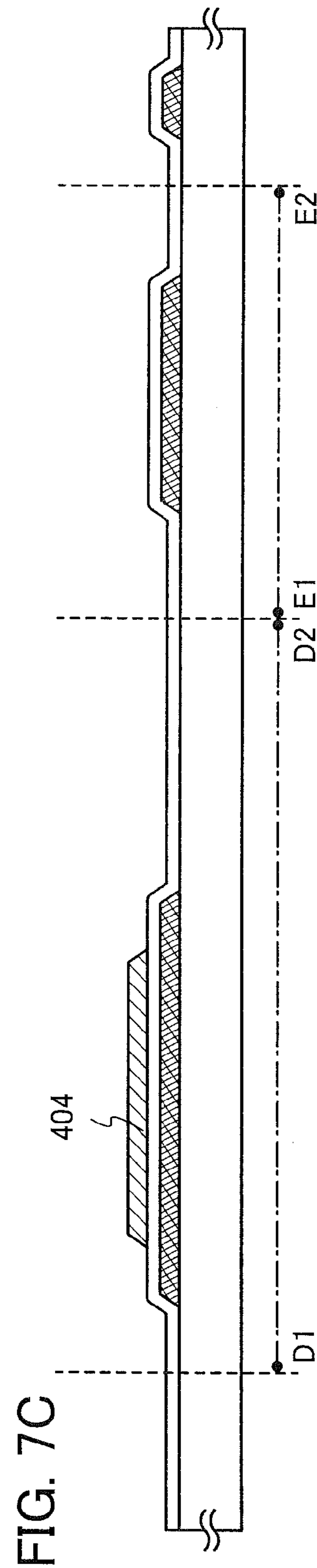


FIG. 7C
404
D1
D2
E1
E2

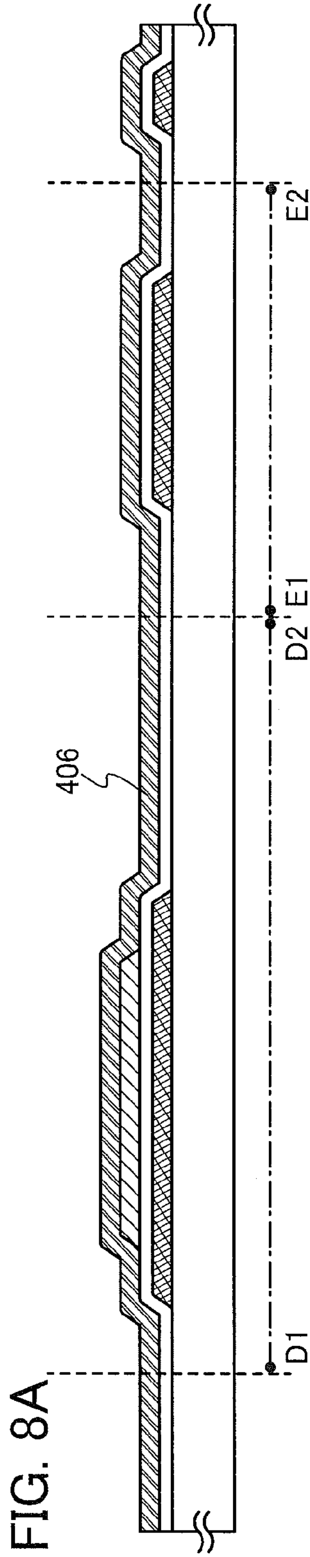


FIG. 8A
406
D1
D2
E1
E2

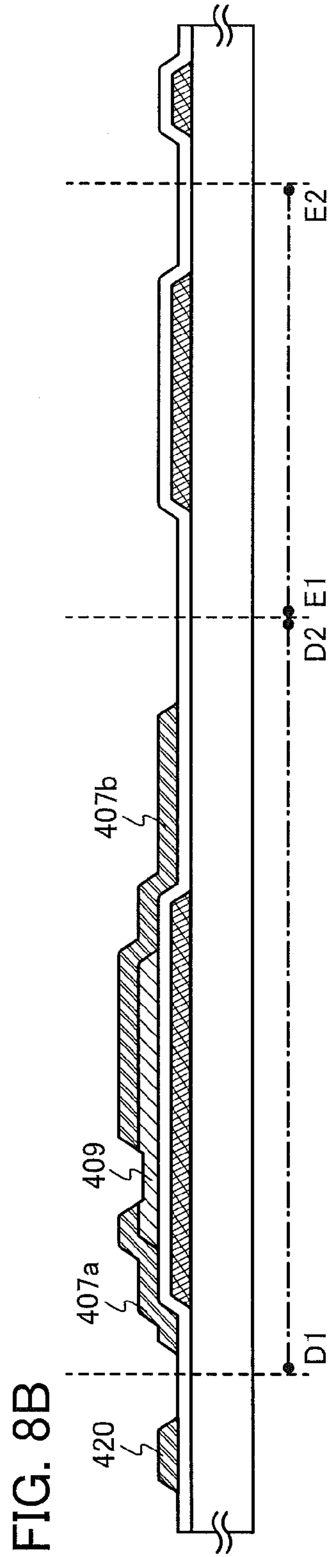


FIG. 8B
420
407a
409
407b
D1
D2
E1
E2

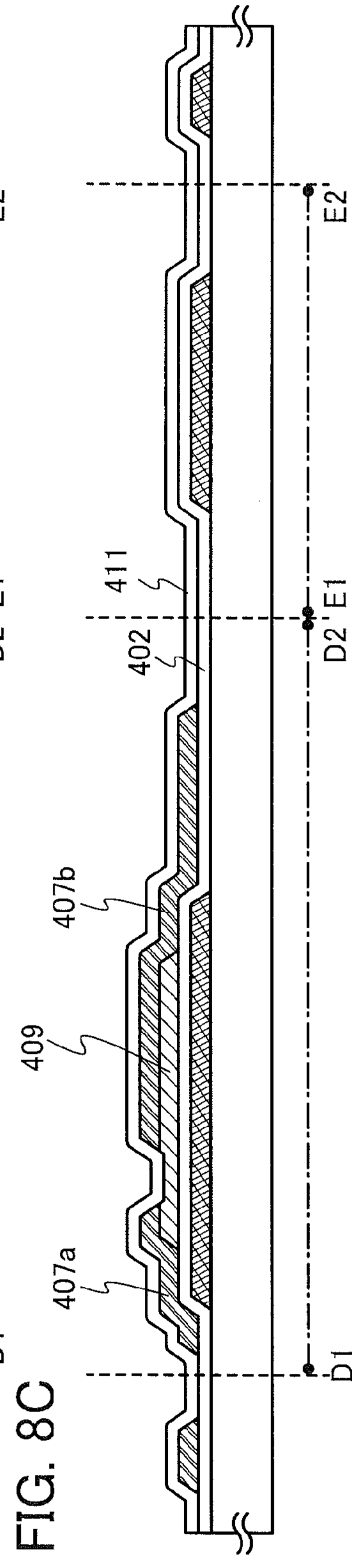


FIG. 8C
407a
409
407b
402
411
D1
D2
E1
E2

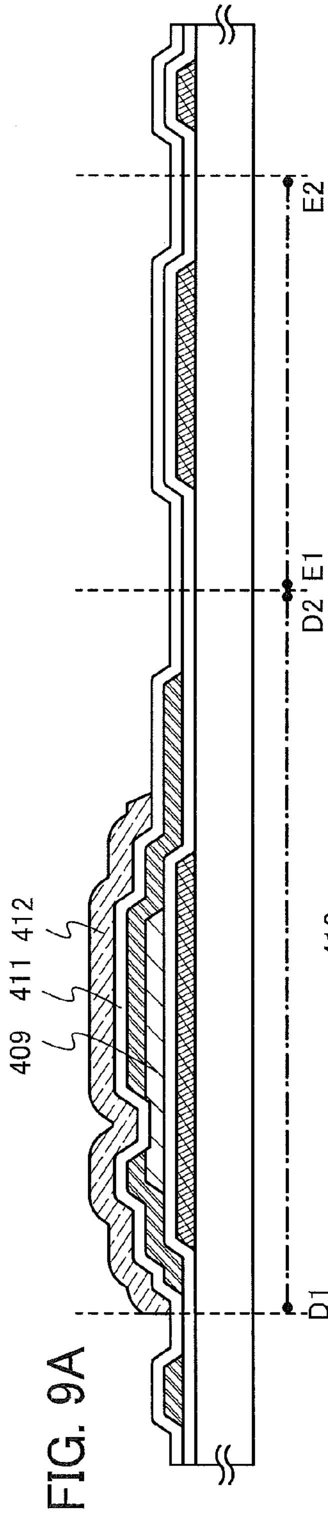


FIG. 9A

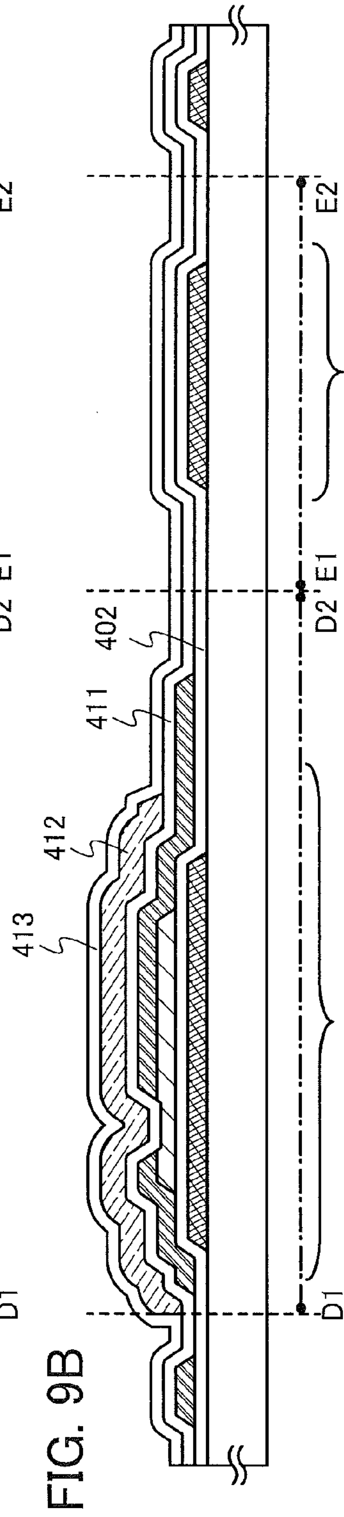


FIG. 9B

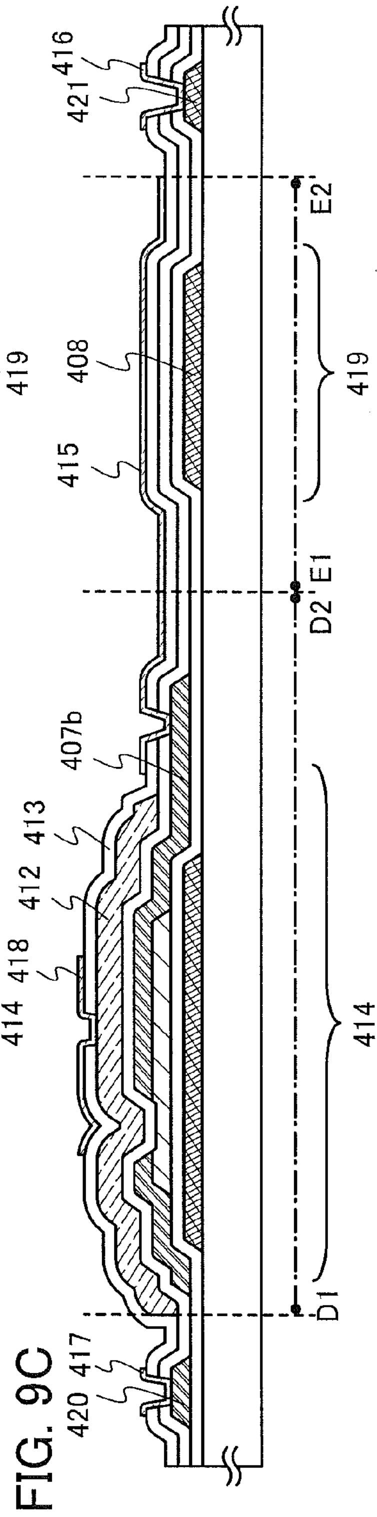


FIG. 9C

FIG. 10

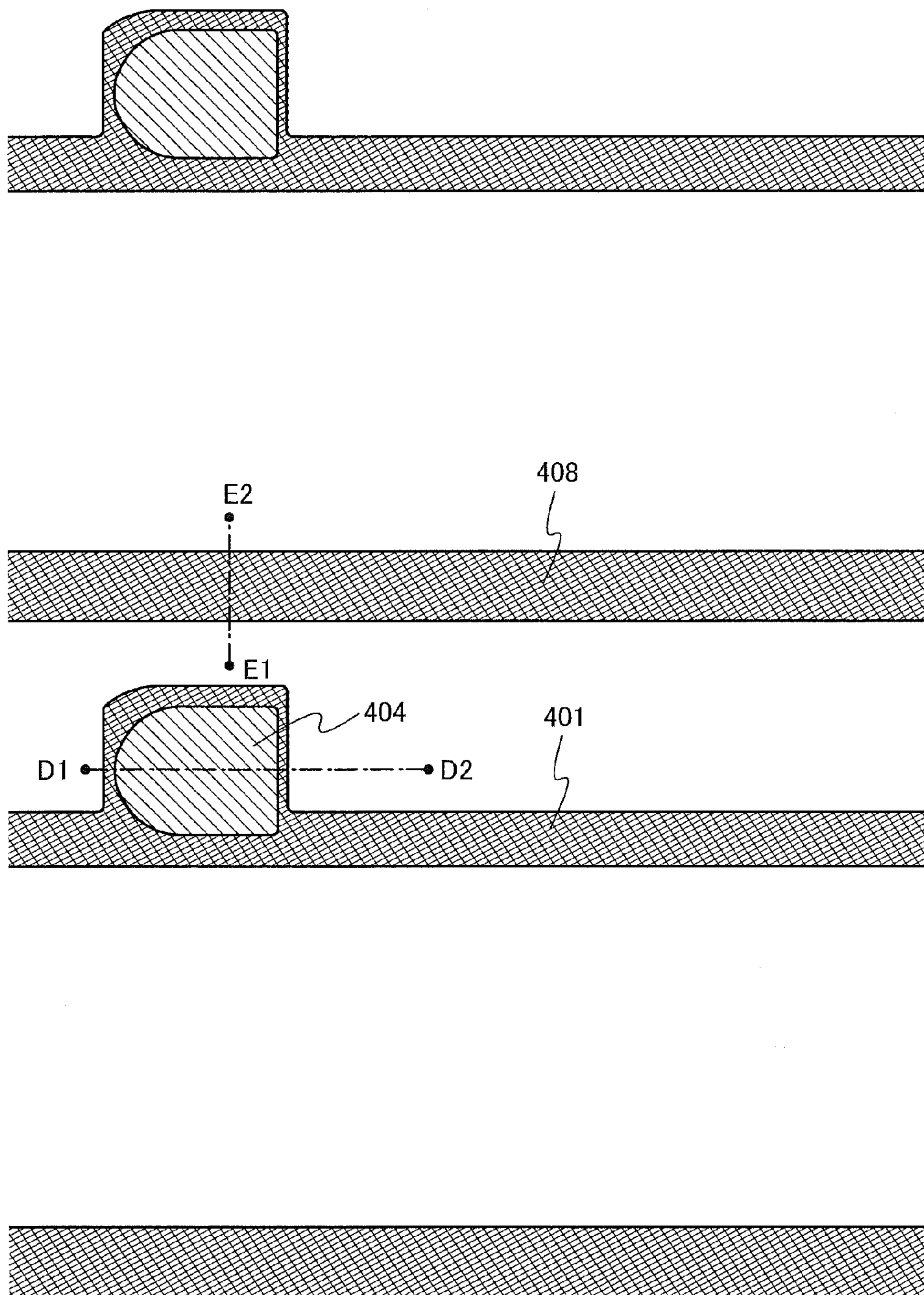


FIG. 11

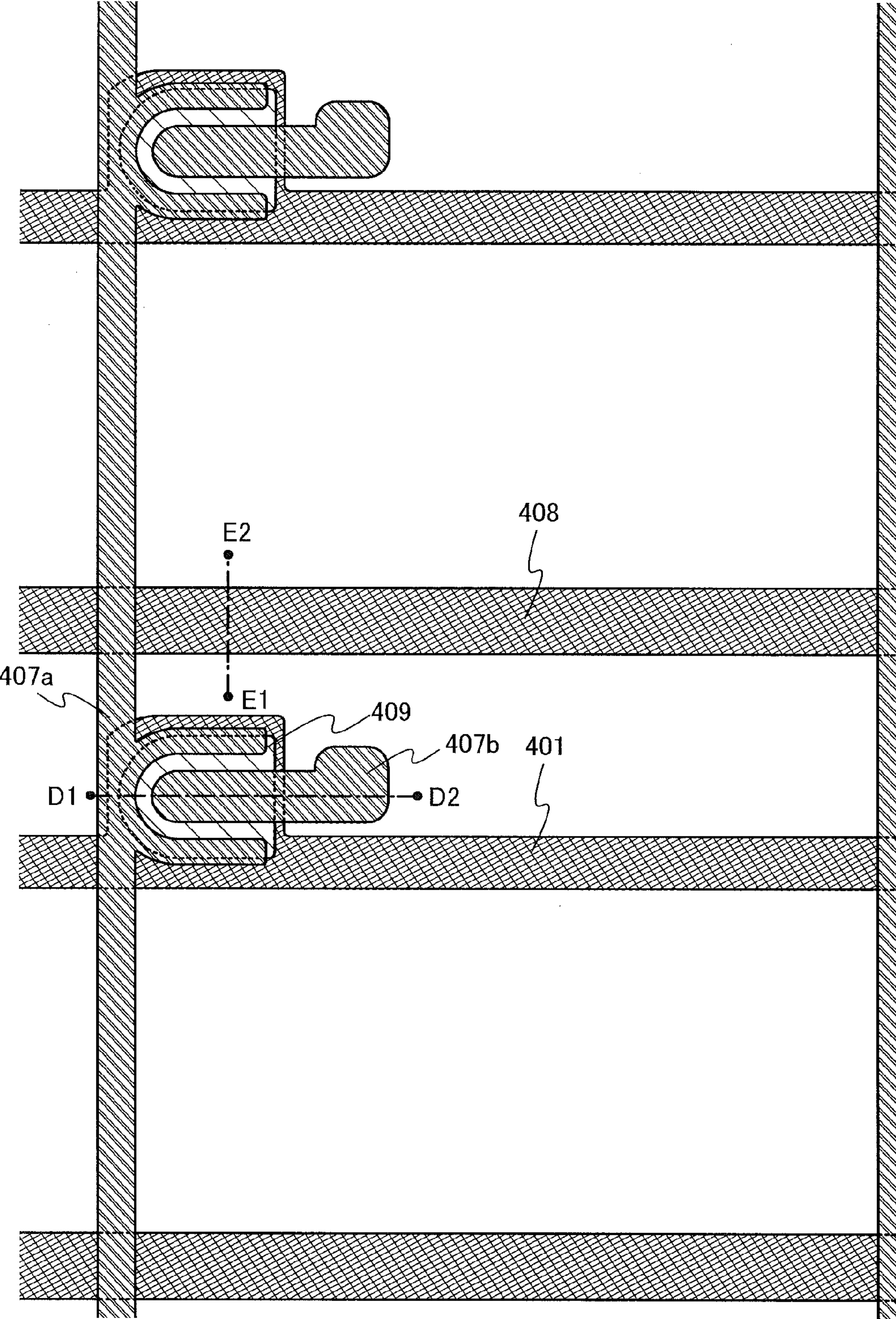


FIG. 12

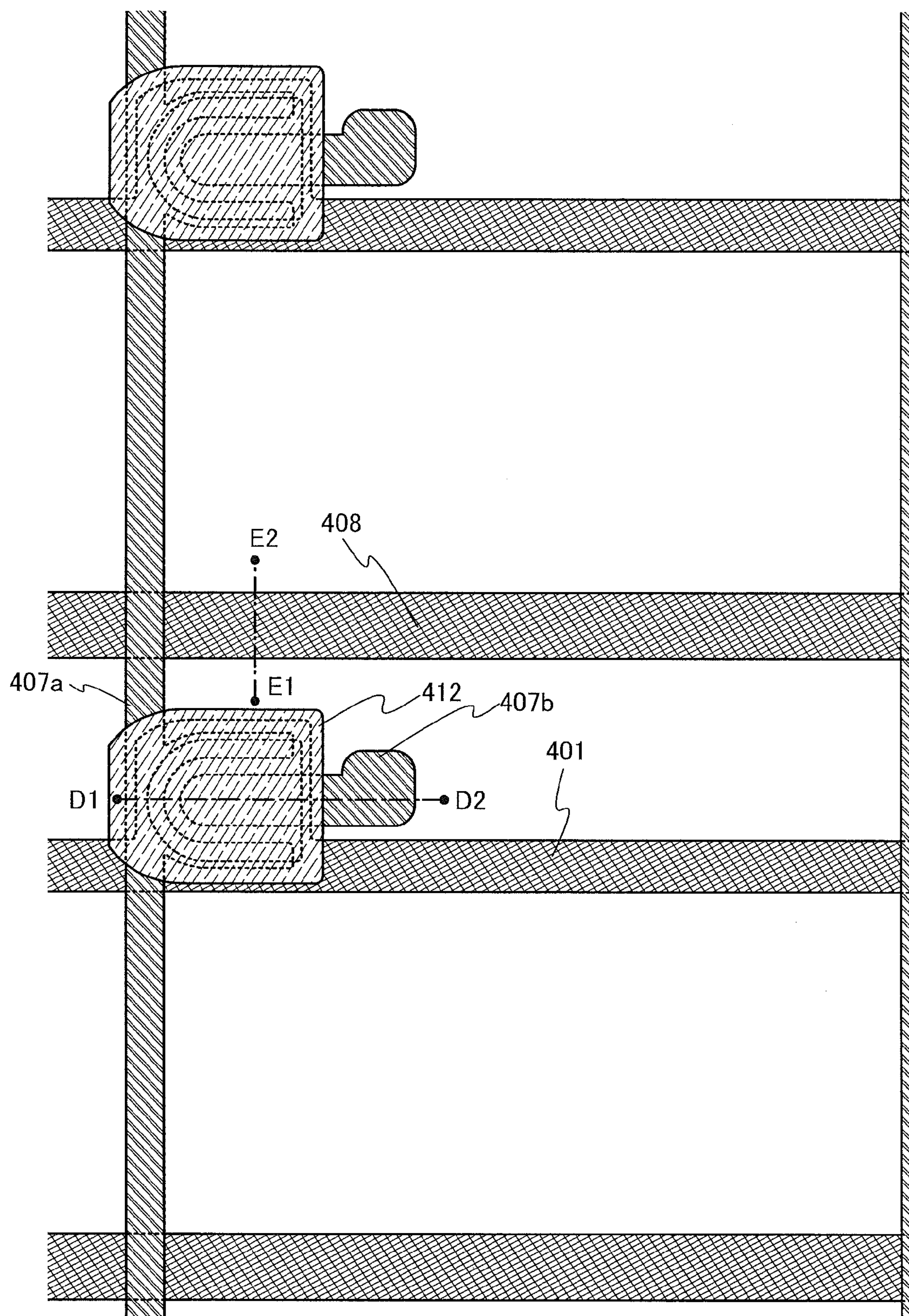
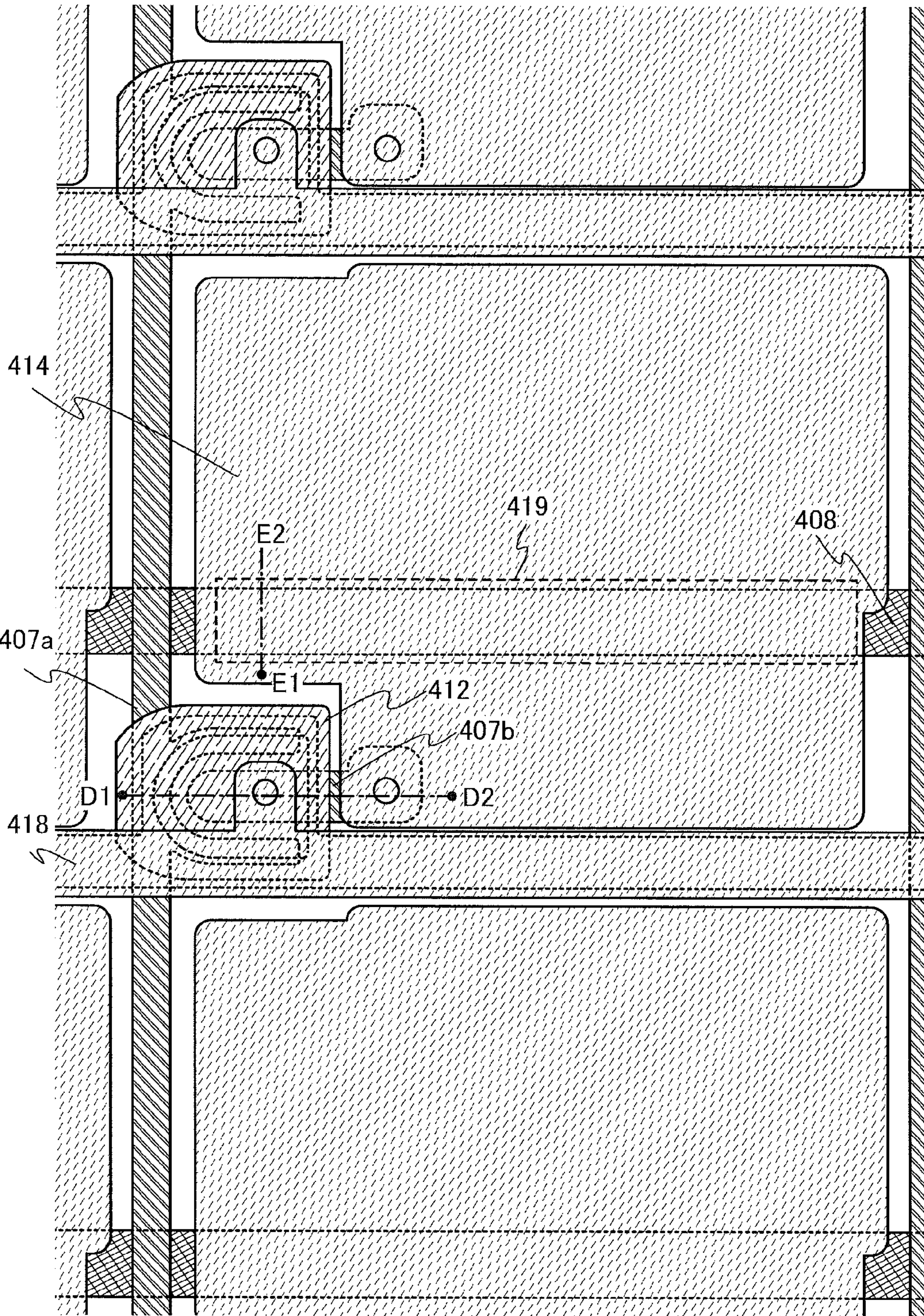


FIG. 13



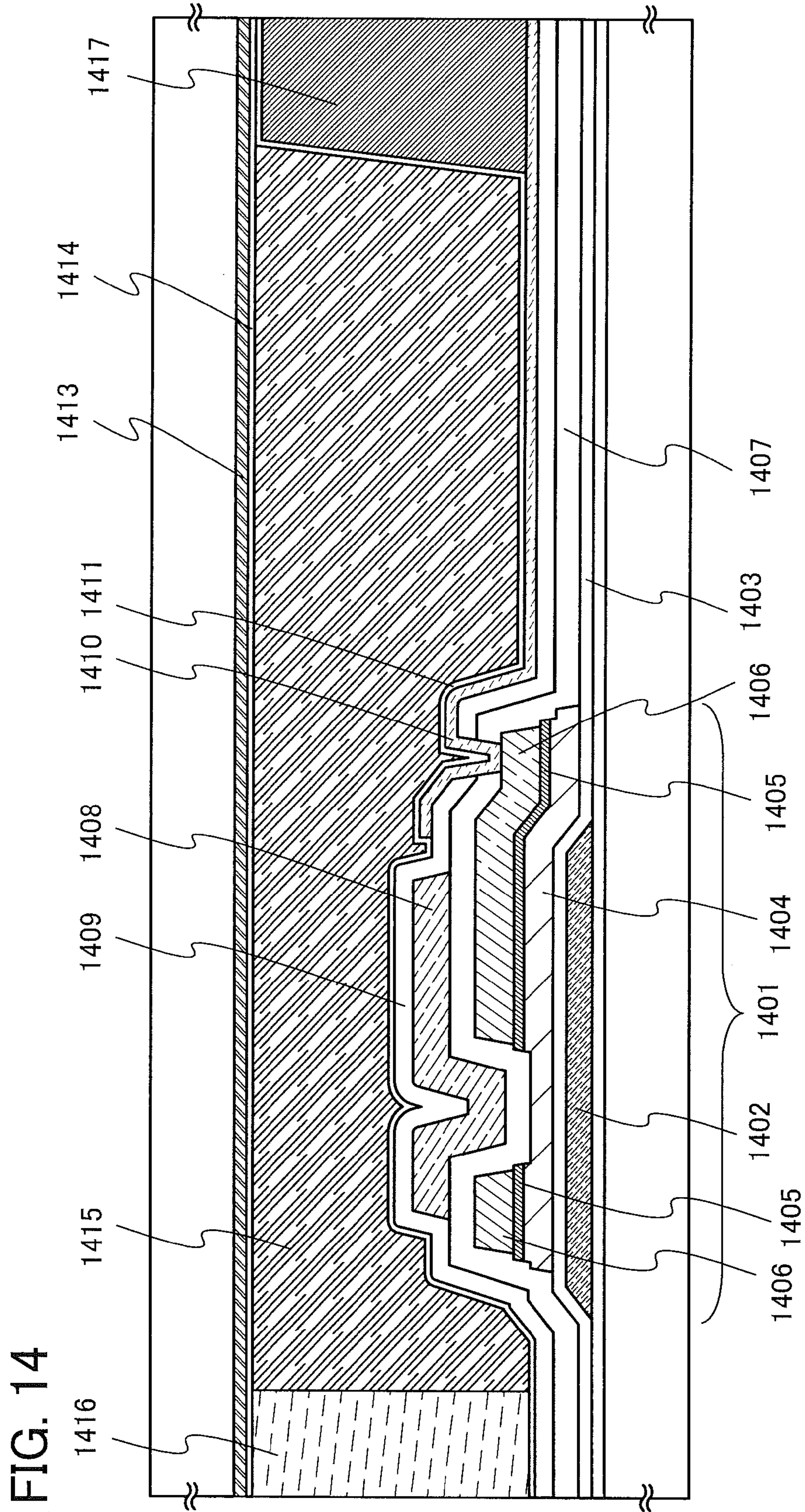


FIG. 14
1417
1414
1413
1410 1411
1408
1409
1415
1416
1407
1403
1406
1405
1404
1401
1402
1405
1406

FIG. 15A

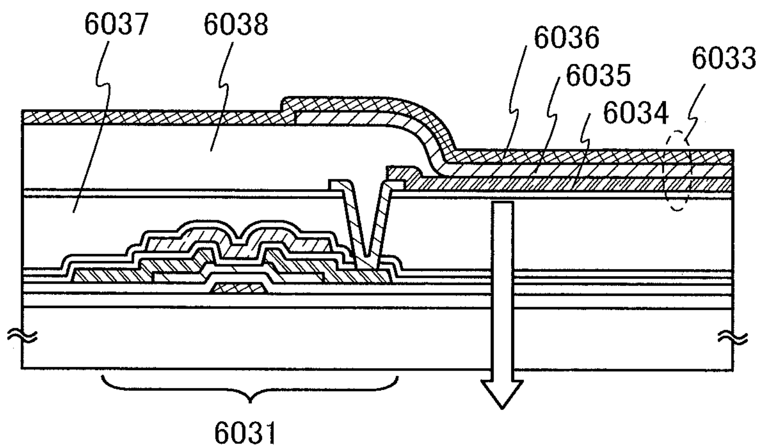


FIG.15B

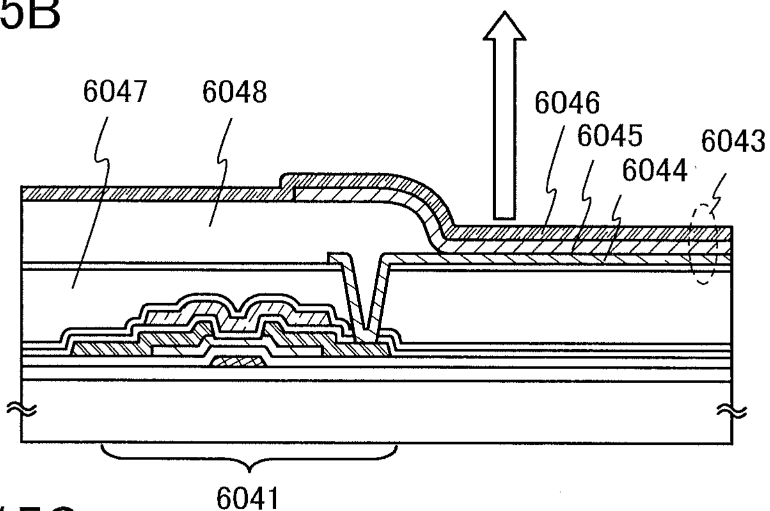


FIG. 15C

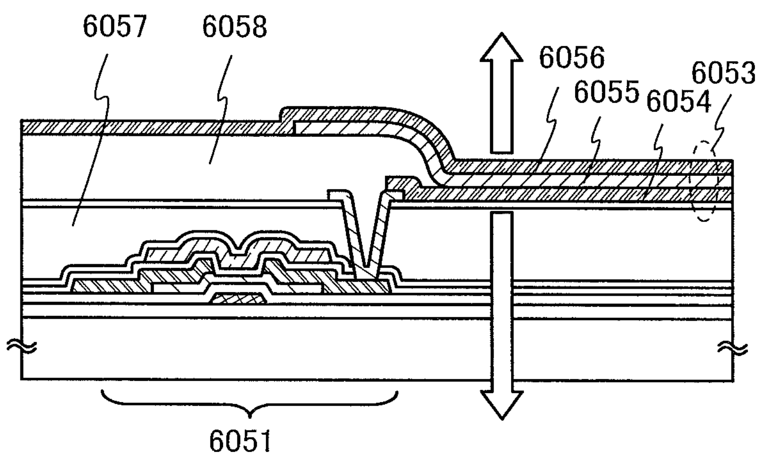


FIG. 16

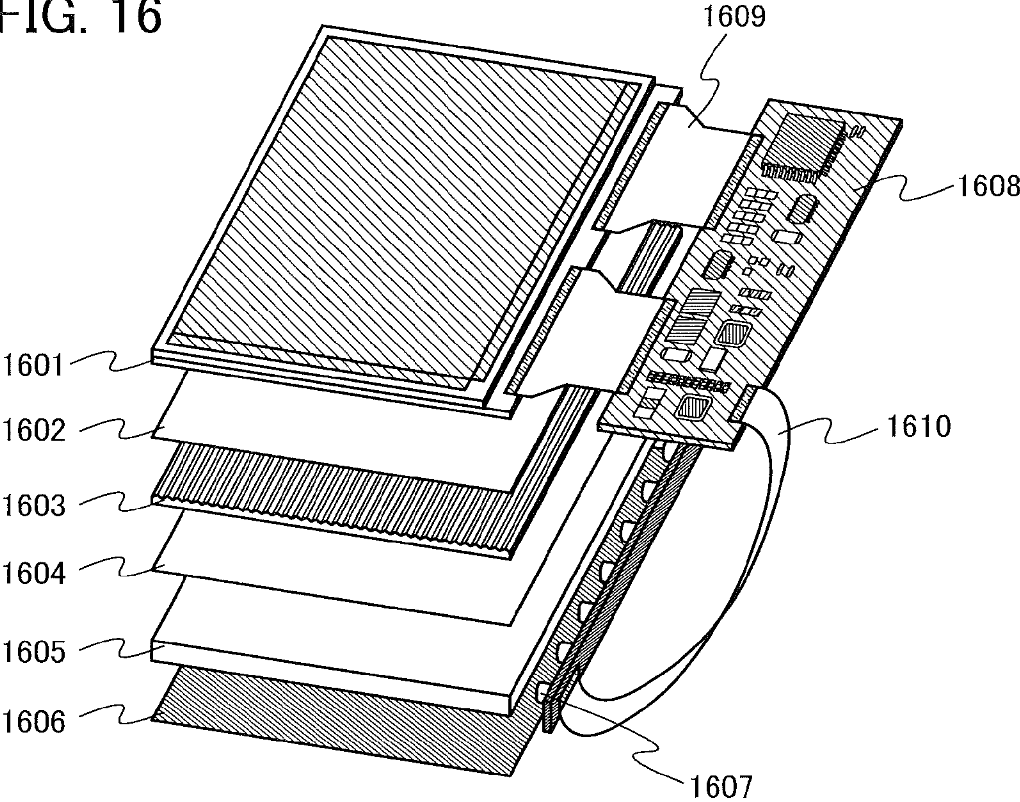


FIG. 17A

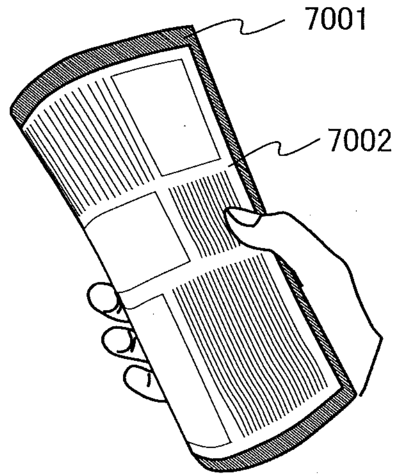


FIG. 17B

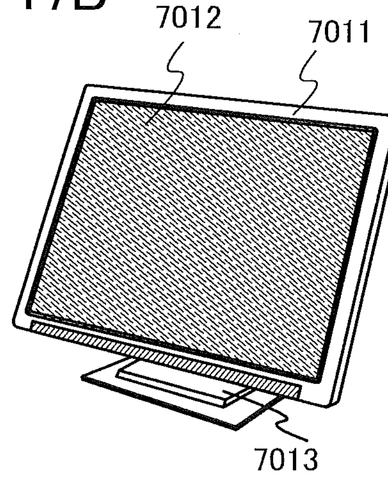


FIG. 17C

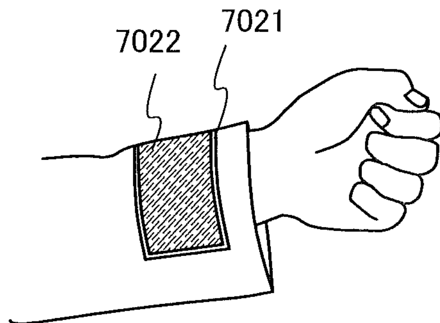


FIG. 17D

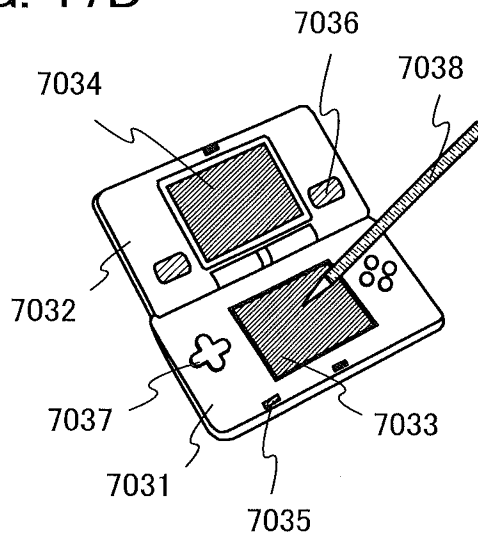
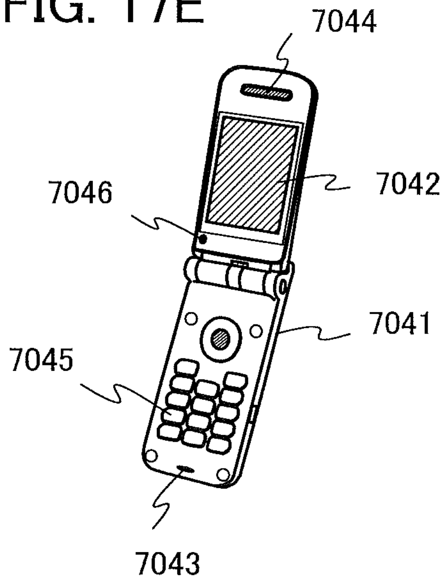


FIG. 17E



SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. application Ser. No. 12/893,513, filed Sep. 29, 2010, now allowed, which claims the benefit of a foreign priority application filed in Japan as Serial No. 2009-229323 on Oct. 1, 2009, both of which are incorporated by reference.

TECHNICAL FIELD

[0002] The present invention relates to a semiconductor device including an oxide semiconductor and a manufacturing method thereof.

BACKGROUND ART

[0003] A thin film transistor in which a semiconductor film is formed on an insulating surface is a semiconductor element that is essential to a flat panel display such as a liquid crystal display device or a light-emitting device and a semiconductor device such as an IC. Since there is limitation on manufacture of a thin film transistor in terms of allowable temperature limit of a substrate, a thin film transistor in which amorphous silicon that can be deposited at relatively low temperature, polysilicon that can be obtained by crystallization with use of laser light or a catalytic element, or the like is included in an active layer is mainly used for a semiconductor display device.

[0004] In recent years, as a novel semiconductor material which has a mobility as high as polysilicon and realizes such uniform element characteristics as are obtained with the use of amorphous silicon, a metal oxide having semiconductor characteristics which is called an oxide semiconductor has attracted attention. A metal oxide is used for various applications. For example, indium oxide is a well-known metal oxide and used as a transparent electrode material included in a liquid crystal display device or the like. Examples of such metal oxides having semiconductor characteristics include tungsten oxide, tin oxide, indium oxide, and zinc oxide. Thin film transistors including such metal oxide having semiconductor characteristics in its channel formation region have been proposed (Patent Documents 1 to 4 and Non-Patent Document 1).

[0005] As metal oxides, multi-component oxides as well as single-component oxides are known. For example, $InGaO_3(ZnO)_m$ (m: natural number) having a homologous series is known as a multi-component oxide semiconductor including In, Ga, and Zn (Non-Patent Documents 2 to 4). Furthermore, it is confirmed that an oxide semiconductor including such an In—Ga—Zn-based oxide is applicable to a channel layer of a thin film transistor (Patent Document 5, Non-Patent Documents 5 and 6).

REFERENCE

Patent Document

[0006] [Patent Document 1] Japanese Published Patent Application No. S60-198861

[0007] [Patent Document 2] Japanese Published Patent Application No. H8-264794

[0008] [Patent Document 3] Japanese Translation of PCT International Application No. H11-505377

[0009] [Patent Document 4] Japanese Published Patent Application No. 2000-150900

[0010] [Patent Document 5] Japanese Published Patent Application No. 2004-103957

Non-Patent Document

[0011] [Non-Patent Document 1] M. W. Prins, K. O. Grosse-Holz, G Muller, J. F. M. Cillessen, J. B. Giesbers, R. P. Weening, and R. M. Wolf, "A ferroelectric transparent thin-film transistor", *Appl. Phys. Lett.,* 17 Jun. 1996, Vol. 68, pp. 3650-3652

[0012] [Non-Patent Document 2] M. Nakamura, N. Kimizuka, and T. Mohri, "The Phase Relations in the In_2—O_3—Ga_2ZnO_4—ZnO System at 1350° C.", *J. Solid State Chem.,* 1991, Vol. 93, pp. 298-315

[0013] [Non-Patent Document 3] N. Kimizuka, M. Isobe, and M. Nakamura, "Syntheses and Single-Crystal Data of Homologous Compounds, $In_2O_3(ZnO)_m$ (m=3, 4, and 5), $InGaO_3(ZnO)_3$, and $Ga_2O_3(ZnO)_m$ (m=7, 8, 9, and 16) in the In_2O_3—$ZnGa_2O_4$—ZnO System", *J. Solid State Chem.,* 1995, Vol. 116, pp. 170-178

[0014] [Non-Patent Document 4] M. Nakamura, N. Kimizuka, T. Mohri, and M. Isobe, "Syntheses and crystal structures of new homologous compounds, indium iron zinc oxides ($InFeO_3(ZnO)_m$) (m: natural number) and related compounds", *KOTAI BUTSURI* (*SOLID STATE PHYSICS*), 1993, Vol. 28, No. 5, pp. 317-327

[0015] [Non-Patent Document 5] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor", *SCIENCE,* 2003, Vol. 300, pp. 1269-1272

[0016] [Non-Patent Document 6] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors", *NATURE,* 2004, Vol. 432, pp. 488-492

DISCLOSURE OF INVENTION

[0017] Variation in the threshold voltage due to time degradation is required to be small for a transistor included in a driver circuit of a flat panel display or a transistor used as a switching element of a pixel. An object of the present invention is to provide a method for manufacturing a highly reliable semiconductor device which includes a thin film transistor using an oxide semiconductor and having stable electric characteristics. Another object of the present invention is to provide a highly reliable semiconductor device which includes a thin film transistor using an oxide semiconductor and having stable electric characteristics.

[0018] In manufacture of a semiconductor device including a transistor in which an oxide semiconductor is used for a channel formation region, after an oxide semiconductor film is formed, a conductive film including a metal, a metal compound, or an alloy that can absorb or adsorb moisture, a hydroxy group, or hydrogen is formed to overlap with the oxide semiconductor film with an insulating film provided therebetween. Then, heat treatment under a reduced-pressure atmosphere or an inert gas atmosphere is performed in the state where the conductive film is exposed; in such a manner, activation treatment for removing moisture, oxygen, hydrogen, or the like adsorbed onto a surface of or in the conductive film is performed. The heat treatment is performed at 350° C. to 650° C. By the above activation treatment, impurities such

as moisture, a hydroxy group, or hydrogen which are present in the oxide semiconductor film, in a gate insulating film, or at the interface between the oxide semiconductor film and another insulating film and its vicinity are absorbed or adsorbed by the conductive film which has been activated; therefore, deterioration in characteristics of the transistor due to the impurities can be prevented.

[0019] After the activation treatment, an insulating film is formed so as to cover the conductive film, whereby moisture and oxygen in the atmosphere can be prevented from being adsorbed onto the surface of or in the conductive film; therefore, the conductive film can be kept to be activated, and reliability of the transistor can be increased.

[0020] The conductive film can be formed using one or more metals that easily absorb or adsorb moisture, a hydroxy group, or hydrogen. Specifically, as a metal having the above characteristics, titanium, platinum, vanadium, zirconium, hafnium, palladium, magnesium, niobium, a rare earth metal, or the like can be given. As the rare earth metal, an alloy including cerium (40% to 50%), lanthanum (20% to 40%), and a rare earth metal such as praseodymium, neodymium, or yttrium, which is called a misch metal (Mm), can also be used. The conductive film may be a mixture, a metal compound, or an alloy which includes one or more of the above metals.

[0021] The conductive film may be used as a gate electrode of the thin film transistor, or may be used as a source electrode or a drain electrode of the thin film transistor. Alternatively, the conductive film may be used as a back gate electrode which is formed to overlap with a gate electrode with the oxide semiconductor film provided therebetween.

[0022] In order to reduce impurities such as moisture, a hydroxy group, and hydrogen in the oxide semiconductor film, after the oxide semiconductor film is formed, heat treatment is performed under an inert gas atmosphere such as a nitrogen atmosphere or a rare gas (e.g., argon or helium) atmosphere in the state where the oxide semiconductor film is exposed. The heat treatment is preferably performed at 400° C. or higher and lower than the temperature at which an oxide semiconductor is almost crystallized (i.e., lower than 700° C.). Note that this heat treatment is performed at a temperature not exceeding the allowable temperature limit of the substrate to be used.

[0023] As the oxide semiconductor, a four-component metal oxide such as an In—Sn—Ga—Zn—O-based oxide semiconductor, a three-component metal oxide such as an In—Ga—Zn—O-based oxide semiconductor, an In—Sn—Zn—O-based oxide semiconductor, an In—Al—Zn—O-based oxide semiconductor, a Sn—Ga—Zn—O-based oxide semiconductor, an Al—Ga—Zn—O-based oxide semiconductor, or a Sn—Al—Zn—O-based oxide semiconductor, a two-component metal oxide such as an In—Zn—O-based oxide semiconductor, a Sn—Zn—O-based oxide semiconductor, an Al—Zn—O-based oxide semiconductor, a Zn—Mg—O-based oxide semiconductor, a Sn—Mg—O-based oxide semiconductor, an In—Mg—O-based oxide semiconductor, or an In—Ga—O-based oxide semiconductor, an In—O-based oxide semiconductor, a Sn—O-based oxide semiconductor, a Zn—O-based oxide semiconductor, or the like can be used. Note that in this specification, for example, an In—Sn—Ga—Zn—O-based oxide semiconductor means a metal oxide including indium (In), tin (Sn), gallium (Ga), and zinc (Zn). There is no particular limitation on the stoichiometric proportion. The above oxide semiconductor may include silicon.

[0024] Moreover, oxide semiconductors can be represented by the chemical formula, $InMO_3(ZnO)_m$ (m>0). Here, M represents one or more metal elements selected from Ga, Al, Mn, or Co.

[0025] Note that the resistance of the oxide semiconductor film is reduced by the heat treatment. After that, an oxide insulating film is formed in contact with the low-resistance oxide semiconductor film, whereby the carrier concentration of at least a region in the low-resistance oxide semiconductor film in contact with the oxide insulating film is reduced (preferably to lower than $1\times10^{18}/cm^3$, more preferably to $1\times10^{14}/cm^3$ or lower), so that the resistance of at least the region is increased. As described above, in a manufacturing process of a semiconductor device, the carrier concentration and resistance of the oxide semiconductor film can be controlled by formation of the oxide insulating film or the like, so that a semiconductor device which includes a thin film transistor with favorable electric characteristics and high reliability can be manufactured and provided.

[0026] Note that as the oxide insulating film formed to be in contact with the low-resistance oxide semiconductor film, an inorganic insulating film which blocks impurities such as moisture, hydrogen ions, and OH^- is used. Specifically, a silicon oxide film or a silicon nitride oxide film is used.

[0027] The transistor may be a bottom-gate transistor, a top-gate transistor, or a bottom-contact transistor. The bottom-gate transistor includes, for example, a gate electrode over an insulating surface; a gate insulating film over the gate electrode; an oxide semiconductor film overlapping with the gate electrode with the gate insulating film provided therebetween; a source electrode and a drain electrode over the oxide semiconductor film; an oxide insulating film over the oxide semiconductor film, the source electrode, and the drain electrode; and a back gate electrode overlapping with the oxide semiconductor film with the oxide insulating film provided therebetween. The top-gate transistor includes, for example, an oxide semiconductor film over an insulating surface; a gate insulating film which is an oxide insulating film over the oxide semiconductor film; and a gate electrode overlapping with the oxide semiconductor film with the gate insulating film provided therebetween and functioning as a conductive film. The bottom-contact transistor includes, for example, a gate electrode over an insulating surface; a gate insulating film over the gate electrode; a source electrode and a drain electrode over the gate insulating film; an oxide semiconductor film which is over the source electrode and the drain electrode and overlaps with the gate electrode with the gate insulating film provided therebetween; an oxide insulating film over the oxide semiconductor film; and a back gate electrode overlapping with the oxide semiconductor film with the oxide insulating film provided therebetween.

[0028] Heat treatment in a furnace or a rapid thermal annealing method (RTA method) is used for the heat treatment. As the RTA method, a method using a lamp light source or a method in which a substrate is moved in a heated gas and heat treatment is performed for a short time can be employed. With the use of the RTA method, it is also possible to make the time necessary for heat treatment shorter than 0.1 hour. Note that in the case where a glass substrate is used as a substrate, heat treatment is performed at higher than or equal to 300° C. and lower than or equal to the strain point of the glass substrate.

[0029] A thin film transistor having stable electric characteristics can be manufactured and provided. In addition, a

semiconductor device which includes a highly reliable thin film transistor having favorable electric characteristics can be provided.

BRIEF DESCRIPTION OF DRAWINGS

[0030] FIGS. **1**A to **1**E illustrate a method for manufacturing a semiconductor device.

[0031] FIGS. **2**A and **2**B are top views of a manufactured thin film transistor.

[0032] FIGS. **3**A to **3**D illustrate a method for manufacturing a semiconductor device.

[0033] FIGS. **4**A and **4**B are top views of a manufactured thin film transistor.

[0034] FIGS. **5**A to **5**E illustrate a method for manufacturing a semiconductor device.

[0035] FIGS. **6**A and **6**B are top views of a manufactured thin film transistor.

[0036] FIGS. **7**A to **7**C illustrate a method for manufacturing a semiconductor device.

[0037] FIGS. **8**A to **8**C illustrate a method for manufacturing a semiconductor device.

[0038] FIGS. **9**A to **9**C illustrate a method for a manufacturing a semiconductor device.

[0039] FIG. **10** illustrates a method for manufacturing a semiconductor device.

[0040] FIG. **11** illustrates a method for manufacturing a semiconductor device.

[0041] FIG. **12** illustrates a method for manufacturing a semiconductor device.

[0042] FIG. **13** illustrates a method for manufacturing a semiconductor device.

[0043] FIG. **14** is a cross-sectional view of a liquid crystal display device.

[0044] FIGS. **15**A to **15**C are cross-sectional views of light-emitting devices.

[0045] FIG. **16** illustrates a structure of a liquid crystal display device module.

[0046] FIGS. **17**A to **17**E illustrate electronic devices using semiconductor devices.

BEST MODE FOR CARRYING OUT THE INVENTION

[0047] Embodiments and an example of the present invention will be hereinafter described in detail with reference to the accompanying drawings. Note that the present invention is not limited to the description below, and those skilled in the art will appreciate that a variety of modifications can be made to the modes and details without departing from the spirit and scope of the present invention. Therefore, the present invention is not construed as being limited to the description of embodiments and an example below.

[0048] The present invention can be applied to manufacture of any kind of semiconductor devices including microprocessors, integrated circuits such as image processing circuits, RF tags, semiconductor display devices, and the like. A semiconductor device means any device which can function by utilizing semiconductor characteristics, and a semiconductor display device, a semiconductor circuit, and an electronic device are all included in the category of the semiconductor device. The semiconductor display devices include the following in its category: liquid crystal display devices, light-emitting devices in which a light-emitting element typified by an organic light-emitting element (OLED) is provided for each pixel, electronic papers, digital micromirror devices (DMDs), plasma display panels (PDPs), field emission displays (FEDs), and other semiconductor display devices in which a circuit element using a semiconductor film is included in a driver circuit.

Embodiment 1

[0049] A method for manufacturing a semiconductor device will be described with reference to FIGS. **1**A to **1**E and FIGS. **2**A and **2**B with use of a bottom-gate thin film transistor as an example.

[0050] As illustrated in FIG. **1**A, a gate electrode **101** is formed over a substrate **100** having an insulating surface. An insulating film serving as a base film may be provided between the substrate **100** and the gate electrode **101**. The base film can be formed to have a single-layer structure or a stacked-layer structure using one or more insulating films which prevent diffusion of impurity elements from the substrate **100**, specifically, a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, or a silicon oxynitride film. The gate electrode **101** can be formed to have a single-layer structure or a stacked-layer structure using one or more conductive films using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, neodymium, or scandium; an alloy material which contains any of these metal materials as its main component; or a nitride which contains any of these metals. Note that aluminum or copper can also be used as the above metal material as long as it can withstand the temperature of heat treatment performed later.

[0051] For example, as a two-layer structure of the gate electrode **101**, a two-layer structure in which a titanium nitride film and a molybdenum film are stacked is preferable. As a three-layer structure of the gate electrode **101**, a three-layer structure in which a tungsten film or a tungsten nitride film, an aluminum-silicon alloy film or an aluminum-titanium alloy film, and a titanium nitride film or a titanium film are stacked is preferable.

[0052] Note that in this specification, an oxynitride is a substance that contains more oxygen than nitrogen, and a nitride oxide is a substance that contains more nitrogen than oxygen.

[0053] The gate electrode **101** is formed to a thickness of 10 nm to 400 nm, preferably 100 nm to 200 nm. In this embodiment, a conductive film for the gate electrode is formed to a thickness of 150 nm by a sputtering method using a tungsten target, and then, the conductive film is processed (patterned) into a desired shape by etching; in such a manner, the gate electrode **101** is formed.

[0054] Next, a gate insulating film **102** is formed over the gate electrode **101**. The gate insulating film **102** can be formed to have a single-layer structure or a stacked-layer structure of a silicon oxide film, a silicon nitride film, a silicon oxynitride film, and/or a silicon nitride oxide film by a plasma CVD method, a sputtering method, or the like. For example, a silicon oxynitride film may be formed using a deposition gas including silane (for example, monosilane), oxygen, and nitrogen by a plasma CVD method.

[0055] In this embodiment, the gate insulating film **102** is formed to a thickness of 200 nm by a plasma CVD method. The gate insulating film **102** is formed under the following conditions: the flow rate of a silane gas is 4 sccm; the flow rate of dinitrogen monoxide (N_2O) is 800 sccm; and the substrate temperature is 400° C.

[0056] Next, an oxide semiconductor film is formed over the gate insulating film **102**. The oxide semiconductor film is formed by a sputtering method using an oxide semiconductor target. Moreover, the oxide semiconductor film can be formed by a sputtering method under a rare gas (for example, argon) atmosphere, an oxygen atmosphere, or an atmosphere including a rare gas (for example, argon) and oxygen.

[0057] Note that before the oxide semiconductor film is formed by a sputtering method, dust attached to a surface of the gate insulating film **102** is preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated. The reverse sputtering refers to a method in which, without application of voltage to a target side, an RF power source is used for application of voltage to a substrate side in an argon atmosphere to generate plasma in the vicinity of the substrate to modify a surface. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere, or the like may be used. Alternatively, an argon atmosphere to which oxygen, nitrous oxide, or the like is added may be used. Alternatively, an argon atmosphere to which chlorine, carbon tetrafluoride, or the like is added may be used.

[0058] The oxide semiconductor film for forming a channel formation region may be formed using an oxide material having semiconductor characteristics described above.

[0059] The thickness of the oxide semiconductor film is set to 5 nm to 300 nm, preferably 10 nm to 100 nm. In this embodiment, as the oxide semiconductor film, an In—Ga—Zn—O-based non-single-crystal film with a thickness of 50 nm, which is obtained by a sputtering method using an oxide semiconductor target including indium (In), gallium (Ga), and zinc (Zn) (In_2O_3:Ga_2O_3:ZnO=1:1:1), is used. In this embodiment, a DC sputtering method is employed, the flow rate of argon is 30 sccm, the flow rate of oxygen is 15 sccm, and the substrate temperature is room temperature.

[0060] The gate insulating film **102** and the oxide semiconductor film may be formed successively without exposure to air. Successive film formation without exposure to air makes it possible to obtain each interface of stacked layers, which is not contaminated by atmospheric components or impurity elements floating in air, such as water, hydrocarbon, or the like. Therefore, variation in characteristics of the thin film transistor can be reduced.

[0061] Next, as illustrated in FIG. **1**A, the oxide semiconductor film is processed (patterned) into a desired shape by etching or the like, so that an island-shaped oxide semiconductor film **103** is formed over the gate insulating film **102** so as to overlap with the gate electrode **101** with the gate insulating film **102** provided therebetween.

[0062] Next, the island-shaped oxide semiconductor film **103** is subjected to heat treatment at higher than or equal to 400° C. and lower than or equal to 700° C., preferably higher than or equal to 450° C. and lower than or equal to 650° C. under a reduced-pressure atmosphere, an inert gas atmosphere such as a nitrogen atmosphere or a rare gas atmosphere, an oxygen atmosphere, or an ultra-dry air (i.e., air having a moisture content of 20 ppm (−55° C. by dew-point conversion) or less, preferably 1 ppm or less, more preferably 10 ppb or less in the case where the measurement is performed with use of a CRDS (cavity-ring-down spectroscopy) type dew-point meter) atmosphere. Then, the island-shaped oxide semiconductor film **103** is slowly cooled to a temperature which is higher than or equal to room temperature and lower than 100° C. under an inert atmosphere. By heat treatment performed on the oxide semiconductor film **103** under the above-described atmosphere, moisture, hydrogen, and a hydroxy group included in the oxide semiconductor film **103** are eliminated; in such a manner, an island-shaped oxide semiconductor film **104** is formed as illustrated in FIG. **1**B. Therefore, deterioration in characteristics of a thin film transistor in which the oxide semiconductor film **104** serves as a channel formation region due to the above impurities can be prevented.

[0063] In this embodiment, heat treatment is performed for 60 minutes under a nitrogen atmosphere in the state where the substrate temperature reaches 450° C. For the heat treatment, a heating method using an electric furnace or an instantaneous heating method such as a gas rapid thermal anneal (GRTA) method using a heated gas or a lamp rapid thermal anneal (LRTA) method using lamp light can be used. For example, in the case of performing heat treatment using an electric furnace, the temperature rise characteristics are preferably set at higher than or equal to 0.1° C./min and lower than or equal to 20° C./min and the temperature drop characteristics are preferably set at higher than or equal to 0.1° C./min and lower than or equal to 15° C./min

[0064] Note that in the heat treatment, it is preferable that moisture, hydrogen, and the like be not contained in nitrogen or a rare gas such as helium, neon, or argon. Alternatively, it is preferable that nitrogen or a rare gas such as helium, neon, or argon introduced into an apparatus for heat treatment have a purity of 6N (99.9999%) or more, preferably, 7N (99.99999%) or more (that is, the impurity concentration is 1 ppm or lower, preferably, 0.1 ppm or lower).

[0065] Alternatively, the heat treatment may be performed under air where the dew point under an atmospheric pressure is −60° C. or lower and the moisture content is small, instead of an inert gas atmosphere such as a nitrogen atmosphere or a rare gas atmosphere.

[0066] The island-shaped oxide semiconductor film **104** which is formed through the heat treatment under an inert gas atmosphere or a reduced-pressure atmosphere may be partially crystallized.

[0067] Note that after the heat treatment is performed on the oxide semiconductor film **104**, heat treatment is performed on the oxide semiconductor film **104** under an oxygen atmosphere, whereby impurities such as moisture included in the oxide semiconductor film **104** can be removed. In addition, the heat treatment is performed under an oxygen atmosphere in order that the oxide semiconductor film **104** may include excessive oxygen, whereby resistance thereof can be increased. The heat treatment is performed at a temperature where a metal having a low melting point such as Zn included in the oxide semiconductor is less likely to be evaporated, for example, higher than or equal to 100° C. and lower than 350° C., preferably higher than or equal to 150° C. and lower than 250° C. It is preferable that an oxygen gas used for the heat treatment under an oxygen atmosphere do not include moisture, hydrogen, or the like. Alternatively, an oxygen gas which is introduced into the heat treatment apparatus preferably has a purity of 6N (99.9999%) or more, more preferably 7N (99.99999%) or more (that is, the impurity concentration in oxygen is 1 ppm or lower, preferably 0.1 ppm or lower).

[0068] Next, as illustrated in FIG. **1**C, a conductive film for a source electrode and a drain electrode is formed over the island-shaped oxide semiconductor film **104**, and then, the conductive film is patterned by etching or the like to form a source electrode **105** and a drain electrode **106**. In the patterning for forming the source electrode **105** and the drain

electrode **106**, an exposed portion of the island-shaped oxide semiconductor film **104** is partly etched, whereby an island-shaped oxide semiconductor film **107** having a groove (a recessed portion) is formed.

[0069] The conductive film is preferably formed using a material that can withstand heat treatment in a later step. For example, as a material of the conductive film for the source electrode and the drain electrode, an element selected from chromium, tantalum, titanium, molybdenum, tungsten, zirconium, beryllium, thorium, manganese, or magnesium, an alloy containing one or more of these elements as its component, or the like can be given. In order to further improve heat resistance to heat treatment which is to be performed after the source electrode **105** and the drain electrode **106** are formed, the conductive film for the source electrode and the drain electrode may be formed in combination of the above material with a heat resistant conductive material such as neodymium, scandium, or a nitride of these elements.

[0070] The source electrode **105** and the drain electrode **106** are formed to a thickness of 10 nm to 400 nm, preferably 100 nm to 300 nm. In this embodiment, a conductive film for the source electrode and the drain electrode is formed to a thickness of 200 nm by a sputtering method using a molybdenum target, and then, the conductive film is processed (patterned) into a desired shape by etching, whereby the source electrode **105** and the drain electrode **106** are formed.

[0071] FIG. **2**A is a top view of a semiconductor device illustrated in FIG. **1**C. FIG. **1**C corresponds to a cross-sectional view taken along dashed line A**1**-A**2** in FIG. **2**A.

[0072] Next, as illustrated in FIG. **1**D, an oxide insulating film **108** is formed in contact with the island-shaped oxide semiconductor film **107**, the source electrode **105**, and the drain electrode **106** by a sputtering method. The oxide insulating film **108** is formed in contact with the low-resistance island-shaped oxide semiconductor film **107** and formed using an inorganic insulating film which includes impurities such as moisture, hydrogen, oxygen, and a hydroxy group as little as possible and blocks entry of these impurities from the outside, specifically, a silicon oxide film, a silicon nitride oxide film, or the like.

[0073] In this embodiment, a silicon oxide film with a thickness of 300 nm is formed as the oxide insulating film **108**. The substrate temperature at the time of the film formation may be higher than or equal to room temperature and lower than or equal to 300° C., and is set at 100° C. in this embodiment. Formation of the silicon oxide film by a sputtering method can be performed under a rare gas (for example, argon) atmosphere, an oxygen atmosphere, or an atmosphere including a rare gas (for example, argon) and oxygen. Further, a silicon oxide target or a silicon target may be used as a target. For example, with use of a silicon target, a silicon oxide film can be formed by a sputtering method under an atmosphere including oxygen and nitrogen.

[0074] When the oxide insulating film **108** is formed in contact with the low-resistance oxide semiconductor film **107** by a sputtering method, a PCVD method, or the like, the carrier concentration of at least a region in the low-resistance oxide semiconductor film **107** in contact with the oxide insulating film **108** is reduced, preferably to lower than $1\times10^{18}/cm^3$, so that the resistance of at least the region is increased. Thus, a high-resistance oxide semiconductor region can be formed. By the formation of the oxide insulating film **108**, the oxide semiconductor film **107** has a high-resistance oxide semiconductor region in the vicinity of the interface between the oxide insulating film **108** and the oxide semiconductor film **107**.

[0075] Note that after the source electrode **105** and the drain electrode **106** are formed and before the oxide insulating film **108** is formed, the oxide semiconductor film **107** may be again subjected to heat treatment under a reduced-pressure atmosphere, an inert gas atmosphere such as a nitrogen atmosphere or a rare gas atmosphere, an oxygen atmosphere, or an ultra-dry air (i.e., air having a moisture content of 20 ppm (−55° C. by dew-point conversion) or less, preferably 1 ppm or less, more preferably 10 ppb or less in the case where the measurement is performed with use of a CRDS (cavity-ringdown spectroscopy) type dew-point meter) atmosphere in order to eliminate moisture, hydrogen, and a hydroxy group included in the oxide semiconductor film **107**. In consideration of heat resistance of the source electrode **105** and the drain electrode **106**, the heat treatment after the source electrode **105** and the drain electrode **106** are formed is preferably performed at a temperature lower than the temperature of the heat treatment before the source electrode **105** and the drain electrode **106** are formed. Specifically, the heat treatment after the source electrode **105** and the drain electrode **106** are formed may be performed at higher than or equal to 350° C. and lower than or equal to 650° C., preferably higher than or equal to 400° C. and lower than or equal to 600° C.

[0076] Next, as illustrated in FIG. **1**D, a conductive film is formed over the oxide insulating film **108** with use of one or more metals that easily absorb or adsorb moisture, a hydroxy group, or hydrogen, and then, the conductive film is patterned, whereby a back gate electrode **109** is formed to overlap with the oxide semiconductor film **107**. Specifically, as the metal having such characteristics, titanium, platinum, vanadium, zirconium, hafnium, palladium, magnesium, niobium, a rare earth metal, or the like can be given. As the rare earth metal, an alloy including cerium (40% to 50%), lanthanum (20% to 40%), and a rare earth metal such as praseodymium, neodymium, or yttrium, which is called a misch metal (Mm), can also be used. The back gate electrode **109** may be a mixture, a metal compound, or an alloy which includes one or more of the above metals.

[0077] As the alloy used for the back gate electrode **109**, an alloy called a hydrogen absorbing alloy can also be given. As the hydrogen absorbing alloy, for example, an AB_5 alloy, an AB_2 (Laves phase) alloy, an A_2B alloy, or the like can be given. In the AB_5 alloy, one or more of a rare earth metal, niobium, and zirconium are included in A site, and one or more transition metals having a catalytic effect such as nickel, cobalt, aluminum, and tin are included in B site. As the rare earth metal, a misch metal can also be used. As the AB_5 alloy, for example, $LaNi_5$ or the like can be used for the back gate electrode **109**. In the AB_2 (Laves phase) alloy, one or more of titanium, zirconium, and hafnium are included in A site, and one or more transition metals such as manganese, nickel, chromium, and vanadium are included in B site; for example, a Ti—Mn-based alloy, a Ti—Cr-based alloy, a Zr—Mn-based alloy, a Ti—V—Mn-based alloy, or the like can be given. As the AB_2 alloy, for example, $TiCr_2$, $TiMn_2$, or the like can be used for the back gate electrode **109**. In the A_2B alloy, one or more of magnesium and titanium are included in A site, and one or more of nickel and copper are included in B site. As the A_2B alloy, for example, Mg_2Ni, Mg_2Cu, Ti_2Ni, or the like can be used for the back gate electrode **109**. Note that in these hydrogen absorbing alloys, at least part of an element in A site

or B site can be replaced with another element, and the actual composition is not necessarily in due faun. As the hydrogen absorbing alloy, in addition to the above type alloys, a Ti—Fe alloy, a V-type alloy, a Pd-type alloy, a Ca-type alloy, a BCC alloy, or the like can be used for the back gate electrode **109**.

[0078] The thickness of the back gate electrode **109** is set to 10 nm to 400 nm, preferably 100 nm to 200 nm. In this embodiment, a conductive film of 200 nm thick is formed using $TiCr_2$ by a sputtering method under the following conditions: an alloy that is a target (ϕ:6 inches) whose composition ratio of titanium to chromium is 1:2 is used; an argon gas is introduced into a chamber with a flow rate of 50 sccm; the pressure is 0.4 Pa; the electric power is 2 kW; and the film formation temperature is room temperature. Then, a photolithography step is performed. A resist mask is formed, and an unnecessary portion is removed by plasma etching with use of chlorine and oxygen as an etching gas so that the conductive film is processed (patterned) into a desired shape; in such a manner, the back gate electrode **109** is formed.

[0079] Next, after the back gate electrode **109** is formed, heat treatment is performed under a reduced-pressure atmosphere or an inert gas (such as nitrogen, helium, neon, or argon) atmosphere in the state where the back gate electrode **109** is exposed, whereby activation treatment for removing moisture, oxygen, hydrogen, or the like adsorbed onto a surface of or in the back gate electrode **109** is performed. In consideration of the heat resistance of the source electrode **105** and the drain electrode **106**, the heat treatment is preferably performed at a temperature lower than the temperature of the heat treatment before the source electrode **105** and the drain electrode **106** are formed. Specifically, the heat treatment is performed at higher than or equal to 300° C. and lower than or equal to 650° C., preferably higher than or equal to 350° C. and lower than or equal to 600° C.

[0080] By the activation treatment, impurities such as moisture, a hydroxy group, or hydrogen which are present, for example, in the oxide semiconductor film **107**, in the gate insulating film **102**, at the interface between the oxide semiconductor film **107** and the gate insulating film **102** and its vicinity, or at the interface between the oxide semiconductor film **107** and the oxide insulating film **108** and its vicinity are absorbed or adsorbed by the back gate electrode **109** which has been activated; therefore, deterioration in the characteristics of the transistor due to the impurities can be prevented.

[0081] In addition, impurities such as moisture or hydrogen included in an atmosphere in which the semiconductor device is placed can be prevented from being taken into the oxide semiconductor film **107**.

[0082] In this embodiment, heat treatment is performed for 10 minutes in the state where the substrate temperature reaches 400° C. and a treatment chamber is kept to a reduced-pressure atmosphere having a degree of vacuum of 5×10^{-3} Pa or less, preferably 10^{-5} Pa or less by an evacuation unit such as a turbo molecular pump. For the heat treatment, a heating method using an electric furnace or an instantaneous heating method such as a gas rapid thermal anneal (GRTA) method using a heated gas or a lamp rapid thermal anneal (LRTA) method using lamp light can be used. For example, in the case of performing heat treatment using an electric furnace, the temperature rise characteristics are preferably set at higher than or equal to 0.1° C./min and lower than or equal to 20° C./min and the temperature drop characteristics are preferably set at higher than or equal to 0.1° C./min and lower than or equal to 15° C./min.

[0083] Note that heat treatment for activation is performed in the state where the oxide semiconductor film **107** is in contact with the oxide insulating film **108**. Therefore, a region of the oxide semiconductor film **107** in contact with the oxide insulating film **108** uniformly has higher resistance; thus, variation in electric characteristics of a thin film transistor **111** can be reduced.

[0084] Next, after the activation treatment is performed, an insulating film **110** is formed so as to cover the back gate electrode **109** as illustrated in FIG. **1**E. The insulating film **110** is preferably formed using a material having a high barrier property so that moisture and oxygen in the atmosphere are prevented from being adsorbed onto the surface of or in the back gate electrode **109**. For example, the insulating film **110** can be formed to have a single-layer structure or a stacked-layer structure of a silicon nitride film, a silicon nitride oxide film, an aluminum nitride film, an aluminum nitride oxide film, or the like, as an insulating film having a high barrier property, by a plasma CVD method, a sputtering method, or the like. In order to obtain an effect of a barrier property, the insulating film **110** is preferably formed to a thickness of 15 nm to 400 nm, for example.

[0085] In this embodiment, an insulating film is formed to a thickness of 300 nm by a plasma CVD method. The insulating film is formed under the following conditions: the flow rate of a silane gas is 4 sccm; the flow rate of dinitrogen monoxide (N_2O) is 800 sccm; and the substrate temperature is 400° C.

[0086] By the formation of the insulating film **110**, moisture and oxygen in the atmosphere can be prevented from being adsorbed onto the surface of or in the back gate electrode **109**; therefore, the back gate electrode **109** can be kept to be activated, and reliability of the transistor can be increased.

[0087] FIG. **2**B is a top view of the semiconductor device in FIG. **1**E. FIG **1**E corresponds to a cross-sectional view taken along dashed line **A1**-**A2** in FIG. **2**B.

[0088] The thin film transistor **111** includes the gate electrode **101**; the gate insulating film **102** over the gate electrode **101**; the oxide semiconductor film **107** over the gate insulating film **102**; the source electrode **105** and the drain electrode **106** over the oxide semiconductor film **107**; the oxide insulating film **108** over the source electrode **105** and the drain electrode **106**; and the back gate electrode **109** over the oxide insulating film **108**. The back gate electrode **109** is formed to overlap with the oxide semiconductor film **107**, whereby impurities such as moisture, a hydroxy group, or hydrogen which are present, for example, in the oxide semiconductor film **107**, in the gate insulating film **102**, at the interface between the oxide semiconductor film **107** and the gate insulating film **102** and its vicinity, or at the interface between the oxide semiconductor film **107** and the oxide insulating film **108** and its vicinity are absorbed or adsorbed by the back gate electrode **109** which has been activated; therefore, deterioration in the characteristics of the transistor due to the impurities can be prevented. In addition, impurities such as moisture or hydrogen included in the atmosphere in which the semiconductor device is placed can be prevented from being taken into the oxide semiconductor film **107**.

[0089] Note that in FIG. **2**B, an example in which the back gate electrode **109** covers the whole oxide semiconductor film **107** is shown; however, the present invention is not limited to this structure. Since the back gate electrode **109** covers the whole oxide semiconductor film **107**, an effect of reducing

the impurities in the oxide semiconductor film **107** can be enhanced. However, the above effect can be obtained also in the case where at least the entire portion serving as a channel formation region in the oxide semiconductor film **107** or part of the portion overlaps with the back gate electrode **109**.

[0090] Further, the back gate electrode **109** may be electrically insulated and in a floating state, or may be in a state where the back gate electrode **109** is supplied with a potential. In the case of the latter, the back gate electrode **109** may be supplied with the same potential as the gate electrode **101**, or may be supplied with a fixed potential such as a ground potential. The level of the potential supplied to the back gate electrode **109** is controlled, whereby the threshold voltage of the thin film transistor **111** can be controlled. Note that in the case where the back gate electrode **109** is formed using a metal material having low electrical conductivity such as $TiCr_2$, a conductive film having low resistance is fanned in contact with the back gate electrode **109** and the combined resistance of these conductive films is low; in such a manner, increase in power consumption due to the parasitic resistance may be prevented.

[0091] The step of performing heat treatment for activating the back gate electrode **109** and the step of forming the insulating film **110** in contact with the back gate electrode **109** are successively performed without exposure to air (such a process is also referred to as successive treatment or an insitu process), whereby moisture and oxygen in an atmosphere can be prevented from being adsorbed onto the surface of or in the back gate electrode **109**. As a result, the back gate electrode **109** can be kept to be activated, and the reliability of the thin film transistor **111** can be more increased.

[0092] Note that a substrate transfer step, an alignment step, a heating or cooling step, or the like may be provided between the step of performing heat treatment for activating the back gate electrode **109** and the step of forming the insulating film **110** in contact with the back gate electrode **109**. Such a process is also within the scope of the successive treatment in this specification. However, the following case is not within the scope of the successive treatment in this specification: there is a step in which liquid is used, such as a cleaning step, a wet etching step, or a resist formation step between the above two steps.

[0093] Note that in this embodiment, although an example in which the back gate electrode **109** is formed using one or more metals that easily absorb or adsorb moisture, a hydroxy group, or hydrogen is described, the gate electrode **101** may be formed using one or more metals that easily absorb or adsorb moisture, a hydroxy group, or hydrogen. In this case, after the gate electrode **101** is formed, the gate electrode **101** may be subjected to heat treatment for activation under the same condition as the back gate electrode **109**. The gate electrode **101** is formed using a metal having the above characteristics, whereby impurities such as moisture, a hydroxy group, and hydrogen which are present, for example, in the oxide semiconductor film **107**, in the gate insulating film **102**, at the interface between the oxide semiconductor film **107** and the gate insulating film **102** and its vicinity, or at the interface between the oxide semiconductor film **107** and the oxide insulating film **108** and its vicinity are absorbed or adsorbed by the gate electrode **101** which has been activated; therefore, deterioration in the characteristics of the transistor due to the impurities can be prevented.

Embodiment 2

[0094] In this embodiment, a method for manufacturing a semiconductor device including a bottom-contact thin film transistor having a structure which is different from the structure of the thin film transistor **111** described in Embodiment 1 will be described._The same portion as or a portion having a function similar to those described in Embodiment 1 can be formed in a manner similar to that described in Embodiment 1, and also the steps similar to those of Embodiment 1 can be performed in a manner similar to those described in Embodiment 1; therefore, repetitive description is omitted.

[0095] A method for manufacturing a semiconductor device will be described with reference to FIGS. **3**A to **3**D and FIGS. **4**A and **4**B.

[0096] As illustrated in FIG. **3**A, a gate electrode **201** is formed over a substrate **200** having an insulating surface. An insulating film serving as a base film may be provided between the substrate **200** and the gate electrode **201**. The material and the structure of the gate electrode **101** described in Embodiment 1 may be referred to for the material and the structure of the gate electrode **201**. The material and the structure of the base film described in Embodiment 1 may be referred to for the material and the structure of the base film.

[0097] Next, a gate insulating film **202** is formed over the gate electrode **201**. The material, the structure, and the formation method of the gate insulating film **102** described in Embodiment 1 may be referred to for the material, the structure, and the formation method of the gate insulating film **202**.

[0098] In this embodiment, the gate insulating film **202** is formed to a thickness of 200 nm by a plasma CVD method. The gate insulating film **202** is formed under the following conditions: the flow rate of a silane gas is 4 sccm; the flow rate of dinitrogen monoxide (N_2O) is 800 sccm; and the substrate temperature is 400° C.

[0099] Next, a conductive film for a source electrode and a drain electrode is formed over the gate insulating film **202**. Then, the conductive film is processed (patterned) into a desired shape by etching or the like, whereby a source electrode **203** and a drain electrode **204** are formed. The material and the structure of the conductive film which is patterned for forming the source electrode **105** and the drain electrode **106** in Embodiment 1 may be referred to for the material and the structure of the conductive film. In order to prevent defective coverage such as breakage of an oxide semiconductor film to be formed later, the source electrode **203** and the drain electrode **204** are formed to have a smaller thickness than the source electrode and the drain electrode in Embodiment 1, and are formed to a thickness of 10 nm to 300 nm, preferably 100 mn to 200 nm.

[0100] In this embodiment, a conductive film for the source electrode and the drain electrode is formed to a thickness of 150 nm by a sputtering method using a molybdenum target, and then, the conductive film is processed (patterned) into a desired shape by etching, whereby the source electrode **203** and the drain electrode **204** are formed.

[0101] Next, an oxide semiconductor film is formed over the source electrode **203**, the drain electrode **204**, and the gate insulating film **202**. An oxide semiconductor film for forming a channel formation region may be formed using an oxide material having semiconductor characteristics described in Embodiment 1. The oxide semiconductor film is formed by a sputtering method using an oxide semiconductor target. Moreover, the oxide semiconductor film can be formed by a sputtering method under a rare gas (for example, argon) atmo-

sphere, an oxygen atmosphere, or an atmosphere including a rare gas (for example, argon) and oxygen.

[0102] Note that before the oxide semiconductor film is formed by a sputtering method, dust attached to a surface of the gate insulating film **202** is preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated.

[0103] The thickness of the oxide semiconductor film is set to 5 nm to 300 nm, preferably 10 nm to 100 nm. In this embodiment, as the oxide semiconductor film, an In—Ga—Zn—O-based non-single-crystal film with a thickness of 50 nm, which is obtained by a sputtering method using an oxide semiconductor target including indium (In), gallium (Ga), and zinc (Zn) (In_2O_3:Ga_2O_3:ZnO=1:1:1), is used. In this embodiment, a DC sputtering method is employed, the flow rate of argon is 30 sccm, the flow rate of oxygen is 15 sccm, and the substrate temperature is room temperature.

[0104] Next, as illustrated in FIG. **3**A, the oxide semiconductor film is processed (patterned) into a desired shape by etching or the like, so that an island-shaped oxide semiconductor film **205** is formed over the gate insulating film **202** so as to overlap with the gate electrode **201** with the gate insulating film **202** provided therebetween.

[0105] Next, the island-shaped oxide semiconductor film **205** is subjected to heat treatment under a reduced-pressure atmosphere, an inert gas atmosphere such as a nitrogen atmosphere or a rare gas atmosphere, an oxygen atmosphere, or an ultra-dry air (i.e., air having a moisture content of 20 ppm (−55° C. by dew-point conversion) or less, preferably 1 ppm or less, more preferably 10 ppb or less in the case where the measurement is performed with use of a CRDS (cavity-ring-down spectroscopy) type dew-point meter) atmosphere. The heat treatment for the oxide semiconductor film **103** described in Embodiment 1 may be referred to for the heat treatment for the oxide semiconductor film **205**. Note that the heat treatment may be performed at higher than or equal to 350° C. and lower than or equal to 650° C., preferably higher than or equal to 400° C. and lower than or equal to 600° C. in consideration of the heat resistance of the source electrode **203** and the drain electrode **204**. By heat treatment performed on the oxide semiconductor film **205** under the above-described atmosphere, moisture, hydrogen, and a hydroxy group included in the oxide semiconductor film **205** are eliminated; in such a manner, an island-shaped oxide semiconductor film **206** is formed as illustrated in FIG. **3**B. Therefore, deterioration in characteristics of a thin film transistor in which the oxide semiconductor film **206** serves as a channel formation region due to the above impurities can be prevented.

[0106] In this embodiment, heat treatment is performed for 60 minutes under a nitrogen atmosphere in the state where the substrate temperature reaches 450° C.

[0107] Note that after the heat treatment is performed on the oxide semiconductor film **205** to form the oxide semiconductor film **206**, heat treatment is performed on the oxide semiconductor film **206** under an oxygen atmosphere, whereby impurities such as moisture included in the oxide semiconductor film **206** can be removed. In addition, the heat treatment is performed under an oxygen atmosphere in order that the oxide semiconductor film **206** may include excessive oxygen, whereby resistance thereof can be increased. The heat treatment under an oxygen atmosphere for the oxide semiconductor film **104** described in Embodiment 1 may be referred to for the heat treatment under an oxygen atmosphere for the oxide semiconductor film **206**.

[0108] FIG. **4**A is a top view of the semiconductor device in FIG. **3**B. FIG. **3**B corresponds to a cross-sectional view taken along dashed line B**1**-B**2** in FIG. **4**A.

[0109] Next, as illustrated in FIG. **3**C, an oxide insulating film **207** is formed in contact with the island-shaped oxide semiconductor film **206**, the source electrode **203**, and the drain electrode **204** by a sputtering method. The oxide insulating film **207** is formed in contact with the low-resistance island-shaped oxide semiconductor film **206** and formed using an inorganic insulating film which includes impurities such as moisture, hydrogen, oxygen, and a hydroxy group as little as possible and blocks entry of these impurities from the outside, specifically, a silicon oxide film, a silicon nitride oxide film, or the like.

[0110] In this embodiment, a silicon oxide film with a thickness of 300 nm is formed as the oxide insulating film **207**. The substrate temperature at the time of the film formation may be higher than or equal to room temperature and lower than or equal to 300° C., and is set at 100° C. in this embodiment. Formation of the silicon oxide film by a sputtering method can be performed under a rare gas (for example, argon) atmosphere, an oxygen atmosphere, or an atmosphere including a rare gas (for example, argon) and oxygen. Further, a silicon oxide target or a silicon target may be used as a target. For example, with use of a silicon target, a silicon oxide film can be formed by a sputtering method under an atmosphere including oxygen and nitrogen.

[0111] When the oxide insulating film **207** is formed in contact with the low-resistance oxide semiconductor film **206** by a sputtering method, a PCVD method, or the like, the carrier concentration of at least a region in the low-resistance oxide semiconductor film **206** in contact with the oxide insulating film **207** is reduced, preferably to lower than $1\times10^{18}/cm^3$, so that the resistance of at least the region is increased. Thus, a high-resistance oxide semiconductor region can be formed. By the formation of the oxide insulating film **207**, the oxide semiconductor film **206** has a high-resistance oxide semiconductor region in the vicinity of the interface between the oxide insulating film **207** and the oxide semiconductor film **206**.

[0112] Next, as illustrated in FIG. **3**C, a conductive film is formed over the oxide insulating film **207** with use of one or more metals that easily absorb or adsorb moisture, a hydroxy group, or hydrogen, and then, the conductive film is patterned, whereby a back gate electrode **208** is formed to overlap with the oxide semiconductor film **206**. The material and the structure of the back gate electrode **109** described in Embodiment 1 may be referred to for the material and the structure of the back gate electrode **208**.

[0113] In this embodiment, a conductive film of 200 nm thick is formed using $TiCr_2$ by a sputtering method under the following conditions: an alloy that is a target (ϕ:6 inches) whose composition ratio of titanium to chromium is 1:2 is used; an argon gas is introduced into a chamber with a flow rate of 50 sccm; the pressure is 0.4 Pa; the electric power is 2 kW; and the film formation temperature is room temperature. Then, a photolithography step is performed. A resist mask is formed, and an unnecessary portion is removed by plasma etching with use of chlorine and oxygen as an etching gas so that the conductive film is processed (patterned) into a desired shape; in such a manner, the back gate electrode **208** is formed.

[0114] Next, after the back gate electrode 208 is formed, heat treatment is performed under a reduced-pressure atmosphere or an inert gas atmosphere in the state where the back gate electrode 208 is exposed, whereby activation treatment for removing moisture, oxygen, hydrogen, or the like adsorbed onto a surface of or in the back gate electrode 208 is performed. The condition of the activation treatment for the back gate electrode 109 described in Embodiment 1 can be referred to for the condition of the activation treatment.

[0115] By the above activation treatment, impurities such as moisture, a hydroxy group, and hydrogen which are present, for example, in the oxide semiconductor film 206, in the gate insulating film 202, at the interface between the oxide semiconductor film 206 and the gate insulating film 202 and its vicinity, or at the interface between the oxide semiconductor film 206 and the oxide insulating film 207 and its vicinity are absorbed or adsorbed by the back gate electrode 208 which has been activated; therefore, deterioration in the characteristics of the transistor due to the impurities can be prevented.

[0116] In addition, impurities such as moisture and hydrogen included in an atmosphere in which the semiconductor device is placed can be prevented from being taken into the oxide semiconductor film 206.

[0117] In this embodiment, heat treatment is performed for 10 minutes in the state where the substrate temperature reaches 400° C. and a treatment chamber is kept to a reduced-pressure atmosphere having a degree of vacuum of 5×10^{-3} Pa or less, preferably 10^{-5} Pa or less by an evacuation unit such as a turbo molecular pump.

[0118] Note that heat treatment for activation is performed in the state where the oxide semiconductor film 206 is in contact with the oxide insulating film 207. Therefore, a region of the oxide semiconductor film 206 in contact with the oxide insulating film 207 uniformly has higher resistance; thus, variation in electric characteristics of a thin film transistor 211 can be reduced.

[0119] Next, after the activation treatment is performed, an insulating film 210 is formed so as to cover the back gate electrode 208 as illustrated in FIG. 3D. The insulating film 210 is preferably formed using a material having a high barrier property so that moisture and oxygen in the atmosphere are prevented from being adsorbed onto the surface of or in the back gate electrode 208. The material and the structure of the insulating film 110 described in Embodiment 1 may be referred to for the material and the structure of the insulating film 210.

[0120] In this embodiment, an insulating film is formed to a thickness of 300 nm by a plasma CVD method. The insulating film is formed under the following conditions: the flow rate of a silane gas is 4 sccm; the flow rate of dinitrogen monoxide (N_2O) is 800 sccm; and the substrate temperature is 400° C.

[0121] By the formation of the insulating film 210, moisture and oxygen in the atmosphere can be prevented from being adsorbed onto the surface of or in the back gate electrode 208; therefore, the back gate electrode 208 can be kept to be activated, and reliability of the transistor can be increased.

[0122] FIG. 4B is a top view of the semiconductor device in FIG. 3D. FIG. 3D corresponds to a cross-sectional view taken along dashed line B1-B2 in FIG. 4B.

[0123] The thin film transistor 211 includes the gate electrode 201; the gate insulating film 202 over the gate electrode 201; the source electrode 203 and the drain electrode 204 over the gate insulating film 202; the oxide semiconductor film 206 over the gate electrode 201, the source electrode 203, and the drain electrode 204; the oxide insulating film 207 over the oxide semiconductor film 206; and the back gate electrode 208 over the oxide insulating film 207. The back gate electrode 208 is formed to overlap with the oxide semiconductor film 206, whereby impurities such as moisture, a hydroxy group, and hydrogen which are present, for example, in the oxide semiconductor film 206, in the gate insulating film 202, at the interface between the oxide semiconductor film 206 and the gate insulating film 202 and its vicinity, or at the interface between the oxide semiconductor film 206 and the oxide insulating film 207 and its vicinity are absorbed or adsorbed by the back gate electrode 208 which has been activated; therefore, deterioration in the characteristics of the transistor due to the impurities can be prevented. In addition, impurities such as moisture and hydrogen included in the atmosphere in which the semiconductor device is placed can be prevented from being taken into the oxide semiconductor film 206.

[0124] Note that in FIG. 4B, an example in which the back gate electrode 208 covers the whole oxide semiconductor film 206 is shown; however, the present invention is not limited to this structure. Since the back gate electrode 208 covers the whole oxide semiconductor film 206, an effect of reducing the impurities in the oxide semiconductor film 206 can be enhanced. However, the above effect can be obtained also in the case where at least the entire portion serving as a channel formation region in the oxide semiconductor film 206 or part of the portion overlaps with the back gate electrode 208.

[0125] Further, the back gate electrode 208 may be electrically insulated and in a floating state, or may be in a state where the back gate electrode 208 is supplied with a potential. In the case of the latter, the back gate electrode 208 may be supplied with the same potential as the gate electrode 201, or may be supplied with a fixed potential such as a ground potential. The level of the potential supplied to the back gate electrode 208 is controlled, whereby the threshold voltage of the thin film transistor 211 can be controlled. Note that in the case where the back gate electrode 208 is formed using a metal material having low electrical conductivity such as $TiCr_2$, a conductive film having low resistance is formed in contact with the back gate electrode 208 and the combined resistance of these conductive films is low; in such a manner, increase in power consumption due to the parasitic resistance may be prevented.

[0126] The step of performing heat treatment for activating the back gate electrode 208 and the step of forming the insulating film 210 in contact with the back gate electrode 208 are successively performed without exposure to air (such a process is also referred to as successive treatment or an insitu process), whereby moisture and oxygen in an atmosphere can be prevented from being adsorbed onto the surface of or in the back gate electrode 208. As a result, the back gate electrode 208 can be kept to be activated, and the reliability of the thin film transistor 211 can be more increased.

[0127] Note that a substrate transfer step, an alignment step, a heating or cooling step, or the like may be provided between the step of performing heat treatment for activating the back gate electrode 208 and the step of forming the insulating film 210 in contact with the back gate electrode 208. Such a process is also within the scope of the successive treatment in this specification. However, the following case is not within the scope of the successive treatment in this speci-

fication: there is a step in which liquid is used, such as a cleaning step, a wet etching step, or a resist formation step between the above two steps.

[0128] Note that in this embodiment, although an example in which the back gate electrode **208** is formed using one or more metals that easily absorb or adsorb moisture, a hydroxy group, or hydrogen is described, the gate electrode **201** may be formed using one or more metals that easily absorb or adsorb moisture, a hydroxy group, or hydrogen. In this case, after the gate electrode **201** is formed, the gate electrode **201** may be subjected to heat treatment for activation under the same condition as the back gate electrode **208**. The gate electrode **201** is formed using a metal having the above characteristics, whereby impurities such as moisture, a hydroxy group, and hydrogen which are present, for example, in the oxide semiconductor film **206**, in the gate insulating film **202**, at the interface between the oxide semiconductor film **206** and the gate insulating film **202** and its vicinity, or at the interface between the oxide semiconductor film **206** and the oxide insulating film **207** and its vicinity are absorbed or adsorbed by the gate electrode **201** which has been activated; therefore, deterioration in the characteristics of the transistor due to the impurities can be prevented.

[0129] This embodiment can be implemented in combination with another embodiment as appropriate.

Embodiment 3

[0130] In this embodiment, a method for manufacturing a semiconductor device including a bottom-gate thin film transistor having a structure which is different from the structure of the thin film transistor **111** described in Embodiment 1 and the structure of the thin film transistor **211** described in Embodiment 2 will be described. The same portion as or a portion having a function similar to those described in Embodiment 1 can be formed in a manner similar to that described in Embodiment 1, and also the steps similar to those of Embodiment 1 can be performed in a manner similar to those described in Embodiment 1; therefore, repetitive description is omitted.

[0131] A method for manufacturing a semiconductor device will be described with reference to FIGS. **5**A to **5**E and FIGS. **6**A and **6**B.

[0132] As illustrated in FIG. **5**A, a gate electrode **301** is formed over a substrate **300** having an insulating surface. An insulating film serving as a base film may be provided between the substrate **300** and the gate electrode **301**. The material and the structure of the gate electrode **101** described in Embodiment 1 may be referred to for the material and the structure of the gate electrode **301**. The material and the structure of the base film described in Embodiment 1 may be referred to for the material and the structure of the base film.

[0133] Next, a gate insulating film **302** is formed over the gate electrode **301**. The material, the structure, and the formation method of the gate insulating film **102** described in Embodiment 1 may be referred to for the material, the structure, and the formation method of the gate insulating film **302**.

[0134] In this embodiment, the gate insulating film **302** is formed to a thickness of 200 nm by a plasma CVD method. The gate insulating film **302** is formed under the following conditions: the flow rate of a silane gas is 4 sccm; the flow rate of dinitrogen monoxide (N_2O) is 800 sccm; and the substrate temperature is 400° C.

[0135] Next, an oxide semiconductor film is formed over the gate insulating film **302**. An oxide semiconductor film for forming a channel formation region may be formed using an oxide material having semiconductor characteristics described in Embodiment 1. The oxide semiconductor film is formed by a sputtering method using an oxide semiconductor target. Moreover, the oxide semiconductor film can be formed by a sputtering method under a rare gas (for example, argon) atmosphere, an oxygen atmosphere, or an atmosphere including a rare gas (for example, argon) and oxygen.

[0136] Note that before the oxide semiconductor film is formed by a sputtering method, dust attached to a surface of the gate insulating film **302** is preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated.

[0137] The thickness of the oxide semiconductor film is set to 5 nm to 300 nm, preferably 10 nm to 100 nm. In this embodiment, as the oxide semiconductor film, an In—Ga—Zn—O-based non-single-crystal film with a thickness of 50 nm, which is obtained by a sputtering method using an oxide semiconductor target including indium (In), gallium (Ga), and zinc (Zn) (In_2O_3:Ga_2O_3:ZnO=1:1:1), is used. In this embodiment, a DC sputtering method is employed, the flow rate of argon is 30 sccm, the flow rate of oxygen is 15 sccm, and the substrate temperature is room temperature.

[0138] Next, as illustrated in FIG. **5**A, the oxide semiconductor film is processed (patterned) into a desired shape by etching or the like, so that an island-shaped oxide semiconductor film **303** is formed over the gate insulating film **302** so as to overlap with the gate electrode **301** with the gate insulating film **302** provided therebetween.

[0139] Next, the island-shaped oxide semiconductor film **303** is subjected to heat treatment under an inert gas (such as nitrogen, helium, neon, or argon) atmosphere. The heat treatment for the oxide semiconductor film **103** described in Embodiment 1 may be referred to for the heat treatment for the oxide semiconductor film **303**. By heat treatment performed on the oxide semiconductor film **303** under the above-described atmosphere, moisture, hydrogen, and a hydroxy group included in the oxide semiconductor film **303** are eliminated; in such a manner, an island-shaped oxide semiconductor film **304** is formed as illustrated in FIG. **5**B. Therefore, deterioration in characteristics of a thin film transistor in which the oxide semiconductor film **304** serves as a channel formation region due to the above impurities can be prevented.

[0140] In this embodiment, heat treatment is performed for 60 minutes under a nitrogen atmosphere in the state where the substrate temperature reaches 450° C.

[0141] Note that after the heat treatment is performed on the oxide semiconductor film **303** to form the oxide semiconductor film **304**, heat treatment is performed on the oxide semiconductor film **304** under an oxygen atmosphere, whereby impurities such as moisture included in the oxide semiconductor film **304** can be removed. In addition, the heat treatment is performed under an oxygen atmosphere in order that the oxide semiconductor film **304** may include excessive oxygen, whereby resistance thereof can be increased. The heat treatment under an oxygen atmosphere for the oxide semiconductor film **104** described in Embodiment 1 may be referred to for the heat treatment under an oxygen atmosphere for the oxide semiconductor film **304**.

[0142] Next, as illustrated in FIG. **5**C, a channel protective film **305** is formed over the oxide semiconductor film **304** so as to overlap with a portion of the oxide semiconductor film **304**, which serves as a channel formation region later. The

channel protective film **305** can prevent the portion of the oxide semiconductor film **304**, which serves as a channel formation region later, from being damaged in a later step (for example, reduction in thickness due to plasma or an etchant in etching). Therefore, reliability of the thin film transistor can be improved.

[0143] The channel protective film **305** can be formed using an inorganic material including oxygen (such as silicon oxide, silicon oxynitride, or silicon nitride oxide). The channel protective film **305** can be formed by a vapor deposition method such as a plasma CVD method or a thermal CVD method, or a sputtering method. After the formation of the channel protective film **305**, the shape thereof is processed by etching. Here, the channel protective film **305** is formed in such a manner that a silicon oxide film is formed by a sputtering method and processed by etching using a mask formed by photolithography.

[0144] When the channel protective film **305** which is an oxide insulating film is formed in contact with the island-shaped oxide semiconductor film **304** by a sputtering method, a PCVD method, or the like, the carrier concentration of at least a region in the island-shaped oxide semiconductor film **304** in contact with the channel protective film **305** is reduced, preferably to lower than $1\times10^{18}/cm^3$, more preferably to $1\times10^{14}/cm^3$ or lower, so that the resistance of at least the region is increased. Thus, a high-resistance oxide semiconductor region can be formed. By the formation of the channel protective film **305**, the oxide semiconductor film **304** has a high-resistance oxide semiconductor region in the vicinity of the interface between the oxide semiconductor film **304** and the channel protective film **305**.

[0145] Next, a conductive film for a source electrode and a drain electrode is formed over the island-shaped oxide semiconductor film **304**. Then, the conductive film is processed (patterned) into a desired shape by etching or the like, whereby a source electrode **306** and a drain electrode **307** are formed in contact with the island-shaped oxide semiconductor film **304** as illustrated in FIG. **5**C. The material and the structure of the conductive film which is patterned for forming the source electrode **105** and the drain electrode **106** described in Embodiment 1 may be referred to for the material and the structure of the conductive film.

[0146] In this embodiment, a conductive film for the source electrode and the drain electrode is formed to a thickness of 200 nm by a sputtering method using a molybdenum target, and then, the conductive film is processed (patterned) into a desired shape by etching; in such a manner, the source electrode **306** and the drain electrode **307** are formed.

[0147] FIG. **6**A is a top view of the semiconductor device in FIG. **5**C. FIG. **5**C corresponds to a cross-sectional view taken along dashed line C**1**-C**2** in FIG. **6**A.

[0148] Next, as illustrated in FIG. **5**D, an oxide insulating film **308** is formed over the island-shaped oxide semiconductor film **304**, the source electrode **306**, and the drain electrode **307** by a sputtering method. The oxide insulating film **308** is formed over the low-resistance island-shaped oxide semiconductor film **304** and formed using an inorganic insulating film which includes impurities such as moisture, hydrogen, oxygen, and a hydroxy group as little as possible and blocks entry of these impurities from the outside, specifically, a silicon oxide film, a silicon nitride oxide film, or the like.

[0149] In this embodiment, a silicon oxide film with a thickness of 300 nm is formed as the oxide insulating film **308**. The substrate temperature at the time of the film formation may be higher than or equal to room temperature and lower than or equal to 300° C., and is set at 100° C. in this embodiment. Formation of the silicon oxide film by a sputtering method can be performed under a rare gas (for example, argon) atmosphere, an oxygen atmosphere, or an atmosphere including a rare gas (for example, argon) and oxygen. Further, a silicon oxide target or a silicon target may be used as a target. For example, with use of a silicon target, a silicon oxide film can be formed by a sputtering method under an atmosphere including oxygen and nitrogen.

[0150] Next, as illustrated in FIG. **5**D, a conductive film is formed over the oxide insulating film **308** with use of one or more metals that easily absorb or adsorb moisture, a hydroxy group, or hydrogen, and then, the conductive film is patterned, whereby a back gate electrode **309** is formed to overlap with the oxide semiconductor film **304**. The material and the structure of the back gate electrode **109** described in Embodiment 1 may be referred to for the material and the structure of the back gate electrode **309**.

[0151] In this embodiment, a conductive film of 200 nm thick is formed using $TiCr_2$ by a sputtering method under the following conditions: an alloy that is a target (ϕ:6 inches) whose composition ratio of titanium to chromium is 1:2 is used; an argon gas is introduced into a chamber with a flow rate of 50 scan; the pressure is 0.4 Pa; the electric power is 2 kW; and the film formation temperature is room temperature. Then, a photolithography step is performed. A resist mask is formed, and an unnecessary portion is removed by plasma etching with use of chlorine and oxygen as an etching gas so that the conductive film is processed (patterned) into a desired shape; in such a manner, the back gate electrode **309** is formed.

[0152] Next, after the back gate electrode **309** is formed, heat treatment is performed under a reduced-pressure atmosphere or an inert gas atmosphere in the state where the back gate electrode **309** is exposed, whereby activation treatment for removing moisture, oxygen, hydrogen, or the like adsorbed onto a surface of or in the back gate electrode **309** is performed. The condition of the activation treatment for the back gate electrode **109** described in Embodiment 1 can be referred to for the condition of the activation treatment.

[0153] By the above activation treatment, impurities such as moisture, a hydroxy group, and hydrogen which are present, for example, in the oxide semiconductor film **304**, in the gate insulating film **302**, at the interface between the oxide semiconductor film **304** and the gate insulating film **302** and its vicinity, or at the interface between the oxide semiconductor film **304** and the oxide insulating film **308** and its vicinity are absorbed or adsorbed by the back gate electrode **309** which has been activated; therefore, deterioration in the characteristics of the transistor due to the impurities can be prevented.

[0154] In addition, impurities such as moisture and hydrogen included in an atmosphere in which the semiconductor device is placed can be prevented from being taken into the oxide semiconductor film **304**.

[0155] In this embodiment, heat treatment is performed for 10 minutes in the state where the substrate temperature reaches 400° C. and a treatment chamber is kept to a reduced-pressure atmosphere having a degree of vacuum of 5×10^{-3} Pa or less, preferably 10^{-5} Pa or less by an evacuation unit such as a turbo molecular pump.

[0156] Note that heat treatment for activation is performed in the state where the oxide semiconductor film **304** is in

contact with the channel protective film **305**. Therefore, a region of the oxide semiconductor film **304** in contact with the channel protective film **305** uniformly has higher resistance; thus, variation in electric characteristics of a thin film transistor **311** can be reduced.

[0157] Next, after the activation treatment is performed, an insulating film **310** is formed so as to cover the back gate electrode **309** as illustrated in FIG. **5**E. The insulating film **310** is preferably formed using a material having a high barrier property so that moisture and oxygen in the atmosphere are prevented from being adsorbed onto the surface of or in the back gate electrode **309**. The material and the structure of the insulating film **110** described in Embodiment 1 may be referred to for the material and the structure of the insulating film **310**.

[0158] In this embodiment, an insulating film is formed to a thickness of 300 nm by a plasma CVD method. The insulating film is formed under the following conditions: the flow rate of a silane gas is 4 sccm; the flow rate of dinitrogen monoxide (N_2O) is 800 sccm; and the substrate temperature is 400° C.

[0159] By the formation of the insulating film **310**, moisture and oxygen in the atmosphere can be prevented from being adsorbed onto the surface of or in the back gate electrode **309**; therefore, the back gate electrode **309** can be kept to be activated, and reliability of the transistor can be increased.

[0160] FIG. **6**B is a top view of the semiconductor device in FIG. **5**E. FIG. **5**E corresponds to a cross-sectional view taken along dashed line **C1**-**C2** in FIG. **6**B.

[0161] The thin film transistor **311** includes the gate electrode **301**; the gate insulating film **302** over the gate electrode **301**; the oxide semiconductor film **304** over the gate insulating film **302**; the channel protective film **305**, the source electrode **306**, and the drain electrode **307** over the oxide semiconductor film **304**; the oxide insulating film **308** over the channel protective film **305**, the source electrode **306**, and the drain electrode **307**; and the back gate electrode **309** over the oxide insulating film **308**. The back gate electrode **309** is formed to overlap with the oxide semiconductor film **304**, whereby impurities such as moisture, a hydroxy group, and hydrogen which are present, for example, in the oxide semiconductor film **304**, in the gate insulating film **302**, at the interface between the oxide semiconductor film **304** and the gate insulating film **302** and its vicinity, or at the interface between the oxide semiconductor film **304** and the oxide insulating film **308** and its vicinity are absorbed or adsorbed by the back gate electrode **309** which has been activated; therefore, deterioration in the characteristics of the transistor due to the impurities can be prevented. In addition, impurities such as moisture and hydrogen included in the atmosphere in which the semiconductor device is placed can be prevented from being taken into the oxide semiconductor film **304**.

[0162] Note that in FIG. **6**B, an example in which the back gate electrode **309** covers the whole oxide semiconductor film **304** is shown; however, the present invention is not limited to this structure. Since the back gate electrode **309** covers the whole oxide semiconductor film **304**, an effect of reducing the impurities in the oxide semiconductor film **304** can be enhanced. However, the above effect can be obtained also in the case where at least the entire portion serving as a channel formation region in the oxide semiconductor film **304** or part of the portion overlaps with the back gate electrode **309**.

[0163] Further, the back gate electrode **309** may be electrically insulated and in a floating state, or may be in a state where the back gate electrode **309** is supplied with a potential. In the case of the latter, the back gate electrode **309** may be supplied with the same potential as the gate electrode **301**, or may be supplied with a fixed potential such as a ground potential. The level of the potential supplied to the back gate electrode **309** is controlled, whereby the threshold voltage of the thin film transistor **311** can be controlled. Note that in the case where the back gate electrode **309** is formed using a metal material having low electrical conductivity such as $TiCr_2$, a conductive film having low resistance is formed in contact with the back gate electrode **309** and the combined resistance of these conductive films is low; in such a manner, increase in power consumption due to the parasitic resistance may be prevented.

[0164] The step of performing heat treatment for activating the back gate electrode **309** and the step of forming the insulating film **310** in contact with the back gate electrode **309** are successively performed without exposure to air (such a process is also referred to as successive treatment or an insitu process), whereby moisture or oxygen in an atmosphere can be prevented from being adsorbed onto the surface of or in the back gate electrode **309**. As a result, the back gate electrode **309** can be kept to be activated, and the reliability of the thin film transistor **311** can be more increased.

[0165] Note that a substrate transfer step, an alignment step, a heating or cooling step, or the like may be provided between the step of performing heat treatment for activating the back gate electrode **309** and the step of forming the insulating film **310** in contact with the back gate electrode **309**. Such a process is also within the scope of the successive treatment in this specification. However, the following case is not within the scope of the successive treatment in this specification: there is a step in which liquid is used, such as a cleaning step, a wet etching step, or a resist formation step between the above two steps.

[0166] Note that in this embodiment, although an example in which the back gate electrode **309** is formed using one or more metals that easily absorb or adsorb moisture, a hydroxy group, or hydrogen is described, the gate electrode **301** may be formed using one or more metals that easily absorb or adsorb moisture, a hydroxy group, or hydrogen. In this case, after the gate electrode **301** is formed, the gate electrode **301** may be subjected to heat treatment for activation under the same condition as the back gate electrode **309**. The gate electrode **301** is formed using a metal having the above characteristics, whereby impurities such as moisture, a hydroxy group, or hydrogen which are present, for example, in the oxide semiconductor film **304**, in the gate insulating film **302**, at the interface between the oxide semiconductor film **304** and the gate insulating film **302** and its vicinity, or at the interface between the oxide semiconductor film **304** and the oxide insulating film **308** and its vicinity are absorbed or adsorbed by the gate electrode **301** which has been activated; therefore, deterioration in the characteristics of the transistor due to the impurities can be prevented.

[0167] This embodiment can be implemented in combination with another embodiment as appropriate.

Embodiment 4

[0168] In this embodiment, a method for manufacturing a semiconductor display device according to one embodiment of the present invention will be described with reference to

FIGS. **7**A to **7**C, FIGS. **8**A to **8**C, FIGS. **9**A to **9**C, FIG. **10**, FIG. **11**, FIG. **12**, and FIG. **13**.

[0169] In FIG. **7**A, as a substrate **400** having a light-transmitting property, any of a variety of glass substrates that are used in the electronics industry such as aluminosilicate glass, barium borosilicate glass, and aluminoborosilicate glass can be used. A substrate formed from a flexible synthetic resin, such as plastic, generally tends to have a low upper temperature limit, but can be used as the substrate **400** as long as the substrate can withstand processing temperatures in the manufacturing process performed later. Examples of a plastic substrate include polyester typified by polyethylene terephthalate (PET), polyethersulfone (PES), polyethylene naphthalate (PEN), polycarbonate (PC), polyetheretherketone (PEEK), polysulfone (PSF), polyetherimide (PEI), polyarylate (PAR), polybutylene terephthalate (PBT), polyimide, acrylonitrile-butadiene-styrene resin, polyvinyl chloride, polypropylene, polyvinyl acetate, acrylic resin, and the like.

[0170] Next, a conductive film is formed over an entire surface of the substrate **400**, and then a first photolithography step is performed. A resist mask is formed, and then an unnecessary portion is removed by etching, so that wirings and electrodes (a gate wiring including a gate electrode **401**, a capacitor wiring **408**, and a first terminal **421**) are formed. At this time, the etching is performed so that at least an end portion of the gate electrode **401** has a tapered shape.

[0171] The conductive film can be formed to have a single-layer structure or a stacked-layer structure using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, neodymium, or scandium; an alloy material which contains any of these metal materials as its main component; or a nitride which contains any of these metals. Note that for the conductive film, aluminum or copper can also be used as the above metal material as long as it can withstand the temperature of heat treatment performed later.

[0172] For example, as a two-layer structure of the conductive film, a two-layer structure in which a titanium nitride film and a molybdenum film are stacked is preferable. As a three-layer structure of the conductive film, a three-layer structure in which a tungsten film or a tungsten nitride film, an aluminum-silicon alloy film or an aluminum-titanium alloy film, and a titanium nitride film or a titanium film are stacked is preferable.

[0173] Next, as illustrated in FIG. **7**B, a gate insulating film **402** is formed over the gate electrode **401**, the capacitor wiring **408**, and the first terminal **421**. The gate insulating film **402** is formed to a thickness of 50 nm to 250 nm by a sputtering method, a PCVD method, or the like.

[0174] For example, as the gate insulating film **402**, a silicon oxide film is formed to a thickness of 100 nm by a sputtering method. Needless to say, the gate insulating film **402** is not necessarily formed using such a silicon oxide film and may be formed to have a single-layer structure or a stacked-layer structure using another insulating film such as a silicon oxynitride film, a silicon nitride film, an aluminum oxide film, a tantalum oxide film, or the like.

[0175] Next, an island-shaped oxide semiconductor film (an In—Ga—Zn—O-based non-single-crystal film) **403** is formed over the gate insulating film **402**. It is effective to form the In—Ga—Zn—O-based non-single-crystal film without exposure to air after the plasma treatment because dust and moisture do not adhere to the interface between the gate insulating film **402** and the oxide semiconductor film **403**. Here, the oxide semiconductor film **403** is formed in an argon atmosphere, an oxygen atmosphere, or an atmosphere including both argon and oxygen under the conditions where the target is an oxide semiconductor target including In, Ga, and Zn (an In—Ga—Zn—O-based oxide semiconductor target (In_2O_3:Ga_2O_3:ZnO=1:1:1)) with a diameter of 8 inches, the distance between the substrate **400** and the target is set to 170 mm, the pressure is set at 0.4 Pa, and the direct current (DC) power supply is set at 0.5 kW. Note that a pulse direct current (DC) power supply is preferable because dust can be reduced and the film thickness can be uniform. The In—Ga—Zn—O-based non-single-crystal film is formed to have a thickness of 5 nm to 200 nm. In this embodiment, as the oxide semiconductor film **403**, for example, a 50-nm-thick In—Ga—Zn—O-based non-single-crystal film is fainted by a sputtering method using an In—Ga—Zn—O-based oxide semiconductor target.

[0176] The oxide semiconductor film **403** for forming a channel formation region may be formed using an oxide material having semiconductor characteristics described above.

[0177] Examples of the sputtering method include an RF sputtering method in which a high-frequency power source is used as a sputtering power source, a DC sputtering method, and a pulsed DC sputtering method in which a bias is applied in a pulsed manner. An RF sputtering method is mainly used in the case where an insulating film is formed, and a DC sputtering method is mainly used in the case where a metal film is formed.

[0178] In addition, there is a multi-source sputtering apparatus in which a plurality of targets of different materials can be set. With the multi-source sputtering apparatus, films of different materials can be formed to be stacked in the same chamber, or a film of plural kinds of materials can be deposited by electric discharge at the same time in the same chamber.

[0179] In addition, there are a sputtering apparatus provided with a magnet system inside the chamber and used for a magnetron sputtering, and a sputtering apparatus used for an ECR sputtering in which plasma generated with the use of microwaves is used without using glow discharge.

[0180] Furthermore, as a deposition method using sputtering, there are also a reactive sputtering method in which a target substance and a sputtering gas component are chemically reacted with each other during deposition to form a thin compound film thereof, and a bias sputtering in which a voltage is also applied to a substrate during deposition.

[0181] Next, a second photolithography step is performed. A resist mask is formed, and then the oxide semiconductor film is etched so that the shape of the island-shaped oxide semiconductor film **403** can be processed. For example, an unnecessary portion is removed by wet etching using a mixed solution of phosphoric acid, acetic acid, and nitric acid, so that the island-shaped oxide semiconductor film **403** is formed to overlap with the gate electrode **401**. Note that etching here is not limited to wet etching, and dry etching may also be performed.

[0182] As the etching gas for dry etching, a gas containing chlorine (chlorine-based gas such as chlorine (Cl_2), boron chloride (BCl_3), silicon chloride ($SiCl_4$), or carbon tetrachloride (CCl_4)) is preferably used.

[0183] Alternatively, a gas containing fluorine (fluorine-based gas such as carbon tetrafluoride (CF_4), sulfur fluoride (SF_6), nitrogen fluoride (NF_3), or trifluoromethane (CHF_3));

hydrogen bromide (HBO; oxygen (O_2); any of these gases to which a rare gas such as helium (He) or argon (Ar) is added; or the like can be used.

[0184] As the dry etching method, a parallel plate RIE (reactive ion etching) method, an ICP (inductively coupled plasma) etching method, or the like can be used. In order to etch the films into desired shapes, the etching condition (the amount of electric power applied to a coil-shaped electrode, the amount of electric power applied to an electrode on a substrate side, the temperature of the electrode on the substrate side, or the like) is adjusted as appropriate.

[0185] As an etchant used for wet etching, ITO-07N (produced by KANTO CHEMICAL CO., INC.) may be used.

[0186] The etchant used in the wet etching is removed by cleaning together with the material which is etched off. Waste liquid of the etchant containing the removed material may be purified and the material contained in the waste liquid may be reused. When a material such as indium included in the oxide semiconductor film is collected from the waste liquid after the etching and reused, the resources can be efficiently used and the cost can be reduced.

[0187] The etching conditions (such as an etchant, etching time, and temperature) are appropriately adjusted depending on the material so that the material can be etched into a desired shape.

[0188] Next, the oxide semiconductor film **403** is subjected to heat treatment under a reduced-pressure atmosphere, an inert gas atmosphere such as a nitrogen atmosphere or a rare gas atmosphere, an oxygen atmosphere, or an ultra-dry air (i.e., air having a moisture content of 20 ppm (−55° C. by dew-point conversion) or less, preferably 1 ppm or less, more preferably 10 ppb or less in the case where the measurement is performed with use of a CRDS (cavity-ring-down spectroscopy) type dew-point meter) atmosphere, whereby an oxide semiconductor film **404** is formed. Specifically, the island-shaped oxide semiconductor film **403** is subjected to heat treatment at higher than or equal to 400° C. and lower than or equal to 700° C., preferably higher than or equal to 450° C. and lower than or equal to 650° C. under an inert gas (such as nitrogen, helium, neon, or argon) atmosphere. Then, the heated island-shaped oxide semiconductor film is slowly cooled to a temperature which is higher than or equal to room temperature and less than 100° C. under an inert atmosphere. By heat treatment performed on the oxide semiconductor film **403** under the above-described atmosphere, moisture, hydrogen, and a hydroxy group included in the oxide semiconductor film **403** are eliminated. Therefore, deterioration in characteristics of a thin film transistor in which the oxide semiconductor film **404** serves as a channel formation region due to the above impurities can be prevented.

[0189] For the heat treatment, a heating method using an electric furnace or an instantaneous heating method such as a gas rapid thermal anneal (GRTA) method using a heated gas or a lamp rapid thermal anneal (LRTA) method using lamp light can be used. For example, in the case of performing heat treatment using an electric furnace, the temperature rise characteristics are preferably set at higher than or equal to 0.1° C./min and lower than or equal to 20° C./min and the temperature drop characteristics are preferably set at higher than or equal to 0.1° C./min and lower than or equal to 15° C./min.

[0190] Note that in the heat treatment, it is preferable that moisture, hydrogen, and the like be not contained in nitrogen or a rare gas such as helium, neon, or argon. Alternatively, it is preferable that nitrogen or a rare gas such as helium, neon, or argon introduced into an apparatus for heat treatment have a purity of 6N (99.9999%) or more, preferably, 7N (99.99999%) or more (that is, the impurity concentration is set to 1 ppm or lower, preferably, 0.1 ppm or lower).

[0191] Alternatively, the heat treatment may be performed under air where the dew point under an atmospheric pressure is −60° C. or lower and the moisture content is small, instead of an inert gas atmosphere such as a nitrogen atmosphere or a rare gas atmosphere.

[0192] The island-shaped oxide semiconductor film **404** which is formed through the heat treatment under an inert gas atmosphere may be partially crystallized.

[0193] Note that after the heat treatment is performed on the oxide semiconductor film **404**, heat treatment is performed on the oxide semiconductor film **404** under an oxygen atmosphere, whereby impurities such as moisture included in the oxide semiconductor film **404** can be removed. In addition, the heat treatment is performed under an oxygen atmosphere in order that the oxide semiconductor film **404** may include excessive oxygen, whereby resistance thereof can be increased. The heat treatment is performed at a temperature where a metal having a low melting point such as Zn included in the oxide semiconductor is less likely to be evaporated, for example, higher than or equal to 100° C. and lower than 350° C., preferably higher than or equal to 150° C. and lower than 250° C. It is preferable that an oxygen gas used for the heat treatment under an oxygen atmosphere do not include moisture, hydrogen, or the like. Alternatively, an oxygen gas which is introduced into the heat treatment apparatus preferably has a purity of 6N (99.9999%) or more, more preferably 7N (99.99999%) or more (that is, the impurity concentration in oxygen is 1 ppm or lower, preferably 0.1 ppm or lower).

[0194] Cross-sectional views taken along dashed lines D**1**-D**2** and E**1**-E**2** in FIG. **7**C correspond to cross-sectional views taken along dashed lines D**1**-D**2** and E**1**-E**2** in a plan view illustrated in FIG. **10**, respectively.

[0195] Next, as illustrated in FIG. **8**A, a conductive film **406** is formed using a metal material over the oxide semiconductor film **404** by a sputtering method or a vacuum evaporation method. As a material of the conductive film **406**, an element selected from chromium, tantalum, titanium, molybdenum, tungsten, zirconium, beryllium, thorium, manganese, or magnesium, an alloy containing one or more of these elements as its component, or the like can be given. In order to further improve heat resistance to heat treatment which is to be performed after a source electrode **407***a* and a drain electrode **407***b* are formed, the conductive film **406** may be formed in combination of the above material with a heat resistant conductive material such as neodymium, scandium, or a nitride of these elements.

[0196] Next, a third photolithography step is performed. A resist mask is formed, and unnecessary portions are removed by etching, so that the source electrode **407***a*, the drain electrode **407***b*, and a second terminal **420** are formed as illustrated in FIG. **8**B. Wet etching or dry etching is employed as an etching method at this time. For example, when a molybdenum film is used as the conductive film **406**, wet etching using a solution including phosphoric acid as an etchant can be carried out.

[0197] In this etching step, an exposed region of the oxide semiconductor film **404** is also partly etched in some cases. In this case, an oxide semiconductor film **409** has a region whose thickness is small between the source electrode **407***a* and the drain electrode **407***b*.

[0198] In this third photolithography step, the second terminal **420** which is formed using the same material as the source electrode **407**_a_ or the drain electrode **407**_b_ is left in a terminal portion. Note that the second terminal **420** is electrically connected to a source wiring (a source wiring including the source electrode **407**_a_ or the drain electrode **407**_b_).

[0199] Further, by use of a resist mask having regions with plural thicknesses (e.g., two different thicknesses) which is formed using a multi-tone mask, the number of resist masks can be reduced, resulting in simplified process and lower costs.

[0200] Next, the resist mask is removed, and then, the oxide semiconductor film **409** may be again subjected to heat treatment under a reduced-pressure atmosphere, an inert gas atmosphere such as a nitrogen atmosphere or a rare gas atmosphere, an oxygen atmosphere, or an ultra-dry air (i.e., air having a moisture content of 20 ppm (−55° C. by dew-point conversion) or less, preferably 1 ppm or less, more preferably 10 ppb or less in the case where the measurement is performed with use of a CRDS (cavity-ring-down spectroscopy) type dew-point meter) atmosphere in order to eliminate moisture, hydrogen, and a hydroxy group included in the oxide semiconductor film **409**. In consideration of heat resistance of the source electrode **407**_a_ and the drain electrode **407**_b_, the heat treatment after the source electrode **407**_a_ and the drain electrode **407**_b_ are formed is preferably performed at a temperature lower than the temperature of the heat treatment before the source electrode **407**_a_ and the drain electrode **407**_b_ are formed. Specifically, the heat treatment after the source electrode **407**_a_ and the drain electrode **407**_b_ are formed may be performed at higher than or equal to 350° C. and lower than or equal to 650° C., preferably higher than or equal to 400° C. and lower than or equal to 600° C.

[0201] Cross-sectional views taken along dashed lines D**1**-D**2** and E**1**-E**2** in FIG. **8**B correspond to cross-sectional views taken along dashed lines D**1**-D**2** and E**1**-E**2** in a plan view illustrated in FIG. **11**, respectively.

[0202] Next, as illustrated in FIG. **8**C, an oxide insulating film **411** which covers the gate insulating film **402**, the oxide semiconductor film **409**, the source electrode **407**_a_, and the drain electrode **407**_b_ is formed. The oxide insulating film **411** is formed using a silicon oxynitride film by a PCVD method. The oxide insulating film **411** which is a silicon oxynitride film and an exposed region of the oxide semiconductor film **409** which is provided between the source electrode **407**_a_ and the drain electrode **407**_b_ are in contact with each other, whereby the resistance of a region of the oxide semiconductor film **409** in contact with the oxide insulating film **411** is increased (i.e., the carrier concentration is reduced, preferably to lower than $1\times10^{18}/cm^3$). Thus, a high-resistance channel formation region can be formed.

[0203] Heat treatment may be performed after formation of the oxide insulating film **411**. The treatment may be performed in an air atmosphere or a nitrogen atmosphere at higher than or equal to 350° C. and lower than or equal to 650° C., preferably higher than or equal to 400° C. and lower than or equal to 600° C. In such heat treatment, the oxide semiconductor film **409** in the state of being in contact with the oxide insulating film **411** is heated, which leads to increase in resistance of the oxide semiconductor film **409**; thus, electric characteristics of the transistor can be improved and variation in electric characteristics can be reduced. There is no particular limitation on the timing of the heat treatment as long as it is performed after the oxide insulating film **411** is formed. When this heat treatment also serves as heat treatment in another step, e.g., heat treatment in formation of a resin film or heat treatment for reducing resistance of a transparent conductive film, the number of steps can be prevented from increasing.

[0204] Next, as illustrated in FIG. **9**A, a conductive film is formed over the oxide insulating film **411** with use of one or more metals that easily absorb or adsorb moisture, a hydroxy group, or hydrogen, and then, the conductive film is patterned, whereby a back gate electrode **412** is formed to overlap with the oxide semiconductor film **409**. Specifically, as the metal having such characteristics, titanium, platinum, vanadium, zirconium, hafnium, palladium, magnesium, niobium, a rare earth metal, or the like can be given. As the rare earth metal, an alloy including cerium (40% to 50%), lanthanum (20% to 40%), and a rare earth metal such as praseodymium, neodymium, or yttrium, which is called a misch metal (Mm), can also be used. The back gate electrode **412** may be a mixture, a metal compound, or an alloy which includes one or more of the above metals.

[0205] As the alloy used for the back gate electrode **412**, an alloy called a hydrogen absorbing alloy can also be given. As the hydrogen absorbing alloy, for example, an AB_5 alloy, an AB_2 (Laves phase) alloy, an A_2B alloy, or the like can be given. In the AB_5 alloy, one or more of a rare earth metal, niobium, and zirconium are included in A site, and one or more transition metals having a catalytic effect such as nickel, cobalt, aluminum, and tin are included in B site. As the rare earth metal, a misch metal can also be used. As the AB_5 alloy, for example, $LaNi_5$ or the like can be used for the back gate electrode **412**. In the AB_2 (Laves phase) alloy, one or more of titanium, zirconium, and hafnium are included in A site, and one or more transition metals such as manganese, nickel, chromium, and vanadium are included in B site; for example, a Ti—Mn-based alloy, a Ti—Cr-based alloy, a Zr—Mn-based alloy, a Ti—V—Mn-based alloy, or the like can be given. As the AB_2 alloy, for example, $TiCr_2$, $TiMn_2$, or the like can be used for the back gate electrode **412**. In the A_2B alloy, one or more of magnesium and titanium are included in A site, and one or more of nickel and copper are included in B site. As the A_2B alloy, for example, Mg_2Ni, Mg_2Cu, Ti_2Ni, or the like can be used for the back gate electrode **412**. Note that in these hydrogen absorbing alloys, at least part of an element in A site or B site can be replaced with another element, and the actual composition is not necessarily in due form. As the hydrogen absorbing alloy, in addition to the above type alloys, a Ti—Fe alloy, a V-type alloy, a Pd-type alloy, a Ca-type alloy, a BCC alloy, or the like can be used for the back gate electrode **412**.

[0206] The thickness of the back gate electrode **412** is set to 10 nm to 400 nm, preferably 100 nm to 200 nm. In this embodiment, a conductive film of 200 nm thick is formed using $TiCr_2$ by a sputtering method under the following conditions: an alloy that is a target (ϕ:6 inches) whose composition ratio of titanium to chromium is 1:2 is used; an argon gas is introduced into a chamber with a flow rate of 50 sccm; the pressure is 0.4 Pa; the electric power is 2 kW; and the film formation temperature is room temperature. Then, a photolithography step is performed. A resist mask is formed, and an unnecessary portion is removed by plasma etching with use of chlorine and oxygen as an etching gas so that the conductive film is processed (patterned) into a desired shape; in such a manner, the back gate electrode **412** is formed.

[0207] Next, after the back gate electrode **412** is formed, heat treatment is performed under a reduced-pressure atmo-

sphere or an inert gas atmosphere in the state where the back gate electrode **412** is exposed, whereby activation treatment for removing moisture, oxygen, hydrogen, or the like adsorbed onto a surface of or in the back gate electrode **412** is performed. In consideration of the heat resistance of the source electrode **407***a* and the drain electrode **407***b*, the heat treatment is preferably performed at a temperature lower than the temperature of the heat treatment before the source electrode **407***a* and the drain electrode **407***b* are formed. Specifically, the heat treatment is performed at higher than or equal to 300° C. and lower than or equal to 650° C., preferably higher than or equal to 350° C. and lower than or equal to 600° C.

[0208] By the activation treatment, impurities such as moisture, a hydroxy group, or hydrogen which are present, for example, in the oxide semiconductor film **409**, in the gate insulating film **402**, at the interface between the oxide semiconductor film **409** and the gate insulating film **402** and its vicinity, or at the interface between the oxide semiconductor film **409** and the oxide insulating film **411** and its vicinity are absorbed or adsorbed by the back gate electrode **412** which has been activated; therefore, deterioration in the characteristics of the transistor due to the impurities can be prevented.

[0209] In addition, impurities such as moisture or hydrogen included in an atmosphere in which the semiconductor device is placed can be prevented from being taken into the oxide semiconductor film **409**.

[0210] In this embodiment, heat treatment is performed for 10 minutes in the state where the substrate temperature reaches 400° C. and a treatment chamber is kept to a reduced-pressure atmosphere having a degree of vacuum of 5×10^{-3} Pa or less, preferably 10^{-5} Pa or less by an evacuation unit such as a turbo molecular pump. For the heat treatment, a heating method using an electric furnace or an instantaneous heating method such as a gas rapid thermal anneal (GRTA) method using a heated gas or a lamp rapid thermal anneal (LRTA) method using lamp light can be used. For example, in the case of performing heat treatment using an electric furnace, the temperature rise characteristics are preferably set at higher than or equal to 0.1° C./min and lower than or equal to 20° C./min and the temperature drop characteristics are preferably set at higher than or equal to 0.1° C./min and lower than or equal to 15° C./min.

[0211] Note that heat treatment for activation is performed in the state where the oxide semiconductor film **409** is in contact with the oxide insulating film **411**. Therefore, a region of the oxide semiconductor film **409** in contact with the oxide insulating film **411** uniformly has higher resistance; thus, variation in electric characteristics of a thin film transistor **414** can be reduced.

[0212] Next, after the activation treatment is performed, an insulating film **413** is formed so as to cover the back gate electrode **412** as illustrated in FIG. **9**B. The insulating film **413** is preferably formed using a material having a high barrier property so that moisture and oxygen in the atmosphere are prevented from being adsorbed onto the surface of or in the back gate electrode **412**. For example, the insulating film **413** can be formed to have a single-layer structure or a stacked-layer structure of a silicon nitride film, a silicon nitride oxide film, an aluminum nitride film, or an aluminum nitride oxide film, or the like, as an insulating film having a high barrier property, by a plasma CVD method, a sputtering method, or the like. In order to obtain an effect of a barrier property, the insulating film **413** is preferably formed to a thickness of 15 nm to 400 nm, for example.

[0213] In this embodiment, the insulating film **413** is formed to a thickness of 300 nm by a plasma CVD method. The insulating film **413** is formed under the following conditions: the flow rate of a silane gas is 4 sccm; the flow rate of dinitrogen monoxide (N_2O) is 800 sccm; and the substrate temperature is 400° C.

[0214] By the formation of the insulating film **413**, moisture and oxygen in the atmosphere can be prevented from being adsorbed onto the surface of or in the back gate electrode **412**; therefore, the back gate electrode **412** can be kept to be activated, and reliability of the transistor can be increased.

[0215] Cross-sectional views taken along dashed lines D**1**-D**2** and E**1**-E**2** in FIG. **9**B correspond to cross-sectional views taken along dashed lines D**1**-D**2** and E**1**-E**2** in a plan view illustrated in FIG. **12**, respectively.

[0216] Through the above steps, the thin film transistor **414** can be manufactured.

[0217] Next, a fourth photolithography step is performed. A resist mask is formed, and the gate insulating film **402**, the oxide insulating film **411**, and the insulating film **413** are etched, so that contact holes are formed to expose part of the drain electrode **407***b*, part of the first terminal **421**, part of the second terminal **420**, and part of the back gate electrode **412**. Next, the resist mask is removed, and then a transparent conductive film is formed. The transparent conductive film is formed of indium oxide (In_2O_3), indium oxide-tin oxide alloy (In_2O_3—SnO_2, abbreviated to ITO), or the like by a sputtering method, a vacuum evaporation method, or the like. Such a material is etched with a hydrochloric acid-based solution. However, since a residue is easily generated particularly in etching ITO, indium oxide-zinc oxide alloy (In_2O_3—ZnO) may be used to improve etching processability. Further, when heat treatment for reducing resistance of the transparent conductive film is performed, the heat treatment can also serve as heat treatment for increasing resistance of the oxide semiconductor film **409**, which results in improvement of electric characteristics of the transistor and reduction of variation in the electric characteristics thereof.

[0218] Next, a fifth photolithography step is performed. A resist mask is formed and an unnecessary portion is removed by etching, so that a pixel electrode **415** which is connected to the drain electrode **407***b*, a transparent conductive film **416** which is connected to the first terminal **421**, a transparent conductive film **417** which is connected to the second terminal **420**, and a transparent conductive film **418** which is connected to the back gate electrode **412** are formed.

[0219] The transparent conductive films **416** and **417** function as electrodes or wirings connected to an FPC. The transparent conductive film **416** formed over the first terminal **421** is a connection terminal electrode which functions as an input terminal of the gate wiring. The transparent conductive film **417** formed over the second terminal **420** is a connection terminal electrode which functions as an input terminal of the source wiring. The transparent conductive film **418** is a wiring for supplying the back gate electrode **412** with a power supply potential.

[0220] In this fifth photolithography step, a storage capacitor **419** is formed with the capacitor wiring **408** and the pixel electrode **415**, in which the gate insulating film **402**, the oxide insulating film **411**, and the insulating film **413** are used as dielectrics.

[0221] Cross-sectional views after the resist mask is removed are illustrated in FIG. **9**C. Cross-sectional views taken along dashed lines D**1**-D**2** and E**1**-E**2** in FIG. **9**C correspond to cross-sectional views taken along dashed lines D**1**-D**2** and E**1**-E**2** in a plan view illustrated in FIG. **13**, respectively.

[0222] Through these five photolithography steps, the storage capacitor **419** and the thin film transistor **414** which is a bottom-gate staggered thin film transistor can be completed using the five photomasks. By disposing the thin film transistor and the storage capacitor in each pixel in a pixel portion in which pixels are arranged in a matrix form, one of substrates for manufacturing an active matrix display device can be obtained. In this specification, such a substrate is referred to as an active matrix substrate for convenience.

[0223] In the case of manufacturing an active matrix liquid crystal display device, an active matrix substrate and a counter substrate provided with a counter electrode are bonded to each other with a liquid crystal layer interposed therebetween.

[0224] Instead of providing the capacitor wiring, the pixel electrode may be overlapped with a gate wiring of an adjacent pixel with the oxide insulating film and the gate insulating film interposed therebetween, to form a storage capacitor.

[0225] In an active matrix liquid crystal display device, pixel electrodes arranged in a matrix form are driven, so that a display pattern is formed on a screen. Specifically, voltage is applied between a selected pixel electrode and a counter electrode corresponding to the pixel electrode, so that a liquid crystal layer provided between the pixel electrode and the counter electrode is optically modulated and this optical modulation is recognized as a display pattern by an observer.

[0226] When a light-emitting display device is manufactured, a partition formed using an organic resin film may be provided between organic light-emitting elements in some cases. In such a case, the organic resin film is subjected to heat treatment, and the heat treatment can also serve as heat treatment for increasing resistance of the oxide semiconductor film **409**, which results in improvement of electric characteristics of the transistor and reduction of variation in the electric characteristics thereof.

[0227] The use of an oxide semiconductor for a thin film transistor leads to reduction in manufacturing cost. In particular, since impurities such as moisture, hydrogen, and OH can be reduced for increasing purity of the oxide semiconductor film by the heat treatment, it is not necessary to use an ultrapure oxide semiconductor target and a special sputtering apparatus provided with a deposition chamber whose dew point is lowered. Further, a semiconductor display device including a highly reliable thin film transistor with excellent electric characteristics can be manufactured.

[0228] The channel formation region in the semiconductor film is a high-resistance region; thus, electric characteristics of the thin film transistor are stabilized and increase in off current can be prevented. Therefore, a semiconductor display device including a thin film transistor having high electric characteristics and high reliability can be provided.

[0229] This embodiment can be implemented in combination with any of the above embodiments.

Embodiment 5

[0230] In this embodiment, a structure of a liquid crystal display device according to one embodiment of the present invention will be described.

[0231] FIG. **14** illustrates a cross-sectional view of a liquid crystal display device according to one embodiment of the present invention, as an example. A thin film transistor **1401** illustrated in FIG. **14** includes a gate electrode **1402** formed on an insulating surface; a gate insulating film **1403** formed so as to cover the gate electrode **1402**; an oxide semiconductor film **1404** formed so as to overlap with the gate electrode **1402** with the gate insulating film **1403** interposed therebetween; a pair of semiconductor films **1405** functioning as a source region and a drain region, which are formed over the oxide semiconductor film **1404**; a pair of conductive films **1406** functioning as a source electrode and a drain electrode, which are formed over the pair of semiconductor films **1405**; an oxide insulating film **1407**; and a back gate electrode **1408** formed over the oxide insulating film **1407**. The back gate electrode **1408** is covered with an insulating film **1409**. The oxide insulating film **1407** is in contact with at least the oxide semiconductor film **1404** and formed so as to cover the gate electrode **1402**, the gate insulating film **1403**, the oxide semiconductor film **1404**, the pair of semiconductor films **1405**, and the pair of conductive films **1406**.

[0232] An opening is provided in part of the oxide insulating film **1407** and the insulating film **1409**, and a pixel electrode **1410** is formed so as to be in contact with one of the conductive films **1406** in the opening.

[0233] Further, a spacer **1417** for controlling a cell gap of a liquid crystal element is formed over the pixel electrode **1410**. An insulating film is etched to have a desired shape, so that the spacer **1417** can be formed. A cell gap may also be controlled by dispersing a filler on the insulating film **1409**.

[0234] An alignment film **1411** is formed over the pixel electrode **1410**. The alignment film **1411** can be formed by subjecting an insulating film to rubbing treatment, for example. Further, a counter electrode **1413** is provided in a position opposed to the pixel electrode **1410**, and an alignment film **1414** is formed on the side of the counter electrode **1413**, which is close to the pixel electrode **1410**. Furthermore, a liquid crystal **1415** is provided in a region which is surrounded by a sealant **1416** between the pixel electrode **1410** and the counter electrode **1413**. Note that a filler may be mixed in the sealant **1416**.

[0235] The pixel electrode **1410** and the counter electrode **1413** can be formed using a transparent conductive material such as indium tin oxide including silicon oxide (ITSO), indium tin oxide (ITO), zinc oxide (ZnO), indium zinc oxide (IZO), or gallium-doped zinc oxide (GZO), for example. Note that this embodiment describes an example of manufacturing a transmissive type liquid crystal element by using a light-transmitting conductive film for the pixel electrode **1410** and the counter electrode **1413**. However, the present invention is not limited to this structure. The liquid crystal display device according to one embodiment of the present invention may be a semi-transmissive type liquid crystal display device or a reflective type liquid crystal display device.

[0236] The liquid crystal display device illustrated in FIG. **14** may be provided with a color filter, a shielding film (a black matrix) for preventing disclination (a black matrix), or the like.

[0237] Although a liquid crystal display device of a TN (twisted nematic) mode is described in this embodiment, the thin film transistor of the present invention can be used for other liquid crystal display devices of a VA (vertical alignment) mode, an OCB (optically compensated birefringence) mode, an IPS (in-plane-switching) mode, and the like.

[0238] The liquid crystal display device according to one embodiment of the present invention has high reliability.

[0239] This embodiment can be implemented in combination with another embodiment as appropriate.

Embodiment 6

[0240] In this embodiment, a structure of a light-emitting device including the thin film transistor according to one embodiment of the present invention for a pixel will be described. In this embodiment, a cross-sectional structure of a pixel in the case where a transistor for driving a light-emitting element is an n-channel transistor is described with reference to FIGS. **15**A to **15**C. Note that FIGS. **15**A to **15**C illustrate the case where a first electrode is a cathode and a second electrode is an anode; however, the first electrode may be an anode and the second electrode may be a cathode.

[0241] A cross-sectional view of a pixel in the case where a transistor **6031** is an n-channel transistor, and light emitted from a light-emitting element **6033** is extracted from a first electrode **6034** side is illustrated in FIG. **15**A. The transistor **6031** is covered with an insulating film **6037**, and over the insulating film **6037**, a bank **6038** having an opening is formed. In the opening of the bank **6038**, the first electrode **6034** is partially exposed, and the first electrode **6034**, an electroluminescent layer **6035**, and a second electrode **6036** are sequentially stacked in the opening.

[0242] The first electrode **6034** is formed using such a material or to such a thickness as to transmit light, and can be formed using a metal, an alloy, an electrically conductive compound, a mixture thereof, or the like having a low work function. Specifically, an alkaline metal such as Li or Cs, an alkaline earth metal such as Mg, Ca, or Sr, an alloy containing such metals (e.g., Mg:Ag, Al:Li, or Mg:In), a compound of such materials (e.g., calcium fluoride or calcium nitride), or a rare-earth metal such as Yb or Er can be used. Further, in the case where an electron-injection layer is provided, another conductive layer such as an aluminum layer may be used as well. Then, the first electrode **6034** is formed to such a thickness as to transmit light (preferably, about 5 nm to 30 nm). Furthermore, the sheet resistance of the first electrode **6034** may be suppressed by formation of a light-transmitting conductive layer of a light-transmitting oxide conductive material so as to be in contact with and over or under the above-described conductive layer having such a thickness that it can transmit light. Alternatively, the first electrode **6034** may be formed of only a conductive layer of another light-transmitting oxide conductive material such as indium tin oxide (ITO), zinc oxide (ZnO), indium zinc oxide (IZO), or gallium-doped zinc oxide (GZO). Furthermore, a mixture in which zinc oxide (ZnO) is mixed at 2% to 20% in ITO, indium tin oxide including silicon oxide (hereinafter referred to as ITSO), or indium oxide including silicon oxide may be used as well. In the case of using the light-transmitting oxide conductive material, it is preferable to provide an electron-injection layer in the electroluminescent layer **6035**.

[0243] The second electrode **6036** is formed using such a material and to such a thickness as to reflect or shield light, and formed using a material suitable for being used as an anode. For example, a single-layer film including one or more of titanium nitride, zirconium nitride, titanium, tungsten, nickel, platinum, chromium, silver, aluminum, and the like, a stacked layer of a titanium nitride film and a film including aluminum as a main component, a three-layer structure of a titanium nitride film, a film including aluminum as a main component, and a titanium nitride film, or the like can be used for the second electrode **6036**.

[0244] The electroluminescent layer **6035** is formed with a single layer or a plurality of layers. When the electroluminescent layer **6035** is formed with a plurality of layers, these layers can be classified into a hole-injection layer, a hole-transport layer, a light-emitting layer, an electron-transport layer, an electron-injection layer, and the like in view of the carrier-transport property. However, in the case where the electroluminescent layer **6035** has any of a hole-injection layer, a hole-transport layer, an electron-transport layer, and an electron-injection layer in addition to the light-emitting layer, the electron-injection layer, the electron-transport layer, the light-emitting layer, the hole-transport layer, and the hole-injection layer are sequentially stacked from the first electrode **6034**. Note that the boundary between the layers is not necessarily clear, and there may be the case where the boundary is unclear since materials for forming the layers are partially mixed with each other. Each layer may be formed with an organic material or an inorganic material. As an organic material, any of a high molecular weight organic material, a medium molecular weight organic material, and a low molecular weight organic material may be used. Note that a medium molecular weight organic material corresponds to a low polymer in which the number of repetitions of a structural unit (the degree of polymerization) is about 2 to 20. There is no clear distinction between a hole-injection layer and a hole-transport layer, and the hole-injection layer and the hole-transport layer are the same in a sense that a hole-transport property (hole mobility) is an especially important characteristic. A layer being in contact with the anode is referred to as a hole-injection layer and a layer being in contact with the hole-injection layer is referred to as a hole-transport layer for convenience. The same is also true for the electron-transport layer and the electron-injection layer; a layer being in contact with the cathode is referred to as an electron-injection layer and a layer being in contact with the electron-injection layer is referred to as an electron transport-layer. In some cases, the light-emitting layer also functions as the electron-transport layer, and it is therefore referred to as a light-emitting electron-transport layer, too.

[0245] In the case of the pixel illustrated in FIG. **15**A, light emitted from the light-emitting element **6033** can be extracted from the first electrode **6034** side as shown by a hollow arrow.

[0246] Next, a cross-sectional view of a pixel in the case where a transistor **6041** is an n-channel transistor, and light emitted from a light-emitting element **6043** is extracted from a second electrode **6046** side is illustrated in FIG. **15**B. The transistor **6041** is covered with an insulating film **6047**, and over the insulating film **6047**, a bank **6048** having an opening is formed. In the opening of the bank **6048**, a first electrode **6044** is partially exposed, and the first electrode **6044**, an electroluminescent layer **6045**, and the second electrode **6046** are sequentially stacked in the opening.

[0247] The first electrode **6044** is formed using such a material or to such a thickness as to reflect or shield light, and can be formed using a metal, an alloy, an electrically conductive compound, a mixture thereof, or the like having a low work function. Specifically, an alkaline metal such as Li or Cs, an alkaline earth metal such as Mg, Ca, or Sr, an alloy containing such metals (e.g., Mg:Ag, Al:Li, or Mg:In), a compound of such materials (e.g., calcium fluoride or calcium nitride), or a rare-earth metal such as Yb or Er can be

used. Further, in the case where an electron-injection layer is provided, another conductive layer such as an aluminum layer may be used as well.

[0248] The second electrode **6046** is formed using such a material or to such a thickness as to transmit light, and formed using a material suitable for being used as an anode. For example, another light-transmitting oxide conductive material such as indium tin oxide (ITO), zinc oxide (ZnO), indium zinc oxide (IZO), or gallium-doped zinc oxide (GZO) can be used for the second electrode **6046**. Further, a mixture in which zinc oxide (ZnO) is mixed at 2% to 20% in ITO, ITSO, or indium oxide including silicon oxide may be used as well for the second electrode **6046**. Furthermore, a single-layer film including one or more of titanium nitride, zirconium nitride, titanium, tungsten, nickel, platinum, chromium, silver, aluminum, and the like, a stacked layer of a titanium nitride film and a film including aluminum as a main component, a three-layer structure of a titanium nitride film, a film including aluminum as a main component, and a titanium nitride film, or the like can be used for the second electrode **6046**. However, in the case of using a material other than the light-transmitting oxide conductive material, the second electrode **6046** is formed to such a thickness as to transmit light (preferably, about 5 nm to 30 nm).

[0249] The electroluminescent layer **6045** can be formed in a manner similar to that of the electroluminescent layer **6035** of FIG. **15**A.

[0250] In the case of the pixel illustrated in FIG. **15**B, light emitted from the light-emitting element **6043** can be extracted from the second electrode **6046** side as shown by a hollow arrow.

[0251] Next, a cross-sectional view of a pixel in the case where a transistor **6051** is an re-channel transistor, and light emitted from a light-emitting element **6053** is extracted from a first electrode **6054** side and a second electrode **6056** side is illustrated in FIG. **15**C. The transistor **6051** is covered with an insulating film **6057**, and over the insulating film **6057**, a bank **6058** having an opening is formed. In the opening of the bank **6058**, the first electrode **6054** is partially exposed, and the first electrode **6054**, an electroluminescent layer **6055**, and the second electrode **6056** are sequentially stacked in the opening.

[0252] The first electrode **6054** can be formed in a manner similar to that of the first electrode **6034** of FIG. **15**A. The second electrode **6056** can be formed in a manner similar to that of the second electrode **6046** of FIG. **15**B. The electroluminescent layer **6055** can be formed in a manner similar to that of the electroluminescent layer **6035** of FIG. **15**A.

[0253] In the case of the pixel illustrated in FIG. **15**C, light emitted from the light-emitting element **6053** can be extracted from the first electrode **6054** side and the second electrode **6056** side as shown by hollow arrows.

[0254] This embodiment can be implemented in combination with another embodiment as appropriate.

Embodiment 7

[0255] In this embodiment, a structure of a liquid crystal display device according to one embodiment of the present invention will be described.

[0256] FIG. **16** illustrates an example of a perspective view showing a structure of a liquid crystal display device of the present invention. The liquid crystal display device shown in FIG. **16** is provided with a liquid crystal panel **1601** in which a liquid crystal element is formed between a pair of substrates, a first diffusing plate **1602**, a prism sheet **1603**, a second diffusing plate **1604**, a light guide plate **1605**, a reflection plate **1606**, a light source **1607**, and a circuit substrate **1608**.

[0257] The liquid crystal panel **1601**, the first diffusing plate **1602**, the prism sheet **1603**, the second diffusing plate **1604**, the light guide plate **1605**, and the reflection plate **1606** are sequentially stacked. The light source **1607** is provided at an end portion of the light guide plate **1605**. The liquid crystal panel **1601** is uniformly irradiated with light from the light source **1607** which is diffused inside the light guide plate **1605** due to the first diffusing plate **1602**, the prism sheet **1603**, and the second diffusing plate **1604**.

[0258] Although the first diffusing plate **1602** and the second diffusing plate **1604** are used in this embodiment, the number of diffusing plates is not limited to two. The number of diffusing plates may be one, or may be three or more. It is acceptable as long as the diffusing plate is provided between the light guide plate **1605** and the liquid crystal panel **1601**. Therefore, a diffusing plate may be provided only on the side closer to the liquid crystal panel **1601** than the prism sheet **1603**, or may be provided only on the side closer to the light guide plate **1605** than the prism sheet **1603**.

[0259] Further, the cross section of the prism sheet **1603** is not limited to a sawtooth shape shown in FIG. **16**. The prism sheet **1603** is acceptable as long as it has a shape with which light from the light guide plate **1605** can be concentrated on the liquid crystal panel **1601** side.

[0260] The circuit substrate **1608** is provided with a circuit which generates various kinds of signals input to the liquid crystal panel **1601**, a circuit which processes the signals, or the like. In FIG. **16**, the circuit substrate **1608** and the liquid crystal panel **1601** are connected to each other through an FPC (flexible printed circuit) **1609**. Note that the circuit may be connected to the liquid crystal panel **1601** by using a chip on glass (COG) method, or part of the circuit may be connected to the FPC **1609** by using a chip on film (COF) method.

[0261] FIG. **16** illustrates an example in which the circuit substrate **1608** is provided with a controlling circuit which controls driving of the light source **1607** and the controlling circuit and the light source **1607** are connected to each other through an FPC **1610**. Note that the above-described controlling circuit may be formed over the liquid crystal panel **1601**. In that case, the liquid crystal panel **1601** and the light source **1607** are connected to each other through an FPC or the like.

[0262] Note that although FIG. **16** illustrates an edge-light type light source where the light source **1607** is provided on the edge of the liquid crystal panel **1601**, a direct type light source where the light source **1607** are provided directly below the liquid crystal panel **1601** may be used.

[0263] This embodiment can be implemented in combination with any of the above embodiments as appropriate.

EXAMPLE

[0264] By using a semiconductor display device according to one embodiment of the present invention, a highly reliable electronic device can be provided.

[0265] Moreover, by using a semiconductor display device of the present invention, the heat treatment temperature in manufacturing steps can be suppressed; therefore, a highly reliable thin film transistor with excellent characteristics can be formed even when the thin film transistor is formed over a substrate formed using a flexible synthetic resin which has lower heat resistance than glass, such as plastic. Accordingly,

with the use of the manufacturing method according to one embodiment of the present invention, a highly reliable, lightweight, and flexible semiconductor display device with low power consumption can be provided. Examples of a plastic substrate include polyester typified by polyethylene terephthalate (PET), polyethersulfone (PES), polyethylene naphthalate (PEN), polycarbonate (PC), polyetheretherketone (PEEK), polysulfone (PSF), polyetherimide (PEI), polyarylate (PAR), polybutylene terephthalate (PBT), polyimide, acrylonitrile-butadiene-styrene resin, polyvinyl chloride, polypropylene, polyvinyl acetate, acrylic resin, and the like.

[0266] The semiconductor display device according to one embodiment of the present invention can be used for display devices, laptops, or image reproducing devices provided with recording media (typically, devices which reproduce the content of recording media such as digital versatile discs (DVDs) and have displays for displaying the reproduced images). Besides, examples of the electronic device that can use a semiconductor display device according to one embodiment of the present invention include mobile phones, portable game machines, portable information terminals, e-book readers, cameras such as video cameras or digital still cameras, display goggles (head-mounted displays), navigation systems, audio reproducing devices (car audio systems, digital audio players, or the like), copying machines, facsimiles, printers, versatile printers, automated teller machines (ATMs), vending machines, and the like. Specific examples of these electronic devices are illustrated in FIGS. **17**A to **17**E.

[0267] FIG. **17**A illustrates an e-book reader including a housing **7001**, a display portion **7002**, and the like. The semiconductor display device according to one embodiment of the present invention can be used for the display portion **7002**. The use of the semiconductor display device according to one embodiment of the present invention for the display portion **7002** can provide a highly reliable e-book reader. Moreover, with the use of a flexible substrate, the semiconductor display device used for the display portion **7002** can have flexibility. Thus, a highly reliable, flexible, lightweight, and useful display device can be provided.

[0268] FIG. **17**B illustrates a display device including a housing **7011**, a display portion **7012**, a supporting base **7013**, and the like. The semiconductor display device according to one embodiment of the present invention can be used for the display portion **7012**. The use of the semiconductor display device according to one embodiment of the present invention for the display portion **7012** can provide a highly reliable display device. Note that the display device includes all of information display devices for personal computers, TV receivers, advertisement displays, and the like.

[0269] FIG. **17**C illustrates a display device including a housing **7021**, a display portion **7022**, and the like. The semiconductor display device according to one embodiment of the present invention can be used for the display portion **7022**. The use of the semiconductor display device according to one embodiment of the present invention for the display portion **7022** can provide a highly reliable display device. Moreover, with the use of a flexible substrate, the semiconductor display device, the signal processing circuit, or the like included in the display portion **7022** can have flexibility. Thus, a highly reliable, flexible, and lightweight display device can be provided. Accordingly, as illustrated in FIG. **17**C, the display device can be used while being fixed to fabric or the like, and an application range of the semiconductor display device is dramatically widened.

[0270] FIG. **17**D illustrates a portable game machine including a housing **7031**, a housing **7032**, a display portion **7033**, a display portion **7034**, a microphone **7035**, speakers **7036**, an operation key **7037**, a stylus **7038**, and the like. The semiconductor display device according to one embodiment of the present invention can be used for the display portion **7033** and the display portion **7034**. The use of the semiconductor display device according to one embodiment of the present invention for the display portion **7033** and the display portion **7034** can provide a highly reliable portable game machine. Note that although the portable game machine illustrated in FIG. **17**D includes two display portions **7033** and **7034**, the number of display portions included in the portable game machine is not limited to two.

[0271] FIG. **17**E illustrates a mobile phone including a housing **7041**, a display portion **7042**, an audio-input portion **7043**, an audio-output portion **7044**, operation keys **7045**, a light-receiving portion **7046**, and the like. Light received in the light-receiving portion **7046** is converted into electrical signals, whereby external images can be loaded. The semiconductor device according to one embodiment of the present invention can be used for the display portion **7042**. The use of the semiconductor display device according to one embodiment of the present invention for the display portion **7042** can provide a highly reliable mobile phone.

[0272] This example can be implemented in combination with any of the above embodiments as appropriate.

[0273] This application is based on Japanese Patent Application serial no. 2009-229323 filed with Japan Patent Office on Oct. 1, 2009, the entire contents of which are hereby incorporated by reference.

1. A semiconductor device comprising:

a gate electrode on an insulating surface;

a gate insulating film over the gate electrode;

an oxide semiconductor film over the gate insulating film;

a source electrode and a drain electrode over the oxide semiconductor film;

an insulating film over the oxide semiconductor film, the source electrode, and the drain electrode and in contact with the oxide semiconductor film; and

a back gate electrode over the insulating film and overlapping with the gate electrode and the oxide semiconductor film,

wherein the back gate electrode includes a hydrogen absorbing alloy.

2. The semiconductor device according to claim **1**, wherein the hydrogen absorbing alloy is at least one of $LaNi_5$, Ti—Mn-based alloy, a Ti—Cr-based alloy, a Zr—Mn-based alloy, a Ti—V—Mn-based alloy, Mg_2Ni, Mg_2Cu, and Ti_2Ni.

3. The semiconductor device according to claim **1**, wherein the insulating film is an oxide insulating film.

4. The semiconductor device according to claim **1**, further comprising an insulating film over the back gate electrode.

5. A semiconductor device comprising:

a gate electrode on an insulating surface;

a gate insulating film over the gate electrode;

a source electrode and a drain electrode over the gate insulating film;

an oxide semiconductor film over the source electrode and the drain electrode;

an insulating film over the oxide semiconductor film, the source electrode, and the drain electrode and in contact with the oxide semiconductor film; and

a back gate electrode over the insulating film and overlapping with the gate electrode and the oxide semiconductor film,

wherein the back gate electrode includes a hydrogen absorbing alloy.

6. The semiconductor device according to claim **5**, wherein the hydrogen absorbing alloy is at least one of $LaNi_5$, Ti—Mn-based alloy, a Ti—Cr-based alloy, a Zr—Mn-based alloy, a Ti—V—Mn-based alloy, Mg_2Ni, Mg_2Cu, and Ti_2Ni.

7. The semiconductor device according to claim **5**, wherein the insulating film is an oxide insulating film.

8. The semiconductor device according to claim **5**, further comprising an insulating film over the back gate electrode.

9. A semiconductor device comprising:

a gate electrode on an insulating surface;

a gate insulating film over the gate electrode;

an oxide semiconductor film over the gate insulating film;

a channel protective film over the oxide semiconductor film;

a source electrode and a drain electrode over the oxide semiconductor film;

an insulating film over the channel protective film, the source electrode, and the drain electrode; and

a back gate electrode over the insulating film and overlapping with the gate electrode and the oxide semiconductor film,

wherein the back gate electrode includes a hydrogen absorbing alloy.

10. The semiconductor device according to claim **9**, wherein the hydrogen absorbing alloy is at least one of $LaNi_5$, Ti—Mn-based alloy, a Ti—Cr-based alloy, a Zr—Mn-based alloy, a Ti—V—Mn-based alloy, Mg_2Ni, Mg_2Cu, and Ti_2Ni.

11. The semiconductor device according to claim **9**, wherein the insulating film is an oxide insulating film

12. The semiconductor device according to claim **9**, further comprising an insulating film over the back gate electrode.

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