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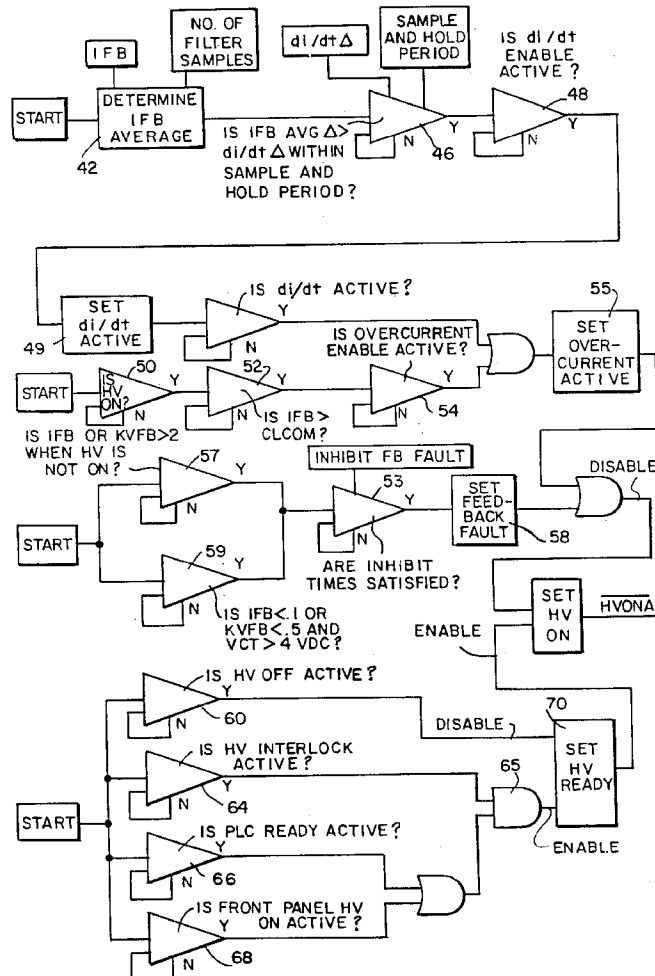
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(54) **SYSTEME DE COMMANDE D'ALIMENTATION**

(54) **POWER SUPPLY CONTROL SYSTEM**



(57) Alimentation haute tension constituée : d'un premier circuit générant un premier signal correspondant à une haute tension de sortie désirée dans une paire de bornes de sortie de l'alimentation; d'un second circuit générant un second signal correspondant à un courant de sortie d'alimentation de la haute tension; et d'un troisième

(57) Disclosed is a high magnitude potential supply comprising a first circuit for generating a first signal related to a desired output high magnitude potential across a pair of output terminals of the supply, a second circuit for generating a second signal related to an output current from the high magnitude potential supply, and a





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circuit assurant l'application d'une tension de fonctionnement à l'alimentation haute tension afin qu'elle puisse produire la haute tension de fonctionnement. Le troisième circuit comprend une borne de commande. Un quatrième circuit est couplé au premier et au second circuits, ainsi qu'à la borne de commande. Le quatrième circuit reçoit le premier signal et le second signal provenant du premier et du second circuits et commande la tension de fonctionnement appliquée à l'alimentation haute tension par le troisième circuit. Un cinquième circuit permet de couper de façon sélective la tension de fonctionnement appliquée à l'alimentation haute tension afin de l'empêcher de générer la haute tension. Le cinquième circuit est également couplé à la borne de commande.

third circuit for supplying an operating potential to the high magnitude potential supply so that it can produce the high magnitude operating potential. The third circuit has a control terminal. A fourth circuit is coupled to the first and second circuits and to the control terminal. The fourth circuit receives the first and second signals from the first and second circuits and controls the operating potential supplied to the high magnitude potential supply by the third circuit. A fifth circuit is provided to selectively disable the supply of operating potential to the high magnitude potential supply so that no high magnitude operating potential can be supplied by it. The fifth circuit is also coupled to the control terminal.

POWER SUPPLY CONTROL SYSTEM**ABSTRACT OF THE DISCLOSURE**

Disclosed is a high magnitude potential supply comprising a first circuit for generating a first signal related to a desired output high magnitude potential across a pair of output terminals of the supply, a second circuit for generating a second signal related to an output current from the high magnitude potential supply, and a third circuit for supplying an operating potential to the high magnitude potential supply so that it can produce the high magnitude operating potential. The third circuit has a control terminal. A fourth circuit is coupled to the first and second circuits and to the control terminal. The fourth circuit receives the first and second signals from the first and second circuits and controls the operating potential supplied to the high magnitude potential supply by the third circuit. A fifth circuit is provided to selectively disable the supply of operating potential to the high magnitude potential supply so that no high magnitude operating potential can be supplied by it. The fifth circuit is also coupled to the control terminal.

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-1-

POWER SUPPLY CONTROL SYSTEMBackground of the Invention

This invention relates to controllers for high magnitude potential sources used in, for example, electrostatically aided coating material atomization and dispensing devices. Many such systems are known. There are, for example, the systems illustrated
5 and described in U. S. Patents: 3,851,618; 3,875,892; 3,894,272; 4,075,677; 4,187,527; 4,324,812; 4,481,557; 4,485,427; 4,745,520; and, 5,159,544, to identify but a few.

Disclosure of the Invention

10 According to the invention, a high magnitude potential supply comprises a first circuit for generating a first signal related to a desired output high magnitude potential across a pair of output terminals of the supply, a second circuit for generating a second signal related to an output current from the high magnitude potential supply, and a third circuit for supplying an operating potential to the high magnitude potential supply so
15 that it can produce the high magnitude operating potential. The third circuit has a control terminal. A fourth circuit is coupled to the first and second circuits and to the control terminal. The fourth circuit receives the first and second signals from the first and second circuits and controls the operating potential supplied to the high magnitude potential supply by the third circuit. A fifth circuit is provided to selectively disable the supply of
20 operating potential to the high magnitude potential supply so that no high magnitude operating potential can be supplied by it. The fifth circuit is also coupled to the control terminal.

Illustratively, the first and second circuits comprise a programmable logic controller (PLC), and a high speed bus for coupling the PLC to the fourth circuit.

25 Additionally illustratively, the first and second circuits respectively comprise first and second potentiometers for selecting a desired output high magnitude potential and output current, respectively, and conductors for coupling the first and second potentiometers to the fourth circuit.

Further illustratively, first and second switches selectively couple one of
30 the PLC and the first potentiometer, and one of the PLC and the second potentiometer, respectively, to the fourth circuit.

3030-29010

-2-

Additionally illustratively according to the invention, the third circuit comprises a high magnitude potential transformer having a primary winding and a secondary winding. The primary winding has a center tap and two end terminals. Third and fourth switches are coupled to respective ones of the end terminals. A source of oppositely phased first and second switching signals controls the third and fourth switches, respectively.

Illustratively, the fourth circuit comprises a switching regulator having an input terminal forming a summing junction for the first signal and the second signal and an output terminal coupled to the center tap. The fifth circuit includes a microprocessor (μ P) and a fifth switch coupled to the μ P to receive a third switching signal from the μ P. The fifth switch is coupled to the summing junction to couple the third switching signal to the switching regulator to disable the supply of operating potential to the center tap.

Illustratively, the fifth switch is coupled to the summing junction through a filter which smooths the switching signals generated by the fifth switch in response to the μ P's control.

Further illustratively, the apparatus comprises a sixth circuit cooperating with the μ P to determine if operating potential is being supplied to the high magnitude potential supply, and a seventh circuit cooperating with the μ P to determine if the high magnitude potential supply is indicating that it is generating high magnitude potential. The μ P indicates a fault if the operating potential is not being supplied to the high magnitude potential supply and the high magnitude potential supply is indicating that it is generating high magnitude potential. Illustratively, the μ P also indicates a fault if the operating potential is being supplied to the high magnitude potential supply and the high magnitude potential supply is indicating that it is not generating high magnitude potential.

Brief Description of the Drawings

The invention may best be understood by referring to the following detailed description and accompanying drawings which illustrate the invention. In the drawings:

Figs. 1-2 illustrate flow diagrams useful in understanding the invention; and,

3030-29010

-3-

Figs. 3-5, 6a-i, 7a-f and 8 illustrate, in block and schematic form, circuits useful in understanding the invention.

Detailed Description of an Illustrative Embodiment

5 In the detailed descriptions that follow, several integrated circuits and other components are identified, with particular circuit types and sources. In many cases, terminal names and pin numbers for these specifically identified circuit types and sources are noted. This should not be interpreted to mean that the identified circuits are the only circuits available from the same, or any other, sources that will perform the described
10 functions. Other circuits are typically available from the same, and other, sources which will perform the described functions. The terminal names and pin numbers of such other circuits may or may not be the same as those indicated for the specific circuits identified in this application.

Flow diagrams of the routines which are executed by the μP 40 are
15 illustrated in Figs. 1-4. Referring particularly to Fig. 1, high voltage power supply ground return current feedback, IFB, and a number of filter samples are provided to a function 42 which calculates a current feedback average, IFB AVerage from these variables. A di/dt Δ setting is provided to the μP 40 from a display/set functions routine 44. di/dt Δ and the length of a sample and hold period are provided to a decision block 46 which determines
20 whether the change in IFB average, IFB AVG Δ , over the sample and hold period is greater than di/dt Δ . This decision block 46 continues to be interrogated until IFB AVGA is greater than di/dt Δ over the sample and hold period. Once this result is achieved, the routine next determines 48 if di/dt enable is active. This decision block 48 continues to be interrogated until di/dt enable is detected active. Once this decision 48 is achieved, di/dt
25 is set active at 49.

Another routine includes a decision block 50, "is High Voltage on?" This decision block 50 continues to be interrogated until HV is detected on. Once HV on is detected, a decision block 52 is reached, "is IFB greater than Current Limit COMmand?" Decision block 52 continues to be interrogated until IFB greater than CLCOM is
30 detected. A decision block 54 is then reached, "is overcurrent enable active?" Decision block 54 continues to be interrogated until overcurrent enable is detected active. Once either di/dt or overcurrent enable is achieved, overcurrent is set active at 55.

3030-29010

-4-

Another decision that will disable HV On will now be explained. There are certain occurrences in the feedback paths for output high voltage and ground return current to the high voltage supply that the system interprets as feedback faults. If any of these faults occurs, the system is disabled by the μ P 40. In the illustrated system, if IFB is greater than 2 μ A or KiloVoltFeedBack is greater than 2 KV, 57, after a preselected INHIBIT time interval 53 after initialization of the system, the μ P 40 interprets 58 this occurrence as a feedback fault and disables the system. This corresponds to the situation of an output with no input. Similarly, if IFB is less than .1 μ A or KVFB is less than .5 KV and the Voltage at the Center Tap of the high magnitude potential supply input transformer is greater than 4 volts DC, 59, after the passage of the INHIBIT interval, the μ P interprets 58 this occurrence as a feedback fault and disables the system. This corresponds to the situation of an input with no output.

Assuming that HV On is not disabled by either of these routines, the μ P 40 determines 60 if HV Off is active. This decision block 60 continues to be interrogated until HV Off is detected active. Once HV Off is detected active, Set HV On is disabled at 62. If HV On is not disabled along one of these paths, the μ P 40 next determines 64 if the system's Interlock is active. This decision block 64 continues to be interrogated until the interlock is detected active. The interlock active decision 64 gates 65 either the "Is Programmable Logic Controller Ready Active?" decision 66 or the "Is Front Panel HV On Active?" decision 68. Gating of either of these decisions 66, 68 by "Is Interlock Active?" 64 results 70 in the Setting of HV Ready. This results 72 in the Setting of HV On unless Set HV On has been disabled by Set Overcurrent Active 55 or Set FeedBack Fault 58.

Turning now to the regulation of the Voltage at the Center Tap, and with reference to Fig. 2, the μ P 40 first determines 74 if the function Voltage Ramp is enabled. This decision block 74 continues to be interrogated until V.Ramp is enabled. Once V.Ramp is enabled, the μ P 40 next determines 76 if KVFB Δ is greater than V.Ramp Δ . This decision block 76 continues to be interrogated until KVFB Δ is greater than V.Ramp Δ . Once this decision is detected, V.Ramp is set active at 78. This is one way that pulses can be furnished to the V Center Tap controller 80.

Pulses will also be sent to VCT controller 80 if the feedback current IFB is greater than the feedback current limit, I LIMit. This decision block is illustrated at 81.

3030-29010

-5-

A third way in which pulses will be sent to the VCT controller 80 is if di/dt is active. This decision is illustrated at 49. This state is detected as described above in connection with the discussion of Fig. 1. In the illustrated embodiment, this method may or may not be employed at the option 82 of the operator.

5 Pulses having pulsewidths and frequencies determined in a manner which will be described are supplied to the VCT shutdown switch 84. The output from the VCT shutdown switch 84 is an input to the VCT regulator IC 86. Other inputs to the VCT regulator IC 86 include the KVFB signal buffered by the KVFB buffer 88, and a commanded KV setting. Commanded KV COM may come from either of two sources, a
10 KV adjust potentiometer 90 on the front panel of the apparatus or from a PLC as one of the I/O functions 89. See also Fig. 3. To select KV adjust from among the I/O functions, the operator needs to select the remote position of a local/remote switch 96 on the front panel.

Turning now to the block diagrams of the two printed circuit boards that
15 comprise the system, the μ P board, Fig. 4, includes the μ P 40 itself, a display 100 and a high speed network I/O 102, such as a standard Control Area Network BUS (CANBUS) I/O. μ P 40 illustratively is a type 80C196KB-12 μ P. The μ P 40 A/D converts several inputs, including: the commanded KV setting, KVCOM, from the front panel; the commanded high magnitude potential supply output current limit, Current Limit
20 COMmand, from the front panel; the KV FeedBack signal from the output of the high magnitude potential supply; the ground return current feedback, IFB, at the high magnitude potential supply's ground connection; and, the magnitude of the center tap voltage, VCT, to the primary winding of the high magnitude potential supply's high voltage transformer. The μ P 40 generates from these inputs and others outputs including:
25 a Phase Lock ENable signal to enable the high magnitude potential supply's phase locked loop oscillator 112; a Corona SSeNSe signal to the VCT regulator 86; an Air Trigger control to trigger the flow of, for example, atomizing or shaping air to a pneumatically assisted atomizer 113 (Fig. 8), such as an automatic gun-type atomizer, or a rotary atomizer such as a bell- or disk-type atomizer; a Fluid Trigger control to trigger the flow
30 of, for example, coating material or solvent during a coating operation or color change, respectively; KV Set, which will be either KVCOM in the local control mode or the output high magnitude voltage setting commanded by a PLC in the remote control mode;

3030-29010

-6-

I Set which will be either CLCOM in the local control mode or the current setting commanded by a PLC in the remote control mode; and, the HV On signal which switches on the high magnitude potential supply 106 to the atomizing device 113.

The output printed circuit board, Fig. 5, includes: a buffer amplifier 114 which receives the IFB signal and outputs the buffered IFB signal to the μ P 40 and to an analog slope control circuit 116; and, buffer amplifier 88 which receives the KVFB signal and outputs the buffered KVFB signal to the μ P 40, to the analog slope control circuit 116, and to one throw 118a of a single pole, double throw primary/secondary feedback select switch 118. The pole 118b of the switch 118 is coupled through a scaling amplifier 120 to the FeedBack terminal of the VCT regulator 86. The output board also includes a KV Set input to the VCT regulator 86. The output terminal of the VCT regulator 86 is coupled through a buffer 122 to the center tap 108 of the primary winding of the high magnitude potential transformer. This terminal is also coupled through a scaling amplifier 124 to the remaining throw 118c of feedback select switch 118. Thus, the operator has the ability to select 118b the source of the voltage feedback signal to the voltage feedback input terminal of the VCT regulator 86 the operator can select either the VCT input voltage, appropriately scaled by amplifier 124 appearing at terminal 118c, or the high magnitude potential supply's output voltage, KVFB appearing at terminal 118a. The output printed circuit board also includes the VCT shutdown switch 84 which disables the VCT regulator 86 by switching the COMPensating input terminal of the VCT regulator 86 in response to the Corona SSense A signal from the μ P 40. The output board also includes the phase locked loop high magnitude potential supply oscillator 112, with its Phase Lock ENable and Phase Lock FeedBack inputs and its amplified 132, 134 outputs A and B to the two ends of the high magnitude potential supply's input transformer 133 primary winding 133a (Fig. 8).

Turning now to Figs. 6a-i, the partly block and partly schematic diagrams of the process board of the illustrated system, signals and operating potentials are coupled to and from the system's internal bus 140, Figs. 6a-c. μ P 40 includes an A/D port 0, Fig. 6d, which receives from bus 140 the VCT, IFB, KVCOM, PulseWidth Modulation CONTROL, BUFFERed IFB, CLCOM, and BUFFERed KVFB signals from the bus 140. These signals are applied through input circuitry including $270\ \Omega$ -- $.01\ \mu$ F RC circuits and back-to-back diode protection circuits to the P0.7--P0.1 terminals, respectively, of port 0.

3030-29010

-7-

Display 100 is driven by a display driver 142, Fig. 6e, coupled between port 1 of μ P 40 and display 100. Specifically, the P1.0--P1.5 terminals of μ P 40 are coupled to the 1D0--1D3, MODE, and Write terminals, respectively, of display driver 142. Display driver 142 illustratively is a type I CM7218A1 11 display driver.

5 The program executed by μ P 40 is stored in an EPROM 144, Figs. 6f-g. A static RAM 146 provides storage for the calculations made by μ P 40, as well as for data passed back and forth to and from a bus 148. EPROM 144 illustratively is a type 28F001BX EPROM. SRAM 146 illustratively is a type 43256 SRAM. The CANBUS I/O 102 includes a three-to-eight demultiplexer 150, Fig. 6h, whose outputs Q4--Q0
10 drive, among other things, the Corona SSeNSe A, Phase Lock ENable, FLuiD TRIGger, AIR TRIGger, and HVON A# lines, respectively, of the bus 148. Demultiplexer 150 illustratively is a type 74LS259 demultiplexer. The CANBUS I/O 102 also includes a serial-to-parallel/parallel-to-serial converter 154 and bus driver 156. The CAN+ and CAN- terminals of bus 148 are coupled to the BUS+ and BUS- terminals, respectively, of
15 bus driver 156. The RX1 and RX0 terminals, respectively, of the S-P/P-S converter 154 are coupled to the REFeRence and RX terminals, respectively, of the bus driver 156. The TX0 terminal of S-P/P-S converter 154 is coupled to the TX terminal of bus driver 156. S-P/P-S converter 154 illustratively is a type 82C200 S-P/P-S converter. The I/O functions include provisions for an RS232 interface. Consequently, the I/O also includes
20 an RS232-toTTL/TTL-to-RS232 interface 160, Fig. 6i. The TXD and RXD lines, terminals P2.0 and P2.1, respectively, of μ P 40 are coupled to the T2i and R2o terminals, respectively, of interface 160. The T2o and R2i terminals of interface 160 are coupled to the TX232 and RX232 lines, respectively, of the bus 148. Interface 160 illustratively is a type MAX232 interface.

25 Analog signals to the output board, Figs. 7a-f, are generated by a D/A converter 164, Fig. 6g, whose input port DB0--DB7 is coupled to the P3.0--P3.7 terminals, respectively, of μ P 40 via the system AD0--AD7 lines, respectively. The Vout A and Vout B terminals of D/A converter 164 form the KVSET and I SET lines, respectively, of the bus 148. D/A converter 164 illustratively is a type DAC8229 D/A
30 converter. The node address of μ P 40 on the CANBUS is established by an octal switch 166 and 10 K Ω pull-down resistors coupled via an octal latch 168 to the system AD0--AD7 lines. Octal latch 168 illustratively is a type 74ALS245 octal latch. The system is

designed to control a number of different types of power supplies, some using high-Q high magnitude power supply input transformers 133 as taught in U. S. Patent 5,159,544, and some using relatively lower-Q high magnitude power supply input transformers 133. The system needs to be able to identify the type of power supply it is controlling. A line, notRP1000 identifies the power supply being controlled by the illustrated system as one having a high-Q input transformer 133 or not. This line of the bus 148 instructs one bit of input to μ P 40 via one switch of a quad switch 171. Another switch of quad switch 171 is the system's manual HV On switch. Another quad switch 173 controls the system's initialization sequence. These switches are coupled via an octal latch 170 to the system AD0--AD7 lines. Latch 170 illustratively is a type 74ALS245 octal latch. The AD0--AD7 lines are also coupled to the D0--D7 terminals, respectively, of EPROM 144, the O0--O7 terminals, respectively, of SRAM 146, and the AD0--AD7 terminals, respectively, of P-S/S-P converter 154.

The AD0--AD7 lines are also coupled to the D0--D7 lines, respectively, of a buffer/latch 174, Fig. 6f. The output terminals Q0--Q7 of buffer/latch 174 are coupled to the system A0--A7 lines, respectively. Buffer/latch 174 illustratively is a type 74ALS573 buffer/latch. The system A0--A7 lines are coupled to the A0--A7 terminals of EPROM 144, respectively, and to the A0--A7 terminals of SRAM 146, respectively. The P4.0--P4.7 terminals of μ P 40 are coupled via the system A8--A15 lines, respectively, to the A8--A15 terminals, respectively, of EPROM 144, and the A8--A14 lines are also coupled to the A8--A14 terminals of SRAM 146, respectively. High Voltage On, High Voltage ReaDY, OverCURrent and FeedBack FauLT status is indicated to the operator by, among other things, LEDs coupled through appropriate amplifiers to respective ones of the HS0.3, HS0.2, HS0.1, HS0.0 terminals of μ P 40. An EEPROM 180, Fig. 6d, containing initializing parameters for the μ P 40 has its DO, DI, SK and CS terminals, respectively, coupled to the μ P 40's P2.4--P2.7 terminals. EEPROM 180 illustratively is a type 93C46 EEPROM. CANBUS ACTIVE and CANBUS ERROR status is indicated by, among other things, LEDs coupled through appropriate amplifiers, Fig. 6h, to the Q6 and Q7 terminals, respectively, of demultiplexer 150.

Referring now to Figs. 7a-f, the output board includes a phase locked loop IC 198, Fig. 7c, and the A and B drive transistors 132, 134, Fig. 7f. The SIG IN input to the PLL IC 198 is the PhaseLock FeedBack signal shaped by an RC circuit including a

3030-29010

-9-

.0047 μ F capacitor to ground and the series combination of a .01 μ F capacitor and a 1K Ω resistor. The SIG IN input terminal of PLL IC 198 is also coupled to the not Phase Lock IN A signal line. PLL IC 198 illustratively is a type CD4046 PLL IC. Transistors 132, 134 illustratively are type IFR540 FETs. The drive signal for transistor 132 is output
 5 from the VOUT terminal of the PLL IC 198 to the ClocK input terminal of a D flip-flop 200. The oppositely phased Q and notQ outputs of DFF 200 are coupled to two push-pull configured predriver transistor pairs 202, 204, respectively, the outputs of which are coupled through respective wave-shaping parallel RC circuits 206 to the gates of the respective A and B drive transistors 132, 134. The drains of the respective A and B drive
 10 transistors 132, 134 are coupled to the opposite ends, the Drive A and Drive B terminals, respectively, of the primary winding 133a of the input transformer 133 of the high magnitude potential supply, Fig. 8. The sources of transistors 132, 134 are coupled to the system's +24 VDC ground RETurn. D FF 200 illustratively is a type CD4013 D FF.
 15 Transistor pairs 202, 204 illustratively are type TPQ6002 transistor pairs. The remainder of the PLL circuit is generally as described in U. S. Patent 5,159,544.

Turning to Fig. 7b, the PC I SET signal, the current setting coming over to the system from the PLC, is coupled through a 100 K Ω input resistor to the non-inverting (+) input terminal of a difference amplifier 210. The + input terminal of amplifier 210 is
 20 coupled through a 49.9 K Ω resistor to ground. The Analog GrouND line of the system bus is coupled through a 100 K Ω input resistor to the inverting (-) input terminal of amplifier 210. The - input terminal of amplifier 210 is through a 49.9 K Ω feedback resistor to its output terminal. The output terminal of amplifier 210 is coupled through a normally closed pair 212a of relay 212 contacts to a terminal 214. The normally open
 25 pair 212b of contacts of relay 212 is coupled across terminal 214 and the wiper of a 1 K Ω potentiometer 218. This arrangement permits the operator to select either PLC control of the current setting of the system or front panel control of the current setting via potentiometer 218.

A similar configuration including an amplifier 220 permits the system
 30 operator to select either PLC control of the desired output high potential magnitude of the high magnitude potential supply. The PC KV SET signal line is coupled through a 100 K Ω input resistor to the + input terminal of amplifier 220. Series 49.9 K Ω resistors between + 5 VDC supply and ground bias the - input terminal of amplifier at + 2.5 VDC.

3030-29010

-10-

Analog GrouND is coupled through a 100 K Ω resistor to the -input terminal of amplifier 220. An RC parallel feedback circuit including a 25.5 K Ω resistor and a .01 μ F capacitor is coupled across the - input terminal and the output terminal of amplifier 220. The output terminal of amplifier 220 is coupled through the normally closed terminals 222a of a relay 222 to the KV COMmanded line of the system bus. This signal is alternately selectable at the operator's option with a DC voltage established on the + input terminal of a buffer amplifier 224. This DC voltage is established on the wiper of a 1K Ω potentiometer 226. Potentiometer 226 is in series with an 825 Ω resistor and a 500 Ω potentiometer between + 5 VDC and ground. The wiper of the 500 Ω potentiometer is also coupled to ground so that the 825 Ω resistor and the setting of the 500 Ω potentiometer establish the minimum output high magnitude potential settable by the operator at the system front panel. The output of amplifier 220 is selectively coupled across the normally open terminals 222b of relay 222 to the KV COM line. Amplifiers 210, 220 and 224 illustratively 3/4 of a type LF444CN quad amplifier.

Referring now to Fig. 7d, the IFB signal from the system bus is coupled to the + input terminal of amplifier 114 via a 47 K Ω input resistor. A .22 μ F capacitor is coupled between the + input terminal of amplifier 114 and ground. The output terminal of amplifier 114 is coupled to its - input terminal in buffer configuration, and forms the BUFFered IFB terminal which is coupled to the μ P 40. The KVFB signal from the system bus is coupled to the + input terminal of amplifier 88 via a 1 K Ω input resistor. The + input terminal of amplifier 88 is clamped between + .6 VDC and - 15.6 VDC by diodes 226, 228 on its + input terminal. The output terminal of amplifier 88 is coupled to its - input terminal in buffer configuration, and forms the BUFFered KVFB terminal which is coupled to the μ P 40. BUFFKVFB is also coupled to terminal 118a of PRIMARY/SECondary FeedBack switch 118. Terminal 118b of switch 118 is coupled to the - input terminal of scaling amplifier 120 via a 20 K Ω series resistor. The + input terminal of amplifier is biased at +5/3 VDC by a series 20 K Ω --10 K Ω voltage divider. The output terminal of amplifier 120, which forms the PulseWidth Modulator CONTrol line of the system bus, is coupled through a 1 K Ω series resistor to the control input terminal, pin 1, of a switching regulator IC VCT regulator 86. VCT appears across the I+ output terminal, pin 4, of IC 86 and ground. VCT is fed back through series .1 Ω , 5 W and 21.5 K Ω resistors to the - input terminal of scaling amplifier 124. The output

3030-29010

-11-

terminal of amplifier 124 is coupled to its - input terminal through a 15 K Ω feedback resistor, and to terminal 118c of switch 118. Amplifiers 88, 114, 120 and 124 illustratively are a type LF444CN quad amplifier. VCT regulator IC 86 illustratively is a type UC3524A switching regulator.

5 The analog slope control circuit 116 includes a difference amplifier 230, a difference amplifier 232 and a transistor 234. The - input terminal of amplifier 230 receives the BUFFKVFB signal via the wiper of a 100 K Ω potentiometer and a series 100 K Ω resistor from the output terminal of amplifier 88. A 100 K Ω feedback resistor is coupled between the output terminal and the - input terminal of amplifier 230. The
10 output terminal of amplifier 230 is coupled through a 100 K Ω resistor to the - input terminal of amplifier 232. BUFFIFB is also coupled to the - input terminal of amplifier 232 through a 100 K Ω resistor. The - input terminal of amplifier 232 is biased negative via a 100 K Ω resistor to the wiper of a 100 K Ω potentiometer in series between - 15 VDC and ground. The output terminal of amplifier 232 is coupled through a 100 Ω resistor to
15 the base of transistor 234. The collector of transistor 234 is coupled to ground and its emitter is coupled to the COMPensate terminal of IC 86. Amplifiers 230, 232 illustratively are a type LF442CN dual amplifier. Transistor 234 illustratively is a type 2N2907 bipolar transistor.

Referring again to Fig. 7e, the system bus Corona SSeNSe A terminal is
20 coupled to the gate of the VCT shutdown switch 84, and to ground through a 100 K Ω resistor. The drain of switch 84 is coupled through series 6.8 Ω and 390 Ω resistors 240, 242, respectively, to the COMP terminal of IC 86. A 100 μ F smoothing capacitor 244 is coupled between the junction of these resistors and ground. The pulsewidth modulated output Corona SSeNSe A signal from μ P 40 to the gate of switch 84 results in a DC
25 voltage across capacitor 244. This voltage is summed at the COMP terminal of IC 86 with the output signal from the analog slope control circuit 116. This signal can be provided to the COMP terminal of IC 86 in other ways. For example, μ P 40 has a D/A output port. The output signal on the μ P 40's D/A output port provides an even smoother signal than the Corona SSeNSe A output signal filtered by the filter 240, 242,
30 244 to the COMP terminal of IC 86. Using the pulsewidth modulated Corona SSeNSe A output signal from μ P 40, filtered by filter 240, 242, 244, or the D/A port of the μ P 40, permits added flexibility in applications in which more than one dispensing device 113 is

3030-29010

-12-

coupled to system. For example, in a single applicator 113 situation, a delay of, for example, one-half second before the achievement of full high magnitude potential can be tolerated by the system. Where multiple applicators 113 are coupled to a common high magnitude potential supply, however, attempting to raise the high magnitude potential to its full commanded value too rapidly can result in charging current greater than the static overload current I SET. μ P 40 gives the operator the flexibility to ramp the high magnitude potential up to full commanded value KV SET more slowly in these situations, resulting in fewer "nuisance" overcurrent conditions. Additionally, the slower ramping up to full commanded high voltage eases the stress on the high voltage cables which customarily couple the high magnitude supply to the coating dispensing devices 113. The OSCillator terminal of IC 86 is coupled through a series 1 K Ω resistor and 100 pF capacitor to the common emitters of transistor pair 204. Switch 84 illustratively is a type IRFD210 FET. IC 86 and its associated components function generally as described in U. S. Patent 4,745,520.

15 A source code listing of the program executed by μ P 40 is attached hereto as Exhibit A.

3030-29010

-13-

What is claimed is:

1. A high magnitude potential supply comprising a first circuit for generating a first signal related to a desired output high magnitude potential across a pair
5 of output terminals of the supply, a second circuit for generating a second signal related to an output current from the high magnitude potential supply, a third circuit for supplying an operating potential to the high magnitude potential supply so that it can produce the high magnitude operating potential, the third circuit having a control
10 terminal, a fourth circuit coupled to the first and second circuits and to the control terminal, the fourth circuit receiving the first and second signals from the first and second circuits and controlling the operating potential supplied to the high magnitude potential supply by the third circuit, and a fifth circuit for disabling the supply of operating potential to the high magnitude potential supply so that no high magnitude operating potential can be supplied by it, the fifth circuit also coupled to the control terminal.
15
2. The apparatus of claim 1 wherein the first circuit comprises a programmable logic controller (PLC), and a high speed bus for coupling the PLC to the fourth circuit.
- 20 3. The apparatus of claim 2 wherein the first circuit comprises a first potentiometer for selecting a desired output high magnitude potential, and a conductor for coupling the first potentiometer to the fourth circuit.
4. The apparatus of claim 3 further comprising a switch for selectively
25 coupling one of the PLC and the first potentiometer to the fourth circuit.
5. The apparatus of claim 1 wherein the first circuit comprises a first potentiometer for selecting a desired output high magnitude potential, and a conductor for coupling the first potentiometer to the fourth circuit.

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3030-29010

-14-

6. The apparatus of claim 1 wherein the second circuit comprises a programmable logic controller (PLC), and a high speed bus for coupling the PLC to the fourth circuit.

5 7. The apparatus of claim 6 wherein the second circuit comprises a first potentiometer for selecting a desired output current, and a conductor for coupling the first potentiometer to the fourth circuit.

8. The apparatus of claim 7 further comprising a first switch for
10 selectively coupling one of the PLC and the first potentiometer to the fourth circuit.

9. The apparatus of claim 4 wherein the second circuit comprises a second potentiometer for selecting a desired output current, and a conductor for coupling the second potentiometer to the fourth circuit.

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10. The apparatus of claim 9 further comprising a second switch for selectively coupling one of the PLC and the second potentiometer to the fourth circuit.

11. The apparatus of claim 1 wherein the third circuit comprises a high
20 magnitude potential transformer having a primary winding and a secondary winding, the primary winding having a center tap and two end terminals, first and second switches coupled to respective ones of the end terminals, and a source of oppositely phased first and second switching signals for controlling the first and second switches, respectively.

12. The apparatus of claim 11 wherein the fourth circuit comprises a
25 switching regulator having an input terminal forming a summing junction for the first signal and the second signal and an output terminal coupled to the center tap, the fifth circuit including a microprocessor (μ P) and a third switch coupled to the μ P to receive a third switching signal from the μ P, the third switch coupled to the summing junction to
30 couple the third switching signal to the switching regulator to disable the supply of operating potential to the center tap.

3030-29010

-15-

13. The apparatus of claim 12 wherein the third switch is coupled to the summing junction through a filter which smooths the switching signals generated by the third switch in response to the μ P's control.

5 14. The apparatus of claim 4 wherein the third circuit comprises a high magnitude potential transformer having a primary winding and a secondary winding, the primary winding having a center tap and two end terminals, first and second switches coupled to respective ones of the end terminals, and a source of oppositely phased first and second switching signals for controlling the first and second switches, respectively.

10

15 15. The apparatus of claim 14 wherein the fourth circuit comprises a switching regulator having an input terminal forming a summing junction for the first signal and the second signal and an output terminal coupled to the center tap, the fifth circuit including a microprocessor (μ P) and a third switch coupled to the μ P to receive a third switching signal from the μ P, the third switch coupled to the summing junction to couple the third switching signal to the switching regulator to disable the supply of operating potential to the center tap.

20 16. The apparatus of claim 8 wherein the third circuit comprises a high magnitude potential transformer having a primary winding and a secondary winding, the primary winding having a center tap and two end terminals, first and second switches coupled to respective ones of the end terminals, and a source of oppositely phased first and second switching signals for controlling the first and second switches, respectively.

25 17. The apparatus of claim 16 wherein the fourth circuit comprises a switching regulator having an input terminal forming a summing junction for the first signal and the second signal and an output terminal coupled to the center tap, the fifth circuit including a microprocessor (μ P) and a third switch coupled to the μ P to receive a third switching signal from the μ P, the third switch coupled to the summing junction to couple the third switching signal to the switching regulator to disable the supply of operating potential to the center tap.

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3030-29010

-16-

18. The apparatus of claim 10 wherein the third circuit comprises a high magnitude potential transformer having a primary winding and a secondary winding, the primary winding having a center tap and two end terminals, first and second switches coupled to respective ones of the end terminals, and a source of oppositely phased first
5 and second switching signals for controlling the first and second switches, respectively.

19. The apparatus of claim 18 wherein the fourth circuit comprises a switching regulator having an input terminal forming a summing junction for the first signal and the second signal and an output terminal coupled to the center tap, the fifth
10 circuit including a microprocessor (μ P) and a third switch coupled to the μ P to receive a third switching signal from the μ P, the third switch coupled to the summing junction to couple the third switching signal to the switching regulator to disable the supply of operating potential to the center tap.

15 20. The apparatus of claim 12 and further comprising a sixth circuit cooperating with the μ P to determine if operating potential is being supplied to the high magnitude potential supply, and a seventh circuit cooperating with the μ P to determine if the high magnitude potential supply is indicating that it is generating high magnitude potential, the μ P indicating a fault if the operating potential is not being supplied to the
20 high magnitude potential supply and the high magnitude potential supply is indicating that it is generating high magnitude potential.

21. The apparatus of claim 20 wherein the μ P indicates a fault if the operating potential is being supplied to the high magnitude potential supply and the high
25 magnitude potential supply is indicating that it is not generating high magnitude potential.

22. The apparatus of claim 12 and further comprising a sixth circuit cooperating with the μ P to determine if operating potential is being supplied to the high magnitude potential supply, and a seventh circuit cooperating with the μ P to determine if
30 the high magnitude potential supply is indicating that it is generating high magnitude potential, the μ P indicating a fault if the operating potential is being supplied to the high

3030-29010

-17-

magnitude potential supply and the high magnitude potential supply is indicating that it is not generating high magnitude potential.

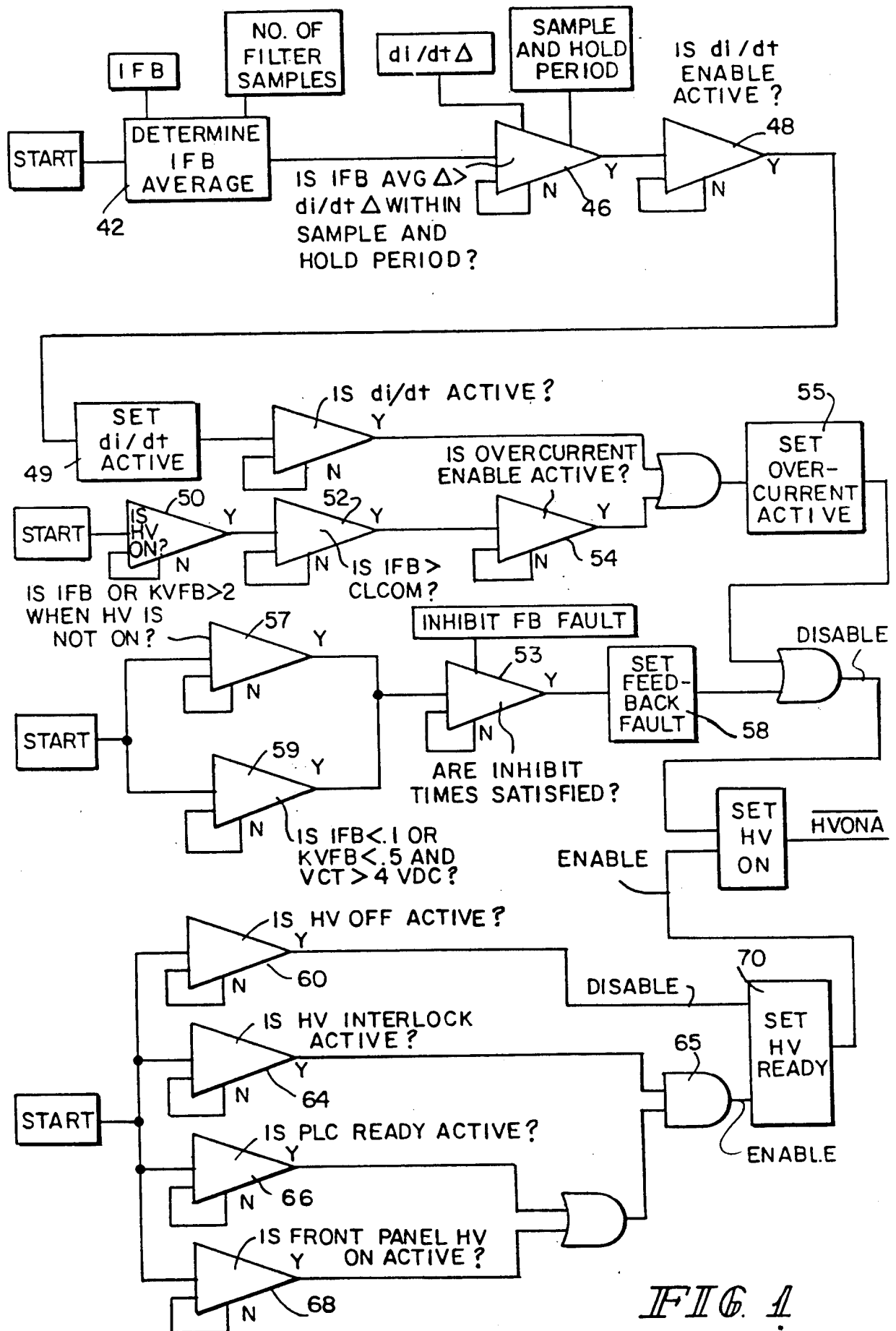


FIG. 1

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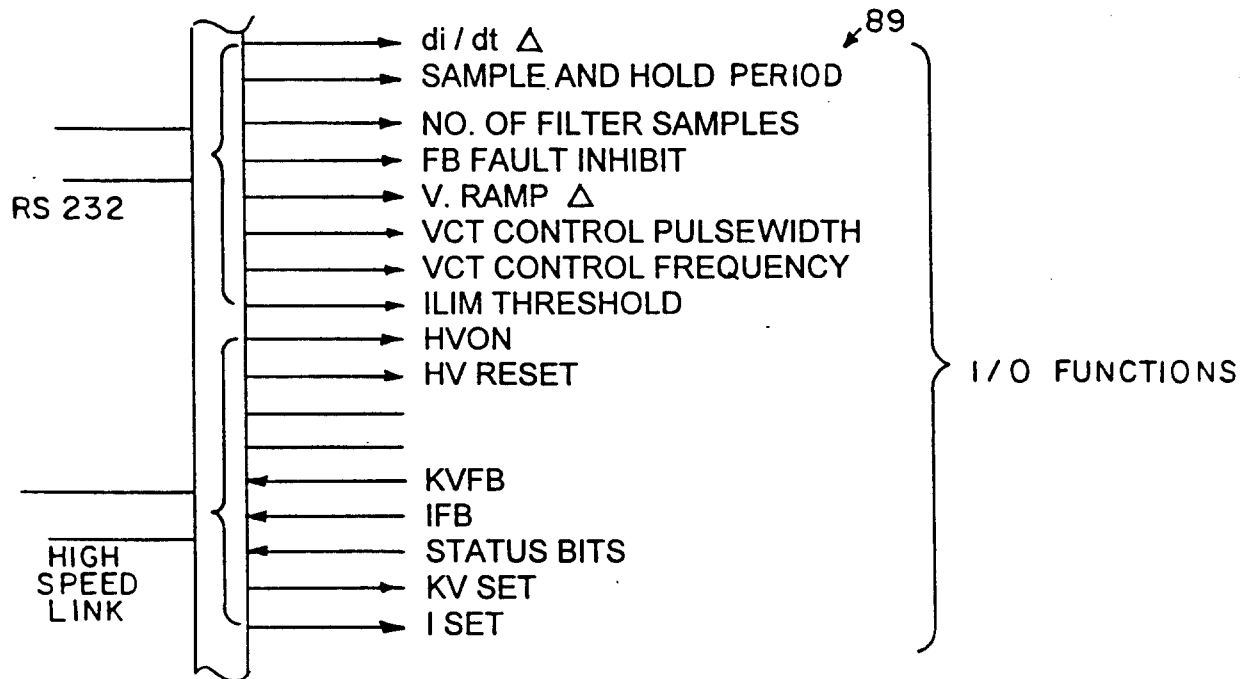


FIG. 3

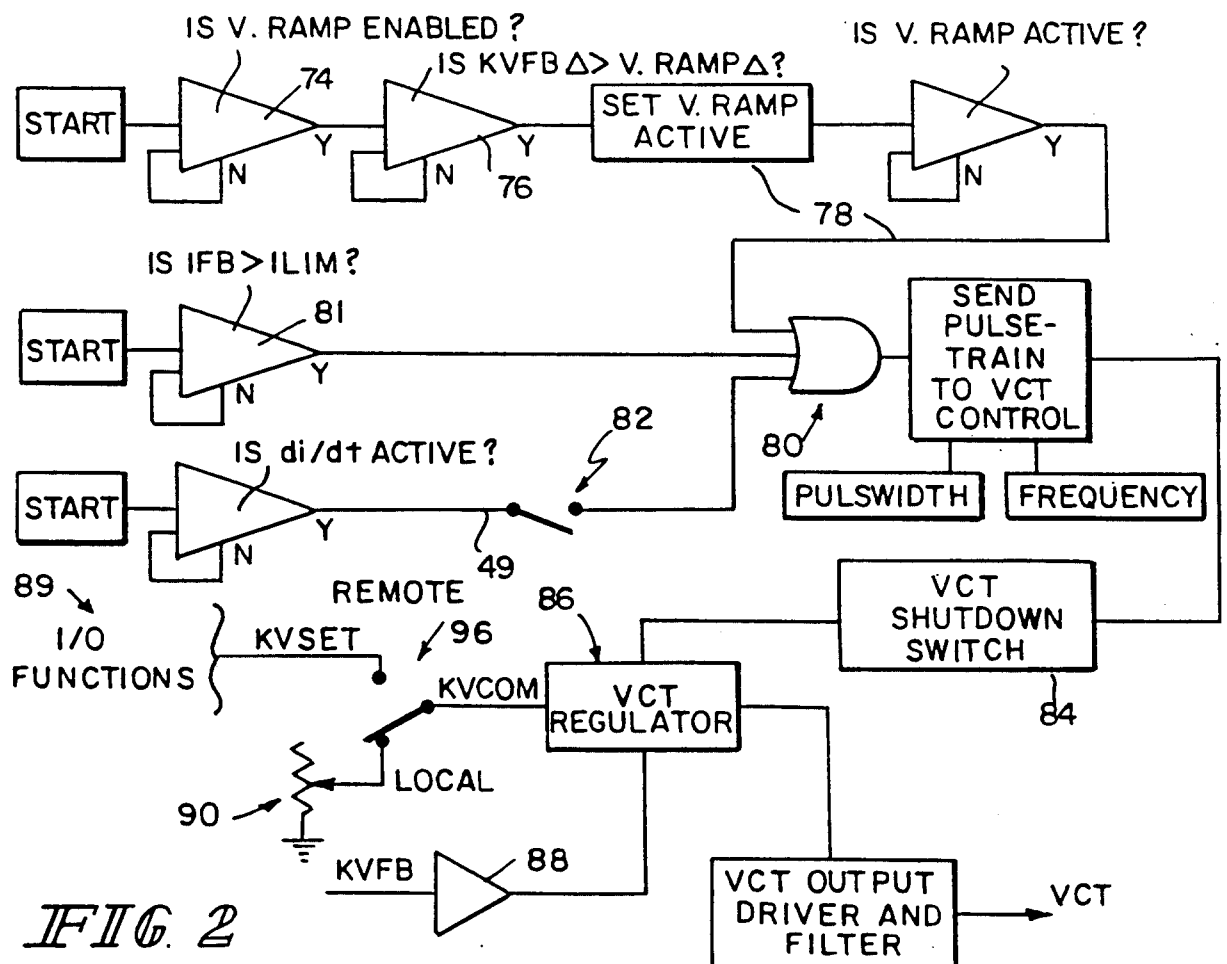
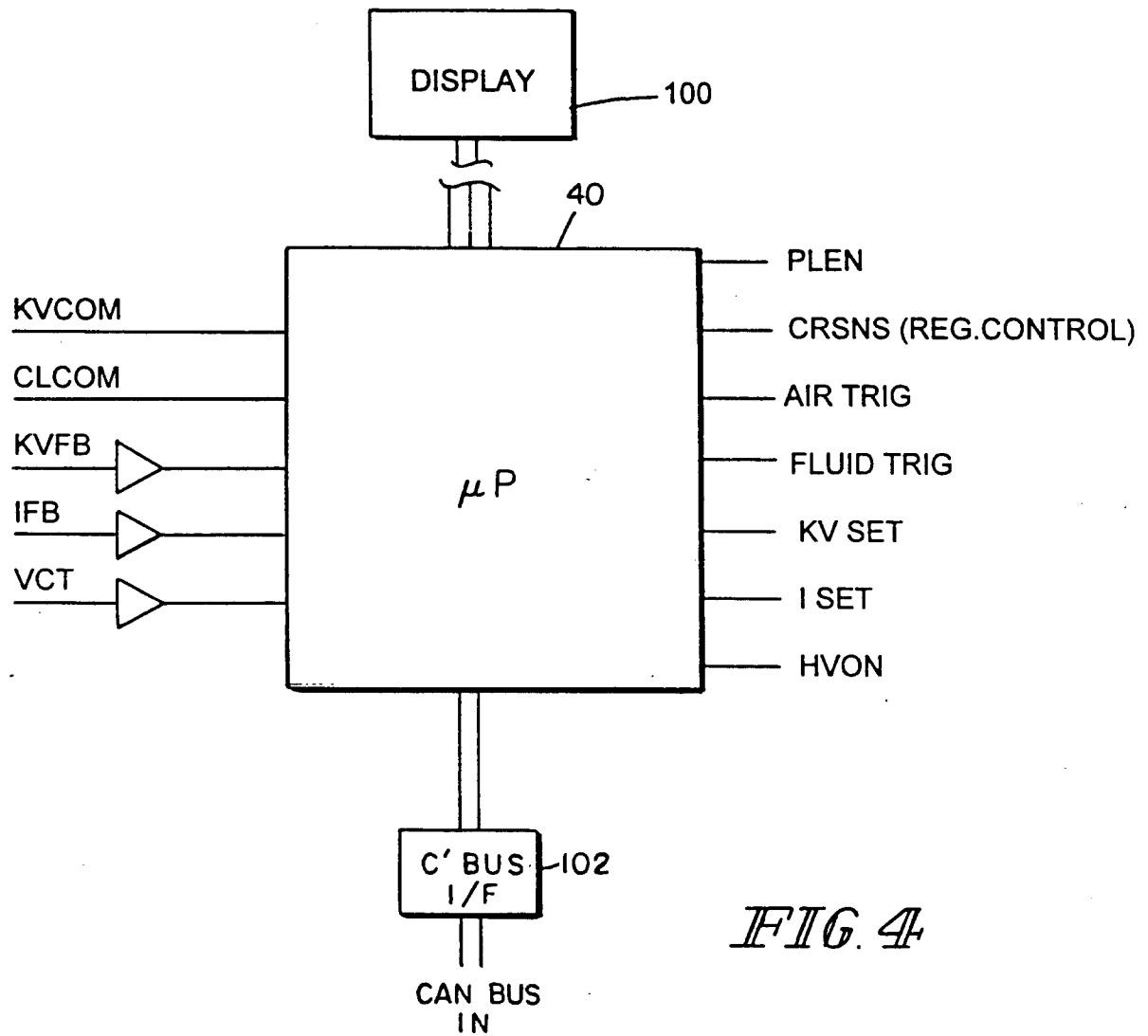
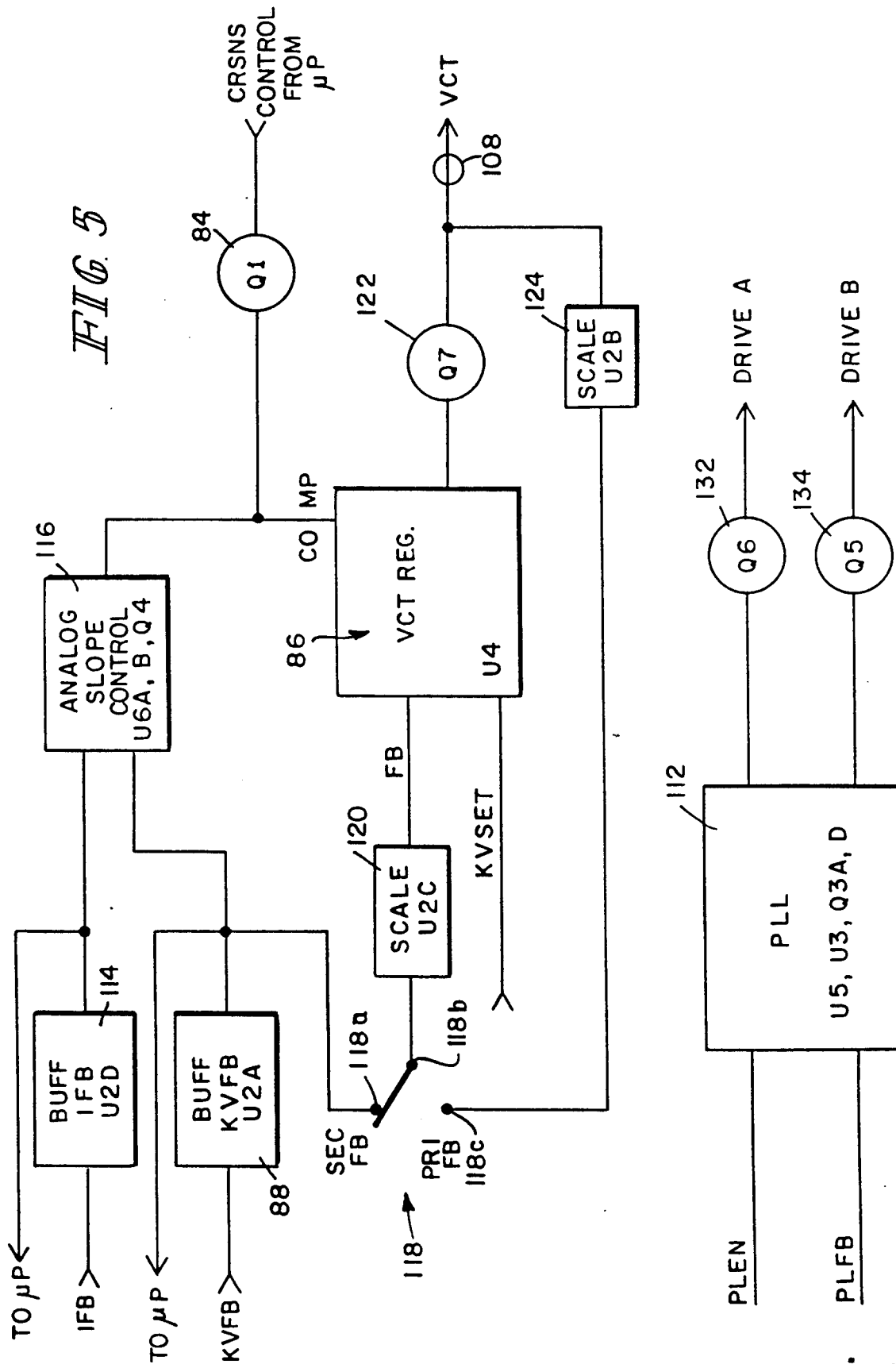


FIG. 2



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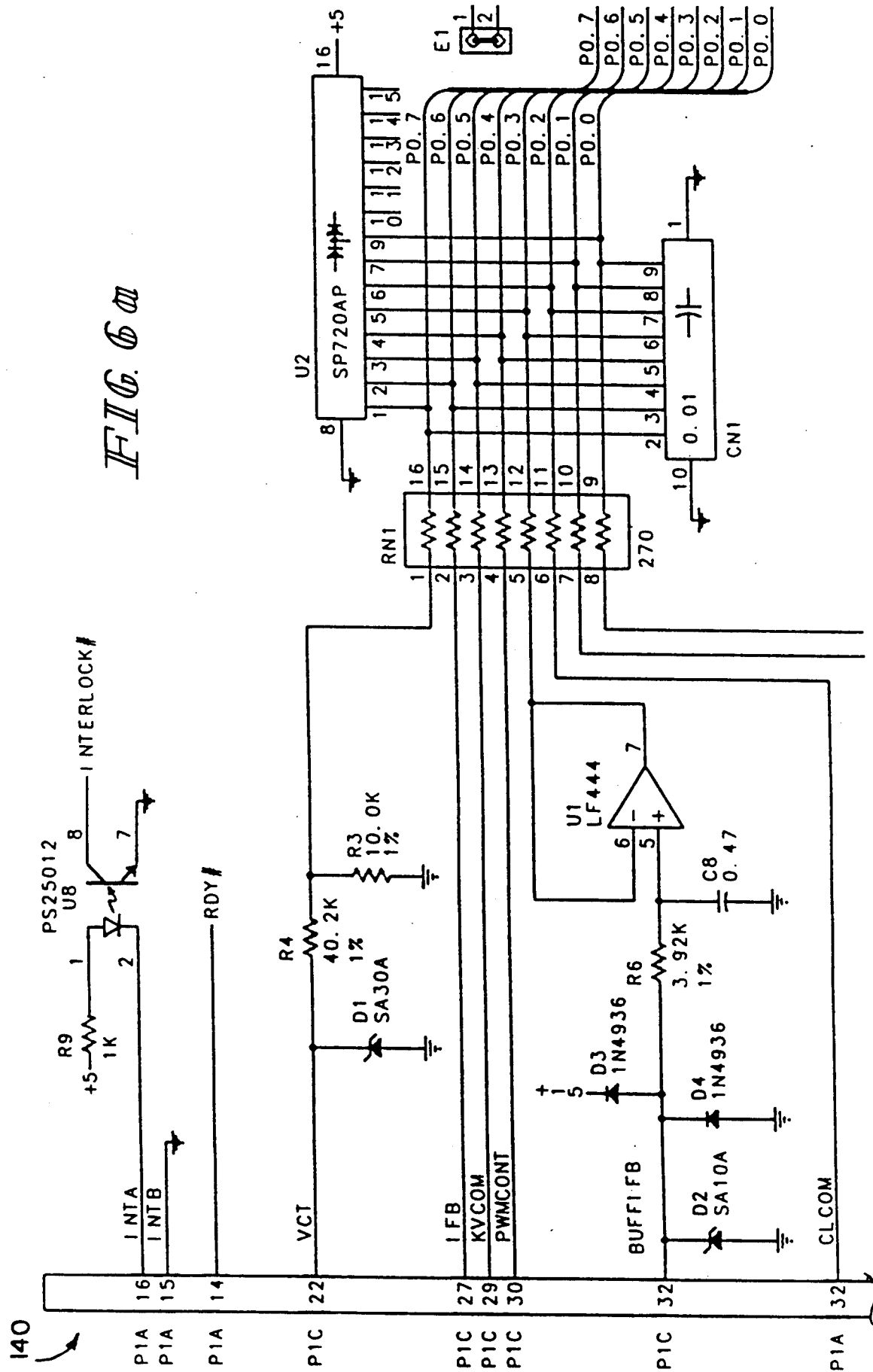
FIG. 5



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FIG. 6a



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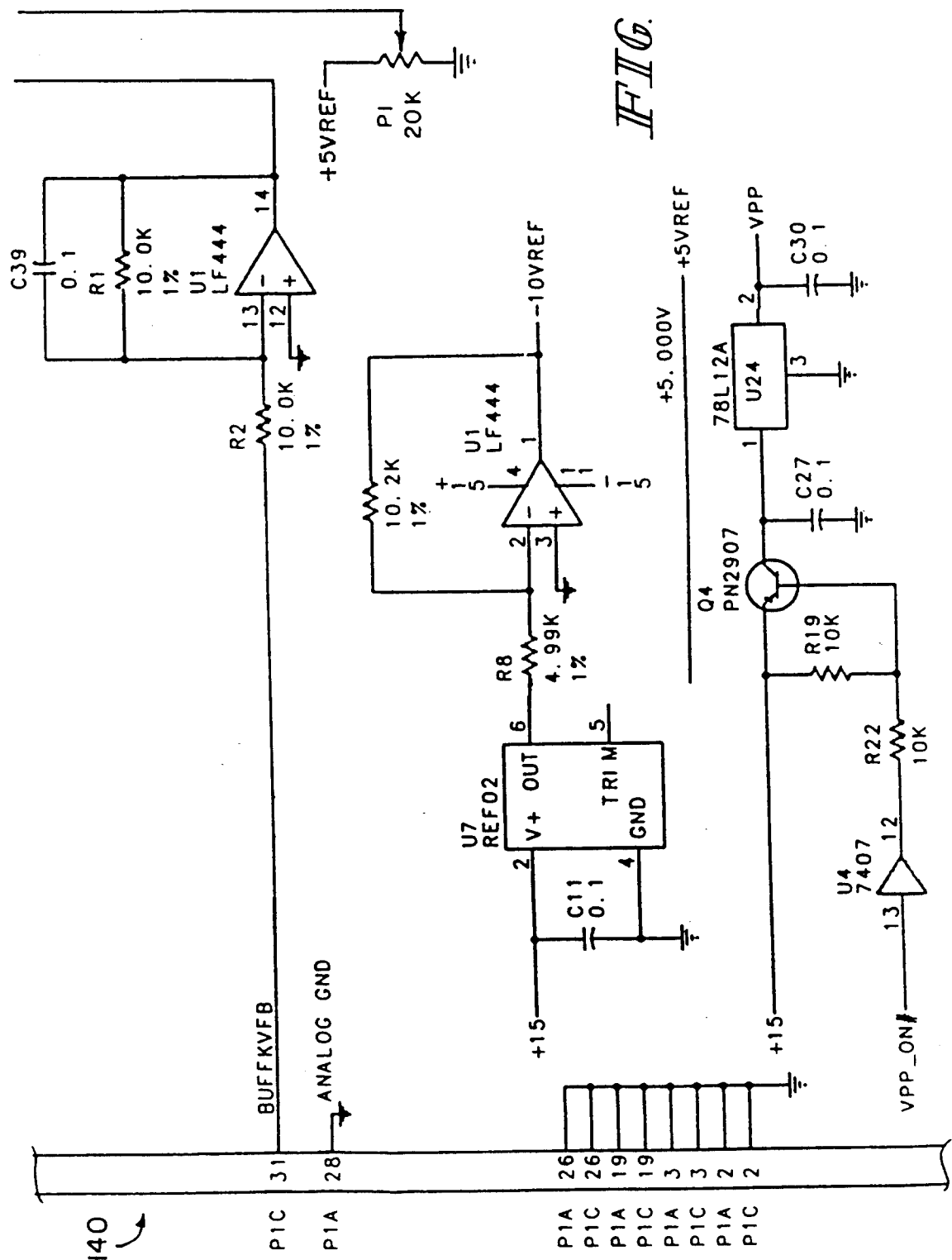
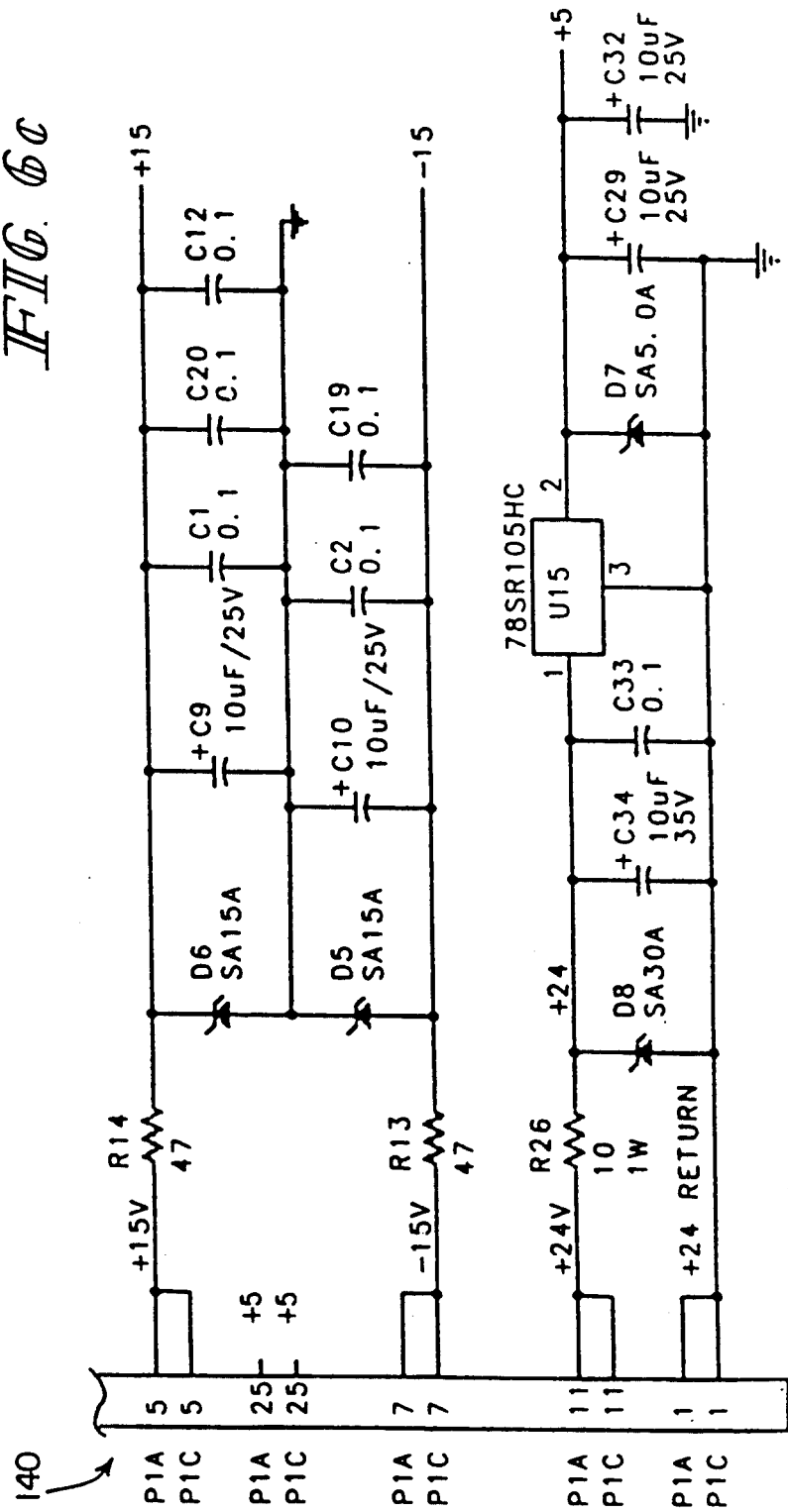


FIG. 6b

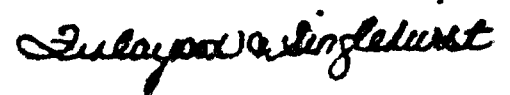
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FIG. 6a



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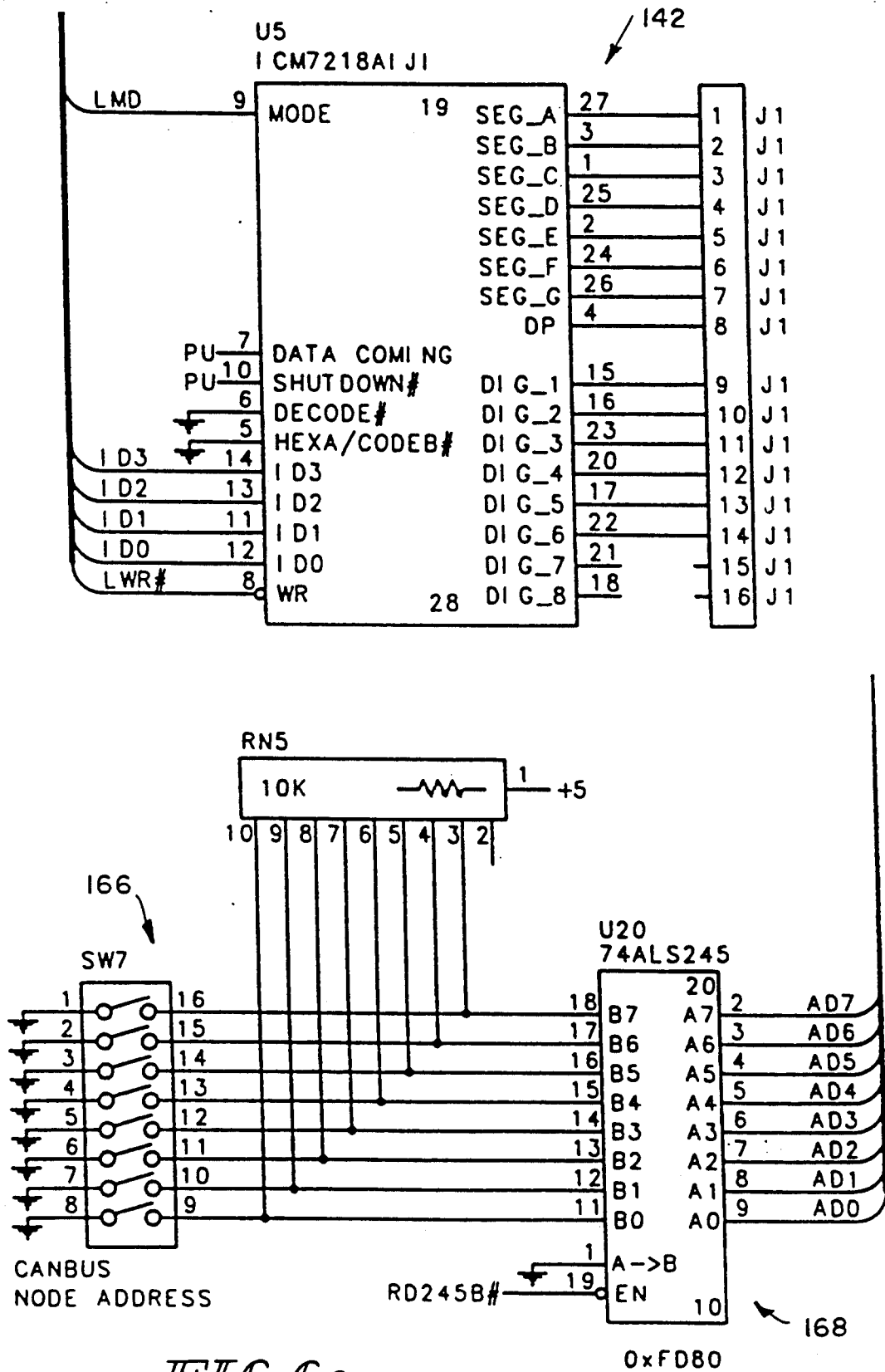
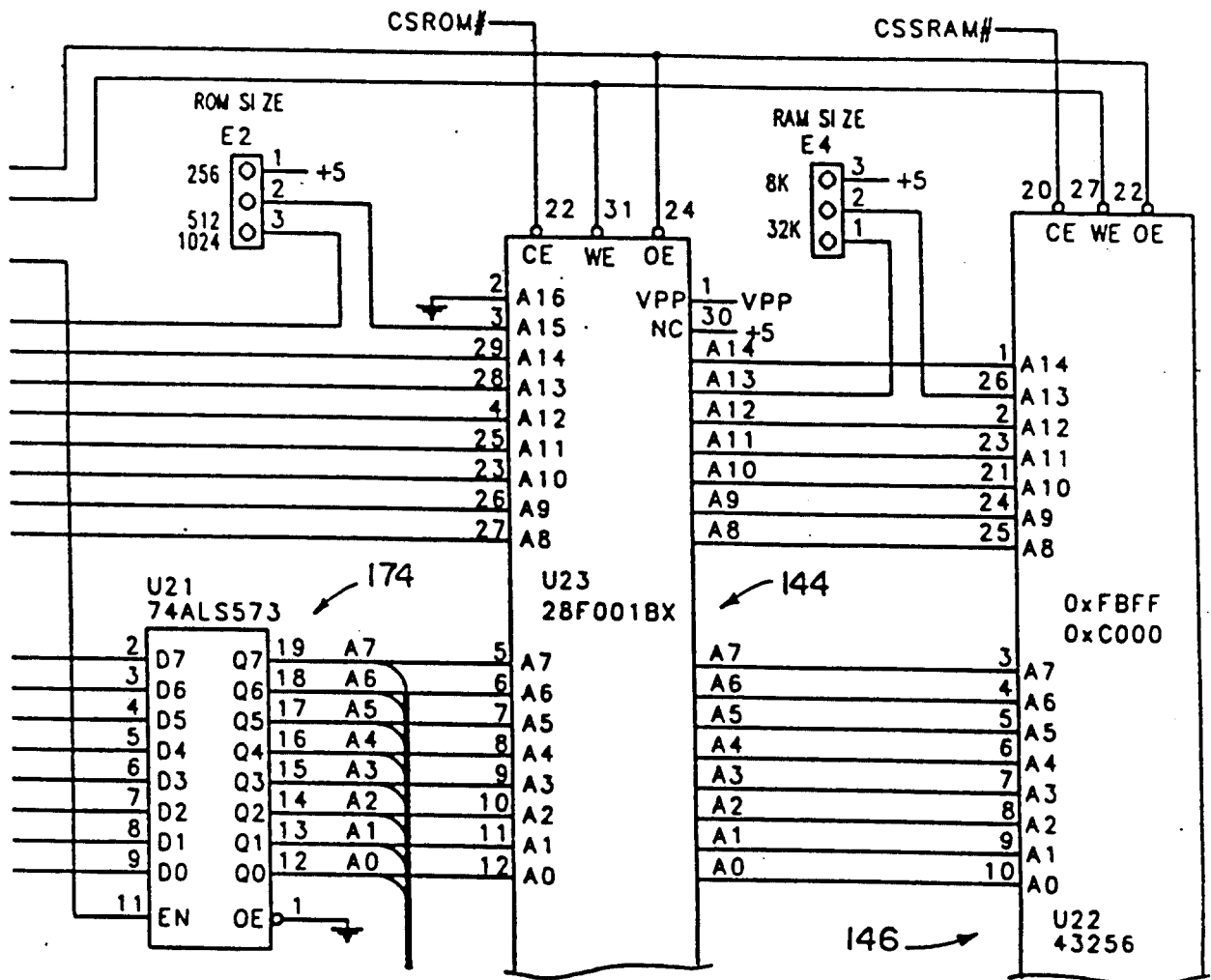
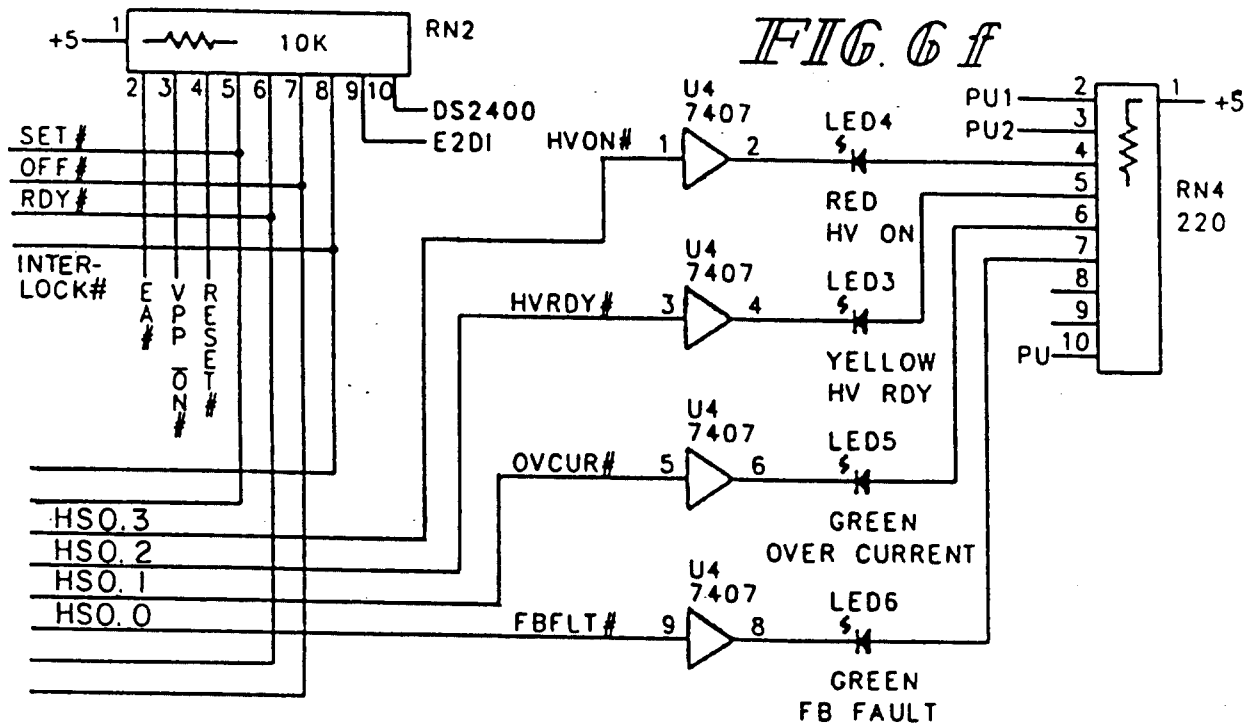


FIG. 6e



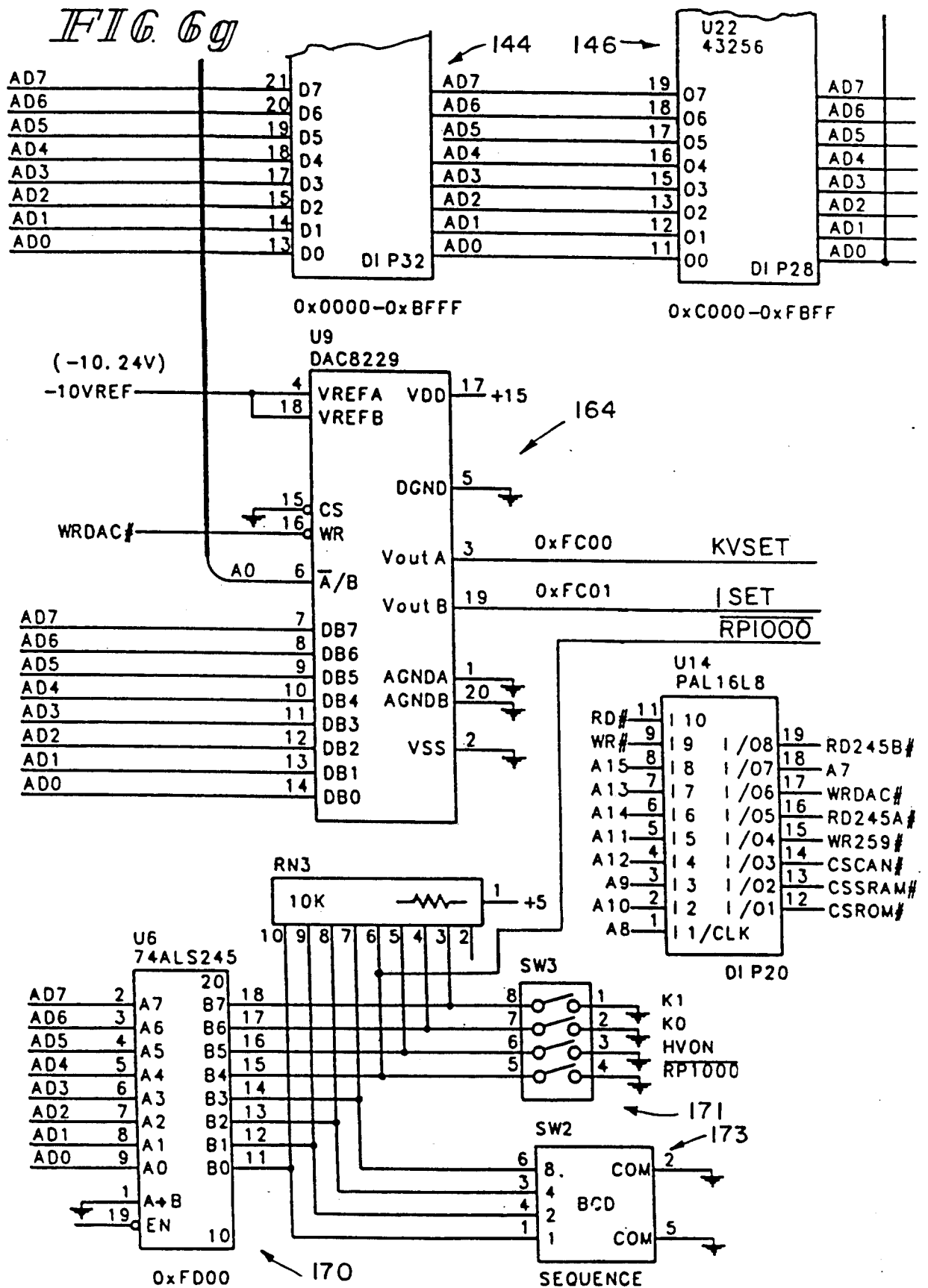
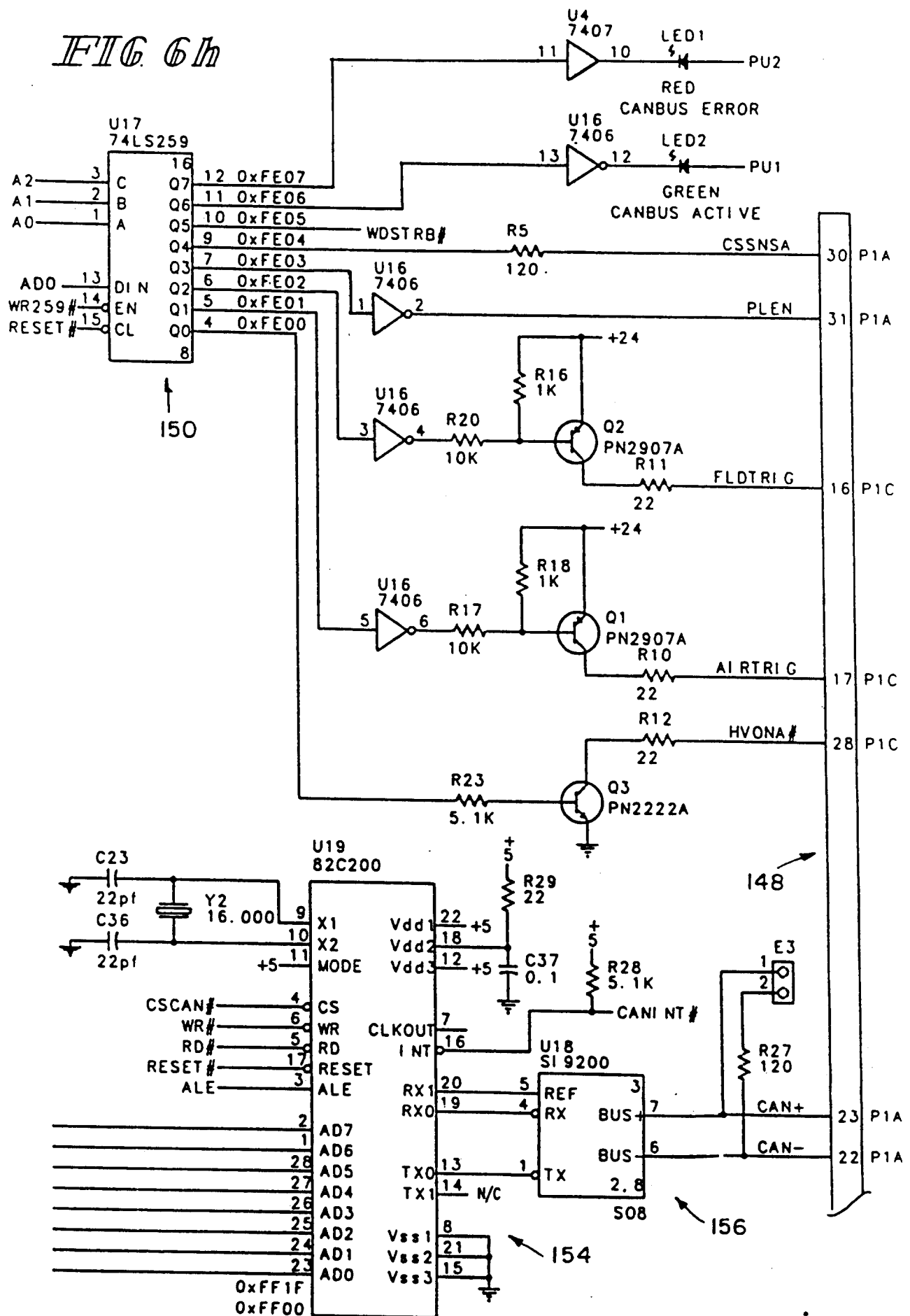


FIG 6h



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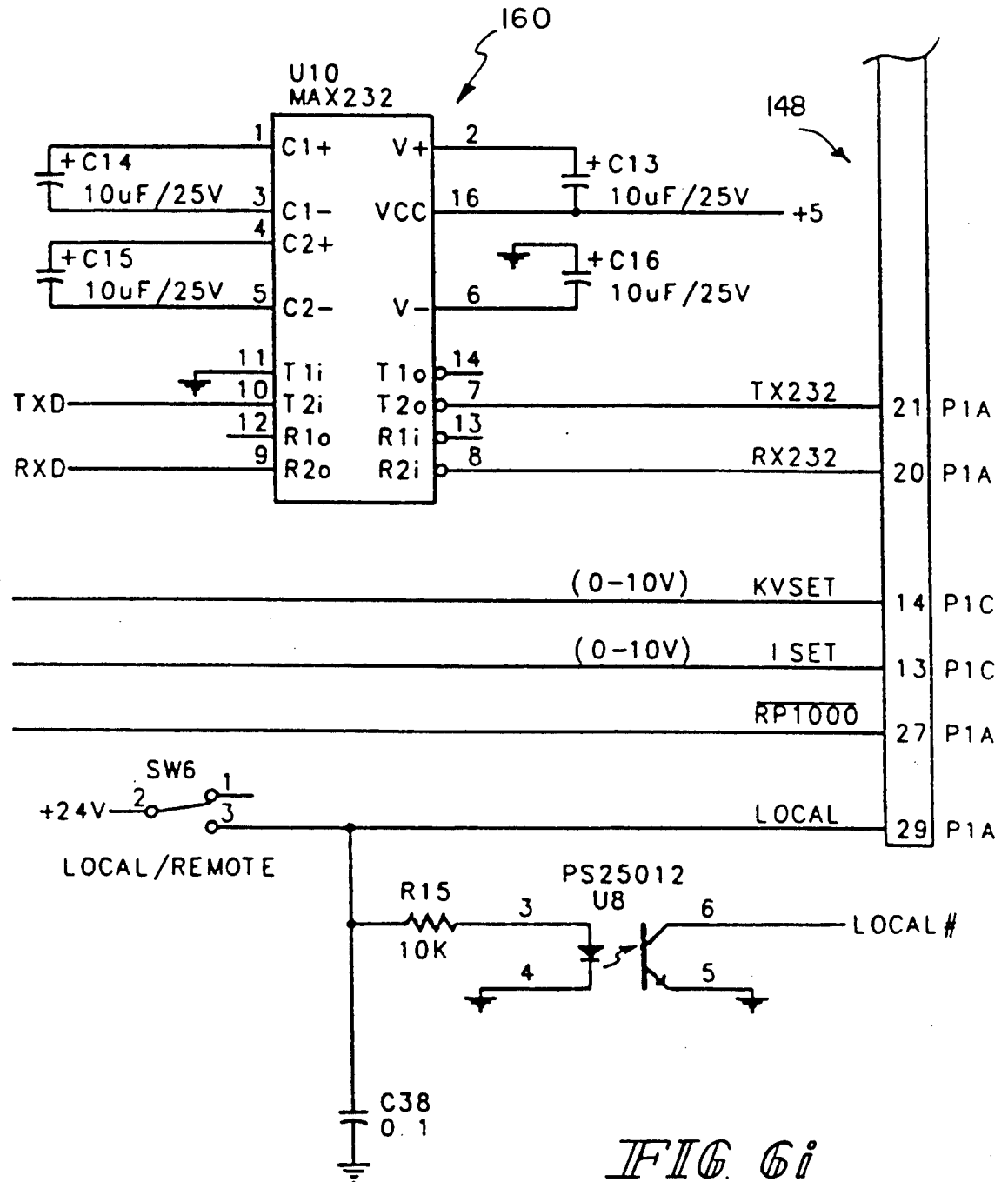
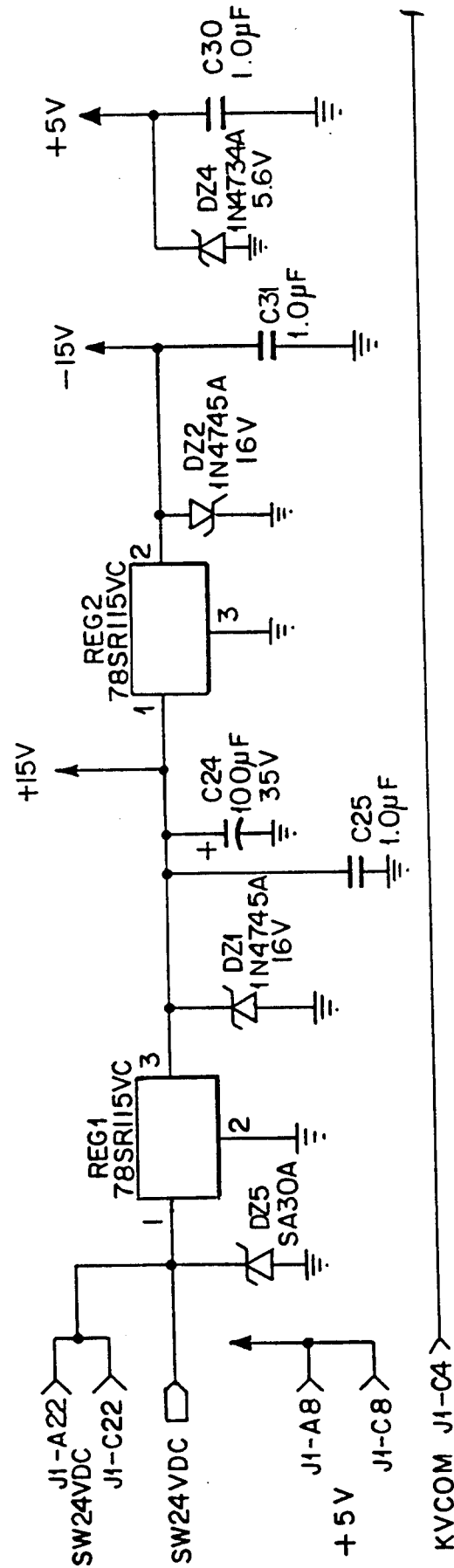
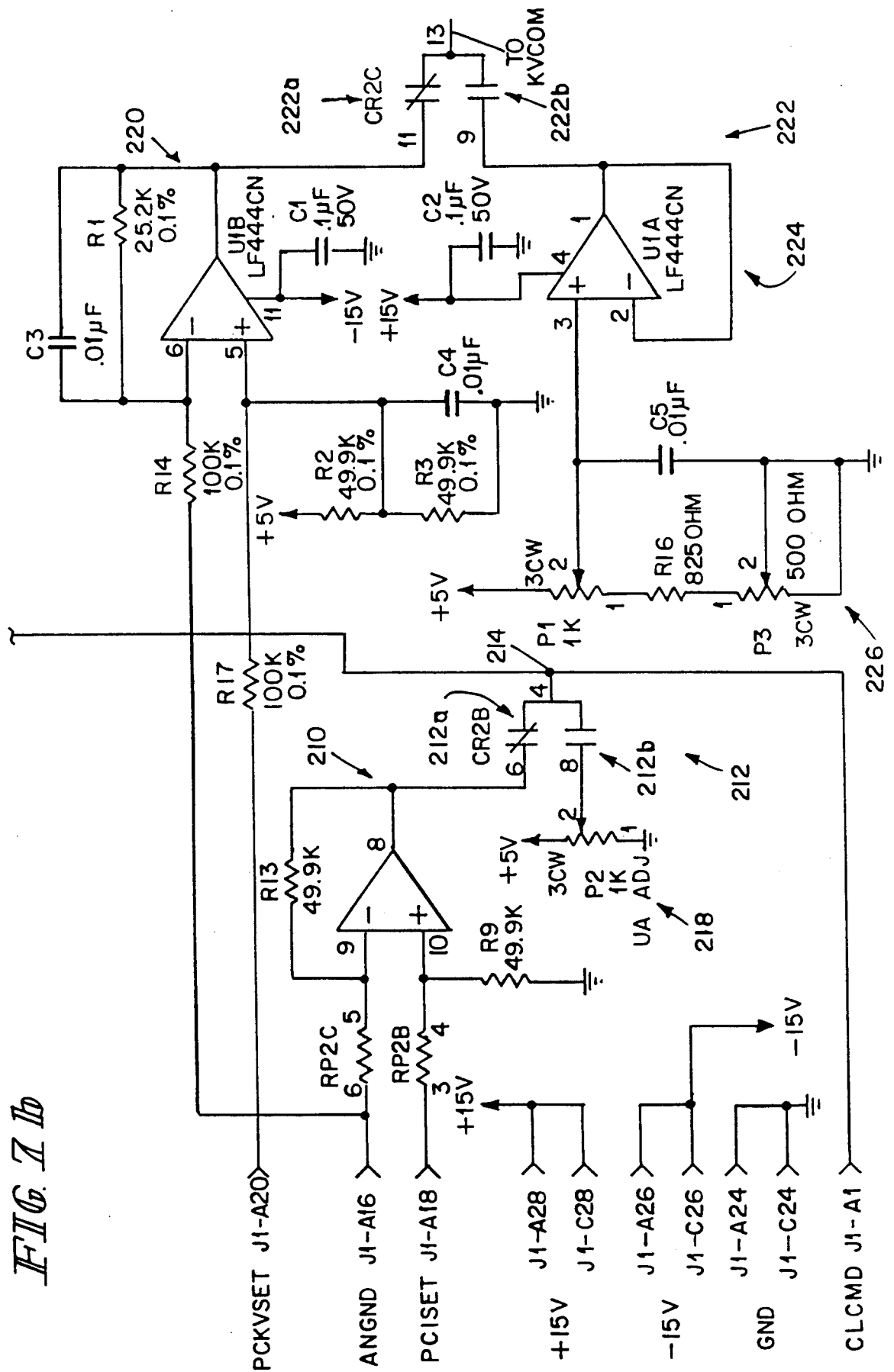


FIG. 7a

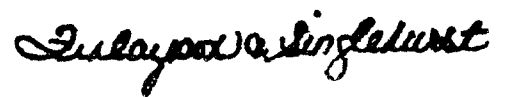


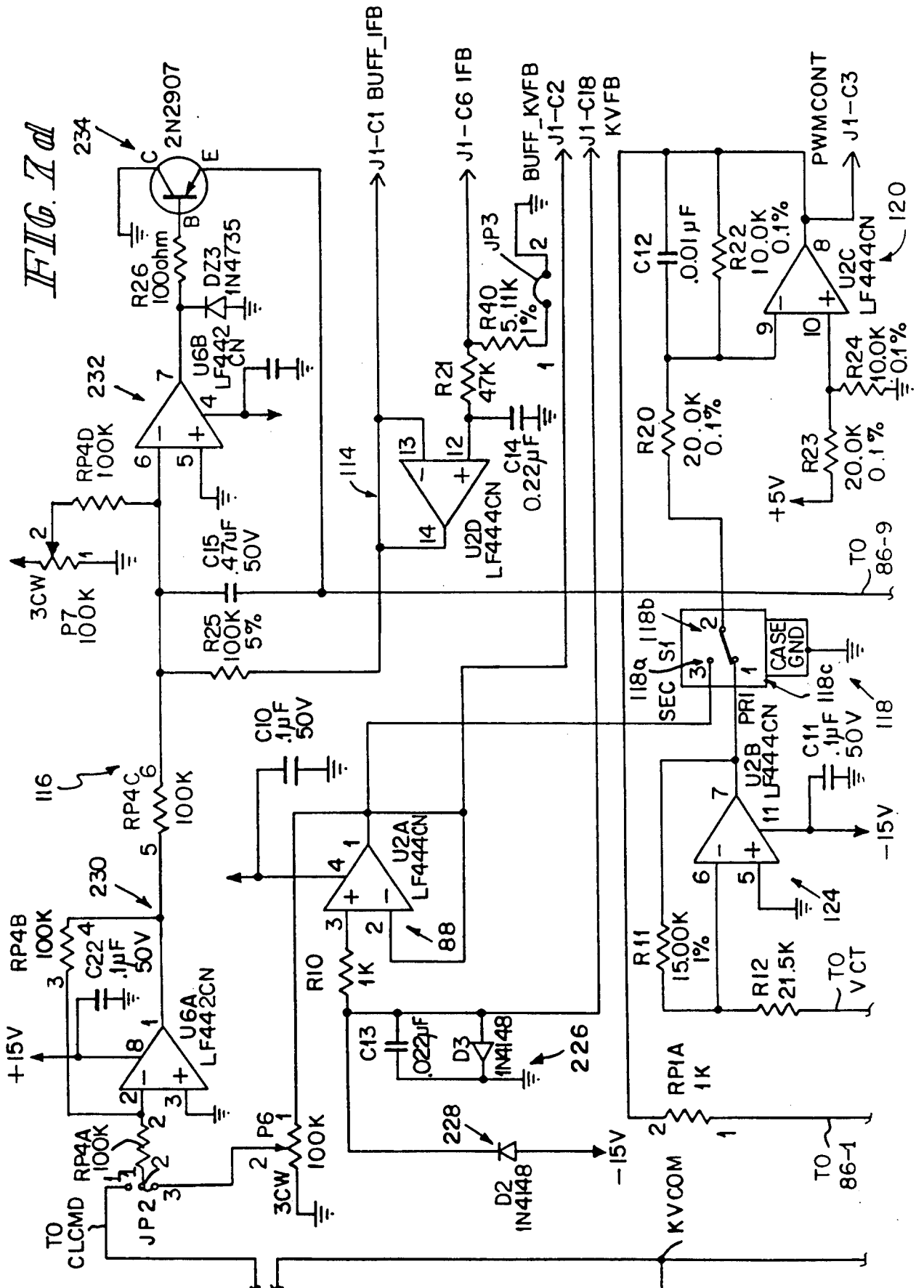
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FIG. 7b



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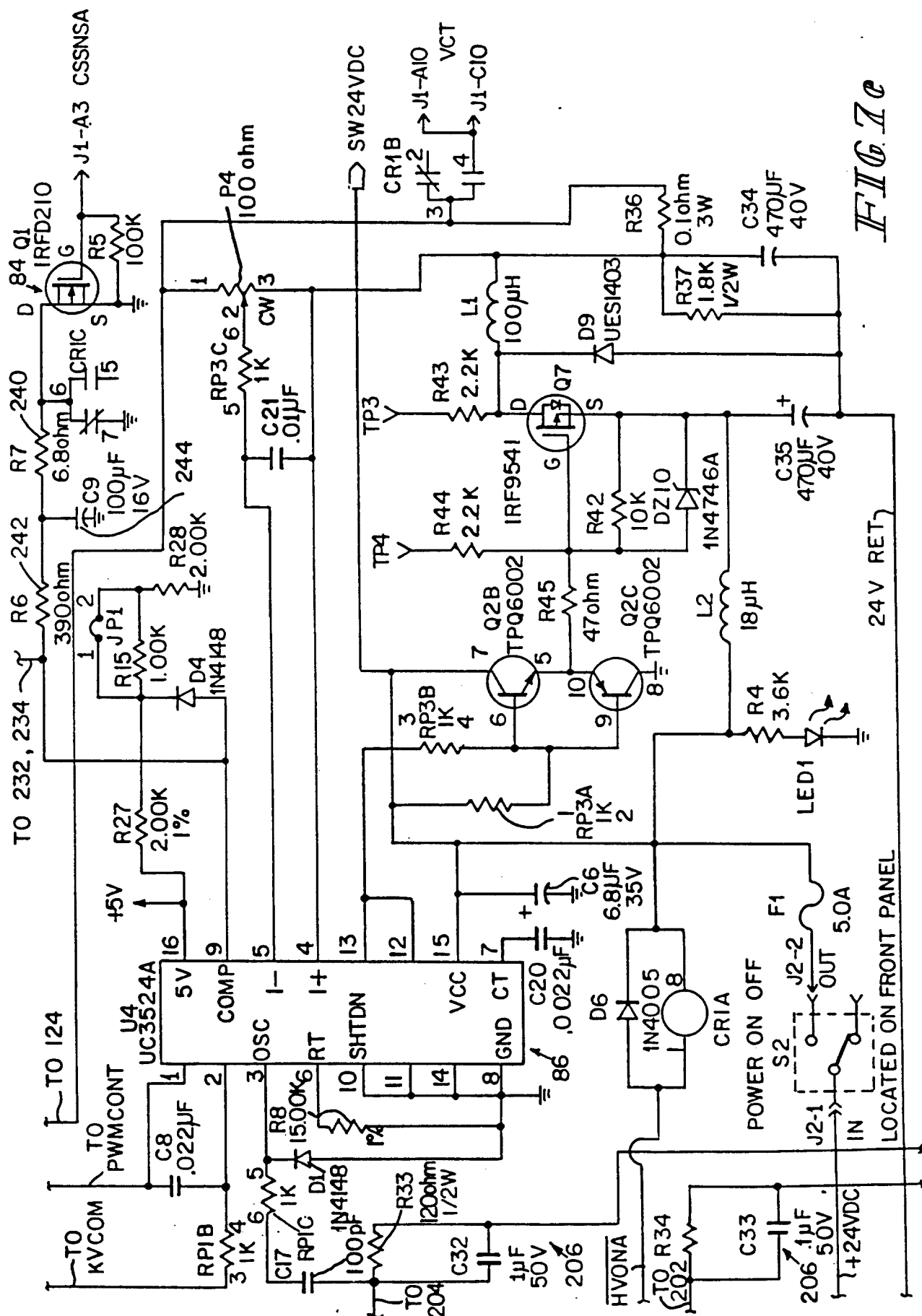


FIG. 7c

Eulayonea singelii West

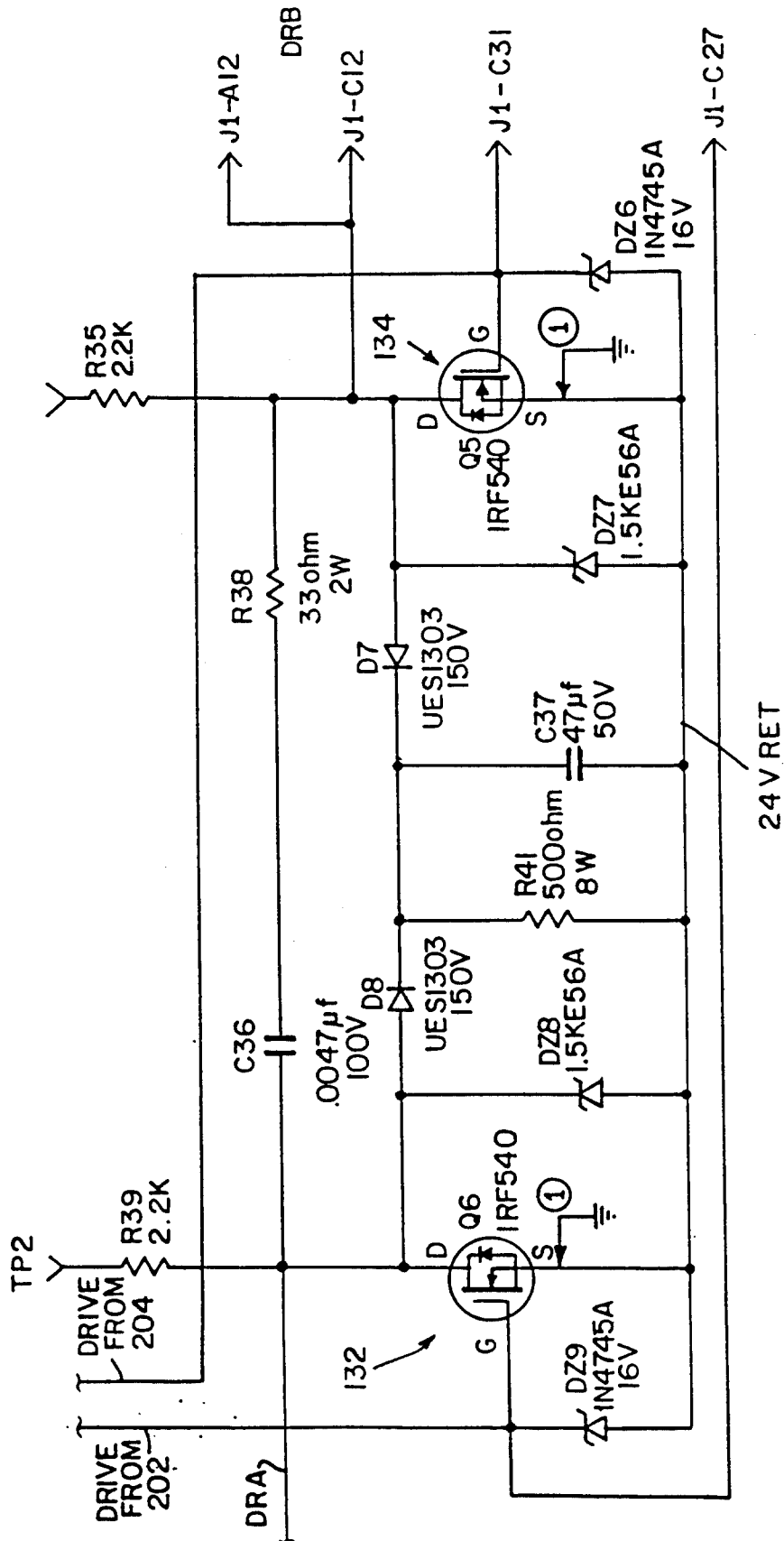


FIG. 7f

Eulayoxa singalensis

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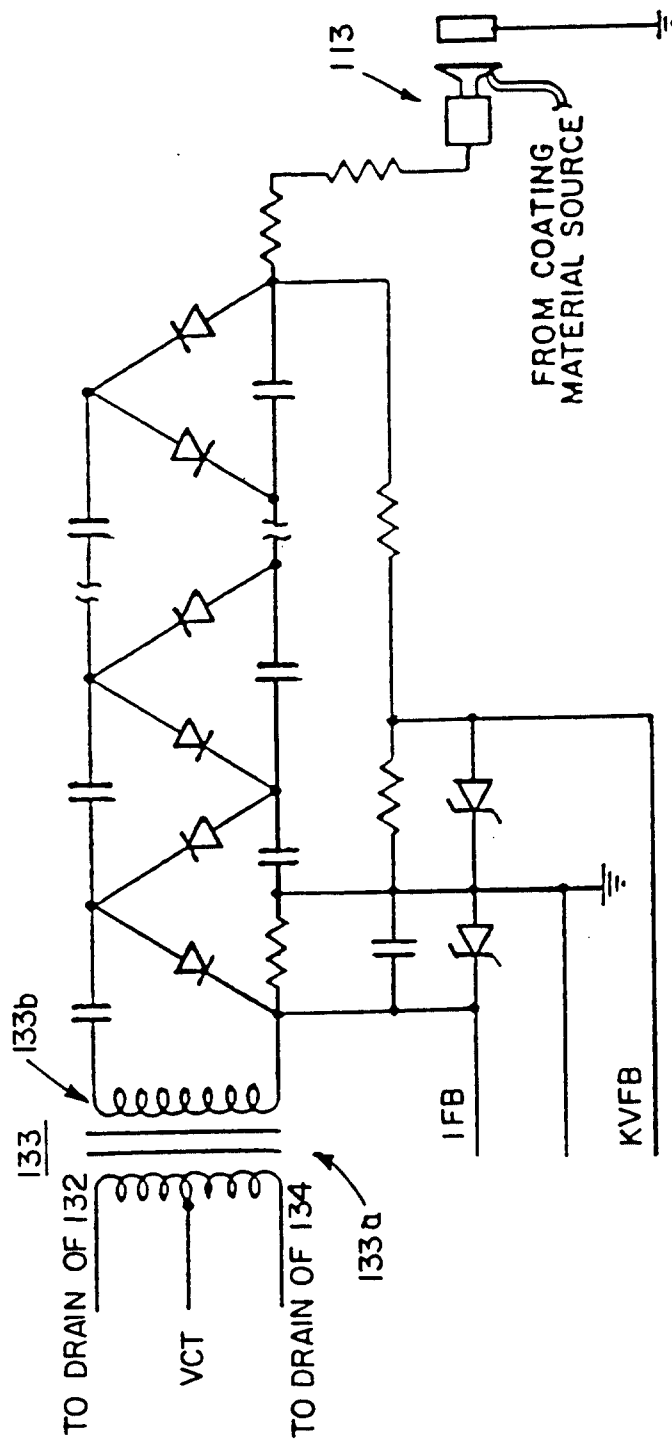


FIG. 8

