

[54] **FUEL INJECTION PULSE WIDTH COMPUTER**

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[58] Field of Search . 340/172.5; 235/150.2, 150.21; 123/32 AE, 32 EA

[56] **References Cited**

OTHER PUBLICATIONS

Williams, M., "Electronic fuel injection reduces auto-

motive pollution." Electronics, Vol. 45, No. 19, Sept. 1972, pp. 121-125, S28040052.

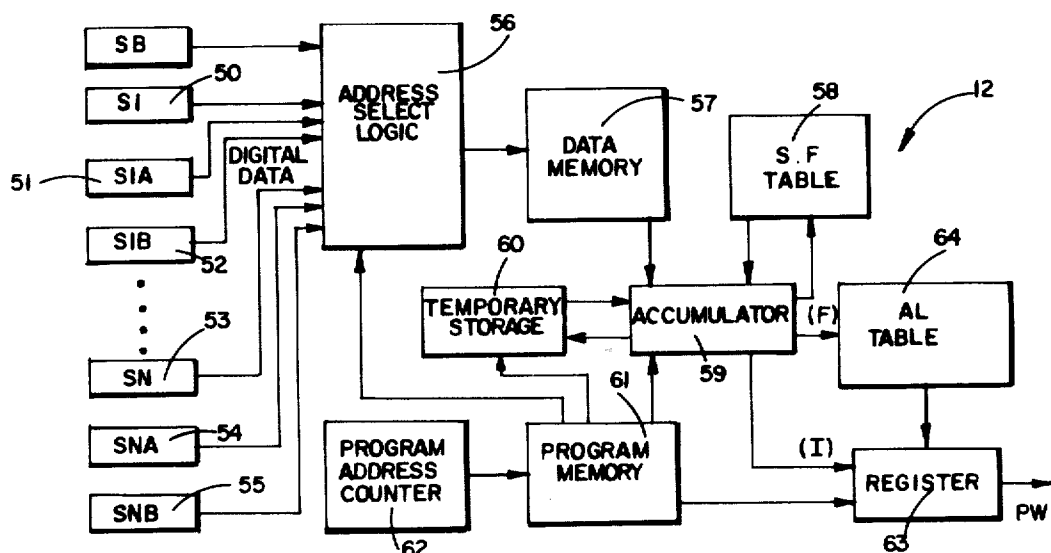
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[57]

ABSTRACT

A real time, digital computer is used to calculate a pulse width, for example, for fuel injection systems. The computer uses data from environmental sensors, data stored internally in fixed memories and an instruction program stored internally in a further fixed memory to calculate the pulse width. In fuel injection systems, the pulse width determines the length of time a fuel injector is operative during each engine cycle.

20 Claims, 3 Drawing Figures



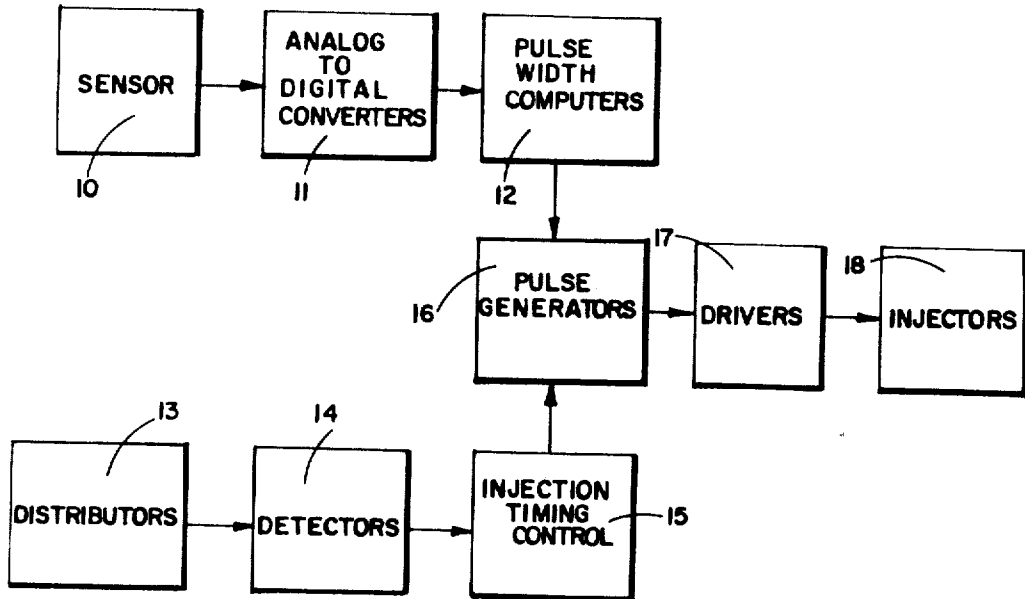


FIG. 1

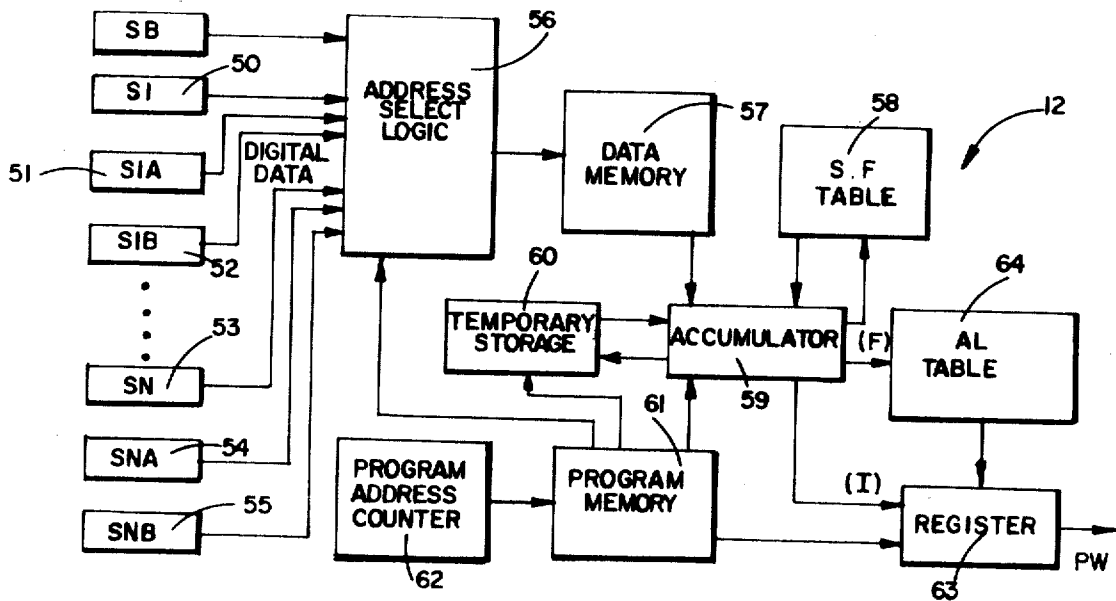


FIG. 2

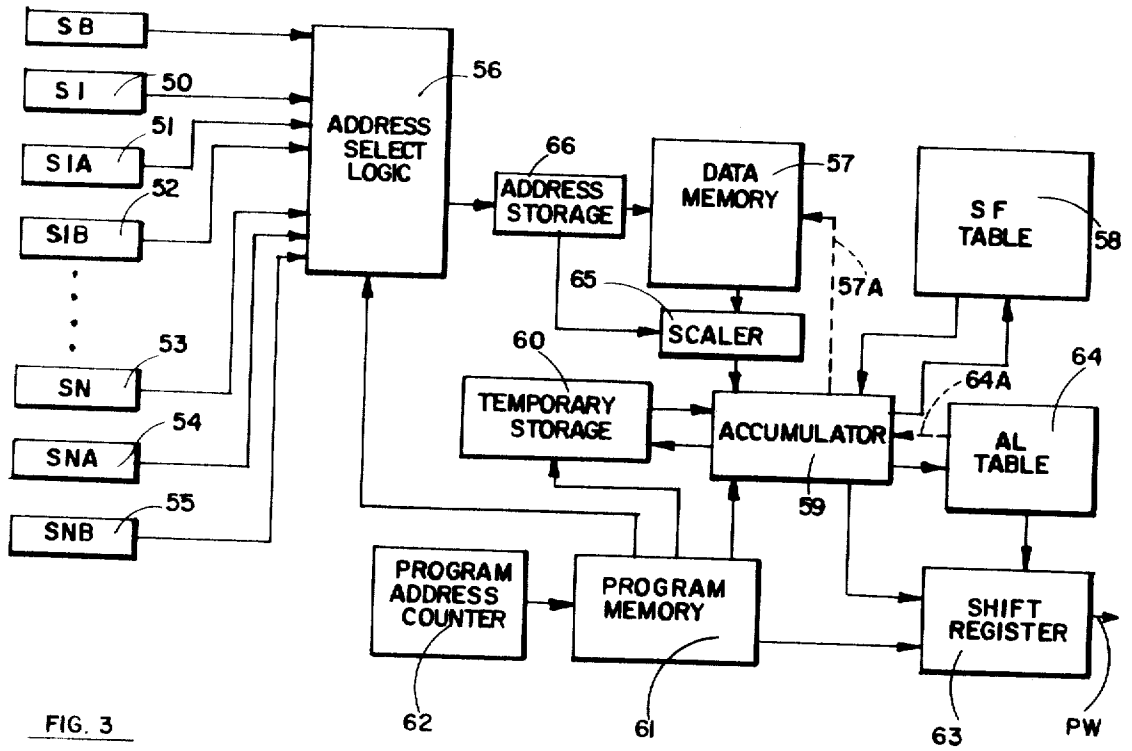


FIG. 3

FUEL INJECTION PULSE WIDTH COMPUTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to control systems particularly associated with fuel injection systems. In particular, the invention relates to fuel injection systems including electronic controls for controlling a pulse width or time duration. It is known that use of fuel injection systems instead of carburetors for engines with controlled ignition results in a certain number of advantages which are based on the greater possibilities for regulation and for adaptation to the particular type of engine. It is, thus, possible to lower the fuel consumption, to increase the power, and above all to reduce the percentage of unburned matter in the exhaust gas, especially the hydrocarbons, oxides of nitrogen and carbon monoxide. This latter advantage is of great importance to alleviate air pollution problems.

The use of conventional injection pumps and systems, known in the art, is generally quite expensive. Moreover, these conventional systems have tolerance problems and exhibit generally sluggish operation. Many fuel injection systems have been proposed. Typical examples of such systems are represented in U.S. Pat. Nos. 3,456,628 and No. 3,710,763 to J. Bassot et al, entitled High Speed Fuel Injection System, and U.S. Pat. No. 2,980,090 to R. W. Sutton, entitled Fuel Injection System. Systems disclosed in these patents demonstrate some of the techniques known in the art. However, these systems still have shortcomings. Therefore, new and improved systems are required. The new systems use sophisticated electronic control systems, especially of the type adaptable to MOS/LSI techniques.

SUMMARY OF THE INVENTION

A special purpose, real-time digital computer is utilized to calculate the width of the fuel injection pulse. With fuel injected under fixed pressure, the pulse width determines the amount of fuel which enters each engine cylinder. The computer uses data from environmental sensors, data stored internally in fixed memories, and an instruction program stored in an additional fixed memory to calculate the pulse width.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a fuel injection system which utilizes the instant invention.

FIG. 2 is a block diagram of one embodiment of a pulse width computer used in conjunction with the system shown in FIG. 1.

FIG. 3 is a block diagram of another embodiment of a pulse width computer used with the system shown in FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. 1, there is shown a block diagram of the electronic control portion of fuel injection system. Many of the electronic components used in this system are known in the art. Specific detailed descriptions of these components are, therefore, not presented herewith. Obviously, those skilled in the art will be able to choose the particular configuration of the individual components as a function of the remainder of the circuit, the type of construction, and so forth.

Sensors 10 may represent one or more sensors such as thermistors, strain gages, potentiometers, etc. which are capable of detecting ambient or environmental conditions such as temperature, pressure, position, and the like. Sensors 10 are connected to analog to digital (A/D) converters 11. The analog signals produced by sensors 10 are converted by A/D converters 11 into digital signals. The digital signals from A/D converters 11 are supplied to pulse width computer 12. The pulse width computer 12 represents the particular invention shown and described herein. The specific configuration of this computer is discussed in detail subsequently. Computer 12 supplies signals to pulse generator 16 as described hereinafter.

Distributor 13 is a standard distributor usually found in any automotive-type vehicle augmented with a second set of points to establish a reference or identification signal once each engine cycle. Actually, distributor 13 may represent any type of signal generating device the output signal of which is functionally related to engine shaft angle. This output signal represents the operation of the unit involved. For example, in this embodiment, distributor 13 is arranged to supply pulses for each engine cycle (to establish a reference position) and for each individual cylinder cycle. For example, an 8 cylinder engine will produce 8 individual distributor signals as well as one engine cycle signal, per engine cycle. In other cases, it may be desirable or suitable to obtain this type of signal from a crankshaft or other representative location.

The signals generated by distributor 13 are supplied to detectors 14 which may be any suitable type of detector such as reed relays, magnetic sensors, logic gates, or the like. The detectors operate upon the signal supplied by distributor 13 to produce an output signal representative of the distributor operation and, thus, the timing arrangement of the device (i.e., engine operation).

Injection timing control 15 is connected to receive signals from detectors 14. Injection timing control 15 operates upon these signals and produces control signals which further control and indicate the operation of the overall device. For example, control circuit 15 may ultimately control the firing of injector drivers and the like. The timing control signals are generated as a function of the device operation as described in greater detail in the co-pending application of G. A. Watson, entitled Timing Control Circuit for Full Injection System bearing Ser. No. 354,296, filed on Apr. 25, 1973, and assigned to the common assignee. Signals from injection timing control 15 are supplied to pulse generator 16 which also receives signals from pulse width computer 12.

Pulse generator 16 operates on the signals supplied by control circuit 15 and computer 12 to produce output signals which are supplied to drivers 17. Drivers 17 are conventional drivers which are used to control the operation of the actual fuel injectors or similar devices. Signals from drivers 17 are supplied to injectors 18 (or other utilization device) to control the operation thereof.

Thus, it is seen that the signals applied to driver 17 and utilization device 18 are functions of pulses supplied by generator 16. Generator 16 supplies pulses which are a function of the actual speed of operation of the utilization devices as established by distributor 13, detectors 14 and control circuitry 15. In addition,

the pulses are functions of other factors such as temperature, pressure, and the like, which are detected by sensors 10 and converted by A/D converters 11 into digital signals which are operated upon by computer 12. This overall system arrangement is relatively standard in the art and does not represent the invention per se.

Referring now to FIG. 2, there is shown a detailed block diagram of pulse width computer 12 shown in FIG. 1. Pulse width computer 12 includes a plurality of input sources 50-55. While six sources are shown, it is clear that any number thereof may be utilized in actual practice.

Each of the sources supplies the digital signal associated with a specific type sensor or transducer. These digital signals are produced by A/D converters 11. For example, digital signals representative of engine temperature, atmospheric pressure or the like may be produced. These signals are designated as signals S1, S1A through SNB. The digital signals represent various environmental conditions produced by sensors 10, manual and/or calibration inputs. Sources 50-55 are connected to supply the digital input signals to address select logic 56.

As will be described hereinafter, the input signals from sources 50-55 operate as address signals to data memory 57. Address logic circuit 56 receives suitable signals from program memory 61 to enable the transmission of address select signals from sources 50-55 through address select logic circuit 56 to memory 57. The program signals from program memory 61 also combine with the digital input signals to form a portion of the address for data memory 57. Program memory 61, which includes the control program for the computer system, receives input signals from program address counter 62. Counter 62 periodically steps and operates memory 61 in sequence.

The output terminals of address select logic circuit 56 are connected to data memory 57. In effect, signals from circuit 56 operate to select the specific memory cell or location in data memory 57. The output terminals of data memory 57 are connected to some of the input terminals of accumulator 59. Other input terminals of accumulator 59 are connected to receive control signals from program memory 61. Accumulator 59 is interconnected with temporary storage 60 so that data stored in accumulator 59 may be selectively shifted to temporary storage 60 and returned in accordance with instructions from program memory 61.

In addition, two memories containing special function table 58 and antilog table 64 are also connected to receive signals from accumulator 59. Special function table 58 also returns signals to accumulator 59. Tables 58 and 64 are also under control of program memory 61 although interconnection thereto is omitted for clarity. Other terminals of accumulator 59 are connected to input terminals of shift register 63. Other input terminals of shift register 63 are connected to output terminals of antilog table 64. Moreover, program memory 61 is connected to supply a control signal to shift register 63. The output terminal of shift register 63 is connected to a utilization device for example pulse generator 16 shown in FIG. 1. The pulse width signal (PW) is produced at the output terminal of shift register 63.

Referring now concurrently to FIGS. 1 and 2, it will be seen that a special-purpose, real-time, digital computer can be used in an automotive fuel injection sys-

tem. The system is shown in FIG. 1 while one embodiment of the computer is shown in FIG. 2. With this system, injection of fuel into an internal combustion engine or the like is controlled in order to provide environmental advantages. If fuel is injected into the engine under fixed pressure, the duration of the injection pulse determines the amount of fuel which enters each engine cylinder. The duration of the injection pulse (of fuel) is determined as a function of the length of the pulse width signal (PW) produced by the computer since the injector is controlled by the signal. For example, electromagnetic injectors of known variety may be rendered operative in response to such a signal. So long as the signal is applied, the injector is in a prescribed status and may, for example, permit fuel to be injected into the engine.

The fuel injection system operates to detect environmental conditions by means of sensors 10 located throughout the vehicle. Sensors 10 produce analog signals. The environmental signals from sensors 10 are converted from analog to digital signals. The digital signals are supplied to pulse width computer 12 which determines the width of the pulse to be supplied to the individual injectors as a function of the environmental signals detected by sensors 10. Basically, the digital computer includes a memory which has stored therein empirically determined data representative of the environmental conditions detected by sensors 10. As a result, pulse width computer 12 produces a pulse which is supplied to pulse generator 16 (along with the timing control signals from control circuit 15). Pulse generator 16 supplies the signal to injector driver 17 which, in effect, operates injectors 18 to permit (or prohibit) the fuel injection into the engine. The fuel injection is, clearly, a direct function of the characteristics of pulse supplied by pulse width computer 12.

The signals produced by sensors 10 are, as noted supra, generally analog signals. A/D converter 11 converts the analog signals to digital signals. The digital signals are supplied via sources 50 through 55 (see FIG. 2). These digital signals are supplied to address select logic circuit 56 on a continuous basis. Thus, the current status or condition detected by the various sensors is available at all times for immediate up-date of information for the computer.

The pulse width computer is under overall control of program memory 61. This memory may comprise a suitably arranged memory which has an instruction program stored therein. Typically, program memory 61 may be a fixed memory such as a diode array or MOS FET ROM. Program address counter 62 is any suitable free running counter of appropriate frequency as determined by the operating rate of the computer. Counter 62 may include any suitable oscillator such as a crystal control oscillator or the like and may include one or more countdown circuits as required. Program address counter 62 continually supplies periodic signals to program memory 61. The signals from counter 62 are effective to sequentially step program memory 61 through the stored instruction program. This operation causes the operation of computer 12 to be sequentially controlled. The specific steps or program instructions (discussed in more detail infra) are carried out in response to the driving signals from counter 62.

Initially, in response to a signal from counter 62, program memory 61 applies a signal to address select logic 56. This signal may be a multibit signal and is a function

of the particular instruction to be carried out by the computer. This instruction (signal) is stored in a memory location which is addressed by counter 62. The signal from program memory 61 is, in effect, an addressing or enabling signal which is supplied to logic circuit 56. When the appropriate signal is supplied by program memory 61, the signal from any one of sources 50 through 55 (i.e., the digital source signal S1-SNB) is individually transferred through to address select logic 56. The source signal and the instruction signal from memory 61 are combined to form a new address signal for application to data memory 57. Data memory 57 may also be fixed memory such as a read only memory (ROM) into which information has been read and stored. Data memory 57 will operate, to a large extent, as a look-up table.

With the application of the address signal from address select logic 56 (under control of program memory 61), to data memory 57, the information stored at the addressed location is transferred to accumulator 59. This information is also transferred in accordance with standard logic operation and may require an instruction from program memory 61. Clearly, program memory 61 is continually stepped through the instruction sequence by counter 62 until each and every source 50 through 55 has been activated or addressed and the information in the appropriate locations of data memory 57 is addressed and utilized.

Regardless of the particular source which is accessed and which data memory location is addressed, the information stored in data memory 57 (in the form of 10-bit binary signal for example) is transferred to and operated upon by accumulator 59. This transfer is, of course, under control of program memory 61.

In a preferred embodiment accumulator 59 may comprise input selection logic circuitry, an adder and a storage register. The input selection logic is under control of gating signals from program memory 61. The gating signals are dependent upon the instruction being executed and serve to gate information from either temporary storage 60, data memory 57 or special function table 58 into inputs to the adder. Additional gating signals from program memory 61 gate the storage register of the accumulator (or zero) into the adder. The contents of the adder are then gated into the storage register of accumulator 59. The resulting operation is typical of accumulating registers with selective multiple data inputs wherein the contents of the accumulating register is replaced with the sum of the contents of the accumulating register (or zero) and the selected input data.

Temporary storage register 60 is an alterable memory, storage register for partially computed information. Data from accumulator 59 can be gated into temporary storage register 60 under control of gating signals from program memory 61. When the instruction program stored in program memory 61 determines that the information stored in temporary storage register 60 can be further utilized in the pulse width computation, storage register 60 is gated back into the accumulator 59.

In typical operation, as the program address counter 62 advances, the program memory 61 issues a sequence of gating signals as a function of the instruction program stored therein. These gating signals enable the data from sequentially selected sources to be used to address (in conjunction with the source selection sig-

nals) the data memory 57. In effect, the source selection signals are also used to select a particular table (portion of memory) stored in data memory 57 and the data from the source is used to address a particular data point stored in the selected table.

The data used from data memory 57 is accumulated in accumulator 59. The accumulation of data from data memory is only one type of instruction, however, and other instructions cause partial accumulations of data to be stored in temporary storage while additional partial accumulations are developed.

Ultimately, after accumulator 59 has achieved a certain information status and program memory 61 reaches a particular instruction the stored program, information from accumulator 59 is supplied to special function table 58. Table 58 may be an additional fixed memory such as a ROM (or even a portion of memory 57). The signals from accumulator 59 will operate as an address signal relative to table 58. Consequently, information stored in table 58 at the memory location addressed will be transferred (under control of program memory 61) into accumulator 59 and operate as new information stored therein.

The information stored in accumulator 59 may be considered to be comprised of the integer (I) and the fraction (F) portions of a log signal. The fraction portion (F) of the information in accumulator 59 is supplied to antilog table 64 for operation thereby. The integer portion (I) of the information stored in accumulator 59 is supplied directly to register 63. In essence, the signal from the memory location in antilog table 64 addressed by signal (F) is stored in register 63. The integer signal portion (I) is then applied to shift register 63 to shift the information therein the appropriate number of places represented by the integer portion of the signal stored in accumulator 59. This operation is, of course, under control of program memory 61. When this operation is completed, the pulse width signal (PW) represents the pulse width of the signal to be supplied to the fuel injection devices.

To better understand the operation of the pulse width computer shown in FIG. 2, an example of the operation thereof is presented herewith. It will be assumed that the computer is utilized to generate the signal PW. The algorithm for the circuit and the engine may be defined as follows:

$$(EQ. 1) \text{ PW} = \text{PW}_{SB} (1 + E_{S1} K_{S1A} K_{S1B}) (1 + E_{S2} K_{S2A} K_{S2B}) \dots (1 + E_{SN} K_{SNA} K_{SNB})$$

where

PW is the final pulse width;

PW_{SB} is the basic or initial pulse width determined by the basic environmental sensor SB;

E_{Si} is the enrichment factor determined by the data from the environmental sensor S_i ; and

K_{SiA} and K_{SiB} are factors by which enrichment E_{Si} is to be multiplied which factors are determined by data from environmental sensors S_{iA} S_{iB} , respectively.

It must be understood, of course, that the foregoing equation or algorithm used for calculating pulse width is representative only. Any of the respective terms can vary. Moreover, any of the respective constants may be set equal to one or zero wherein the individual terms drop out or are modified to form relative to other terms.

In a relatively simple operation, if a single term is used, Equation 1 reduces to

(EQ.2)

$$PW = PW_{SB} (1 + E_{S1} K_{S1A} K_{S1B})$$

If the following values are ascribed to the remaining balance of the term,

$N = 1$; $E_{S1} = 20$ percent; $K_{S1A} = 90$ percent; $K_{S1B} = 75$ percent

the calculation is as follows:

$$PW = PW_{SB} [1 + (0.20)(0.90)(0.75)]$$

$$PW = PW_{SB} [1 + 0.135]$$

$$PW = PW_{SB} (1.135)$$

Thus, the final pulse width (PW) will be enriched 13.5 percent over the basic pulse width (PW_{SB}).

The equations noted above employ the basic form $A = QRS$. Recognizing that this equation may be rewritten as

$$\log_B A = \log_B Q + \log_B R + \log_B S$$

or as
(EQ.4)

$$A = {}_B \log_B A = {}_B \log_B (QRS) = {}_B (\log_B Q + \log_B R + \log_B S)$$

it becomes reasonable to arrange to computer to operate on logarithms. Logarithms are used so that the various multiplication functions represented by the several equations can be performed using addition.

The computer (see FIG. 2) uses the digital data from environmental sensors 10 (see FIG. 1) which represent air temperature, manifold pressure and the like as addresses to fixed memory 57 which stores data representing the basic pulse width (PW_{SB}), enrichment (E), and scale factors (K) in the form of binary numbers. These numbers are read out of the memory and processed in the arithmetic section of the computer in an order determined by the instruction program also stored in program memory 61. Since the data representing the signals is stored as logarithms, the computer can use these numbers to calculate the pulse width in accordance with the instruction program described hereinafter.

Referring to Equation 1 supra, program address counter 62 initiates operation by supplying a signal to program memory 61 which enables a particular portion of address select logic circuit 56. In particular, the signal from program memory 61 selects or enables logic circuit 56 wherein the digital binary signal S1 from source 50 is selected. Signal S1 (along with a portion of the instruction signal from program memory 61) is used as the memory address signal and is applied to data memory 57. In accordance with an additional signal from program memory 61, the data stored at memory location S1 is selected and information representing E_{S1} is transferred to and stored in accumulator 59. Depending upon the operation of accumulator 59, the information stored therein may be transferred to temporary storage 60 under control of program memory 61. Conversely, and in the usual practice, the information $\log_{B1} E_{S1}$ may remain in accumulator 59 and program memory 61 is stepped to select or enable logic circuit 56 to operate upon signal S2 from source 51. Signal S2 (and the instruction signal) operate as an address signal and addresses data memory 57. The signal information stored in memory address S2 is then trans-

ferred to accumulator 59 under control of program memory 61. Thus, the signal $\log_{B1} K_{S2}$ is stored in accumulator 59.

As suggested supra, if accumulator 59 includes an adder circuit the signals $\log_{B1} E_{S1}$ and $\log_{B1} K_{S2}$ are immediately added together. This type operation continues until the signal stored in accumulator 59 represents the sum of the logarithms of signals E_{S1} , K_{S1A} , and K_{S1B} . This summed signal is used as the address signal for special function table 58. As noted, table 58 may represent a separate fixed memory or a data memory 57. Clearly, this particular concept is a function of mechanics only and is determined by the size of the memory utilized in the circuit.

However, this address signal (i.e., the sum of the logs) addresses table 58 and produces an output signal which represents the $\log_{B2} (1 + (B1)^M)$ where M is the table address. This signal represents the total function or term $1 + E_{ij}$ (as shown in equation 1). This signal is represented as $\log_B (X)$ and is transmitted to accumulator 59 under control of program memory 61. The signal is further transferred into temporary storage 60 in accordance with an instruction from program memory 61.

Continuing on with the same mode of operation, each of the other individual terms in equation 1 is calculated. In addition, each term is added to the number previously stored in temporary storage 60. The new number is then placed in temporary storage 60 and represents the new sum.

Ultimately, by continuing with the same process, under the control of program memory 61, the total enrichment factor (TE) is accumulated. This factor is represented as:

$$\log_{B2} TE = \log_{B2} [(1 + E_{S1} K_{S1A} K_{S1B})(1 + E_{S2} K_{S2A} K_{S2B}) \dots (1 + E_{SN} K_{SN4} K_{SNB})]$$

Now, the address from the basic environmental sensor SB is obtained under control of program memory 61 and the information representative of term PW_{SB} is obtained from data memory 57. This signal is added to the other signals (TE) and stored in accumulator 59. The total of this summation (L) is the log of the computer pulse width and may be represented as follows:

(EQ. 6)

$$L = I + F$$

where the signal is now represented by integer (I) and fraction (F) parts. The fraction signal (F) is used as the address for antilog table 64. The signal F functions as the address signal for table 64. Under control of program memory 61, the information, i.e., binary number, stored at the address in table 64 is transferred to register 63. In addition, the integer signal (I) from accumulator 59 is subsequently applied to register 63. Under control of program memory 61, register 63 operates to shift the data stored therein from table 64, I places to the left. This operation has the effect of establishing both the integer and fraction portions of the signal in accumulator 59 in register 63. Once the signal from table 64 has been shifted I places to the left, the resulting number or signal in shift register 63 represents the number PW. This number is used to determine the increment of time that an injector is operative.

In the foregoing discussion the pulse width computer as shown in FIG. 2, would require a large data memory. That is, the memory would require memory locations for each source 50 through 55 times the number of points or locations on the curve representing each of these functions. For example, in the event that there are 16 sources (one basic source, five actual parameters and two modifiers for each parameter) as well as 256 points on each characteristic curve, the memory would require 4,096 storage areas. In the event that each storage location is represented by a 10 bit digit, over 48,000 bit storage elements would be required.

Conversely, if the interpolation computer system embodiment shown in FIG. 3 is utilized, the same 16 source signals and 17 parameter points on the characteristic curve would require only 272 storage areas (2,720 bits).

If the interpolation approach is utilized, scaler 65 is connected between data memory 57 and accumulator 59. In addition, address storage register 66 is connected between address select logic circuit 56, data memory 57 and scaler 65. In this circuit, operation is similar to the circuit shown in FIG. 2 except that the most significant portion (MSP) and the least significant portion (LSP) of the address information are handled separately. For example, the MSP of the data information representing an address signal from logic circuit 56 is applied indirectly to data memory 57 via address register 66 to cause the transfer of information therefrom into scaler 65. The remaining portion of address information from logic circuit 56 is applied (via address register 66) to scaler 65. In addition, the address signal from address select logic 56 is supplied to and stored in storage register 66. In some cases, register 66 may operate upon the address signal to increment the MSP portion of the address and provide a one's complement of the LSP portion. These interconnections permit linear interpolation to be performed on two adjacent memory locations in data memory 57 with two adjacent and related instructions in program memory 61. Thus, information from the prescribed memory location in data memory 57 is applied to accumulator 59 via scaler 65. The program memory 61 is then operative to increment storage register 66 by one count whereby the next data storage area in data memory 57 is addressed and accessed. This information in this storage area is then supplied to accumulator 59 via scaler 65. The effect of this operation is that the information stored in two adjacent memory locations in data memory 57 is called and summed whereby an intermediate information signal is supplied to accumulator 59 representing an interpolated value between the two adjacent locations. Clearly, a smaller memory may be utilized since the same information is used more frequently and intermediate values are calculated. This operation avoids having to store all of the intermediate values in separate memory locations.

If the data path represented by dashed line 64A between accumulator 59 and table 64 is provided, the output signals from antilog table 64 may be entered directly into the accumulator. In addition, if the data path represented by dashed line 57A is used, accumulator 59 can be used to directly address data memory 57. With these interconnections, the special computer can be programmed by inserting appropriate instructions to program memory 61 to handle extremely complex arithmetic expressions for pulse width.

Thus, there has been shown and described a special purpose digital computer which has a special utilization in fuel injection systems. The computer can add, multiply, divide and generate special functions. This type of computer, while discussed in terms of a fuel injection system application, may find utilization in a number of special purpose computer applications.

The embodiments shown herein are illustrative only. Those skilled in the art may develop systems which utilize these general concepts. Such systems are intended to be included in this description. Moreover, the specific implementation of the various types of circuitry are not included herein. For the most part, these types of circuitry are conventional and those skilled in the art would be able to provide detailed circuits and alternatives therefor.

Thus, what is claimed is:

1. In combination,
 - a plurality of source means,
 - control means,
 - logic means connected to receive signals from said source means and said control means,
 - data memory means connected to receive signals from said logic means and to supply information from memory locations addressed by said signals from said logic means,
 - accumulator means connected to receive the information from said memory locations and to operate thereon to produce sum signals,
 - output memory means connected to said accumulator means to receive and operate upon only a first portion of said sum signals and to supply an output memory signal as a function of the portion of said sum signals supplied to said output memory means, and
 - output register means connected to receive said output memory signal and a second portion of said sum signals from said accumulator means to selectively alter the output memory signal previously stored in said output register means.
2. The combination recited in claim 1 including storage means connected to said accumulator means for storing current information from said accumulator means during the insertion of new information therein and for subsequently retiring of said current information to said accumulator means for combination with the new information stored therein.
3. The combination recited in claim 1 including function memory means connected to said accumulator means and said control means whereby the information in said accumulator means operates as an address signal for said function memory means,
 - said function memory means connected to supply information at the memory location addressed by said address signal to said accumulator means.
4. The combination recited in claim 1 wherein said control means includes
 - program memory means, and
 - program address counter means,
 - said program address counter means comprises a free running counter which is connected to supply signals to said program memory means in order to step said program memory means through the instruction program stored therein to control the functions of the entire combination.

5. The combination recited in claim 1 wherein each of said memory means includes a plurality of memory locations, each of said memory means is a read only memory which has specific information stored at each memory location.

6. The combination recited in claim 1 including scaler means connected between said data memory means and said accumulator means to operate upon and modify the information from said memory locations before transfer to said accumulator means, and

address means connected between said logic means and said accumulator means to operate upon the signals from said logic means to change the memory location in said data memory means addressed by the signals from said address means.

7. The combination recited in claim 1 wherein said signals and said information are arranged in digital form.

8. The combination recited in claim 1 wherein said accumulator means is connected to supply address signals to said data memory means.

9. The combination recited in claim 1 wherein said output memory means is connected to supply information signals to said accumulator means.

10. The combination recited in claim 6 wherein said address means includes means for operating upon the signals from said logic means by incrementing a portion thereof and providing a one's complement of another portion thereof.

11. The combination recited in claim 1 wherein output memory means stores information in logarithmic form.

12. The combination recited in claim 11 wherein said output memory means stores information in an antilog form.

13. The combination recited in claim 3 wherein said output register means is connected to receive signals from said output memory means and store the signals so received,

said output register means further connected to said accumulator means to receive signals from said function memory means which alter the signals previously stored in said output register means.

14. The combination recited in claim 1 wherein said logic means includes means for combining the signals received from said source means and the signals received from said control means to produce address signals for selecting the memory locations in said data

memory means which will supply information.

15. The combination recited in claim 1 which produces output signals from said output register means in accordance with the algorithm

$$PW = PW_{SB} (1 + E_{Si} K_{Sij})$$

where

PW is the final pulse width of the output signal,

PW_{SB} is a base pulse width determined by first source SB,

E_{Si} is the enrichment factor determined by the respective source S_i , and

K_{Sij} are constants related to source S_i .

16. The combination recited in claim 1 wherein said sources include transducers for producing signals representative of environmental conditions.

17. The combination recited in claim 1 including utilization means connected to said output register means.

18. The combination recited in claim 4 wherein said program memory means includes a plurality of memory locations,

each of said memory locations has an instruction of said instruction program stored therein,

each instruction is in the form of a multibit digital signal,

25 said program memory means connected to supply each instruction to said logic means in accordance with the operation of said program address counter means,

30 each instruction enables a selected portion of said logic means whereby selected signals from said source means are transferred to said data memory means as address signals.

19. The combination recited in claim 1 wherein said accumulator means includes means for cumulatively storing information supplied thereto whereby the information stored in said accumulator means represents the instantaneous total of all information supplied thereto.

40 20. The combination recited in claim 19 wherein the information stored in said accumulator means represents an address in a portion of said data memory means,

said accumulator means and said portion of said data memory means interconnected so that the information stored at the appropriate address in said portion of said data memory means is transferred to said accumulator means when addressed.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,838,397

Dated September 24, 1974

Inventor(s) George A. Watson et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 3, line 59, change "antilg" to --antilog--.

Column 6, line 14, delete "instructio",
line 14, after "instruction" insert --in--,
line 18, change "signals" to --signal--.

Column 7, line 26, change "to computer" to --the computer--.

Column 8, line 20, change " $\log_B$ " to -- $\log_{B_2}$ --.

Column 9, line 49, change "caled" to --scaled--.

Column 10, line 5, change "retiring" to --returning--.

Column 11, line 31, after "wherein" insert --said--.

Signed and sealed this 7th day of January 1975.

(SEAL)
Attest:

McCOY M. GIBSON JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents