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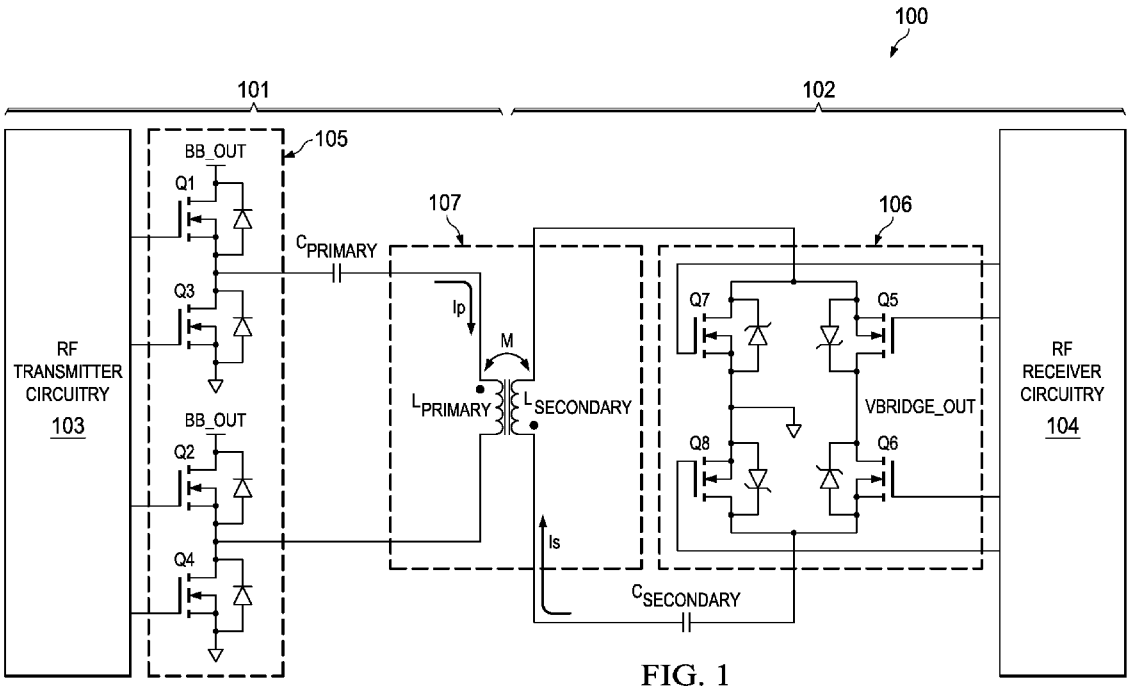

FIG. 1

(57) Abstract: In systems (100) and methods for wireless power transfer with fractional timing resolution, an electrical power transmitter (101) may include: a transistor (Q1); and a rising edge control circuit (103) to control a gate of the transistor (Q1) to produce a rising edge of a pulse at a time selected with a resolution greater than a full-clock period.

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WIRELESS POWER TRANSMISSION WITH FRACTIONAL TIMING RESOLUTION

[0001] This relates generally to wireless power transmission, and more particularly to wireless power transmission with fractional timing resolution.

BACKGROUND

[0002] A wireless power transmission system has a radio-frequency (RF) transmitter and an RF receiver. The RF transmitter is coupled to a source of electrical power (*e.g.*, a mains power line), and it converts an electrical current into an oscillating electromagnetic field using an inductor, coil, antenna, metal plate, or other coupling device. Another coupling device at the RF receiver captures a portion of the radiated electromagnetic field (the two coils in proximity to each other form an electrical transformer), and the RF receiver then converts the received electromagnetic field back into an electrical current.

[0003] In many implementations, the RF transmitter may be disposed within a charging pad or station, and the RF receiver may be coupled to a computing device (such as a desktop, laptop, tablet, smart phone, etc.) or a battery. The energy transferred between the RF transmitter and the RF receiver may then be used to operate the computing device and/or to charge the battery. Hence, transfer efficiency (the amount of energy that is received relative to the amount of energy that is transmitted) is a critical parameter in wireless power transfer design.

[0004] Coils in both the RF transmitter and the RF receiver are controlled using a number of switches or transistors, and increasing the power transfer efficiency often requires precise control of those transistors. However, the high-frequency clocks that would typically be necessary to provide such control would significantly increase cost and complexity.

SUMMARY

[0005] In described examples of systems and methods for wireless power transfer with fractional timing resolution, an electrical power transmitter may include a transistor and a rising edge control circuit configured to control a gate of the transistor to produce a rising edge of a pulse at a time selected with a resolution greater than a full-clock period.

[0006] The electrical power transmitter may also comprise an inductor configured to emit

power wireless over a power carrier frequency, where the full-clock period is the inverse of the power carrier frequency. The electrical power transmitter may also comprise a phased-locked loop (PLL) circuit having a voltage controlled oscillator (VCO), where the VCO is configured to produce a clock signal having a frequency n times greater than a power carrier frequency.

[0007] In some cases, the rising edge control circuit may include a divider circuit coupled to the VCO and configured to divide the clock signal into *n* portions. The rising edge control circuit may also include a multiplexer coupled to the VCO and configured to subdivide each of the *n* portions into a plurality of *m* sub-portions. For example, *m* may be a number of clock phases of the VCO. The rising edge control circuit may further comprise a delay circuit configured to apply a timing delay only to fewer than all possible m values. The resolution may be equal to the inverse of the power carrier frequency divided by a product of *n* times *m*.

[0008] In some implementations, the gate of the transistor may be controlled via a falling edge control circuit that employs the power carrier frequency to produce a falling edge of the pulse at a subsequent time selected with the resolution. The wireless power transmitter further may include a flip-flop having a set input coupled to the rising edge control circuit and a reset input coupled to the falling edge control circuit, such that an output of the flip-flop is used to produce the pulse, and where the pulse is a pulse-width modulated (PWM) pulse usable to drive the gate of the transistor.

[0009] The electrical power transmitter may also include a receiver comprising: another inductor configured to receive the wireless power; and another transistor coupled to the other inductor, where another gate of the other transistor is controlled using another rising edge control circuit and another falling edge control circuit, and where the other rising edge control circuit and the other falling edge control circuit are configured to generate, using the power carrier frequency, another pulse having the resolution. The transistor may be part of an H-bridge circuit, and the other transistor may be part of a rectifier bridge.

[0010] In another embodiment, a computing device may include a processor and a wireless power receiver configured to provide power to the processor, where the wireless power receiver comprises an inductor coupled to a transistor, and where a gate of the transistor is controlled, in part, via a rising edge control circuit configured to employ a power carrier frequency to produce a rising edge of a pulse at a time selected with a resolution greater than an inverse of the power carrier frequency.

[0011] The wireless power receiver may be configured to provide power to the processor by charging a battery. The transistor may be part of a rectifier circuit. And the wireless power receiver further may include a VCO of a PLL circuit, wherein the VCO is configured to receive the power carrier frequency and to produce a clock signal having n times the power carrier frequency.

[0012] The rising edge control circuit may include a divider coupled to the VCO and configured to split the clock signal into *n* portions; and a multiplexer coupled to the VCO and configured to subdivide each of the n portions into a plurality of *m* sub-portions, where m is a number of clock phases of the VCO, and where the resolution is equal to the inverse of the power carrier frequency divided by a product of *n* times *m*. The gate of the transistor may be further controlled, in part, via a falling edge control circuit configured to employ the power carrier frequency to produce a falling edge of the pulse at a subsequent time selected with the resolution, where the wireless power receiver further comprises a flip-flop having a set input coupled to the rising edge control circuit and a reset input coupled to the falling edge control circuit, and where an output of the flip-flop is usable to produce the pulse.

[0013] In yet another embodiment, a method may include receiving electrical power wirelessly via an inductor over a power carrier frequency, where the inductor is coupled to a rectifier having a set of transistors; generating a PWM signal using one or more selected ones of *n* x *m* subdivisions of a VCO output produced by a VCO of a PLL circuit, where the VCO is configured to receive a reference clock having the power carrier frequency and to produce the output having *n* times the power carrier frequency and *m* selectable phases; and controlling each of the set of transistors with the PWM signal. The method may also include providing the power to a battery or computing device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 is a block diagram of an example of a wireless power transmission system according to some embodiments.

[0015] FIG. 2 is a block diagram of an example of a phased-locked loop (PLL)-based pulse-width modulation (PWM) generator with fractional period timing resolution according to some embodiments.

[0016] FIG. 3 is a circuit diagram of an example implementation of the PLL-based PWM generator with fractional period timing resolution according to some embodiments.

[0017] FIG. 4 is a chart illustrating the operation of a PLL-based PWM generator with fractional period timing resolution according to some embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0018] FIG. 1 is a block diagram of an example wireless power transmission system 100 according to some embodiments. As shown, wireless power transmission system 100 includes radio frequency (RF) transmitter 101 and RF receiver 102.

[0019] RF transmitter 101 includes RF transmitter circuitry 103 and H-bridge 105 having a plurality of transistors or switches Q1-Q4. As used herein, the term "H-bridge" refers to an electronic circuit that enables a voltage to be applied across a load in either direction. In various embodiments, transistors Q1-Q4 may each have a diode between source and drain terminals. For example, Q1-Q4 may be implemented as power metal–oxide–semiconductor field-effect transistors (MOSFETs) or the like.

[0020] RF transmitter 101 also includes primary smoothing capacitance ($C_{primary}$) and primary inductor, coil, or antenna ($L_{primary}$) coupled to H-bridge 105. When $L_{primary}$ is electromagnetically coupled to a secondary inductor, coil, or antenna ($L_{secondary}$), it forms electrical transformer 107.

[0021] RF receiver 102 includes $L_{secondary}$ and secondary smoothing capacitance ($C_{secondary}$) coupled to rectifier bridge 106. Rectifier bridge 106 includes a plurality of transistors or switches Q4-Q8 (*e.g.*, power MOSFETs) coupled to RF receiver circuitry 104. The node between Q5 and Q8 provides an output voltage rail (V_{bridge_out}). V_{bridge_out} is then provided to a buck-boost converter, voltage regulator, or the like (not shown), in order to power an electrical load, such as a battery or processor of a computing device.

[0022] Electrical transformer 107 enables primary electric current I_p to be converted into electromagnetic field M, which is then emitted by $L_{primary}$ as a power carrier signal having a power carrier frequency. In turn, $L_{secondary}$ receives a portion of the electromagnetic energy and converts it into secondary electric current I_s.

[0023] The efficiency of the power transfer between RF transmitter 101 and RF receiver 102 is given by the ratio between energy transmitted and energy received, which is proportional to the ratio between electrical currents I_s and I_p. Moreover, this efficiency is largely dependent upon the speed and precision with which transistors Q1-Q8 can be turned on (conductive) and off (non-conductive save for leakage effects), in order to generate I_p and I_s.

[0024] Broadly, transistors Q1-Q8 are controlled by RF transmitter circuitry 103 and RF

receiver circuitry 104, which apply pulse signals to the gate terminals of their respective transistors. In various embodiments, RF transmitter circuitry 103 and RF receiver circuitry 104 may produce pulse-width modulated (PWM) pulses having a timing resolution or granularity selected based upon a fractional division of a clock signal. For example, such a clock signal may the same frequency over which power is wirelessly radiated (power carrier frequency).

[0025] For example, if the power carrier frequency is over several Megahertz, such as 6.78 MHz, then the resolution or granularity for the gate driver pulses (on/off) should be in the 1.1 ns range. Given this requirement, a system clock of 870 MHz would ordinarily be needed as a time basis for generating these pulses. However, operating at this high clock frequency would significantly increase the implementation cost and complexity of the final solution. A major cost adder is the fact that the required process and technology for implementing such a system needs to concurrently support both high voltage and high speed operation. This is usually not easy to achieve at an acceptable cost. Also, the resulting high power consumption is another factor which renders conventional implementations uncompetitive.

[0026] Accordingly, in various embodiments, fractional division of the clock signal may be achieved with a phase-locked loop (PPL) circuit coupled to one or more gate control circuits, as depicted in FIG. 2. Particularly, FIG. 2 is a block diagram of PLL-based PWM pulse generator with fractional period timing resolution 200. In various embodiments, one or more instances of generator 200 may be deployed in RF transmitter circuitry 103 and/or RF receiver circuitry 104.

[0027] As shown, voltage controlled oscillator (VCO) 203 receives, from a PLL filter (not shown), a signal locked to the power carrier frequency (*e.g.*, running 6.78 MHz). In response, VCO 203 produces a clock having a frequency n times greater the power carrier frequency (*e.g.*, if n = 16, then the output clock frequency of VCO 203 is 108.48 MHz). In some implementations, VCO 203 may be an m-stage fully differential ring oscillator (*e.g.*, an 8-stage oscillator running at 108.48 MHz).

[0028] The output of VCO 203 is provided to divider circuit 204 (in this case, divides the clock period in 16 parts or "bins." Rising edge control circuit 201 includes first multiplexer 205 configured to receive one of the m phases of VCO 203, and to select one a value of m (*e.g.*, based upon a 3-bit LSB portion of a control word). Counter selection circuit 209 selects one of the n bins from divider 204 (*e.g.*, based upon a 4-bit MSB portion of the control word). The outputs from multiplexer 205 and counter selection circuit 209 are combined by logic gate 207 to select a

rise time for a PWM pulse with a time resolution or granularity (and/or in discrete time increments) equal to the period of the power carrier frequency divided by the product of n x m.

[0029] Particularly, in the case where the frequency 6.78 MHz, the period of the power carrier signal is ~147 ns; yet when n = 16 and m = 8, the timing resolution for the selected rise time is in the order of 1.15 ns.

[0030] Still referring to FIG. 2, falling edge control circuit 202 is similar to rising edge control circuit 201, in that multiplexer 208 may be another instance of the same device as multiplexer 205, and counter selection circuit 209 may be another instance of the same device as counter selection circuit 206.

[0031] The output of logic gate 207 is coupled to the set input of flip-flop 211, and the output of logic gate 210 is coupled to the reset input of flip-flop 211. Accordingly, the resulting PWM pulse at the output of flip-flop 211 is produced with rising and falling edges selected with the aforementioned increased timing granularity or resolution.

[0032] PLL-based PWM pulse generator 200 is capable of sub-nanosecond PWM pulse fidelity while running only at a 108.48 MHz system clock speed (from VCO 203). Fractional timing resolution may be achieved by tapping intermediate stages within an 8-stage ring oscillator. An all-digital gate-pulse encoder combines the ring oscillator clock phases with state information coming from the PLL feedback divider resulting in a high fidelity, extremely flexible PWM pulse generator.

[0033] The result is a PWM generation scheme with a 1.15 ns resolution for both pulse width and location. Thus, the PWM pulses driving the gates of NexFet devices Q1-Q8 (on both transmitter and synchronous receiver/rectifier) are able to start anywhere and stop anywhere within a 1/6.78 MHz (~147 ns) reference clock cycle.

[0034] On the transmitter side, VCO 203 is part of a PLL frequency synthesizer locked to an external reference clock running at 6.78MHz. The receiver side may use all of the same circuitry except that the 6.78MHz received carrier signal serves as the PLL reference.

[0035] In some implementations, the circuit may yield the rising edge of the PWM pulse any start time (*e.g.*, always at t = 150 ns), while the falling edge may be selected at any discrete time from t = 150 ns + 1.15 ns to t = 150 ns + 1.15 ns x 124 = 292 ns. The pulse width of each of pulse may be controlled as the select of the decoder controlling the falling edge varies between 1 and 124 (7 bits of resolution).

[0036] For example, eight clock phases out of an 8-stage VCO ring oscillator may be combined with a 16 feedback divider (divide by 16) tap to generate PWM control pulses for all 4 gate/FET drivers on both transmitter (primary) and receiver (secondary) sides. Accordingly, the 147 ns (1/6.78 Mhz) reference clock cycle gets divided into 128 slots, each slot being 1.15 ns wide. Finally, the rising edge control output sets the SR FF (which starts the PWM pulse), whereas the falling edge control output resets the SR FF (which ends the PWM pulse).

[0037] Depending upon the speed limitations of the choice of process node, PWM width of 125-128 may not be coverable with circuit 200; but that is not necessary for this application. Yet, in other embodiments, the entire PWM width range may be covered.

[0038] FIG. 3 is a circuit diagram of implementation example 300 of PLL-based PWM generator with fractional period timing resolution 200 according to some embodiments. Here, multiplexer circuit 301 (MUX1) may implement counter selectors 206 and/or 209, and multiplexer circuit 305 may implement multiplexers 206 and/or 208. Implementation example 300 also includes timing circuit 308 configured to operate upon a subset of phases selected via multiplexer 305 prior to being combined with the output of multiplexer circuit 301 via multiplexer 209 and in order to select a particular time for a rising or falling edge of the ultimate PWM pulse.

[0039] Multiplexer circuit 301 includes a first set of logic gates 302 configured to select a first subset of the 16 bins (referred to as bins 0 through 15) resulting from operation of divider 204 using a two-bit portion of a 7-bit control word (*e.g.*, bits 5 and 6). Here, each of the subsets of bins has 4 coarse subdivisions: SEL counters = 0->3, 4->7, 8->11, or 12->15.

[0040] Multiplexer circuit 301 also includes a second set of logic gates 303 or multiplexers configured to select, within each of the subset of bins, a particular one of those bins using another two-bit portion of the 7-bit control word (*e.g.*, bits 3 and 4). Here, COUNTER decode inputs are again dispersed into different groups: COUNTER decode = 0->3, 4->7, 8->11, or 12->15, each COUNTER decode input selecting an individual bin within that subset of bins (finer or more precise selection). Finally, the output of logic gates 302 and 303 are combined by logic gates 304 to select a specific one of the 16 bins by outputting a selected value of *m*.

[0041] Multiplexer circuit 305 includes multiplexer 306 and multiplexer 307. Multiplexer 306 is operable to select one of phases 1, 2, 3, or 4 of VCO 203, and multiplexer 307 is operable to select one of phases 5, 6, 7, or 0. When either multiplexer 306 or 307 selects a phase, the value

of *n* is set and multiplexer 309 issues a rising or falling edge at a time selected with increased resolution (*e.g.*, 1.15 ns). In some cases, timing circuit 308 may be used to adjust the timing of certain phase selections at the output of multiplexer 307 to avoid leakage effects or the like.

[0042] Accordingly, multiplexer circuit 301 selects which one of the 16, CNTR feedback divider phases is used. All the CNTR phases come off the same tap of the VCO, namely VCO PHASE 0. Also, multiplexer circuit 301 gates the VCO phases 1, 2, 3, 4, which at this point can be directly ANDed with whichever COUNTER state is selected, given that the CNTR changes state on Phase 0. Meanwhile, multiplexer circuit 305 has 2 outputs: a first one is the MUXed phases 1, 2, 3, 4, which gets ANDed directly. The second output is the MUXed phases 5, 6, 7, 0, which take another route through clock re-timing circuit 308 in order to not create an unwanted double edge when the COUNTER selected state (clocked by VCO Phase 0) gets ANDed with the MUXed Phase 5, 6, 7, 0.

[0043] In some cases, clock re-timing circuit 308 may use the VCO phase 4 to resample the output and re-time it for subsequent VCO phases 5, 6, 7, 0. Again, this ensures that when VCO phases 5, 6, 7, 0 get ANDed–inside the clock re-timing circuit 308–with the selected and re-timed CNTR state, no double clock is occurring. Finally, multiplexer 309 selects (based on SELclk<2>) which VCO Phase bank (1, 2, 3, 4 or 5, 6, 7, 0) goes to the final output.

[0044] FIG. 4 shows chart 400 illustrating the operation of PLL-based PWM generator with fractional period timing resolution 200 according to some embodiments. VCOCLK signal 401 is the clock signal output by VCO 203, which has 16x the power carrier frequency, shown as REFCLK signal 402 (*e.g.*, 108.48 and 6.78 MHz, respectively). The output of counter selector(s) 403 are bins 0-16 shown in gated curve 403.

[0045] In at least one example, the control word is a 7-bit word divided into two groups, which are: the four upper bits or MSBs; and the three lower bits or LSBs. The first group encodes a selected value for *n* (bin number 0->15) and the second portion encodes a selected value for *m* (phase 0->7). Moreover, the first group is further subdivided into two parts: a first, 2-bit part that indicates a subset of bins, and a second, 2-bit part that indicates an individual bin within the subset.

[0046] In this example, a first pulse has a rising edge 405 given by control word 0011010, in binary form. In sequential order from left to right, in the 4 MSBs, "00" indicates one of the four subset of bins (*e.g.*, one of bins 0-4, in this case bin 0), and "01" pinpoints the third bin within

that subset (in this case, bin 3). Moreover, in the 3 LSBs, "010" indicates the intra-bin subdivision ($m = 2$).

[0047] The pulse then has a falling edge 406 selected by control word 0101110 which, precisely places it at the 6^{th} intra-bin subdivision ($m = 6$) of bin 5 ($n = 5$). Thus, using the granularity afforded by systems and methods described herein, rising edge 405 may be placed at a precisely desired rise time.

[0048] At a later time, a subsequence pulse has a rising edge 407 and falling edge 408 selected by control words 1001110 and 1011001, respectively. Using systems and methods described herein, rising edge 405 is placed at the 6^{th} intra-bin subdivision ($m = 6$) of bin 9 ($n = 9$), and falling edge 408 is placed at the first intra-bin subdivision ($m = 1$) of bin 11 ($n = 11$).

[0049] In contrast with systems and methods described herein, conventional solutions to the foregoing problems fall in one of two categories. First, digital PWM generators exist that invariably rely on a PLL/DLL type implementation with synchronous PWM generation. These implementations require a system clock running at the rate proportional to the required PWM resolution (such as 870 MHz for a ~1.15 ns timing resolution). Moreover, these implementations suffer from high implementation cost, high power consumption and increased complexity.

[0050] Second, analog implementations exist that rely on the counter, digital-to-analog converter (DAC), and comparator schemes to generate PWM pulses. However, these analog techniques suffer from limitations typically associated with analog circuits, such as poor component matching, drift over temperature, variation over process, higher power, potential instability, and/or reduced scalability.

[0051] Also, compared to full-clocked -based designs (such as where the VCO runs at 1/1.15 ns = 870 Mhz), systems and methods described herein may provide a number of features, such as allowing cheaper and/or older technologies to employ high-voltage capabilities needed to drive the external NexFet devices. These systems and methods also use much less power given that the maximum frequency of operation is only 1/8 of the full-clock -based design (RMS power is proportional to the operating frequency).

[0052] Compared with traditional analog PWM generation schemes, the proposed PWM generator provides superior performance without the need for background calibration or trimming. An all-digital implementation results in improved part-to-part matching, and consistent and repeatable performance across wide operating temperature ranges. These systems

and methods are flexible and scalable to any desirable PWM and/or reference frequency.

[0053] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An electrical power transmitter, comprising:

a transistor; and

a rising edge control circuit configured to control a gate of the transistor to produce a rising edge of a pulse at a time selected with a resolution greater than a full-clock period.

2. The electrical power transmitter of claim 1, wherein the electrical power transmitter further comprises an inductor configured to emit power wireless over a power carrier frequency, and wherein the full-clock period is the inverse of the power carrier frequency.

3. The electrical power transmitter of claim 1, wherein the electrical power transmitter further comprises a phased-locked loop (PLL) circuit having a voltage controlled oscillator (VCO), and wherein the VCO is configured to produce a clock signal having a frequency *n* times greater than a power carrier frequency.

4. The electrical power transmitter of claim 3, wherein the rising edge control circuit comprises a divider circuit coupled to the VCO and configured to divide the clock signal into *n* portions.

5. The electrical power transmitter of claim 4, wherein the rising edge control circuit further comprises a multiplexer coupled to the VCO and configured to subdivide each of the *n* portions into a plurality of *m* sub-portions.

6. The electrical power transmitter of claim 5, wherein *m* is a number of clock phases of the VCO.

7. The electrical power transmitter of claim 6, wherein the rising edge control circuit further comprises a delay circuit configured to apply a timing delay only to fewer than all possible *m* values.

8. The electrical power transmitter of claim 5, wherein the resolution is equal to the inverse of the power carrier frequency divided by a product of *n* times *m*.

9. The electrical power transmitter of claim 1, wherein the gate of the transistor is further controlled via a falling edge control circuit that employs the power carrier frequency to produce a falling edge of the pulse at a subsequent time selected with the resolution.

10. The electrical power transmitter of claim 9, wherein the wireless power transmitter further comprises a flip-flop having a set input coupled to the rising edge control circuit and a

reset input coupled to the falling edge control circuit, wherein an output of the flip-flop is used to produce the pulse, and wherein the pulse is a pulse-width modulated (PWM) pulse usable to drive the gate of the transistor.

11. The electrical power transmitter of claim 1, further comprising:

a receiver, comprising: another inductor configured to receive the wireless power; and another transistor coupled to the other inductor, wherein another gate of the other transistor is controlled using another rising edge control circuit and another falling edge control circuit, and wherein the other rising edge control circuit and the other falling edge control circuit are configured to generate, using the power carrier frequency, another pulse having the resolution.

12. The electrical power transmitter of claim 11, wherein the transistor is part of an H-bridge circuit, and wherein the other transistor is part of a rectifier bridge.

13. A computing device, comprising:

a processor; and

a wireless power receiver configured to provide power to the processor, wherein the wireless power receiver comprises an inductor coupled to a transistor, and wherein a gate of the transistor is controlled, in part, via a rising edge control circuit configured to employ a power carrier frequency to produce a rising edge of a pulse at a time selected with a resolution greater than an inverse of the power carrier frequency.

14. The computing device of claim 13, wherein wireless power receiver is configured to provide power to the processor by charging a battery.

15. The computing device of claim 13, wherein the transistor is part of a rectifier circuit.

16. The computing device of claim 13, wherein the wireless power receiver further comprises a voltage controlled oscillator (VCO) of a phased-locked loop (PLL) circuit, wherein the VCO is configured to receive the power carrier frequency and to produce a clock signal having n times the power carrier frequency.

17. The computing device of claim 16, wherein the rising edge control circuit further comprises:

a divider coupled to the VCO and configured to split the clock signal into n portions; and

a multiplexer coupled to the VCO and configured to subdivide each of the n portions into a plurality of m sub-portions, wherein m is a number of clock phases of the VCO, and wherein the resolution is equal to the inverse of the power carrier frequency divided by a product of n

times *m*.

18. The computing device of claim 13, wherein the gate of the transistor is further controlled, in part, via a falling edge control circuit configured to employ the power carrier frequency to produce a falling edge of the pulse at a subsequent time selected with the resolution, wherein the wireless power receiver further comprises a flip-flop having a set input coupled to the rising edge control circuit and a reset input coupled to the falling edge control circuit, and wherein an output of the flip-flop is usable to produce the pulse.

19. A method, comprising:

receiving electrical power wirelessly via an inductor over a power carrier frequency, wherein the inductor is coupled to a rectifier having a set of transistors;

generating a pulse-width modulated (PWM) signal using one or more selected ones of *n* x *m* subdivisions of a voltage controlled oscillator (VCO) output produced by a voltage controlled oscillator (VCO) of a phase-locked loop (PLL) circuit, wherein the VCO is configured to receive a reference clock having the power carrier frequency and to produce the output having *n* times the power carrier frequency and *m* selectable phases; and

controlling each of the set of transistors with the PWM signal.

20. The method of claim 19, further comprising providing the power to a battery or computing device.

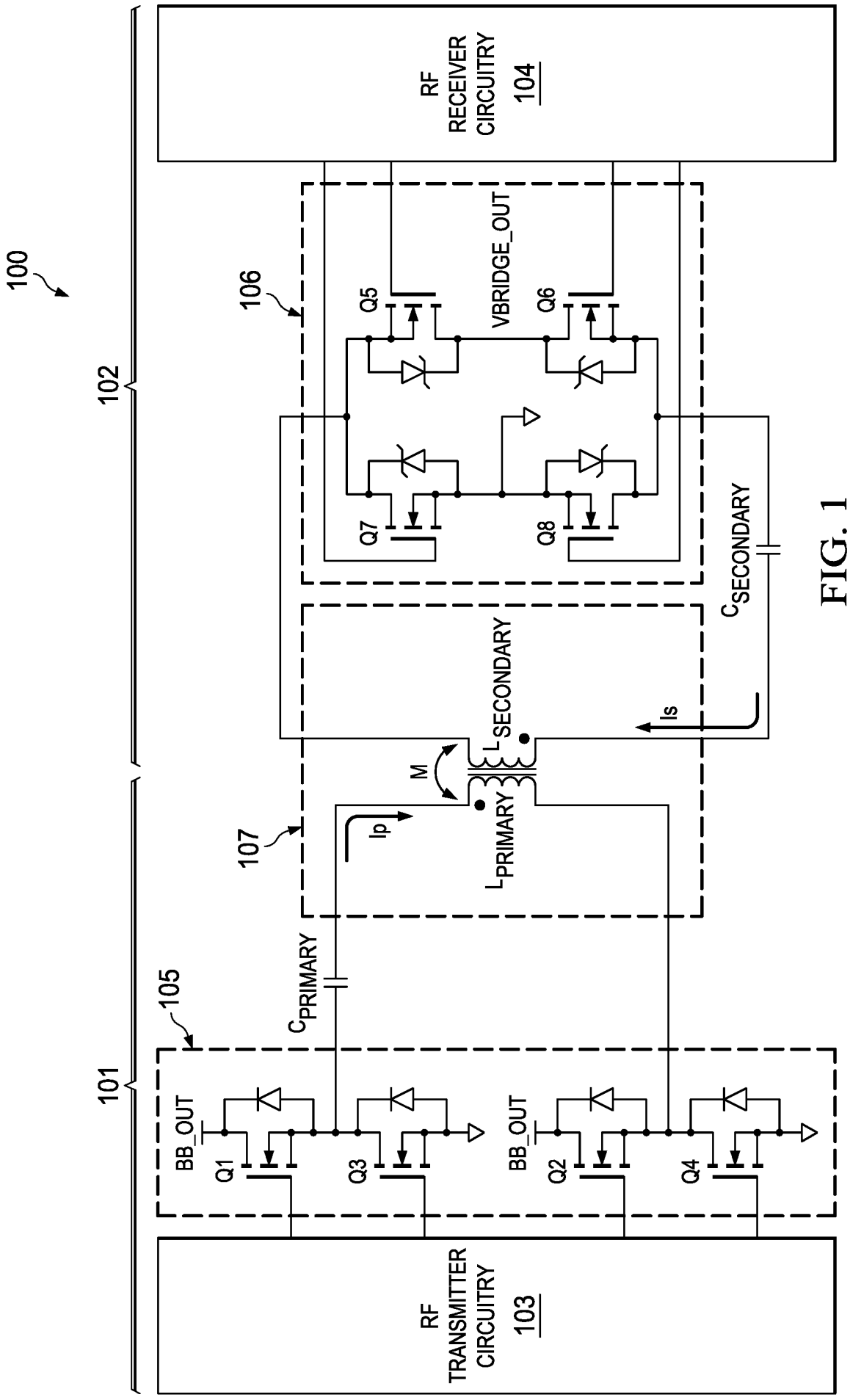
100
101
102
RF TRANSMITTER CIRCUITRY 103
RF RECEIVER CIRCUITRY 104
105
106
107
BB_OUT
Q1
Q3
BB_OUT
Q2
Q4
Q5
VBRIDGE_OUT
Q6
Q7
Q8
$C_{PRIMARY}$
$C_{SECONDARY}$
M
$L_{PRIMARY}$
$L_{SECONDARY}$
Ip
Is

FIG. 1

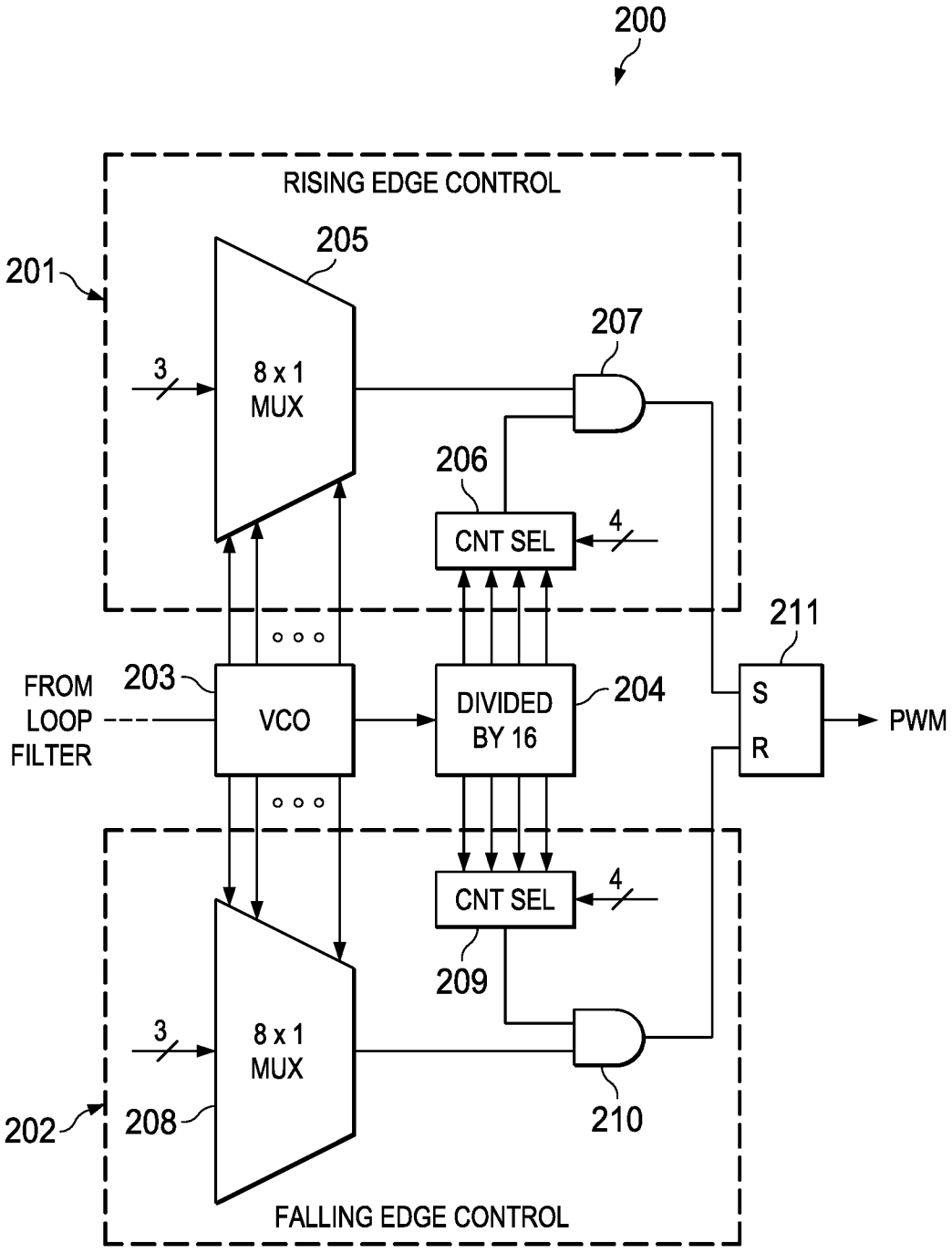
200
RISING EDGE CONTROL
205
201
207
3
8 x 1
MUX
206
CNT SEL
4
211
FROM
LOOP
FILTER
203
VCO
DIVIDED
BY 16
204
S
R
PWM
CNT SEL
4
209
3
8 x 1
MUX
202
208
210
FALLING EDGE CONTROL

FIG. 2

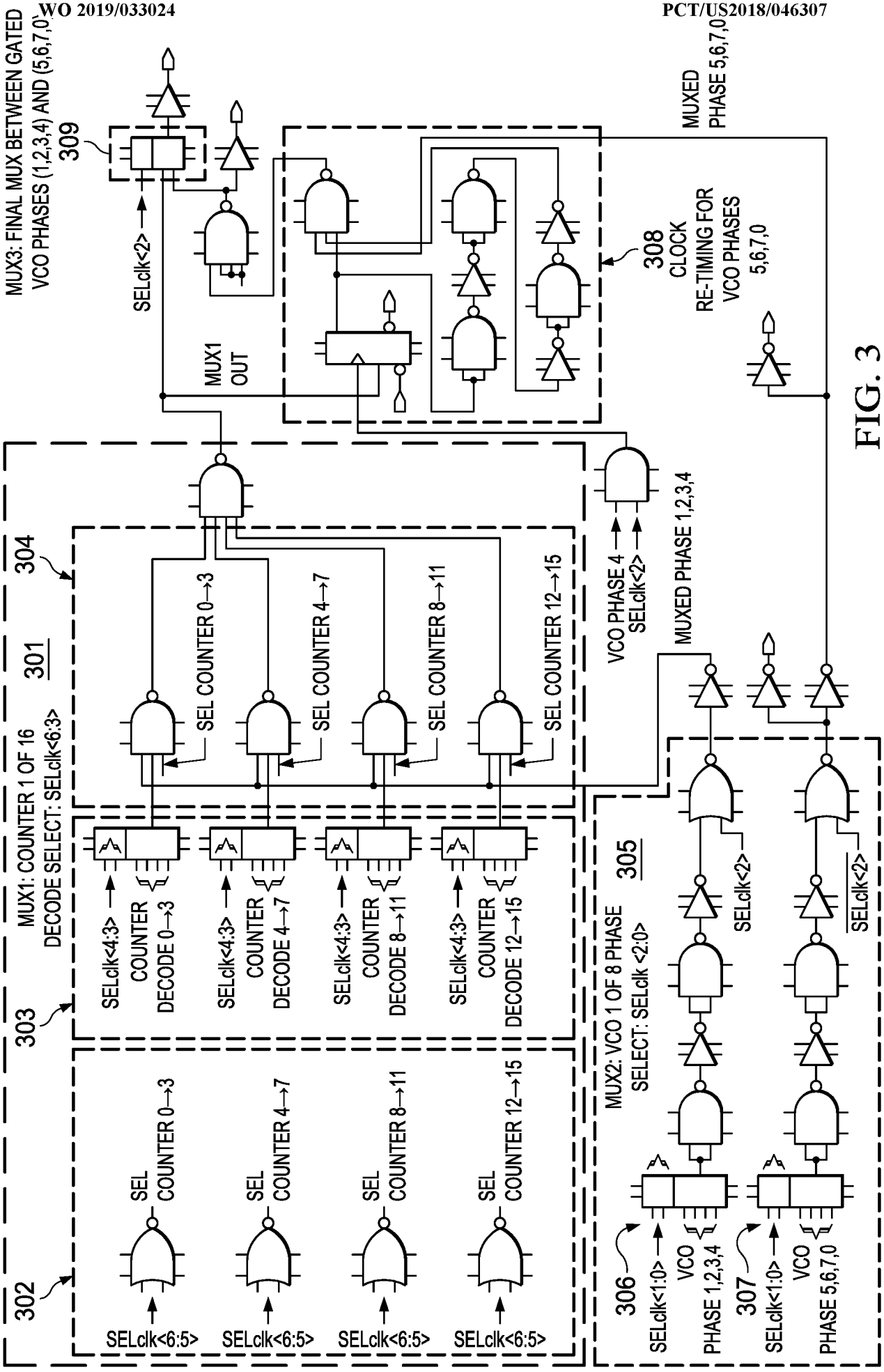
MUX3: FINAL MUX BETWEEN GATED VCO PHASES (1,2,3,4) AND (5,6,7,0)
309
SELclk<2>
MUX1 OUT
MUXED PHASE 5,6,7,0
308
CLOCK RE-TIMING FOR VCO PHASES 5,6,7,0
VCO PHASE 4
SELclk<2>
MUXED PHASE 1,2,3,4
304
MUX1: COUNTER 1 OF 16 DECODE SELECT: SELclk<6:3>
301
SEL COUNTER 0→3
SEL COUNTER 4→7
SEL COUNTER 8→11
SEL COUNTER 12→15
303
SELclk<4:3>
COUNTER DECODE 0→3
COUNTER DECODE 4→7
COUNTER DECODE 8→11
COUNTER DECODE 12→15
302
SEL COUNTER 0→3
SEL COUNTER 4→7
SEL COUNTER 8→11
SEL COUNTER 12→15
SELclk<6:5>
MUX2: VCO 1 OF 8 PHASE SELECT: SELclk <2:0>
305
SELclk<2>
306
307
SELclk<1:0>
VCO PHASE 1,2,3,4
VCO PHASE 5,6,7,0

FIG. 3

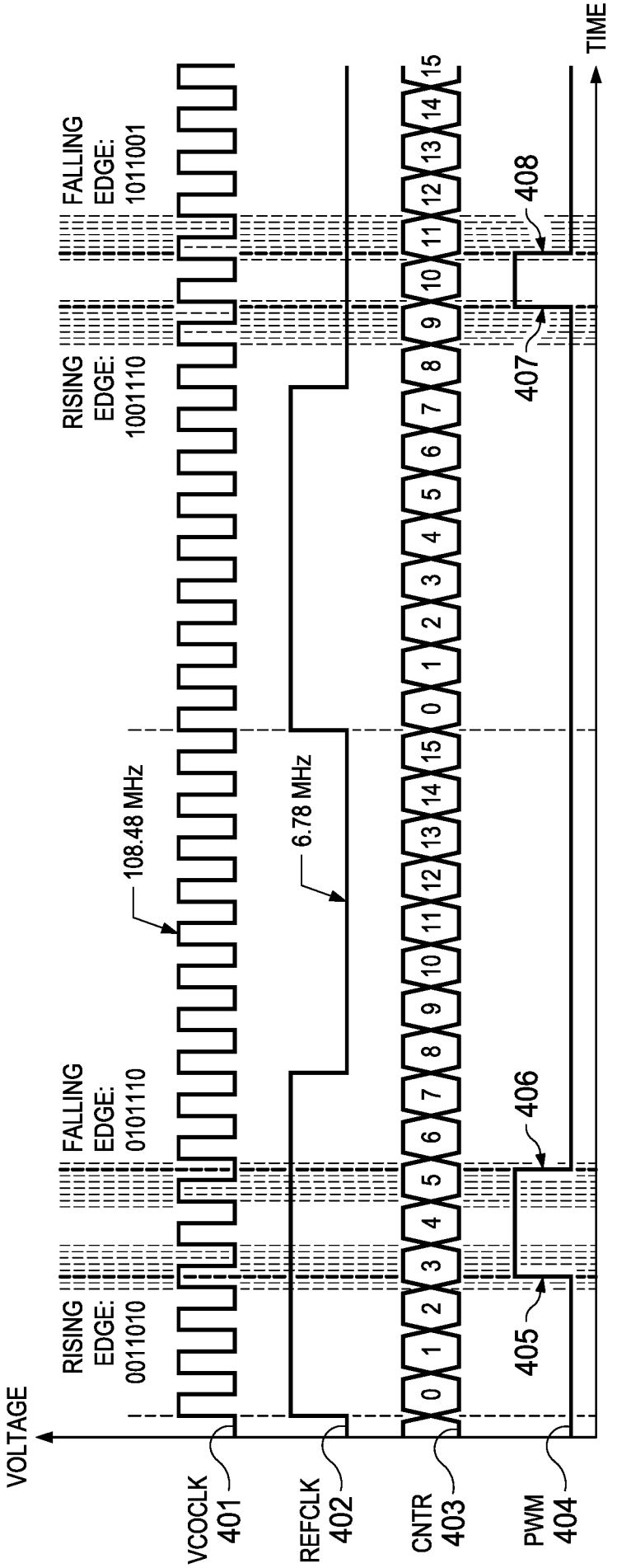
400
VOLTAGE
TIME
RISING EDGE: 0011010
FALLING EDGE: 0101110
RISING EDGE: 1001110
FALLING EDGE: 1011001
108.48 MHz
6.78 MHz
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
405
406
407
408
VCOCLK 401
REFCLK 402
CNTR 403
PWM 404

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2018/046307

A. CLASSIFICATION OF SUBJECT MATTER

H02J 50/10 *(2016.01)*
H02J 50/40 *(2016.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02J 50/10, 50/40

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DWPI, ESP@CENET, PatSearch, USPTO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5657211 A1 (NOKIA TECHNOLOGY GMBH), 12.08.1997, col. 3 lines 36-67, col. 4 lines 1-40, col. 12 lines 13-61, claim 1, fig. 2, 7(a), 10	1
A		2-12
A	WO 2017091312 A1 (QUALCOMM INCORPORATED) 01.06.2017, [0001], [0002], [0006], [0039], [0040], claim 1	13-18
X	EP 2873132 B1 (QUALCOMM INC) 26.06.2013, [0033], claim 1	20
A		19
A	EP 2454799 A2 (KONINKL PHILIPS ELECTRONICS NV (NL)), 23.05.2012	2-19

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 October 2018 (25.10.2018)	06 December 2018 (06.12.2018)

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