(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
31 August 2017 (31.08.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/146719 A1

(51) International Patent Classification:
H01L 21/304 (2006.01)

(21) International Application Number:
PCT/US2016/019721

(22) International Filing Date:
26 February 2016 (26.02.2016)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

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(54) Title: WAFER RETAINER RINGS FOR CHEMICAL MECHANICAL POLISHING

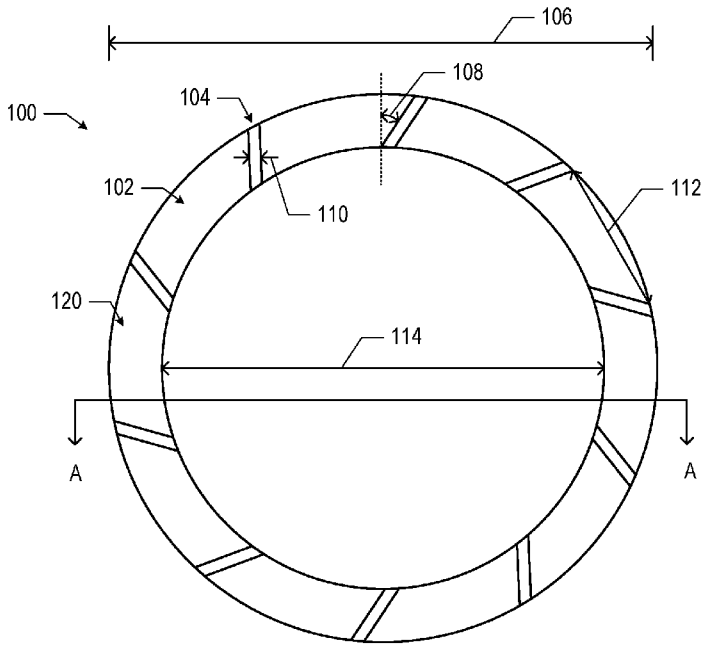

FIG. 1

(57) Abstract: Disclosed herein are wafer retainer rings for chemical mechanical polishing (CMP) systems. Various ones of the wafer retainer rings disclosed herein may meet one or more criteria for limiting the wear on the wafer retainer ring during polishing. For example, in some embodiments, a wafer retainer ring may include a top surface including a plurality of ridges separated by a corresponding plurality of grooves, wherein each of the plurality of ridges has a width; a bottom surface; an inner surface circumscribing an area having a diameter; and an outer surface; wherein a ratio of the diameter to the width is less than 3.8.

WO 2017/146719 A1

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

WAFER RETAINER RINGS FOR CHEMICAL MECHANICAL POLISHING

Technical Field

[0001] The present disclosure relates generally to chemical mechanical polishing (CMP), and more particularly, to wafer retainer rings.

Background

[0002] Chemical mechanical polishing (CMP) typically includes rotating and translating a polishing pad on a wafer to remove material from the wafer and achieve a flat wafer surface. For example, a wafer may be polished to remove an oxide layer prior to a lithography step. The wafer may be held in place on a mechanical arm by a retainer ring during polishing.

Brief Description of the Drawings

[0003] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0004] FIG. 1 is a top view of a wafer retainer ring for a chemical mechanical polishing (CMP) system, in accordance with various embodiments.

[0005] FIGS. 2A and 2B are cross-sectional views of different example embodiments of the wafer retainer ring of FIG. 1.

[0006] FIG. 3 is a side view of the wafer retainer ring of FIG. 2A, in accordance with various embodiments.

[0007] FIG. 4 is a side view of a CMP system including a wafer retainer ring as disclosed herein, in accordance with various embodiments.

[0008] FIG. 5 is a flow diagram of a method of manufacturing a wafer retainer ring, in accordance with various embodiments.

[0009] FIG. 6 is a flow diagram of a method of polishing a wafer, in accordance with various embodiments.

[0010] FIGS. 7A and 7B are top views of a wafer and dies that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein.

[0011] FIG. 8 is a cross-sectional side view of an integrated circuit (IC) device that may have components that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein.

[0012] FIG. 9 is a cross-sectional side view of an IC device assembly that may have components that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein.

[0013] FIG. 10 is a block diagram of an example computing device that may have components that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein.

Detailed Description

[0014] Disclosed herein are wafer retainer rings for chemical mechanical polishing (CMP) systems. Various ones of the wafer retainer rings disclosed herein may meet one or more criteria for limiting the wear on the wafer retainer ring during polishing. For example, a wafer retainer ring may include a top surface including a plurality of ridges separated by a corresponding plurality of grooves, wherein the ridges have a ridge width and the grooves have a groove width; a bottom surface; an inner surface circumscribing an area having a diameter; and an outer surface. In some embodiments, a ratio of the diameter to the ridge width is less than 3.8. In some embodiments, each of the plurality of ridges has a ridge width greater than or equal to 80 millimeters. In some embodiments, the top surface has a hydrophilicity less than or equal to 75 degrees of water contact angle. Other embodiments are also disclosed herein.

[0015] Conventional wafer retainer rings are often designed with grooves to allow slurry to flow across the wafer retainer ring and onto the surface of the wafer during polishing. These grooves have been conventionally designed to promote slurry access, and thus are often quite "wide" relative to the ridges between them. An unobserved and undesired consequence of such "narrow ridge" designs, however, is that, during polishing, the forces arising from the contact between the wafer retainer ring and the polishing pad are concentrated on the "narrow ridges," creating high pressure areas. The result of these high pressures is the rapid wearing away of the wafer retainer ring surface (quantified by, e.g., the rate of ring material removal during polishing) and the polishing pad. This excessive ring and pad wear increases the cost and manufacturing time associated with CMP, at least because of the fast depletion of the ring and pad "consumables" and the tool downtime required for changing out these consumables. In applications in which particularly soft and fragile polishing pads are to be used, this pad wear issue may substantially hinder the manufacturing process.

[0016] Various ones of the embodiments disclosed herein include wafer retainer rings that meet one or more wear-limiting criteria for extending the lifespan of the wafer retainer rings and/or the polishing pads in a CMP system, and improving CMP performance. Adequate slurry access can be achieved while mitigating the high pressures arising between the wafer retainer ring and the polishing pad in conventional CMP systems.

[0017] In the following detailed description, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, embodiments that may be

practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0018] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments.

[0019] For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C). The term "between," when used with reference to measurement ranges, is inclusive of the ends of the measurement ranges.

[0020] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. The disclosure may use perspective-based descriptions such as "above," "below," "top," "bottom," and "side"; such descriptions are used to facilitate the discussion and are not intended to restrict the application of disclosed embodiments. The accompanying drawings are not necessarily drawn to scale.

[0021] FIGS. 1-3 are various views of a wafer retainer ring 100, in accordance with various embodiments. In particular, FIG. 1 is a top view of the wafer retainer ring 100, FIGS. 2A and 2B are cross-sectional views of different embodiments taken along the section A-A of FIG. 1, and FIG. 3 is a side view of the embodiment of FIG. 2A. The wafer retainer ring 100 may include a top surface 120 having multiple ridges 102 separated by grooves 104. A bottom surface 128 may be opposite to the top surface 120. The wafer retainer ring 100 may also include an inner surface 118 and an outer surface 126. The wafer retainer ring 100 may have a substantially annular footprint, and the inner surface 118 may define a circular area having an inner diameter 114. In use, a wafer (e.g., the wafer 160 discussed below with reference to FIG. 4) may be retained in the area bounded by the inner surface 118, and the inner surface 118 may constrain the wafer's horizontal motion. The inner diameter 114 may be close to the diameter of the wafer to be retained by the wafer retainer ring 100 (e.g., less than 1 millimeter greater than the diameter of the wafer), and the diameter of the wafer may take any suitable value (e.g., 200, 300, 400, or 450 millimeters). The outer surface 126

may also have a circular footprint, with an outer diameter 106. The outer diameter 106 may be selected based on the particular CMP system with which the wafer retainer ring 100 will be used (e.g., the CMP system 150 discussed below with reference to FIG. 4) and any desired mechanical properties of the wafer retainer ring 100. For example, in some embodiments in which the inner diameter 114 is approximately 300 millimeters, the outer diameter 106 may be between 340 and 370 millimeters (e.g., between 350 and 360 millimeters). As shown, in some embodiments, the grooves 104 may extend from the inner surface 118 to the outer surface 126, and may allow slurry to move between the inner surface 118 and the outer surface 126.

[0022] The ridges 102 may have a ridge width 112. FIG. 1 depicts an embodiment in which the ridge width 112 is the same for all of the ridges 102, but in some embodiments, different ones of the ridges 102 may have different ridge widths 112. The ridge width 112 illustrated in FIG. 1 is measured along the chord between (1) the intersection of a groove 104 and the outer surface 126 and (2) the intersection of an adjacent groove 104 and the outer surface 126. The grooves 104 may have a groove width 110. FIG. 1 depicts an embodiment in which the sidewalls of the grooves 104 are parallel (and the groove width 110 is measured as the distance between the parallel sidewalls), but in some embodiments, the sidewalls of the grooves 104 may not be parallel. In such embodiments, the groove width 110 may be measured as the average distance between opposing sidewalls of the groove 104, the minimum distance between opposing sidewalls of the groove 104, or the maximum distance between opposing sidewalls of the groove 104. FIG. 1 also depicts an embodiment in which the groove width 110 is the same for all of the grooves 104, but in some embodiments, different ones of the grooves 104 may have different groove widths 110.

[0023] In some embodiments, the grooves 104 may be oriented at an angle relative to a radial direction of the wafer retainer ring 100. For example, FIG. 1 illustrates the grooves 104 oriented at an angle 108 relative to the radial direction of the wafer retainer ring 100. The orientation angle 108 of the grooves 104 may depend on the direction in which the wafer retainer ring 100 is to rotate during CMP, properties of the slurry that will be used during polishing, or other suitable process parameters, as known in the art. In some embodiments, the orientation angle 108 of the grooves 104 may be approximately 45 degrees.

[0024] The grooves 104 may have a depth 116. FIGS. 2A, 2B, and 3 depict embodiments in which the depth 116 is the same for all of the grooves 104, but in some embodiments, different ones of the grooves 104 may have different depths 116. In the embodiment of FIGS. 2A and 2B, the depth 116 may alternately be characterized as the "height" of the ridges 102. The depth 116 of the grooves 104 may be selected based on the volume of desired slurry flow during polishing, or other suitable

process parameters, as known in the art. In some embodiments, the depth 116 may be between 2 and 4 millimeters (e.g., between 2 and 3 millimeters, or between 2 and 2.5 millimeters).

[0025] FIG. 2A depicts an embodiment in which the grooves 104 all have a substantially rectangular profile; the sidewalls of the grooves 104 are substantially perpendicular to the bottoms of the grooves 104 and to the top surface 120, and the sidewalls of the grooves 104 are substantially flat. In some embodiments, the sidewalls of the grooves 104 may not be flat, but may have some curvature. In some embodiments, the sidewalls of the grooves 104 may not be substantially perpendicular to the bottoms of the grooves 104 and to the top surface 120, but may be angled with respect to the bottoms of the grooves 104 and the top surface 120. For example, the grooves 104 may be tapered so as to be narrower towards the bottoms of the grooves 104 and wider towards the top surface 120.

[0026] FIG. 2B depicts an embodiment in which the grooves 104 all have a curved profile; the sidewalls of the grooves 104 curve into the bottoms of the grooves 104 and curve into the top surface 120. The radius of curvature may be different at the top surface 120 and at the bottoms of the grooves 104. In some embodiments, the grooves 104 may exhibit curvature at the top surface 120, and the sidewalls may meet the bottoms of the grooves 104 at a sharper angle (e.g., perpendicularly, or at another angle). Relative to embodiments in which the grooves 104 terminate perpendicularly to the top surface 120 (forming "sharp" corners at which force may concentrate), embodiments in which the sidewalls of the grooves 104 curve into the top surface 120 may result less wear to the wafer retainer ring 100 (and to the CMP polishing pad, as discussed below with reference to FIG. 4) during use. Additionally, wafer retainer rings 100 with sharp corners at the top surface 120 may experience increased wear at those sharp corners, resulting in an eventual rounding off of the corners and therefore a change in performance over time (e.g., as the pressure between the wafer retainer ring 100 and the CMP polishing pad increases due to reduced contact area). Embodiments of the wafer retainer rings 100 having a curved profile of the grooves 104 where the grooves 104 meet the top surface 120 may experience less "rounding off," and thus may help achieve a more consistent CMP process.

[0027] The wafer retainer ring 100 may meet one or more wear-limiting criteria, as disclosed herein. These wear-limiting criteria may represent properties of the wafer retainer ring 100 that may decrease the wear on the wafer retainer ring 100 during use, and thus increase the lifespan of the wafer retainer ring 100. By satisfying one or more of the wear-limiting criteria disclosed herein, the wafer retainer ring 100 may also improve the lifespan of the CMP polishing pad used to polish the wafer retained by the wafer retainer ring 100 (e.g., the CMP polishing pad 158 discussed below

with reference to FIG. 4) by reducing the volume of ground ring particles contaminating the surface of the CMP polishing pad.

[0028] One wear-limiting criterion may relate to the ratio of the inner diameter 114 and the ridge width 112. In some embodiments, one wear-limiting criterion may specify that the ratio of the inner diameter 114 to the ridge width 112 is less than or equal to 3.8. In some embodiments, one wear-limiting criterion may specify that the ratio of the inner diameter 114 to the ridge width 112 is less than or equal to 3.5. In some embodiments, one wear-limiting criterion may specify that the ratio of the inner diameter 114 to the ridge width 112 is less than or equal to 3.2. In some embodiments, one wear-limiting criterion may specify that the ratio of the inner diameter 114 to the ridge width 112 is less than or equal to 3. In some embodiments, one wear-limiting criterion may specify that the ratio of the inner diameter 114 to the ridge width 112 is less than or equal to 2.8.

[0029] Another wear-limiting criterion may relate to the magnitude of the ridge width 112. In some embodiments, one wear-limiting criterion may specify that the ridge width 112 is greater than or equal to 80 millimeters. In some embodiments, one wear-limiting criterion may specify that the ridge width 112 is greater than or equal to 90 millimeters. In some embodiments, one wear-limiting criterion may specify that the ridge width 112 is greater than or equal to 100 millimeters. In some embodiments, one wear-limiting criterion may specify that the ridge width 112 is greater than or equal to 110 millimeters.

[0030] Another wear-limiting criterion may relate to the hydrophilicity of the top surface 120 of the wafer retainer ring 100. In a CMP system (e.g., the CMP system 150, discussed below with reference to FIG. 4), polishing may occur via contact between the wafer retainer ring 100, a wafer disposed therein, and a CMP polishing pad, with slurry provided to the interface between these components. If the wafer retainer ring 100 is formed of a highly hydrophobic material, the slurry may not form a thin liquid film along the interface between the slurry and the wafer retainer ring 100. The consequence may be that polishing occurs under substantially "dry" conditions, increasing the friction between the wafer retainer ring 100 and the CMP polishing pad, and increasing the wear on the wafer retainer ring 100 and the CMP polishing pad. Conversely, if the wafer retainer ring 100 is formed of an adequately hydrophilic material, the slurry may effectively lubricate the polishing process, extending the lifespan of the wafer retainer ring 100 and the CMP polishing pad. The hydrophilicity of the wafer retainer ring 100 may be quantified by its water contact angle. FIG. 3 illustrates a water droplet 122 disposed on the top surface 120 having a water contact angle 124 with the top surface 120. As used herein, a "water contact angle" is the angle at which water meets a surface, thereby quantifying the wettability of the surface. As known in the art, the less the water contact angle, the greater the hydrophilicity of the top surface 120 (and conversely, the less the

hydrophobicity of the top surface 120). In some embodiments, one wear-limiting criterion may specify that the top surface 120 has a hydrophilic water contact angle less than or equal to 75 degrees. In some embodiments, one wear-limiting criterion may specify that the top surface 120 has a hydrophilic water contact angle less than or equal to 70 degrees. In some embodiments, one wear-limiting criterion may specify that the top surface 120 has a hydrophilic water contact angle less than or equal to 65 degrees.

[0031] In some embodiments, the top surface 120 of the wafer retainer ring 100 may satisfy a wear-limiting criterion for hydrophilicity while the bulk of the wafer retainer ring 100 does not. In some embodiments, the entirety of the wafer retainer ring 100 may satisfy a wear-limiting criterion for hydrophilicity. A desired hydrophilicity in the wafer retainer ring 100 may be achieved using techniques known in the art, such as chemical oxidizing, forming the wafer retainer ring 100 with hydrophilic monomers, plasma treatment, and ultraviolet (UV) treatment, among others. Any suitable material or materials may be used for the wafer retainer ring 100, such as hydrocarbon polymers (e.g., aliphatic and/or aromatic), such as hydrocarbon plastic polymers (e.g., polyethylene).

[0032] These wear-limiting criterion may be combined in any desired combination to specify the properties of a wafer retainer ring 100 in accordance with the present disclosure. Moreover, the wear-limiting criteria satisfied by a wafer retainer ring 100 may include secondary criteria in addition to one or more of the criteria discussed above. For example, a secondary criterion may specify that the total number of grooves 104 in the wafer retainer ring 100 is less than 12.

[0033] FIG. 4 is a side view of a CMP system 150 including a wafer retainer ring 100, in accordance with various embodiments. The CMP system 150 may include a CMP conditioning disk 164 disposed on a first arm 152. The CMP conditioning disk 164 of the CMP system 150 may take the form of any of the CMP conditioning disks disclosed herein. The CMP conditioning disk 164 may be secured to the first arm 152 using any suitable mechanism, such as vacuum, a clamp, a frame, or mechanical fasteners, for example. The first arm 152 may include mechanical linkages to allow the CMP conditioning disk 164 to translate "up and down" to bring the CMP conditioning disk 164 into contact with the CMP polishing pad 158 (discussed below). In some embodiments, the first arm 152 may include mechanical linkages to allow the CMP conditioning disk 164 to translate "side to side" while in contact with the CMP polishing pad 158. In some embodiments, the first arm 152 may include a rotor to allow the CMP conditioning disk 164 to rotate while in contact with the CMP polishing pad 158. The first arm 152 may include, for example, a head, as known in the art. In various embodiments, the CMP system 150 may include control circuitry (not shown) to allow a user to control the rotation rate of the CMP conditioning disk 164, the downward force exerted by the

CMP conditioning disk 164 on the CMP polishing pad 158, the "side to side" translation of the CMP conditioning disk 164, and/or other operational properties of the CMP system 150.

[0034] The CMP system 150 may include a CMP polishing pad 158 disposed on a second arm 154. The CMP polishing pad 158 may be formed from a porous material, such as a hard elastomer or a polyurethane-based material. The CMP polishing pad 158 may include other additives to achieve a desired porosity, as known in the art. Different CMP polishing pads 158 may have different mechanical properties, such as hardness (e.g., with "soft" pads having a hardness between 10 and 20 MPa, and "hard" pads having a hardness between 200 and 1500 MPa). The CMP polishing pad 158 may be secured to the second arm 154 using any suitable mechanism, such as vacuum, a clamp, a frame, or mechanical fasteners, for example. The second arm 154 may include mechanical linkages to allow the CMP polishing pad 158 to translate "up and down" to bring the CMP polishing pad 158 into contact with the CMP conditioning disk 164 and/or the wafer 160 (discussed below). In some embodiments, the second arm 154 may include mechanical linkages to allow the CMP polishing pad 158 to translate "side to side" while in contact with the CMP conditioning disk 164 and/or the wafer 160. In some embodiments, the second arm 154 may include a rotor to allow the CMP polishing pad 158 to rotate while in contact with the CMP conditioning disk 164 and/or the wafer 160. The second arm 154 may be, for example, a platen, as known in the art. In various embodiments, the CMP system 150 may include control circuitry (not shown) to allow a user to control the rotation rate of the CMP polishing pad 158, the "side to side" translation of the CMP polishing pad 158, and/or other operational properties of the CMP system 150, as noted above. The amount of conditioning performed by the CMP conditioning disk 164 on the CMP polishing pad 158 may be quantified by the pad cut rate (PCR), the amount of material removed from the CMP polishing pad 158 by the CMP conditioning disk 164 (normalized by time of conditioning).

[0035] The CMP system 150 may include a wafer 160 disposed in a wafer retainer ring 100 on a third arm 156. The wafer retainer ring 100 may take the form of any of the embodiments disclosed herein, and the wafer 160 may have any suitable dimensions (e.g., 200, 300, or 450 millimeters in diameter). The wafer 160 and the wafer retainer ring 100 may be secured to the third arm 156 using any suitable mechanism, such as vacuum, a clamp, a frame, or mechanical fasteners, for example. In particular, the bottom surface 128 of the wafer retainer ring 100 may face the third arm 156, and the top surface 120 may face the CMP polishing pad 158. As discussed above, the wafer retainer ring 100 may help control the "side to side" movement of the wafer 160 during polishing, and vacuum force may be used to hold the wafer 160 against the third arm 156 to control the "up and down" movement of the wafer 160. The third arm 156 may include mechanical linkages to allow the wafer 160 to translate "up and down" to bring the wafer 160 into contact with the CMP polishing

pad 158. In some embodiments, the third arm 156 may include mechanical linkages to allow the wafer 160 to translate "side to side" while in contact with the CMP polishing pad 158. In some embodiments, the third arm 156 may include a rotor to allow the wafer 160 to rotate while in contact with the CMP polishing pad 158. In various embodiments, the CMP system 150 may include control circuitry (not shown) to allow a user to control the rotation rate of the wafer 160, the "side to side" translation of the wafer 160, the downward force exerted by the third arm 156 on the CMP conditioning pad 158, and/or other operational properties of the CMP system 150, as noted above.

[0036] When the CMP conditioning disk 164 is brought into contact with the CMP polishing pad 158, and the two are moved (e.g., rotated and/or translated) relative to one another, the surface of the CMP conditioning disk 164 may "dig" into the surface of the CMP polishing pad 158 and create grooves in the CMP polishing pad 158.

[0037] When the wafer 160 is brought into contact with the CMP polishing pad 158, and the two are moved (e.g., rotated and/or translated) relative to one another, the CMP polishing pad 158 may remove material from the wafer 160 and thereby polish the wafer 160. A slurry 162 may be disposed on the CMP polishing pad 158. When the wafer 160 is brought into contact with the CMP polishing pad 158, and the two are moved (e.g., rotated and/or translated) relative to one another, the slurry 162 may flow between the CMP polishing pad 158 and the wafer 160 to facilitate the polishing of the wafer 160. In particular, the grooves 104 in the wafer retainer ring 100 may allow the slurry 162 to flow to the wafer 160 and away from the wafer 160 during polishing. The slurry 162 may also flow through grooves in the CMP polishing pad 158 formed by the CMP conditioning disk 164. The slurry 162 may take any suitable form known in the art (e.g., an oxide slurry, a metal slurry, or a low-k slurry). Control circuitry (not shown) included in the CMP system 150 may control the rate of flow of the slurry 162 from a slurry source (not shown) in some embodiments.

[0038] In some embodiments, the CMP conditioning disk 164 may be used to condition the CMP polishing pad 158 simultaneously with the CMP polishing pad 158 polishing the wafer 160. That is, the CMP conditioning disk 164 may be in contact with (and rotated relative to) the CMP polishing pad 158 at the same time that the wafer 160 may be in contact with (and rotated relative to) the CMP polishing pad 158. In other embodiments, the CMP polishing pad 158 may be conditioned by the CMP conditioning disk 164 before and/or after (but not simultaneously with) polishing the wafer 160 using the CMP polishing pad 158.

[0039] During polishing, excessive friction between the wafer retainer ring 100 and the CMP polishing pad 158 may cause a temperature rise at the wafer retainer ring 100, the CMP polishing pad 158, and/or the wafer 160. In some embodiments, control circuitry (not shown) of the CMP system 150 may monitor the temperature of one or more of these components (using one or more

temperature sensors) and may slow or stop polishing when the temperature indicates that excessive friction may be occurring (e.g., raising a risk of damage to the CMP system 150, such as a broken timing belt). For example, in some applications, a temperature in the 40-50 degree Celsius range may signal nominal operation, while a higher temperature (e.g., in the 70-90 degree Celsius range) may signal faulty operation and may trigger the control circuitry to slow or cease polishing (or to adjust a process parameter, such as rate of slurry delivery, for example). More generally, temperature information may be used to control any operational parameter or regime, as suitable. As used herein, the term "circuitry" may refer to an application-specific integrated circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group) and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable hardware that provide the described functionality.

[0040] FIG. 5 is a flow diagram of a method 500 of manufacturing a wafer retainer ring, in accordance with various embodiments. Although various operations are arranged in a particular order and illustrated once each, various ones of the operations may be repeated or performed in any suitable order.

[0041] At 502, an annular body may be formed from a polymer material. The polymer material may be a hydrocarbon polymer, such as a hydrocarbon plastic polymer. For example, the polymer material may be polyethylene. The annular body may have an inner diameter in accordance with any of the embodiments of the inner diameter 114 disclosed herein, and an outer diameter in accordance with any of the embodiments of the outer diameter 106 disclosed herein. The annular body may be formed by machining a block of polymer material, three-dimensional printing, gluing or otherwise fastening multiple portions of polymer material together, or any other suitable manufacturing technique.

[0042] At 504, a plurality of ridges may be formed in the annular body to form a wafer retainer ring meeting one or more of the wear-limiting criteria disclosed herein. For example, a plurality of ridges 102 may be formed in the annular body to form a wafer retainer ring 100 in accordance with any of the embodiments disclosed herein. In some embodiments, the plurality of ridges may be formed at 504 by creating grooves in the annular body of 502 (e.g., by laser cutting, milling, or other machining). In some embodiments, the plurality of ridges may be formed at 504 by securing a ridged ring on top of the annular body (e.g., with glue) to form the wafer retainer ring. In some embodiments, the operations of 502 and 504 may be performed concurrently (e.g., when forming the wafer retainer ring by three-dimensional printing).

[0043] FIG. 6 is a flow diagram of a method 600 of polishing a wafer, in accordance with various embodiments. Although various operations are arranged in a particular order and illustrated once each, various ones of the operations may be repeated or performed in any suitable order.

[0044] At 602, a wafer may be retained in a wafer retainer ring meeting one or more of the wear-limiting criteria disclosed herein. For example, a wafer 160 may be retained in a wafer retainer ring 100 in the CMP system 150 in accordance with any of the embodiments disclosed herein. The wafer retainer ring and the wafer of 602 may be secured to a mechanical arm (e.g., the third arm 156 of the CMP system 150 of FIG. 4).

[0045] At 604, after retaining the wafer in the wafer retainer ring, the wafer and a CMP polishing pad may be moved relative to one another while in contact to polish the wafer. For example, the wafer 160 and the wafer retainer ring 100 may be moved (e.g., rotated and/or translated) relative to the CMP polishing pad 158 in the CMP system 150 to polish the wafer 160. In some embodiments, a slurry may be provided (e.g., the slurry 162) on the surface of the CMP polishing pad, and the slurry may be transported across the wafer retainer ring and under the wafer during polishing.

[0046] Devices processed using the CMP systems and techniques disclosed herein (e.g., devices in a wafer retained in any of the wafer retainer rings disclosed herein during CMP) may be included in any suitable electronic device. FIGS. 7-10 illustrate various examples of apparatuses that may include devices processed using the CMP systems and techniques disclosed herein.

[0047] FIGS. 7A-B are top views of a wafer 700 and dies 702 that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein. In particular, the wafer 700 may be the wafer 160 polished in the wafer retainer ring 100 of the CMP system 150 of FIG. 4. The wafer 700 may be composed of semiconductor material and may include one or more dies 702 having IC structures formed on a surface of the wafer 700. Each of the dies 702 may be a repeating unit of a semiconductor product that includes any suitable IC. After the fabrication of the semiconductor product is complete (e.g., after the semiconductor product is polished in accordance with any of the techniques disclosed herein), the wafer 700 may undergo a singulation process in which each of the dies 702 is separated from one another to provide discrete "chips" of the semiconductor product. In particular, devices processed using the CMP systems and techniques disclosed herein may take the form of the wafer 700 (e.g., not singulated) or the form of the die 702 (e.g., singulated). The die 702 may include one or more transistors (e.g., some of the transistors 840 of FIG. 8, discussed below) and/or supporting circuitry to route electrical signals to the transistors, as well as any other IC components. In some embodiments, the wafer 700 or the die 702 may include a memory device (e.g., a static random access memory (SRAM) device), a logic device (e.g., an AND, OR, NAND, or NOR gate), or any other suitable circuit element. Multiple ones of these devices may

be combined on a single die 702. For example, a memory array formed by multiple memory devices may be formed on a same die 702 as a processing device (e.g., the processing device 1002 of FIG. 10) or other logic that is configured to store information in the memory devices or execute instructions stored in the memory array.

[0048] FIG. 8 is a cross-sectional side view of an IC device 800 that may be processed using CMP systems and techniques in accordance with any of the embodiments disclosed herein. The IC device 800 may be formed on a substrate 802 (e.g., the wafer 700 of FIG. 7A) and may be included in a die (e.g., the die 702 of FIG. 7B). The substrate 802 may be a semiconductor substrate composed of semiconductor material systems including, for example, N-type or P-type materials systems. The substrate 802 may include, for example, a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In some embodiments, the semiconductor substrate 802 may be formed using alternative materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Further materials classified as group II-VI, III-V, or IV may also be used to form the substrate 802. Although a few examples of materials from which the substrate 802 may be formed are described here, any material that may serve as a foundation for an IC device 800 may be used. The substrate 802 may be part of a singulated die (e.g., the dies 702 of FIG. 7B) or a wafer (e.g., the wafer 700 of FIG. 7A).

[0049] The IC device 800 may include one or more device layers 804 disposed on the substrate 802. The device layer 804 may include features of one or more transistors 840 (e.g., metal oxide semiconductor field-effect transistors (MOSFETs)) formed on the substrate 802. The device layer 804 may include, for example, one or more source and/or drain (S/D) regions 820, a gate 822 to control current flow in the transistors 840 between the S/D regions 820, and one or more S/D contacts 824 to route electrical signals to/from the S/D regions 820. The transistors 840 may include additional features not depicted for the sake of clarity, such as device isolation regions, gate contacts, and the like. The transistors 840 are not limited to the type and configuration depicted in FIG. 8 and may include a wide variety of other types and configurations such as, for example, planar transistors, non-planar transistors, or a combination of both. Non-planar transistors may include FinFET transistors, such as double-gate transistors or tri-gate transistors, and wrap-around or all-around gate transistors, such as nanoribbon and nanowire transistors.

[0050] Each transistor 840 may include a gate 822 formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide, and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium,

tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[0051] The gate electrode layer may be formed on the gate dielectric layer and may include at least one P-type work function metal or N-type work function metal, depending on whether the transistor 840 is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are work function metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer. For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides (e.g., ruthenium oxide). For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals (e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide).

[0052] In some embodiments, when viewed as a cross-section of the transistor 840 along the source-channel-drain direction, the gate electrode may consist of a U-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In other embodiments, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In other embodiments, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0053] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack to bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In some embodiments, a plurality of spacer pairs may be used; for

instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0054] The S/D regions 820 may be formed within the substrate 802 adjacent to the gate 822 of each transistor 840. The S/D regions 820 may be formed using either an implantation/diffusion process or an etching/deposition process, for example. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate 802 to form the S/D regions 820. An annealing process that activates the dopants and causes them to diffuse farther into the substrate 802 may follow the ion implantation process. In the latter process, the substrate 802 may first be etched to form recesses at the locations of the S/D regions 820. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the S/D regions 820. In some implementations, the S/D regions 820 may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some embodiments, the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In some embodiments, the S/D regions 820 may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. In further embodiments, one or more layers of metal and/or metal alloys may be used to form the S/D regions 820.

[0055] Electrical signals, such as power and/or input/output (I/O) signals, may be routed to and/or from the transistors 840 of the device layer 804 through one or more interconnect layers disposed on the device layer 804 (illustrated in FIG. 8 as interconnect layers 806-810). For example, electrically conductive features of the device layer 804 (e.g., the gate 822 and the S/D contacts 824) may be electrically coupled with the interconnect structures 828 of the interconnect layers 806-810. The one or more interconnect layers 806-810 may form an interlayer dielectric (ILD) stack 819 of the IC device 800.

[0056] The interconnect structures 828 may be arranged within the interconnect layers 806-810 to route electrical signals according to a wide variety of designs (in particular, the arrangement is not limited to the particular configuration of interconnect structures 828 depicted in FIG. 8). Although a particular number of interconnect layers 806-810 is depicted in FIG. 8, embodiments of the present disclosure include IC devices having more or fewer interconnect layers than depicted.

[0057] In some embodiments, the interconnect structures 828 may include trench structures 828a (sometimes referred to as "lines") and/or via structures 828b (sometimes referred to as "holes") filled with an electrically conductive material such as a metal. The trench structures 828a may be arranged to route electrical signals in a direction of a plane that is substantially parallel with a surface of the substrate 802 upon which the device layer 804 is formed. For example, the trench

structures 828a may route electrical signals in a direction in and out of the page from the perspective of FIG. 8. The via structures 828b may be arranged to route electrical signals in a direction of a plane that is substantially perpendicular to the surface of the substrate 802 upon which the device layer 804 is formed. In some embodiments, the via structures 828b may electrically couple trench structures 828a of different interconnect layers 806-810 together.

[0058] The interconnect layers 806-810 may include a dielectric material 826 disposed between the interconnect structures 828, as shown in FIG. 8. In some embodiments, the dielectric material 826 disposed between the interconnect structures 828 in different ones of the interconnect layers 806-810 may have different compositions; in other embodiments, the composition of the dielectric material 826 between different interconnect layers 806-810 may be the same.

[0059] A first interconnect layer 806 (referred to as Metal 1 or "M1") may be formed directly on the device layer 804. In some embodiments, the first interconnect layer 806 may include trench structures 828a and/or via structures 828b, as shown. The trench structures 828a of the first interconnect layer 806 may be coupled with contacts (e.g., the S/D contacts 824) of the device layer 804.

[0060] A second interconnect layer 808 (referred to as Metal 2 or "M2") may be formed directly on the first interconnect layer 806. In some embodiments, the second interconnect layer 808 may include via structures 828b to couple the trench structures 828a of the second interconnect layer 808 with the trench structures 828a of the first interconnect layer 806. Although the trench structures 828a and the via structures 828b are structurally delineated with a line within each interconnect layer (e.g., within the second interconnect layer 808) for the sake of clarity, the trench structures 828a and the via structures 828b may be structurally and/or materially contiguous (e.g., simultaneously filled during a dual-damascene process) in some embodiments.

[0061] A third interconnect layer 810 (referred to as Metal 3 or "M3") (and additional interconnect layers, as desired) may be formed in succession on the second interconnect layer 808 according to similar techniques and configurations described in connection with the second interconnect layer 808 or the first interconnect layer 806.

[0062] The IC device 800 may include a solder resist material 834 (e.g., polyimide or similar material) and one or more bond pads 836 formed on the interconnect layers 806-810. The bond pads 836 may be electrically coupled with the interconnect structures 828 and configured to route the electrical signals of the transistor(s) 840 to other external devices. For example, solder bonds may be formed on the one or more bond pads 836 to mechanically and/or electrically couple a chip including the IC device 800 with another component (e.g., a circuit board). The IC device 800 may have other alternative configurations to route the electrical signals from the interconnect layers 806-

810 than depicted in other embodiments. For example, the bond pads 836 may be replaced by or may further include other analogous features (e.g., posts) that route the electrical signals to external components.

[0063] FIG. 9 is a cross-sectional side view of an IC device assembly 900 that may include components processed using any of the CMP systems and techniques disclosed herein. The IC device assembly 900 includes a number of components disposed on a circuit board 902 (which may be, e.g., a motherboard). The IC device assembly 900 includes components disposed on a first face 940 of the circuit board 902 and an opposing second face 942 of the circuit board 902; generally, components may be disposed on one or both faces 940 and 942.

[0064] In some embodiments, the circuit board 902 may be a printed circuit board (PCB) including multiple metal layers separated from one another by layers of dielectric material and interconnected by electrically conductive vias. Any one or more of the metal layers may be formed in a desired circuit pattern to route electrical signals (optionally in conjunction with other metal layers) between the components coupled to the circuit board 902. In other embodiments, the circuit board 902 may be a non-PCB substrate.

[0065] The IC device assembly 900 illustrated in FIG. 9 includes a package-on-interposer structure 936 coupled to the first face 940 of the circuit board 902 by coupling components 916. The coupling components 916 may electrically and mechanically couple the package-on-interposer structure 936 to the circuit board 902, and may include solder balls (as shown in FIG. 9), male and female portions of a socket, an adhesive, an underfill material, and/or any other suitable electrical and/or mechanical coupling structure.

[0066] The package-on-interposer structure 936 may include an IC package 920 coupled to an interposer 904 by coupling components 918. The coupling components 918 may take any suitable form for the application, such as the forms discussed above with reference to the coupling components 916. Although a single IC package 920 is shown in FIG. 9, multiple IC packages may be coupled to the interposer 904; indeed, additional interposers may be coupled to the interposer 904. The interposer 904 may provide an intervening substrate used to bridge the circuit board 902 and the IC package 920. The IC package 920 may be or include, for example, a die (the die 702 of FIG. 7B), an IC device (e.g., the IC device 800 of FIG. 8), or any other suitable component. Generally, the interposer 904 may spread a connection to a wider pitch or reroute a connection to a different connection. For example, the interposer 904 may couple the IC package 920 (e.g., a die) to a ball grid array (BGA) of the coupling components 916 for coupling to the circuit board 902. In the embodiment illustrated in FIG. 9, the IC package 920 and the circuit board 902 are attached to opposing sides of the interposer 904; in other embodiments, the IC package 920 and the circuit

board 902 may be attached to a same side of the interposer 904. In some embodiments, three or more components may be interconnected by way of the interposer 904.

[0067] The interposer 904 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In some implementations, the interposer 904 may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials. The interposer 904 may include metal interconnects 908 and vias 910, including but not limited to through-silicon vias (TSVs) 906. The interposer 904 may further include embedded devices 914, including both passive and active devices. Such devices may include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, electrostatic discharge (ESD) devices, and memory devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and microelectromechanical systems (MEMS) devices may also be formed on the interposer 904. The package-on-interposer structure 936 may take the form of any of the package-on-interposer structures known in the art.

[0068] The IC device assembly 900 may include an IC package 924 coupled to the first face 940 of the circuit board 902 by coupling components 922. The coupling components 922 may take the form of any of the embodiments discussed above with reference to the coupling components 916, and the IC package 924 may take the form of any of the embodiments discussed above with reference to the IC package 920.

[0069] The IC device assembly 900 illustrated in FIG. 9 includes a package-on-package structure 934 coupled to the second face 942 of the circuit board 902 by coupling components 928. The package-on-package structure 934 may include an IC package 926 and an IC package 932 coupled together by coupling components 930 such that the IC package 926 is disposed between the circuit board 902 and the IC package 932. The coupling components 928 and 930 may take the form of any of the embodiments of the coupling components 916 discussed above, and the IC packages 926 and 932 may take the form of any of the embodiments of the IC package 920 discussed above. The package-on-package structure 934 may be configured in accordance with any of the package-on-package structures known in the art.

[0070] FIG. 10 is a block diagram of an example computing device 1000 that may include one or more components processed using the CMP systems and techniques disclosed herein. For example, any suitable ones of the components of the computing device 1000 may include a die (e.g., the die 702 (FIG. 7B)) processed using the CMP systems and techniques disclosed herein. A number of components are illustrated in FIG. 10 as included in the computing device 1000, but any one or more

of these components may be omitted or duplicated, as suitable for the application. In some embodiments, some or all of the components included in the computing device 1000 may be attached to one or more motherboards. In some embodiments, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die.

[0071] Additionally, in various embodiments, the computing device 1000 may not include one or more of the components illustrated in FIG. 10, but the computing device 1000 may include interface circuitry for coupling to the one or more components. For example, the computing device 1000 may not include a display device 1006, but may include display device interface circuitry (e.g., a connector and driver circuitry) to which a display device 1006 may be coupled. In another set of examples, the computing device 1000 may not include an audio input device 1024 or an audio output device 1008, but may include audio input or output device interface circuitry (e.g., connectors and supporting circuitry) to which an audio input device 1024 or audio output device 1008 may be coupled.

[0072] The computing device 1000 may include a processing device 1002 (e.g., one or more processing devices). As used herein, the term "processing device" or "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. The processing device 1002 may include one or more digital signal processors (DSPs), application-specific integrated circuits (ASICs), central processing units (CPUs), graphics processing units (GPUs), cryptoprocessors (specialized processors that execute cryptographic algorithms within hardware), server processors, or any other suitable processing devices. The computing device 1000 may include a memory 1004, which may itself include one or more memory devices such as volatile memory (e.g., dynamic random access memory (DRAM)), nonvolatile memory (e.g., read-only memory (ROM)), flash memory, solid state memory, and/or a hard drive. In some embodiments, the memory 1004 may include memory that shares a die with the processing device 1002. This memory may be used as cache memory and may include embedded dynamic random access memory (eDRAM) or spin transfer torque magnetic random-access memory (STT-MRAM).

[0073] In some embodiments, the computing device 1000 may include a communication chip 1012 (e.g., one or more communication chips). For example, the communication chip 1012 may be configured for managing wireless communications for the transfer of data to and from the computing device 1000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a nonsolid medium. The term

does not imply that the associated devices do not contain any wires, although in some embodiments they might not.

[0074] The communication chip 1012 may implement any of a number of wireless standards or protocols, including but not limited to Institute for Electrical and Electronic Engineers (IEEE) standards including Wi-Fi (IEEE 802.11 family), IEEE 802.16 standards (e.g., IEEE 802.16-2005 Amendment), Long-Term Evolution (LTE) project along with any amendments, updates, and/or revisions (e.g., advanced LTE project, ultramobile broadband (UMB) project (also referred to as "3GPP2"), etc.). IEEE 802.16 compatible Broadband Wireless Access (BWA) networks are generally referred to as WiMAX networks, an acronym that stands for Worldwide Interoperability for Microwave Access, which is a certification mark for products that pass conformity and interoperability tests for the IEEE 802.16 standards. The communication chip 1012 may operate in accordance with a Global System for Mobile Communication (GSM), General Packet Radio Service (GPRS), Universal Mobile Telecommunications System (UMTS), High Speed Packet Access (HSPA), Evolved HSPA (E-HSPA), or LTE network. The communication chip 1012 may operate in accordance with Enhanced Data for GSM Evolution (EDGE), GSM EDGE Radio Access Network (GERAN), Universal Terrestrial Radio Access Network (UTRAN), or Evolved UTRAN (E-UTRAN). The communication chip 1012 may operate in accordance with Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Evolution-Data Optimized (EV-DO), and derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The communication chip 1012 may operate in accordance with other wireless protocols in other embodiments. The computing device 1000 may include an antenna 1022 to facilitate wireless communications and/or to receive other wireless communications (such as AM or FM radio transmissions).

[0075] In some embodiments, the communication chip 1012 may manage wired communications, such as electrical, optical, or any other suitable communication protocols (e.g., the Ethernet). As noted above, the communication chip 1012 may include multiple communication chips. For instance, a first communication chip 1012 may be dedicated to shorter-range wireless communications such as Wi-Fi or Bluetooth, and a second communication chip 1012 may be dedicated to longer-range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, EV-DO, or others. In some embodiments, a first communication chip 1012 may be dedicated to wireless communications, and a second communication chip 1012 may be dedicated to wired communications.

[0076] The computing device 1000 may include battery/power circuitry 1014. The battery/power circuitry 1014 may include one or more energy storage devices (e.g., batteries or capacitors) and/or

circuitry for coupling components of the computing device 1000 to an energy source separate from the computing device 1000 (e.g., AC line power).

[0077] The computing device 1000 may include a display device 1006 (or corresponding interface circuitry, as discussed above). The display device 1006 may include any visual indicators, such as a heads-up display, a computer monitor, a projector, a touchscreen display, a liquid crystal display (LCD), a light-emitting diode display, or a flat panel display, for example.

[0078] The computing device 1000 may include an audio output device 1008 (or corresponding interface circuitry, as discussed above). The audio output device 1008 may include any device that generates an audible indicator, such as speakers, headsets, or earbuds, for example.

[0079] The computing device 1000 may include an audio input device 1024 (or corresponding interface circuitry, as discussed above). The audio input device 1024 may include any device that generates a signal representative of a sound, such as microphones, microphone arrays, or digital instruments (e.g., instruments having a musical instrument digital interface (MIDI) output).

[0080] The computing device 1000 may include a global positioning system (GPS) device 1018 (or corresponding interface circuitry, as discussed above). The GPS device 1018 may be in communication with a satellite-based system and may receive a location of the computing device 1000, as known in the art.

[0081] The computing device 1000 may include an other output device 1010 (or corresponding interface circuitry, as discussed above). Examples of the other output device 1010 may include an audio codec, a video codec, a printer, a wired or wireless transmitter for providing information to other devices, or an additional storage device.

[0082] The computing device 1000 may include an other input device 1020 (or corresponding interface circuitry, as discussed above). Examples of the other input device 1020 may include an accelerometer, a gyroscope, a compass, an image capture device, a keyboard, a cursor control device such as a mouse, a stylus, a touchpad, a bar code reader, a Quick Response (QR) code reader, any sensor, or a radio frequency identification (RFID) reader.

[0083] The computing device 1000 may have any desired form factor, such as a hand-held or mobile computing device (e.g., a cell phone, a smart phone, a mobile internet device, a music player, a tablet computer, a laptop computer, a netbook computer, an ultrabook computer, a personal digital assistant (PDA), an ultramobile personal computer, etc.), a desktop computing device, a server or other networked computing component, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a vehicle control unit, a digital camera, a digital video recorder, or a wearable computing device. In some embodiments, the computing device 1000 may be any other electronic device that processes data.

[0084] The following paragraphs provide various examples of the embodiments disclosed herein.

[0085] Example 1 is a wafer retainer ring for a chemical mechanical polishing (CMP) system, including: a top surface including a plurality of ridges separated by a corresponding plurality of grooves, wherein each of the plurality of ridges has a width; a bottom surface; an inner surface circumscribing an area having a diameter; and an outer surface; wherein a ratio of the diameter to the width is less than 3.8.

[0086] Example 2 may include the subject matter of Example 1, and may further specify that a total number of grooves is less than 12.

[0087] Example 3 may include the subject matter of any of Examples 1-2, and may further specify that the width is greater than 80 millimeters.

[0088] Example 4 may include the subject matter of any of Examples 1-3, and may further specify that the top surface has a hydrophilic water contact angle less than 75 degrees.

[0089] Example 5 may include the subject matter of any of Examples 1-4, and may further specify that the diameter is greater than 300 millimeters.

[0090] Example 6 may include the subject matter of any of Examples 1-5, and may further specify that the ratio of the diameter to the width is less than 3.

[0091] Example 7 may include the subject matter of any of Examples 1-6, and may further specify that the ratio of the diameter to the width is less than 2.8.

[0092] Example 8 may include the subject matter of any of Examples 1-7, and may further specify that the wafer retainer ring includes a plastic polymer.

[0093] Example 9 is a wafer retainer ring for a chemical mechanical polishing (CMP) system, including: a top surface including a plurality of ridges separated by a corresponding plurality of grooves, wherein each of the plurality of ridges has a ridge width greater than or equal to 80 millimeters; a bottom surface; an inner surface; and an outer surface.

[0094] Example 10 may include the subject matter of Example 9, and may further specify that the inner surface has a circular footprint with a diameter, and a ratio of the diameter to the ridge width is less than 3.8.

[0095] Example 11 may include the subject matter of any of Examples 9-10, and may further specify that a total number of grooves is less than 12.

[0096] Example 12 may include the subject matter of any of Examples 9-11, and may further specify that the top surface has a hydrophilic water contact angle less than 75 degrees.

[0097] Example 13 may include the subject matter of any of Examples 9-12, and may further specify that at least one of the plurality of grooves has a depth of at least 2 centimeters.

[0098] Example 14 may include the subject matter of any of Examples 9-13, and may further specify that the plurality of grooves are oriented at an angle relative to a radial direction of the wafer retainer ring.

[0099] Example 15 may include the subject matter of any of Examples 9-14, and may further specify that each of the plurality of ridges has a ridge width greater than or equal to 100 millimeters.

[0100] Example 16 may include the subject matter of any of Examples 9-15, and may further specify that the wafer retainer ring includes a hydrocarbon plastic polymer.

[0101] Example 17 is a wafer retainer ring for a chemical mechanical polishing (CMP) system, including: a top surface including a plurality of ridges separated by a corresponding plurality of grooves, wherein the top surface has a hydrophilic water contact angle less than or equal to 75 degrees; a bottom surface; an inner surface; and an outer surface.

[0102] Example 18 may include the subject matter of Example 17, and may further specify that at least one of the ridges has a width, the inner surface has a circular footprint with a diameter, and a ratio of the diameter to the width is less than 3.8.

[0103] Example 19 may include the subject matter of any of Examples 17-18, and may further specify that a total number of grooves is less than 12.

[0104] Example 20 may include the subject matter of any of Examples 17-19, and may further specify that all of the plurality of ridges have widths greater than or equal to 80 millimeters.

[0105] Example 21 may include the subject matter of any of Examples 17-20, and may further specify that the wafer retainer ring includes a hydrocarbon polymer.

[0106] Example 22 may include the subject matter of any of Examples 17-21, and may further specify that the top surface has a hydrophilic water contact angle less than or equal to 70 degrees.

[0107] Example 23 may include the subject matter of any of Examples 17-22, and may further specify that the top surface has a hydrophilic water contact angle less than or equal to 65 degrees.

[0108] Example 24 is a chemical mechanical polishing (CMP) system, including: the wafer retainer ring of any of Examples 1-24, wherein the wafer retainer ring is disposed on a first arm; a wafer retained in the wafer retainer ring; and a CMP polishing pad disposed on a second arm; wherein the first and second arms allow the CMP polishing pad to come into contact with, and move relative to, the wafer.

[0109] Example 25 may include the subject matter of Example 24, and may further include slurry disposed on the CMP polishing pad, wherein the slurry is transported across the wafer retainer ring and onto the wafer during polishing.

[0110] Example 26 may include the subject matter of Example 25, and may further specify that the slurry is an oxide slurry, a metal slurry, or a low-k slurry.

[0111] Example 27 may include the subject matter of any of Examples 24-26, and may further include a CMP conditioning disk disposed on a third arm, wherein the second and third arms allow the CMP polishing pad to come into contact with, and move relative to, the CMP conditioning disk.

[0112] Example 28 is a method of polishing a wafer, including: retaining a wafer in the wafer retainer ring of any of Examples 1-24; and after retaining the wafer in the wafer retainer ring, moving the wafer and a CMP polishing pad relative to one another while in contact to polish the wafer.

[0113] Example 29 may include the subject matter of Example 28, and may further include moving the CMP polishing pad and a CMP conditioning disk relative to one another to condition the CMP polishing pad.

[0114] Example 30 is a method of manufacturing a wafer retainer ring for a chemical mechanical polishing (CMP) system, including: forming an annular body from a polymer material; and forming a plurality of ridges in the annular body, wherein the ridges take the form of any of Examples 1-24.

[0115] Example 31 may include the subject matter of Example 30, and may further specify that forming the annular body and forming the plurality of ridges are performed in a three-dimensional manufacturing process.

[0116] Example 32 may include the subject matter of Example 30, and may further specify that forming the plurality of ridges comprises machining a plurality of grooves in the annular body.

[0117] Example 33 may include the subject matter of any of Examples 1-32, and may further specify that individual grooves of the plurality of grooves have a curved profile at the top surface.

[0118] Example 34 may include the subject matter of any of Examples 1-33, and may further specify that individual grooves of the plurality of grooves have a curved bottom profile.

Claims:

1. A wafer retainer ring for a chemical mechanical polishing (CMP) system, comprising:
a top surface including a plurality of ridges separated by a corresponding plurality of grooves, wherein each of the plurality of ridges has a width;
a bottom surface;
an inner surface circumscribing an area having a diameter; and
an outer surface;
wherein a ratio of the diameter to the width is less than 3.8.

2. The wafer retainer ring of claim 1, wherein individual grooves of the plurality of grooves have a curved profile at the top surface.

3. The wafer retainer ring of claim 1, wherein the width is greater than 80 millimeters.

4. The wafer retainer ring of claim 1, wherein the top surface has a hydrophilic water contact angle less than 75 degrees.

5. The wafer retainer ring of any of claims 1-4, wherein the diameter is greater than 300 millimeters.

6. The wafer retainer ring of any of claims 1-4, wherein the ratio of the diameter to the width is less than 3.

7. The wafer retainer ring of any of claims 1-4, wherein the ratio of the diameter to the width is less than 2.8.

8. A wafer retainer ring for a chemical mechanical polishing (CMP) system, comprising:
a top surface including a plurality of ridges separated by a corresponding plurality of grooves, wherein each of the plurality of ridges has a ridge width greater than or equal to 80 millimeters;
a bottom surface;
an inner surface; and
an outer surface.

9. The wafer retainer ring of claim 8, wherein the inner surface has a circular footprint with a diameter, and a ratio of the diameter to the ridge width is less than 3.8.

10. The wafer retainer ring of claim 8, wherein a total number of grooves is less than 12.

11. The wafer retainer ring of claim 8, wherein the top surface has a hydrophilic water contact angle less than 75 degrees.

12. The wafer retainer ring of any of claims 8-11, wherein at least one of the plurality of grooves has a depth of at least 2 centimeters.

13. The wafer retainer ring of any of claims 8-11, wherein the plurality of grooves are oriented at an angle relative to a radial direction of the wafer retainer ring.

14. The wafer retainer ring of any of claims 8-11, wherein each of the plurality of ridges has a ridge width greater than or equal to 100 millimeters.

15. The wafer retainer ring of any of claims 8-11, wherein the wafer retainer ring includes a hydrocarbon plastic polymer.

16. A wafer retainer ring for a chemical mechanical polishing (CMP) system, comprising:

a top surface including a plurality of ridges separated by a corresponding plurality of grooves, wherein the top surface has a hydrophilic water contact angle less than or equal to 75 degrees;

a bottom surface;

an inner surface; and

an outer surface.

17. The wafer retainer ring of claim 16, wherein at least one of the ridges has a width, the inner surface has a circular footprint with a diameter, and a ratio of the diameter to the width is less than 3.8.

18. The wafer retainer ring of claim 16, wherein individual grooves of the plurality of grooves have a curved profile at the top surface.

19. The wafer retainer ring of claim 16, wherein all of the plurality of ridges have widths greater than or equal to 80 millimeters.

20. The wafer retainer ring of any of claims 16-19, wherein the wafer retainer ring includes a hydrocarbon polymer.

21. The wafer retainer ring of any of claims 16-19, wherein the top surface has a hydrophilic water contact angle less than or equal to 70 degrees.

22. The wafer retainer ring of any of claims 16-19, wherein the top surface has a hydrophilic water contact angle less than or equal to 65 degrees.

23. A chemical mechanical polishing (CMP) system, comprising:

the wafer retainer ring of any of claims 1, 8, or 16, wherein the wafer retainer ring is disposed on a first arm;

a wafer retained in the wafer retainer ring; and

a CMP polishing pad disposed on a second arm;

wherein the first and second arms allow the CMP polishing pad to come into contact with, and move relative to, the wafer.

24. The CMP system of claim 23, further comprising:

slurry disposed on the CMP polishing pad, wherein the slurry is transported across the wafer retainer ring and onto the wafer during polishing.

25. The CMP system of claim 23, further comprising:

a CMP conditioning disk disposed on a third arm, wherein the second and third arms allow the CMP polishing pad to come into contact with, and move relative to, the CMP conditioning disk.

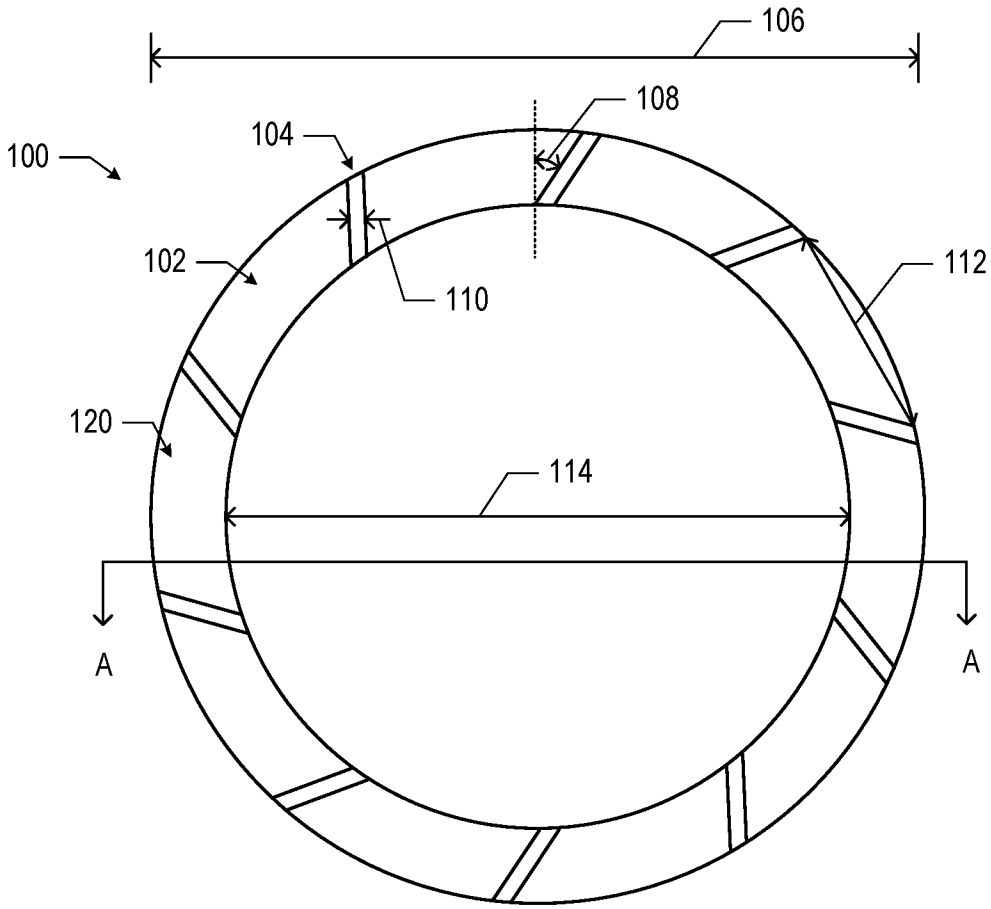

FIG. 1

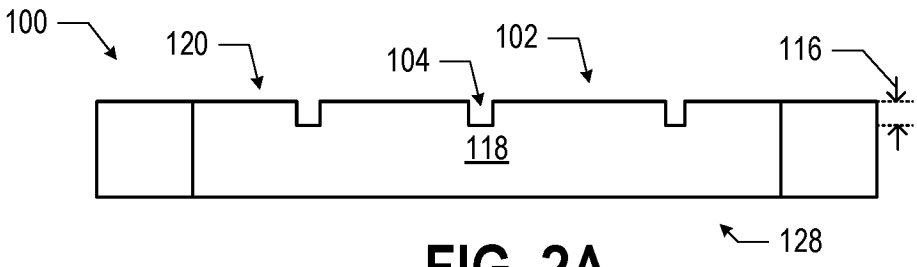

FIG. 2A

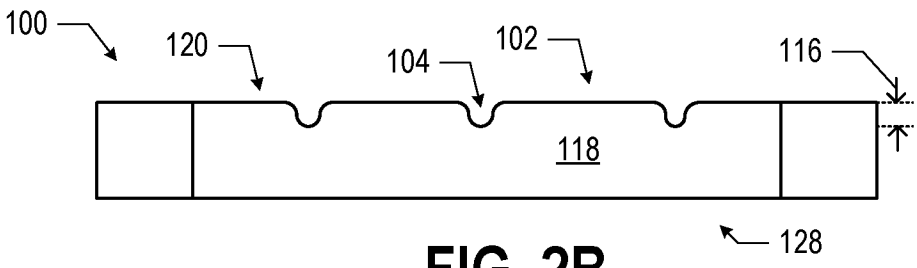

FIG. 2B

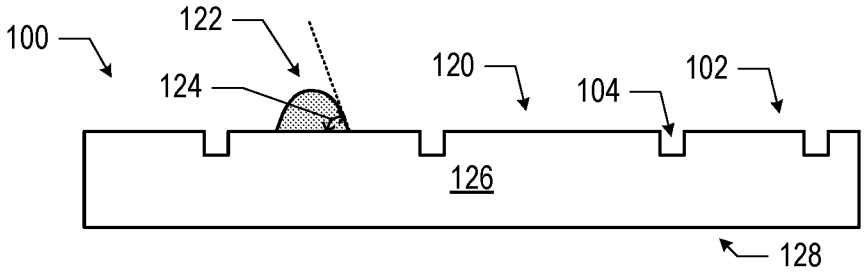

FIG. 3

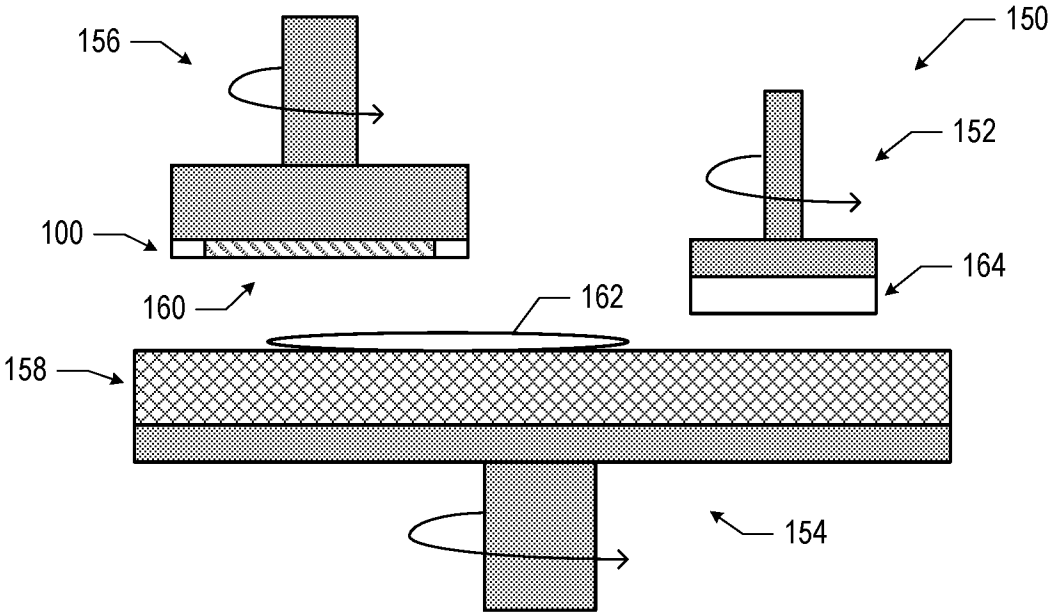

FIG. 4

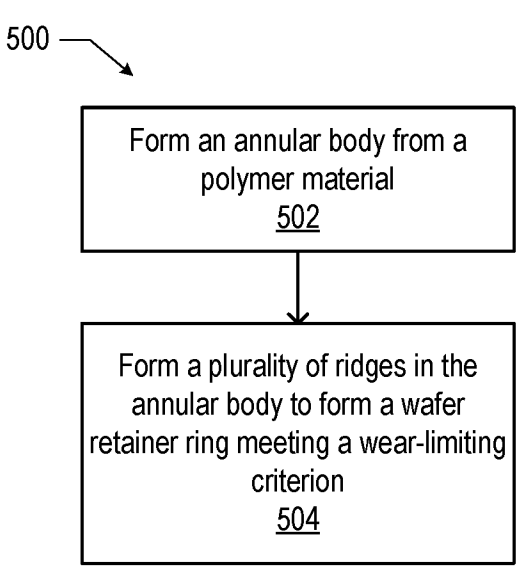

FIG. 5

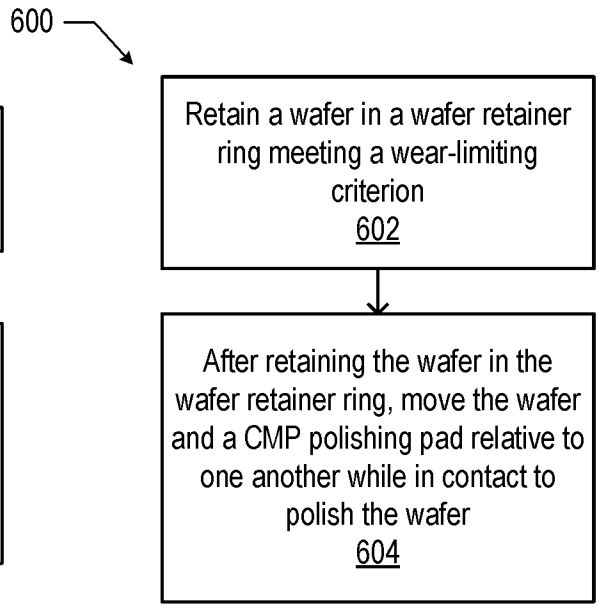

FIG. 6

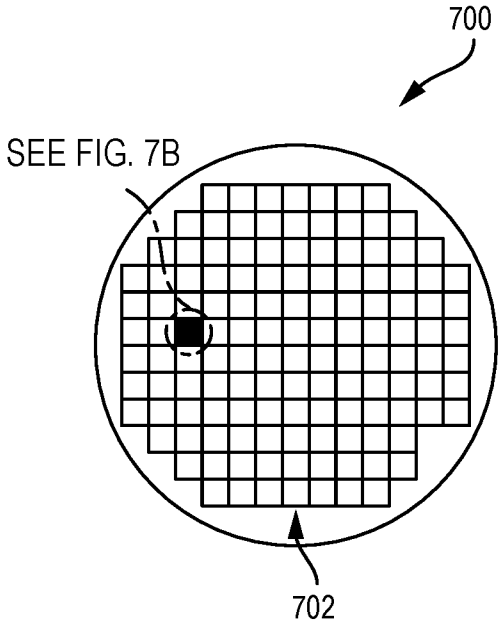

FIG. 7A

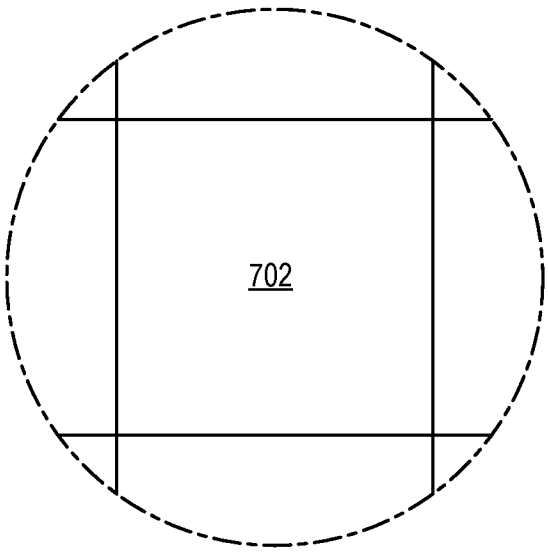

FIG. 7B

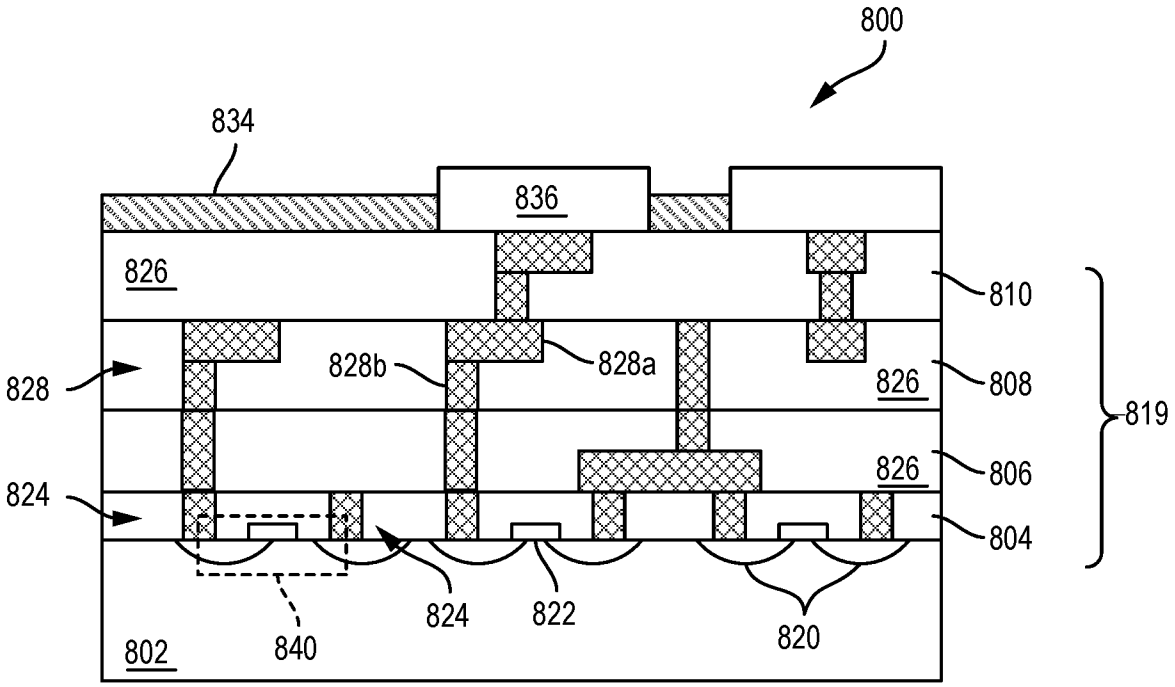

FIG. 8

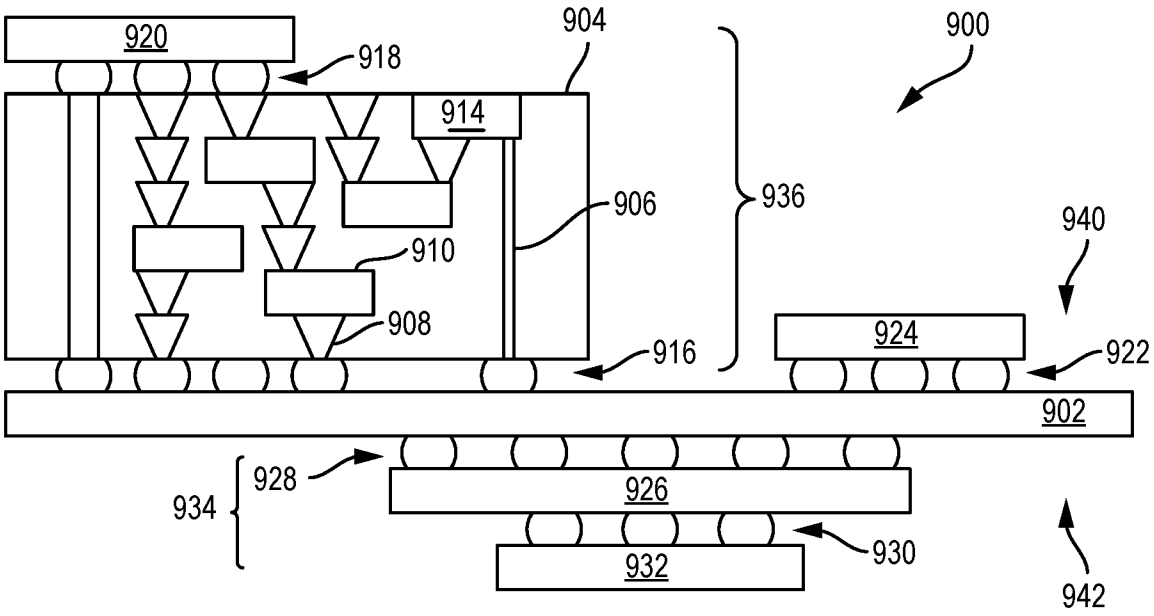
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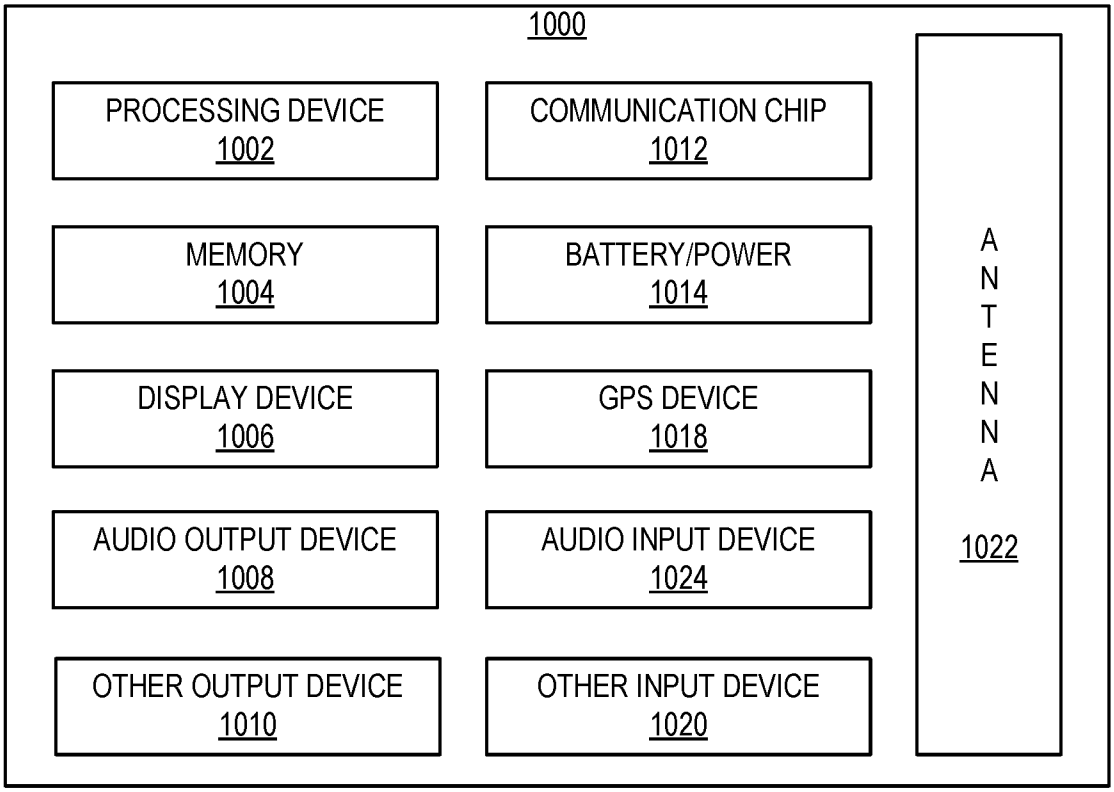
FIG. 9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PROCESSING DEVICE
1002
COMMUNICATION CHIP
1012
MEMORY
1004
BATTERY/POWER
1014
DISPLAY DEVICE
1006
GPS DEVICE
1018
AUDIO OUTPUT DEVICE
1008
AUDIO INPUT DEVICE
1024
OTHER OUTPUT DEVICE
1010
OTHER INPUT DEVICE
1020
ANTENNA
1022

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/019721

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/304(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/304; B24B 5/00; H01L 21/302; B24B 47/02; H01L 21/677; B24B 37/10; H01L 21/461

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: CMP, retainer ring, width of ridge, hydrophilic, groove

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	KR 10-2015-0111044 A (YONG JUN JEON) 05 October 2015 See paragraphs [0026]-[0033], claims 1-5 and figure 4.	1-3,5-10,12-15 ,23-25 4,11,16-22
Y	US 6068549 A (PAUL JACKSON) 30 May 2000 See column 6, lines 54, 55, column 12, lines 25-55, claims 1, 5, 9 and figures 21A-21D.	1-3,5-10,12-15 ,23-25
Y	US 2015-0105005 A1 (APPLIED MATERIALS, INC.) 16 April 2015 See paragraphs [0031]-[0035], claims 1, 7, 15 and figures 1, 2.	23-25
A	US 6224472 B1 (LEI PING LAI et al.) 01 May 2001 See column 8, line 56 - column 10, line 57, claims 1-12 and figure 4.	1-25
A	US 2004-0137739 A1 (VINCENT C. KORTHUIS et al.) 15 July 2004 See paragraph [0036], claim 1 and figure 2.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 November 2016 (24.11.2016)	**24 November 2016 (24.11.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/019721

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