PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 : G06F 11/10, G11C 29/00

A1

(11) International Publication Number: WO 87/ 06737

(43) International Publication Date: 5 November 1987 (05.11.87)

(21) International Application Number: PCT/US87/00593

(22) International Filing Date: 17 March 1987 (17.03.87)

(31) Priority Application Number: 854,232

(32) Priority Date: 21 April 1986 (21.04.86)

(33) Priority Country: US

(71) Applicant: UNISYS CORPORATION [US/US]; Burroughs Place, Detroit, MI 48232 (US).

(72) Inventors: KIM, Dongsung, Robert ; 24872 Grissom Road, Laguna Hills, CA 92653 (US). KRONIES, Reinhard, Kurt ; 9715 La Tierra Ave., Fountain Valley, CA 92708 (US).

(74) Agent: HARRIS, Gordon, K., Jr.; Unisys Corporation, Burroughs Place, Detroit, MI 48232 (US).

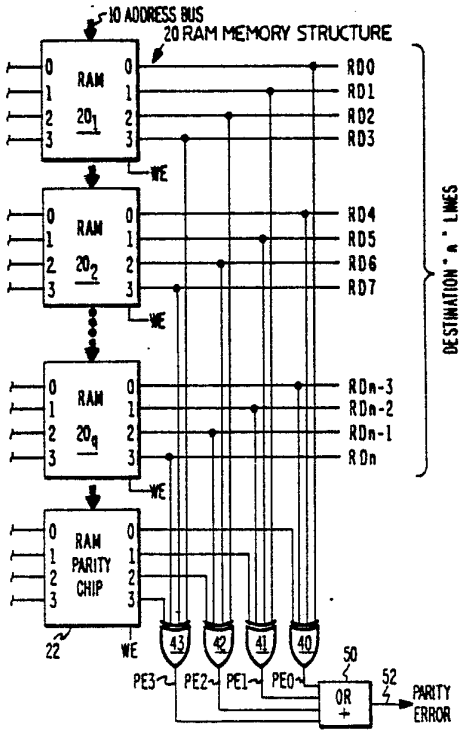
(81) Designated States: AT (European patent), BE (European patent), BR, CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, KR, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.

(54) Title: SPECIALIZED PARITY DETECTION SYSTEM FOR WIDE MEMORY STRUCTURE

(57) Abstract

A parity detection scheme for a wide memory structure of RAM memory chips (20) provides an auxiliary RAM parity memory chip (22) to store a parity data for each corresponding input line of each memory chip (20_1...20_q) corresponding for each address of each memory chip. This parity data is compared to comparable parity data which is read-out of any corresponding address of each of said memory chips.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**FR**	France	**ML**	Mali
AU	Australia	**GA**	Gabon	**MR**	Mauritania
BB	Barbados	**GB**	United Kingdom	**MW**	Malawi
BE	Belgium	**HU**	Hungary	**NL**	Netherlands
BG	Bulgaria	**IT**	Italy	**NO**	Norway
BJ	Benin	**JP**	Japan	**RO**	Romania
BR	Brazil	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CF	Central African Republic			**SE**	Sweden
CG	Congo	**KR**	Republic of Korea	**SN**	Senegal
CH	Switzerland	**LI**	Liechtenstein	**SU**	Soviet Union
CM	Cameroon	**LK**	Sri Lanka	**TD**	Chad
DE	Germany, Federal Republic of	**LU**	Luxembourg	**TG**	Togo
DK	Denmark	**MC**	Monaco	**US**	United States of America
FI	Finland	**MG**	Madagascar		

TITLE

SPECIALIZED PARITY DETECTION SYSTEM FOR WIDE MEMORY STRUCTURE

FIELD OF THE INVENTION:

This disclosure relates to circuitry and systems for proving out data transfer integrity when data bits are placed in a wide memory structure which can be verified by use of specialized parity check circuitry.

BACKGROUND OF THE INVENTION:

Many types of memory chip structures are used in the course of digital circuitry, the simplest memory structure of which is when the memory chips are merely one bit wide. For example, a memory with organization such as a 4K by 1 represents the situation where the memory structure is one bit wide and the memory unit can store 4,092 bits of memory and each individual bit-space can be addressed in order to output the particular data bit which resides in that memory space.

The conventional parity check detection circuitry which is used for such a memory structure (which is made up by one bit wide memory chips) is provided by adding a single parity bit to each word wherein the parity bit is stored into the memory together with the written-in word during the Write time. Subsequently, when the particular word and its parity bit is read out, then a new parity check is accomplished by checking the parity for the particular word that was read out during the Read time.

This scheme works adequately as long as the memory chips used are merely one bit wide in their organization since, in this case, any single chip failure would result in a single bit failure and thus be detected by the Read-out of the word and its parity bit.

However, increasingly today, the memory chips used in memory structure are organized according to multi-bit widths, such as 1K by 4. Under these conditions the normal detection scheme of adding a parity bit to the writing of a wide word and then detecting the parity bit

after the reading out of the word would cause the system to miss many single chip failures since this can result in no failure to a 4 bit failure.

Since the memory structures used very often consist of multi-bit width memory chips, as for example, in such designs as control stores and look-up tables, it is most desirable to have a more accurate parity detection scheme to overcome the inaccuracies inherent in the prior types of parity checking.

BRIEF DESCRIPTION OF THE DRAWINGS:

FIG. 1 is a schematic drawing showing a multi-bit memory structure using, for example, 4-bit wide RAM memory chips which are paralleled to connect a source means of data bits into a memory storage system after which they can be read out on the opposite destination side of the memory structure.

For ease of explanation, the memory chip used in this example is a 1K x 4 organization. However, the usable principle applies to any wide data bit memory organization.

SUMMARY OF THE INVENTION:

The present disclosure is an improved and more accurate parity detection scheme which is applicable to multi-width memory structures. This system generates a set of parity data for each word placed in an addressed location by generating a set of parity bits which is equal to the number of input lines (k) to each of the multi-bit width memory chips which are used in the memory structure.

Thus, the parity bit designated "P0" (FIG. 1) would be the parity sum of the bit "0" of each corresponding input line of each of "q" memory chips. Similarly, the parity bit "Pk" would be the parity sum of all the bit "kn's" of each one of the memory chips. These parity bits are established by tapping each set of k input bit lines on each memory chip which carry data for writing into a memory structure such as a RAM memory 20.

Then after the particular RAM memory is enabled for read-out, each co-relating set of output bit lines of each memory chip are parity summed for comparison with the output of a RAM parity memory chip which correlates the data from the Write cycle bit lines with the data on the Read cycle bit lines at any given address.

A first and second set of exclusive OR gates (XOR) is used to generate first and second sets of "k" resultant parity data for each respective Write-Read cycle that addresses the same memory location.

An auxiliary parity memory chip receives the first set of k resultant parity data for storage in locations which correspond to similar locations in each memory chip so that the same address data will read out the first set of resultant parity data corresponding to each address in the structured memory. This parity data is then input to said second set of exclusive OR gates to provide said second set of "k" resultant parity data.

The outputs of the second set of exclusive OR gates are fed to a single OR gate which will output a

parity error signal should any inconsistencies occur in parity data.

Thus, any single chip failure which can result in one to four bit errors will be detected by this scheme.

DESCRIPTION OF A PREFERRED EMBODIMENT:

As seen in FIG. 1, a typical multi-bit wide memory structure is shown wherein a series of units shown as multiple width RAM chips, 20_1, 20_2 -- 20_q are shown to provide a structured memory storage unit 20 which is fed by a bus from a Source means along a number (n) of data bit lines.

Each memory chip address may be "m" bits for 2^m locations, and each line-group of 4 bit lines of the memory data bus is fed into the four data inputs to the RAM memory chip. These inputs, as shown in FIG. 1, are designated as chip bit k_0, k_1, k_2, and k_3. The inputs to RAM 20_q would be designated as k_{q0}, k_{q1}, k_{q2}, and k_{q3}.

As seen in FIG. 1, the RAM memory structure is provided with an address bus 10 which is used to select which specific locations in the individual memory chips will be used for data to be temporarily stored. Additionally, each RAM memory chip has a Write enable (WE) line which selects whether the memory can be written into or can be read-out from.

Thus, the series of "n" memory data bus lines carrying data bits (FIG. 1) are shown at the left as coming from a Source and then being input into addressed locations in a series of memory chip units after which they can be read out and placed on the memory bus of "n" lines for transfer to a destination.

As will be seen in FIG. 1, each memory chip has an input set of "four" lines, which number of inputs may be designated as "k" since the memory chip may have more or less than the 4 lines shown. Thus, the letter "k" will designate the number of data bit lines such that each particular memory chip is characterized as having k input lines and k output lines.

It will be noted that each bit k_0 of each of the memory chips is connected to an exclusive OR gate 30. Likewise, each k_1 bit line of the RAM memory chips is connected to an exclusive OR gate 31. Likewise, bit k_2 for each of the memory chip inputs is connected to an exclusive OR gate 32 and each input bit k_3 of each of the memory chips is connected to the exclusive OR gate 33.

Each of the exclusive OR gates 30 through 33 will provide a particular parity output signal designated as P_0, P_1, P_2 and P_3. These may be designated as a first set of resultant parity data. These outputs are fed to the RAM parity memory chip 22 in a fashion which correlates the input bit k with the corresponding input bit k of each of the series of RAM memory chips.

On the output side of the RAM memory chips 20_1 through 20_q, there is the Read-out side of the memory bus. In a similar fashion to the input or Write-in side, the Read-out side of the memory bus provides connections which connect each corresponding k bit line of each memory chip to a particular exclusive OR gate. Thus, the exclusive OR gate 40 connects all the k_0 lines; the exclusive OR gate 41 connects all the k_1 bit lines; the exclusive OR

gate 42 connects each of the k_2 bit lines; while the exclusive OR gate 43 connects each of the bit lines k_3.

Additionally, it will be seen that the co-relating "k" outputs of the auxiliary RAM parity memory chip 22 also connect the corresponding bit lines to exclusive OR gates 40, 41, 42 and 43.

The second set of exclusive OR gates have respective resultant parity data lines designated PE_0, PE_1, PE_2 and PE_3. These series of output lines are fed to an OR gate 50, whereby any inconsistency between the outputs of the corresponding parity chip bit lines of RAM 22 and the corresponding parity sum of k output lines of each memory chip will cause a resultant parity error signal to occur at the moment of inconsistency.

As will be noted from the connections shown in FIG. 1, the RAM parity memory chip 22 has a series of address locations which correspond to the same set of address locations in the RAM memory chips 20_1, 20_2---20_q.

Thus, for each set of input data on the Source lines which are placed in a particular address in the wide memory structure of the memory system there will also be written-in a set of corresponding bits P_0, P_1, P_2 and P_3 which will be placed in the corresponding address location inside the RAM parity memory chip 22.

Thereafter, on the Read operation, when a specific memory area is addressed in order to place data bits on the destination side of the memory structure, it will be seen that the same particular memory area is addressed on the RAM parity memory chip in order to provide an output of

parity bits which correspond to that particular address. These then can be transmitted to each of the exclusive OR gates 40, 41, 42 and 43 for comparison with the other inputs to each of these gates in order to see whether parity consistency has been maintained or there is a parity error.

If there is an inconsistency in any one of the inputs to gates 40 through 43, then the parity error signal PE_0, PE_1, PE_2 or PE_3 will indicate this parity error such that any difference in the states of the parity error output lines will be revealed by the OR gate 50 in order to provide a parity error signal on line 52.

Thus, it can be seen that if a memory structure is made of memory chips that are k bits wide and the number of data bit lines in the bus is "n" lines, then it will be seen that if "n" is divided by "k", the number of memory chips required can be given the value of "q".

Thus, "q" equals "n" divided by "k" ($q = \frac{n}{k}$).

The particular parity detection scheme involved provides that even though multi-width memory structures are used, there will be no loss of accuracy in parity detection should an entire memory chip fail or should one portion of a memory chip fail.

In any case, any type of failure in the memory chip will be detected by the parity detection system, since each bit line of data on the input or "Write" side is checked to provide a parity bit to the RAM parity chip which can then be checked with its corresponding bit line data on the "Read" or output side of the memory structure

in order to provide a parity error output signal which can be used to flag a suitable processor unit in order to reschedule or retry the data transmission.

There has been described herein a specialized parity detection scheme for a wide memory structure which overcomes the difficulties which are presented when using the standard parity type detection scheme wherein each word of memory is provided with a parity bit which is then read out of memory with its parity bit and checked to see whether the read-out parity checks with the written-in parity bit, which system could not be completely accurate in its detection of misduplication or lost bits in the course of writing into and reading out of a memory structure.

While certain variations of the above described concepts may be made in structure, it should be understood that the disclosed invention is to be defined and encompassed by the following claims:

What is claimed is:

1. A parity checking system for checking reliability of data transfers of data stored in and read out of a wide memory structure where a data transfer bus has "n" data bit lines organized in line-groups of "k" lines and each group of "k" lines is serviced by a single multiple width memory chip, the combination comprising:

(a) said data transfer bus having "n" data-bit lines for transferring data from a Source means to a Destination means and including:

(a1) a series of "q" line-groups wherein each line-group is composed of "k" consecutive bit lines;

(b) a plurality of "q" memory chips forming said wide memory structure, and connected to receive and store data bits from said Source means, where "q" = $\frac{n}{k}$ and wherein "k" represents the number of data bit lines in said line-group connected to each memory chip, where "k" is also a submultiple of "n", each of said plurality of "q" memory chips being connected to receive a consecutive series of "k" data bit lines from each of said line-groups of said transfer bus for subsequent readout on corresponding data bit output lines for transfer to a Destination means, and wherein each of said memory chips has "k" data-bit input lines for receiving data bits for storage in each particularly addressed memory location, and each consecutive data bit input line to each memory chip is designated as k_0, k_1, k_2---k_x so that each of said memory chips has an input data bit line which corresponds to a co-related input data bit line on each other of said memory chips;

(c) first sense means, connected to said Source means, for sensing each of said data bits on each said corresponding input line on each of said "q" memory chips to provide a first set of "k" resultant parity bits;

(d) second sense means, connected to said Destination means, for sensing each of said data bits on each said corresponding output bit line of each of said "q" memory chips to provide a second set of "k" resultant-parity bits;

(e) checking means for comparing said first set and said second set of "k" resultant-parity bits to determine coincidence or non-coincidence of parity data.

2. The combination of claim 1 wherein said first sense means includes:

(a) a first set of k" exclusive OR gates (XOR) wherein each XOR gate has a series of "k" gate inputs whereby each of said gate inputs is connected to the same corresponding input line on each of said "q" memory chips;

(b) a first set of "k" resultant-parity bit data output lines.

3. The combination of claim 1 wherein said wide memory structure includes:

(a) an auxiliary RAM parity memory chip which duplicates the width and address location of each of said plurality of memory chips and is operated as a parity storage chip for collection of parity data bits which are representative of input data to each address location of said wide memory structure.

4. The combination of claim 2 wherein said second sense means includes:

(a) a second set of "k" exclusive OR gates (XOR) wherein each of said XOR gates has a series of "k" gate inputs whereby each of said gate inputs is connected to the same corresponding one of said data bit output lines from each of said "q" memory chips;

(b) a set of "k" resultant-parity data output lines from each corresponding line of said RAM memory parity chip being connected to each corresponding XOR gate.

5. The combination of claim 1 wherein said checking means includes:

(a) a RAM parity memory chip having k input and output lines and providing a plurality of address locations corresponding to each address location of each of said q memory chips.

6. The combination of claim 1 wherein said checking means includes:

(a) an auxiliary output OR gate (OR) for receiving the outputs of each of said second set of "k" resultant-parity bits to establish an error signal when parity error occurs.

7. A parity checking system for data transferred into and out of a wide memory structure, comprising in combination:

(a) a wide memory bus structure having "q" memory chips operating in parallel, each of said memory chips having a width of "m" bits wherein each of said memory chips receive "k" input bit-lines and include "k" corresponding output bit lines;

(b) addressing means for addressing corresponding locations in each of said plurality of memory chips;

(c) enabling means for enabling the write-in or the read-out of data bits to/from each addressed location in each of said plurality of memory chips;

(d) a series of "q" line-groups wherein each line-group consists of "k" data bit lines for input to each of said memory chips;

(e) parity data sensing means for sampling data bits written into said memory structure for comparison with the data bits read out of said memory structure for each address location in order to determine whether a parity error has occurred, thus indicating faulty data transfer.

8. The combination of claim 7 wherein said parity data sensing means includes:

(a) a first set of "k" XOR gates wherein each one of said XOR gates samples the corresponding input bit line to each of said memory chips and uses an exclusive OR gate operation to provide a first set of output parity bits for each one of said "k" input lines;

(b) a RAM parity memory chip connected to receive each of said first set of "k" parity output bits from said XOR gates and to provide an address location for each corresponding addressed location in said wide memory structure for storage of said first set of "k" parity output bits;

(c) a second set of "k" exclusive OR gates (XOR) wherein each of said gates samples each corresponding one of said output bit lines of each said memory chip in said wide memory structure and additionally samples the corresponding set of output parity data bits from said RAM parity memory chip in order to generate a set of "k" parity error signals which relate to each said bit line of each said memory chip.

9. The combination of claim 8 which includes:

(a) an auxiliary OR gating means for receiving each of the said "k" parity error signals from said second set of XOR gates to generate a parity error signal should there be a non-coincidence of parity data.

10. In a wide structured memory having "q" units of parallel memory chips wherein each memory chip has "m" bits of address lines and has "k" input data lines and "k" output data lines wherein each successive input and output line for each said memory chip is designated as k_0, k_1, k_2---k_q and has "2^m" locations for storage of "k" bits in each location, whereby each one of said "2^m" locations can be addressed for write-in of data or read-out of data, a parity checking system comprising in combination:

(a) first means for sampling each one of said "k" corresponding input data lines of each one of said memory chips at the moment of address occurrence for the selection of a memory location during write-in to each of said memory chips to generate a first set of "k" parity data outputs (P_0, P_1, P_2---P_q);

(b) second means for sampling each one of said "k" corresponding output data lines of each one of said "q" memory chips at the moment of address occurrence during read-out for the selection of the same memory location as was addressed during write-in in order to generate a second set of "k" parity data outputs (PE_0, PE_1, PE_2---PE_q);

(c) an auxiliary parity memory chip having "k" inputs from said first set of "k" parity data outputs and having a set of addressable memory locations storing parity data bits corresponding to each addressable location in each of said "q" memory chips, said parity memory chip providing a set of "k" parity output lines to carry out said stored parity data bits from any addressed location corresponding to the addressed location in each of said memory chips, and wherein said "k" parity data bits from each addressed location of said parity memory chips are compared respectively to said second set of parity data outputs (PE_0, PE_1, PE_2---PE_q) for detection of parity error.

FIG. 1A.

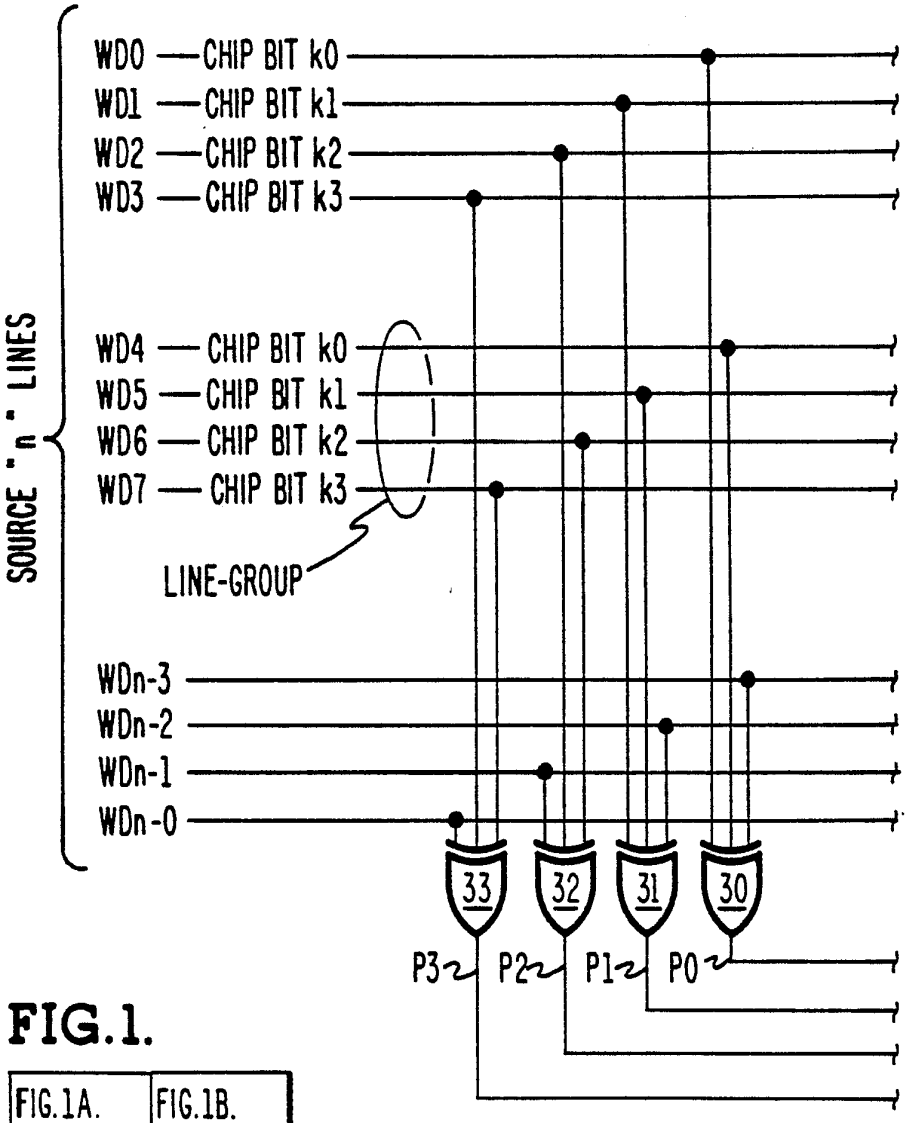

SOURCE "n" LINES
WD0 — CHIP BIT k0
WD1 — CHIP BIT k1
WD2 — CHIP BIT k2
WD3 — CHIP BIT k3
WD4 — CHIP BIT k0
WD5 — CHIP BIT k1
WD6 — CHIP BIT k2
WD7 — CHIP BIT k3
LINE-GROUP
WDn-3
WDn-2
WDn-1
WDn-0
33
32
31
30
P3
P2
P1
P0

FIG. 1.

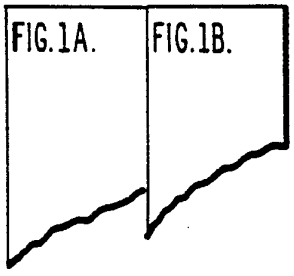
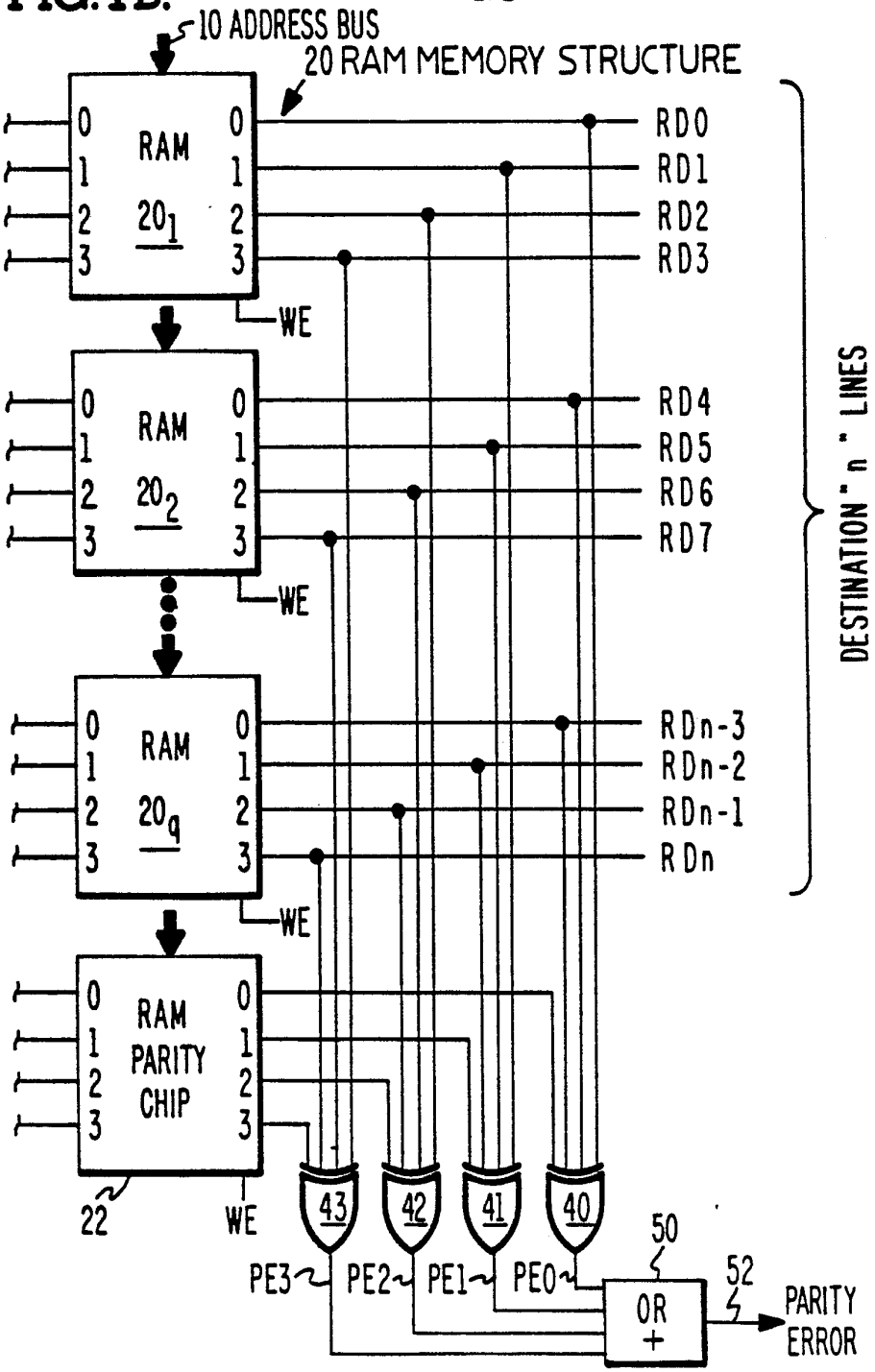


FIG. 1A.
FIG. 1B.

FIG. 1B.


10 ADDRESS BUS
20 RAM MEMORY STRUCTURE
RAM
20_1
20_2
20_q
RAM PARITY CHIP
WE
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
RDn-3
RDn-2
RDn-1
RDn
DESTINATION "n" LINES
43
42
41
40
PE3
PE2
PE1
PE0
22
50
52
OR
+
PARITY ERROR

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/00593

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (4): G06F 11/10; G11C 29/00

U.S.CL. 371/51

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	371/38,49,51

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US, A, 3,789,204 (BARLOW) 29 JANUARY 1974, see Figure 1.	1-10
A	US,A, 4,355,393 (KUBO) 19 OCTOBER 1982, see the entire document.	1-10
A	IBM Technical Disclosure Bulletin, Volume 13, No. 5, issued October 1970 (Armonk, New York), C.H. Schuenemann, "Correction of Single Errors by Double Parity Check", see pages 1324 and 1325.	1-10
Y	F.F. Sellers,Jr., "Error Detecting Logic for Digital Computers", published 1986, by McGraw-Hill Book Company (New York), see pages 207 to 211, especially Figure 12.2d.	1-10

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
11 May 1987	29 MAY 1987
International Searching Authority [1]	Signature of Authorized Officer [20]
ISA/US	Charles E. Atkinson

Form PCT/ISA/210 (second sheet) (May 1986)