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(54) **BEOL DECOUPLING CAPACITOR**

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(57) **ABSTRACT**

An IC including a resistor which is coupled to a metal wiring level through metal contacts, said resistor including a discrete metal-insulator-metal stack, wherein said metal contacts are in contact to one of said metals of said film stack. In the above IC design, current flows laterally through either the top metal electrode, the bottom metal electrode, or both, and any unused electrode is disconnected from the circuit.

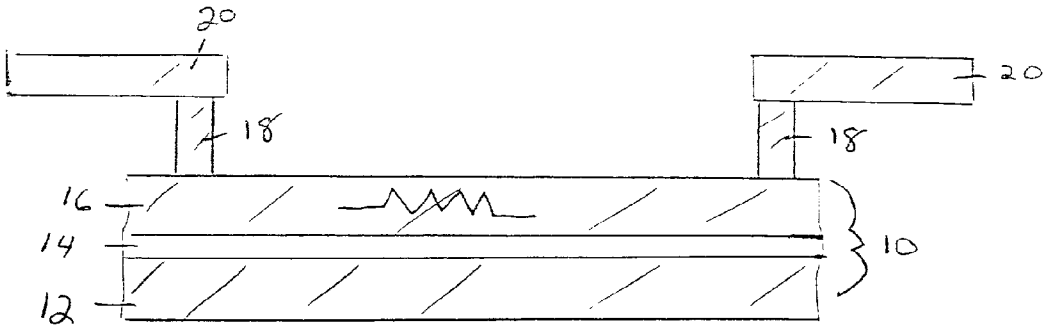


Fig. 1

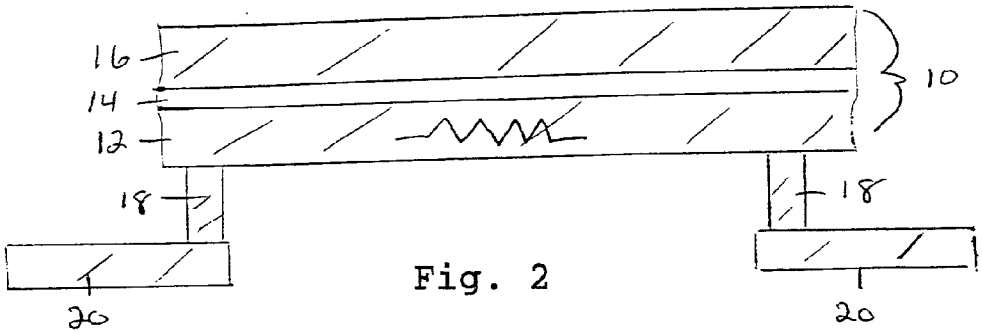


Fig. 2

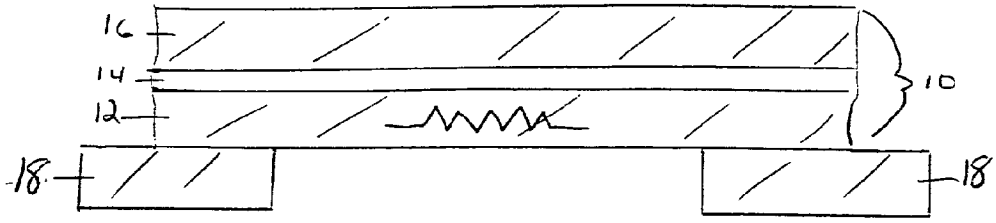


Fig. 3

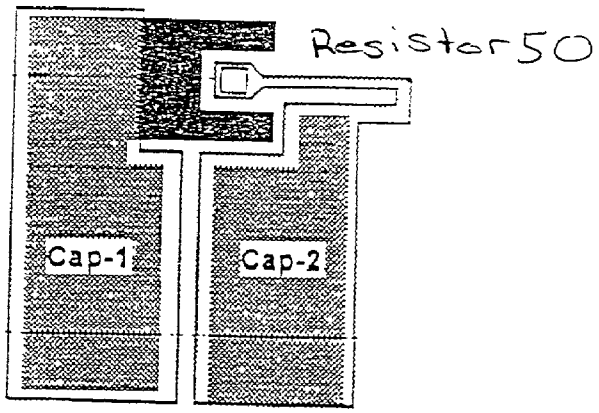


Fig. 4A

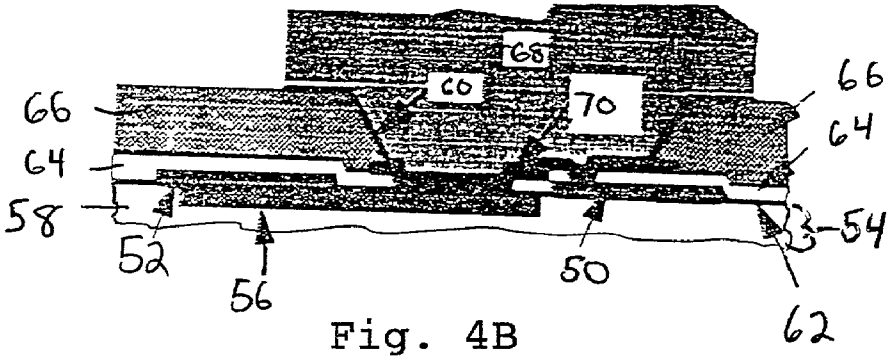


Fig. 4B

# BEOL DECOUPLING CAPACITOR

## RELATED APPLICATIONS

[0001] This application is a continuation-in-part application of U.S. application Ser. No. 09/225,526, filed Jan. 4, 1999.

## FIELD OF THE INVENTION

[0002] The present invention relates to integrated circuits (ICs), and in particular to an integrated circuit which includes at least a resistor having low capacitance coupling to an underlying substrate and a controllable resistance value, said resistor comprising a discrete metal-insulator-metal (MIM) film stack in which metal contacts are in electrical connection therewith. The discrete MIM film stack of the present invention is composed of the same films as the MIM film stack of an adjacent high-capacitance capacitor. The present invention is also directed to a method of fabricating such integrated circuits and to the use of TaN or TaN/α-Ta as interconnects for such integrated circuits.

## BACKGROUND OF THE INVENTION

[0003] High-capacity IC capacitors, on the order of 1 $nF/mm^2$ or above, connected across the power supply and ground buses of modern microprocessor chips are needed to reduce the power and ground noise to an acceptable level. The high-capacity capacitors should be placed very close to the switching circuits, and be connected to the power and ground buses by a low-resistance conductor. To accomplish this goal, one preferred approach is to build the high-capacity capacitors into a BEOL (back end of the line) process.

[0004] The dielectric thin film material for such BEOL decoupling capacitors must satisfy both of the following requirements: (1) a high dielectric constant as compared to conventional dielectrics such as $SiO_2$ and $Si_3N_4$ (for example, a 100 nm thick film with a dielectric constant of 20 would give a capacitance of 1.8 $nF/mm^2$); and (2) a formation temperature which is compatible with the BEOL metallurgy and processing.

[0005] The latter criteria implies that the deposition temperature of the dielectric material used in forming the BEOL decoupling capacitor must be about 450° C. or lower. Such a low deposition temperature is required in order to avoid unwanted instability of the BEOL metallurgy used for the power and ground connections.

[0006] Although a variety of dielectric materials having high dielectric constants are known in the art, prior art dielectrics cannot be employed in BEOL processing due to their required high deposition temperatures. An example of such a high dielectric constant material is the crystalline form of certain perovskite-type oxides. Despite having dielectric constants of about 200 or above, crystalline perovskite-type oxides are typically deposited at temperatures of about 500° C. or higher, or require a post anneal step using temperatures higher than 500° C. As such, the crystalline perovskite-type oxides such as barium strontium titanate (BSTO) cannot be employed in BEOL applications.

[0007] In a typical integrated circuit, capacitor and resistor devices are made from separate films. The use of separate films in fabricating resistors and capacitors adds additional processing steps to the overall manufacturing process which, in turn, increases the overall cost of manufacturing the IC. A need thus exists for providing an integrated circuit which includes a resistor and a capacitor that are fabricated from the same films. Such an integrated circuit would require less processing steps than a conventional integrated circuit; therefore reducing the overall cost of manufacturing the integrated circuit.

[0008] Moreover, an integrated circuit is needed that includes a resistor that has low capacitance coupling to the underlying substrate, as well as a small footprint area which is required to obtain optimum sheet resistance and optimum resistor width and length. Additionally, a resistor is needed that has well controllable and reproducible values which are independent of subsequent processing such as thermal cycling. Such features cannot be meet using typical diffusion- or polysilicon-resistors whose values are functions of many more factors.

## SUMMARY OF THE INVENTION

[0009] One object of the present invention is to provide an integrated circuit (IC) comprising at least a resistor that is integrated with a high-capacitance capacitor, said resistor includes a metal-insulator-metal (MIM) film stack. In the present invention, the insulator of the film stack may be a conventional dielectric material or, more preferably, it is a thin film dielectric having a dielectric constant higher than conventional dielectric materials.

[0010] A further object of the present invention is to provide an IC that comprises an integrated resistor/high-capacitance capacitor that has low-capacitive coupling to the underlying substrate.

[0011] A further object of the present invention is to provide an IC which comprises an integrated resistor/high-capacitance capacitor having optimum resistance.

[0012] A yet further object of the present invention is to provide an IC comprising an integrated resistor/high-capacitance capacitor which has well controlled resistor values which are reproducible.

[0013] An additional object of the present invention is to provide an integrated circuit wherein the resistor and capacitor are fabricated from the same films.

[0014] These and other objects and advantages are achieved in the present invention by providing discrete MIM films stacks and by connecting one of the metal electrodes of a at least one of the discrete MIM film stacks so that current flows laterally through either the top or bottom electrode, or both, and any unused electrode is disconnected from the circuit.

[0015] Specifically, the present invention relates to an IC comprising a resistor which is coupled to a metal wiring level of an interconnect or damascene structure through metal contacts, said resistor including a discrete metal-insulator-metal film stack, wherein said metal contacts are in contact with one of said metals of said film stack. In the present invention, the insulator of the film stack may be a conventional dielectric, e.g., $SiO_2$, $Si_3N_4$ or $Al_2O_3$, or a high dielectric constant dielectric, such as an amorphous dielectric having a dielectric constant of 10 or greater. Combinations of various dielectric materials may also be used herein.

[0016] In the above IC design, current flows laterally through either the top metal electrode, the bottom metal electrode, or both, and any unused electrode is disconnected from the circuit.

[0017] In one embodiment of the present invention, the metal contacts of the inventive IC are composed of TaN or TaN/α-Ta which have a sheet resistance of from about 3 to about 300 ohms/sq. which is significantly above the sheet resistance of typical metal contacts that are composed of Al, W, or Cu (the latter metal contacts have a sheet resistance on the order of 0.04-0.2 ohms/sq.). The use of TaN or TaN/α-Ta metal contacts in the IC design described above allows for a resistor having a size of from about 50 ohms up to the multi-Kohm range and beyond, as well as a resistor line:width ratio of about 20:1.

[0018] In another aspect of the present invention, a method of fabricating the above-described IC structure is provided. Specifically, the method of the present invention comprises, in one embodiment, the steps of:

[0019] (a) providing a metal-insulator-metal film stack on at least a material layer of an interconnect structure;

[0020] (b) patterning said metal-insulator-metal film stack into discrete metal-insulator-metal film stacks;

[0021] (c) forming metal contacts on at least one of said discrete metal-insulator-metal film stacks; and

[0022] (d) forming a wiring region connected to said metal contacts.

[0023] In another embodiment of the present invention, the method comprises the steps of:

[0024] (a) forming metal contacts on a surface of a metal wiring region, said metal wiring region is part of an interconnect or damascene structure; and

[0025] (b) forming a discrete metal-insulator-metal film stack on at least said metal contacts.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0026] **FIG. 1** is a cross-sectional representation of one possible resistor design layout of the present invention.

[0027] **FIG. 2** is a cross-sectional representation of another possible resistor design layout of the present invention.

[0028] **FIG. 3** is a cross-sectional representation of yet another possible resistor design layout of the present invention.

[0029] FIGS. **4A-4B** are pictorial representations of one possible IC structure of the present invention through various views; **4A** is a top view of the inventive IC structure, and **4B** is a side view. In these drawings, the resistor is formed on the top electrode of a MIM film stack.

## DETAILED DESCRIPTION OF THE INVENTION

[0030] The present invention which provides an IC structure having a resistor made from a discrete metal-insulator-metal film stack will now be described in greater detail by referring to the drawings that accompany this application. It should be noted that in the drawings like reference numerals are used for describing like and corresponding elements.

[0031] Referring first to **FIG. 1**, there is shown a cross-sectional view of one possible resistor design of the present invention. Specifically, the resistor design of **FIG. 1** comprises a patterned, discrete metal-insulator-metal (MIM) film stack **10** which includes an insulator film **14** that is sandwiched between bottom electrode **12** and top electrode **16**. The inventive resistor design of **FIG. 1** further includes metal contacts **18** that are formed on at least a portion of top electrode **16** and an overlying metal wiring region **20** that is formed so as to be in electrical contact with metal contacts **18**.

[0032] **FIG. 2** illustrates a cross-sectional view of another inventive resistor design of the present invention. **FIG. 2** is composed of the same components as in **FIG. 1**, but for the fact that metal contacts **18** and wiring region **20** are formed beneath the discrete MIM film stack.

[0033] **FIG. 3** shows yet another resistor design of the present invention. In this drawing, the resistor design includes patterned metal-insulator-metal film stack **10**, bottom electrode **12**, insulator film **14**, top electrode **16** and contact metal **18**. In this design layout, the contact metal, which may be in the form of a metal line or via, is part of a damascene structure.

[0034] It is noted that each of the above resistor design layouts represents one component of an IC structure which could be made using BEOL processes or damscene processes. Additionally, in each of the resistor design layouts shown in FIGS. **1-3**, the current flows laterally through either the top or bottom electrode, or both and any unused electrode of the MIM resistor is disconnected from the circuit. It should be noted that in each of the design layouts described above, the other discrete MIM film stacks may be used as resistors, or alternatively, as high-capacitance capacitors.

[0035] Electrodes **12** and **16** are composed of conventional conductive materials including, but not limited to: TaN, Pt, Ir, ruthenium oxide, Al, Au, Cu, Ta, TaSiN and mixtures or multilayers thereof. Other conventional conductive materials can also be employed in the present invention. The electrodes are formed utilizing conventional deposition processes including, but not limited to: sputtering, plating, evaporation, chemical vapor deposition (CVD), plasma-assisted CVD, chemical solution deposition and other like deposition processes.

[0036] Insulator film **14** may be composed of a conventional dielectric material such as $SiO_2$, $Si_3N_4$ or $Al_2O_3$, or more preferably, it is composed of a high dielectric constant dielectric (dielectric constant greater than 10). Combinations of varies dielectric materials are contemplated herein. In one highly preferred embodiment, insulator film **14** is an amorphous high dielectric constant thin film which is composed of a perovskite-type oxide. The term "perovskite-type oxide" is used herein to denote a material which includes at least one acidic oxide containing at least one metal selected from Group IVB (Ti, Zr or Hf), VB (V, Nb or Ta), VIB (Cr, Mo or W), VIIB (Mn or Re) or IB (Cu, Ag or Au) of the Periodic Table of Elements (CAS version) and at least one additional cation having a positive formal charge of from about 1 to about 3. Such perovskite-type oxides typically

have the basic formula: $ABO_3$ wherein A is one of the above mentioned cations, and B is one of the above mentioned metals.

[0037] Suitable perovskite-type oxides include, but are not limited to: titanate-based dielectrics, manganate-based materials, cuprate-based materials, tungsten bronze-type niobates, tantalates, or titanates, and bismuth layered-tantalates, niobates or titanates. Of these perovskite-type oxides, barium strontium titanate (BSTO), barium titanate (BTO), lead zirconium titanate (PZTO), barium zirconium titanate (BZTO), tantalum titanate (TTO), lead lanthanum titanate (PLTO), barium strontium niobate, barium strontium tantalate or strontium titanate (STO) are preferred in the present invention. A highly preferred perovskite-type oxide is BSTO or BZTO.

[0038] It is emphasized that the perovskite-type oxide employed in the present invention is preferred to be in the amorphous (or low temperature) phase since the crystalline phase of such materials is produced at temperatures which are not compatible with BEOL processing. The term "amorphous phase" is used herein to denote that the crystal structure of the perovskite-type oxide lacks order. This is different from the crystalline phase of the material wherein a highly ordered crystal structure is observed.

[0039] The amorphous thin film dielectric material is formed by a suitable deposition process which is capable of operating at temperatures well below the crystallization temperature of the perovskite-type oxide and thereafter, the deposited material is annealed.

[0040] Typically the temperature of deposition of the amorphous thin film dielectric material is kept below 400° C. and thus the process and the material is compatible with BEOL temperature requirements. In some applications, higher BEOL temperatures may be allowed, up to 450° C. or even 500° C. The amorphous thin film dielectric materials of the present invention retain their properties to well above 500° C., i.e., their amorphous to crystalline transformation occurs well above 500° C.

[0041] Suitable deposition processes that can be employed in the present invention in forming the amorphous thin film dielectric material include, but are not limited to: chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma-assisted CVD, low pressure CVD, high density plasma CVD, ionized-PVD as well as chemical solution deposition (CSD). A sol gel technique can also be employed in the present invention to form the amorphous thin film dielectric material of the present invention.

[0042] The annealing step used in forming the amorphous thin film dielectric material of the present invention is conducted at a temperature of from about 150° to about 450° C. for a time period of from about 0.1 to about 4 hrs. More preferably, annealing of the amorphous dielectric material is carried out at a temperature of from about 300° to about 400° C. for a time period of from about 0.5 to about 4 hrs. Oxidizing gases such as oxygen, $N_2O$, ozone or mixtures such as air may be employed in the annealing step.

[0043] The exact conditions employed in forming the amorphous thin film dielectric material of the present invention may vary depending on the specific technique employed. The only critical limitation is that the deposition and annealing temperatures be kept below the crystalline temperature of the perovskite-type oxide. The term "thin film" is used herein to denote that the deposition process provides a highly conformal layer of the amorphous phase of the perovskite-type oxide. Typically, the thickness of the amorphous thin dielectric material ranges from about 25 to about 500 nm. More preferably, the thickness of the amorphous thin film dielectric material of the present invention is in the range of from about 50 to about 200 nm. It should be noted that the above thickness are applicable for other types of insulators that can be used in the present invention as well.

[0044] The dielectric constant, $\epsilon$, of the amorphous thin film dielectric material of the present invention is about 10 or greater. More preferably, the amorphous thin film dielectric material of the present invention has a dielectric constant of from about 14 to about 50. Although the dielectric constants of the amorphous thin film dielectric material of the present invention are lower than the corresponding crystalline phase of the material, the amorphous dielectric materials of the present invention have dielectric constants which are significantly higher than the typical nitrides and oxides of silicon that are used in most integrated circuits. As stated above, the amorphous thin film dielectric material of the present invention can be fabricated at temperatures below 450° C.; therefore, the amorphous thin film material is compatible with BEOL temperature requirements, especially when Al and Cu based metallurgies are employed.

[0045] Metal contacts **18** are composed of any conductive metallic material including, but not limited to: Al, W, Cu, TaN, TaN/α-Ta, or mixtures and alloys thereof. Of the various metallic materials mentioned above, it is highly preferred to utilize TaN or TaN/α-Ta metal contacts since these materials are capable of achieving a sheet resistance of from about 3 to about 300 ohms/sq.

[0046] The metal contacts employed in the present invention are thin films having a thickness of less than about 100 nm and the contacts are formed utilizing conventional deposition processes well known to those skilled in the art. Lithography and etching may be employed in providing patterned metal contacts.

[0047] Insofar as wiring regions **20** are concerned, the wiring regions are composed of the same or different conductive metal as the metal contacts, with preference given to wiring that is composed Al, W and Cu. The wiring region is formed utilizing conventional deposition processes well known in the art and patterning may also be achieved by lithography and etching.

[0048] The inventive resistor designs illustrated in FIGS. **1-3** have low capacitive coupling to the underlying substrate of the IC (not shown) because of its distance from the substrate as compared with typical gate-level defined polysilicon resistors, as well as a small footprint area due to optimized choice of metal contact, e.g., TaN or TaN/α-Ta, thicknesses to obtain optimum sheet resistance and therefore optimum resistor width and length. Moreover, the resistor value is well-controlled and reproducible because the resistivity is principally a function of film thickness, which is easily controlled by the planar plasma vapor deposition prior to processing. This value is also independent of any subsequent processing such as thermal cycling. The above-mentioned features are in sharp contrast to a typical polysilicon resistor whose values are a function of many more factors.

[0049] It emphasized that the above resistor design layouts involve patterning either a thin metal top electrode, a thin metal bottom electrode or both. The present invention utilizes that thin metal patterned metal as a resistor by connecting it in the manner indicated above, i.e., so that current flows laterally through the top electrode, bottom electrode or both electrodes, and any unused electrode is disconnected from the circuit. At the same time, and as will be described in greater detail hereinbelow, other discrete portions of the metal-insulator-metal film stack may be used as a high-capacity capacitor simply by proper design of the under- and overlying metal contacts to the metal wiring levels. When a high-capacity capacitor is desired, it is highly preferred to use the above-mentioned amorphous dielectric material as the insulator.

[0050] The present invention allows integrated R, RC, LC and RLC analog networks to be added to conventional Si-based ICs. Moreover, in some circumstances wherein TaN and TaN/α-Ta are employed as metal contacts, resistors having a size anywhere from 50 ohm (an important value for RF and Ghz applications) up to multi-Kohm range and beyond, all with reasonable resistor length:width ratios of about 20:1, can be obtained.

[0051] Fabrication of the resistors depicted in FIGS. **1-3** may be broadly accomplished through definition and planarization of metal levels through standard damascene processing, deposition and patterning of the MIM film stack, followed with inter-level insulator deposition and standard contact and wiring definition.

[0052] Specifically, the capacitor design in **FIG. 1** may be formed by depositing bottom electrode **12** on the surface of a material layer, e.g., metal layer, insulator, or substrate, of an interconnect structure using the above-mentioned deposition techniques. The material layer of the interconnect structure is not shown in **FIG. 1**, but would be below the MIM film stack shown Insulator film **14** is then deposited, either conventionally or as described above, and top electrode **16** is formed on the material layer utilizing one of the above-mentioned deposition processes. The metal-insulator-metal film stack is then patterned by conventional lithography and etching, e.g., reactive-ion etching, so as to form discrete MIM film stacks on the interconnect structure. It should be noted that some of the discrete MIM film stacks may be used in the present invention as a high-capacitance capacitor, while other discrete MIM film stacks are used as resistors.

[0053] Next, metal contacts **18**, are formed on some of the discrete MIM films stacks utilizing the above-mentioned deposition processes and the contacts may thereafter be patterned by conventional lithography and etching. Wiring regions **20** are then formed, as described above, and patterned by conventional lithography and etching. It should be noted that in the areas surrounding the metal layers and the MIM resistor film, a conventional passivating or insulating material may be formed utilizing conventional techniques well known to those skilled in the art.

[0054] **FIGS. 4A and 4B** are top and side views showing an IC structure of the present invention in which the resistor design of **FIG. 1** is implemented and is formed on top of the last Cu metal level. Specifically, the IC circuit depicted in these figures includes MIM resistor **50**, MIM capacitor **52**, which are formed on a surface of interconnect structure **54**. Interconnect structure **54** includes wiring region **56** which is surrounded by insulator **58**. As shown in **FIG. 4**B, the MIM capacitor is formed on the wiring region of the interconnect structure and the MIM resistor is formed on the insulator layer of the interconnect structure. The structure in **FIG. 4B** also includes BEOL metallurgy **60**, nitride cap **62**, passivation layer **64**, insulator **66**, contact **68**, and metal cap **70** which are formed utilizing conventional techniques that are well known to those skilled in the art.

[0055] Insofar as the design layout of **FIG. 2** is concerned, the structure shown therein is formed by first forming metal contacts **18** on the surface of wiring region **20** utilizing the above mentioned deposition and patterning processes. Wiring region **20** may be part of an interconnect structure or a via or metal line of a damascene structure. Next, the MIM film stack is formed, as described above, and patterning is conducted to provide the discrete resistor MIM film stack.

[0056] The resistor design of **FIG. 3** is formed utilizing the same basic processes as used in forming the design layout of **FIG. 2** except that metal contact **18** is part of a damascene structure and no additional contact formation is required.

[0057] It is further noted that in the various resistor design layouts of the present invention, the pattern for the MIM films for the resistor may be a rectangle, a meander or a tapered section. Moreover, if the resistor is formed in the top electrode of the MIM film stack, contacts and metal wiring to the resistor are generally at the ends of the resistor in the overlying films, and the underlying metal patterns are defined so that contact is not made to the bottom electrode of the MIM resistor film stack. If, on the other hand, the resistor is defined in the bottom electrode, contacts and metal wires are typically defined at the ends of the resistor in the underlying films, and any overlying metal patterns are defined so that contact is not made to the top resistor electrode. In cases wherein an MIM capacitor and resistor are formed on top of the last metal level of an interconnect or damascene structure, contact may be made to the upper electrode by terminal metals themselves through appropriately defined holes in the terminal via level, See **FIG. 4B**.

[0058] While this invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

Having thus described our invention in detail, what we claims as new, and desire to secure by the Letters Patent is:

**1**. An integrated circuit (IC) comprising at least a resistor which is coupled to a metal wiring level of an interconnect or damascene structure through metal contacts, said resistor including a discrete metal-insulator-metal film stack, wherein said metal contacts are in contact with one of said metals of said film stack.

**2**. The IC of claim 1 wherein current flows laterally through the top metal electrode of said metal-insulator-metal film stack, the bottom metal electrode of said metal-insula-

tor-metal film stack, or both electrodes, and any unused electrode is disconnected from the circuit.

**3**. The IC of claim 1 wherein said insulator of said film stack is an amorphous dielectric having a dielectric constant of 10 or greater.

**4**. The IC of claim 3 wherein said amorphous dielectric is a thin film having a thickness of from about 25 to about 500 nm.

**5**. The IC of claim 3 wherein said amorphous dielectric is a perovskite-type oxide having the formula $ABO_3$ wherein B is at least one acidic oxide containing a metal selected from Group IVB, VB, VIB, VIIB or IB of the Periodic Table of Elements, and A is at least one additional cation having a positive formal charge of from about 1 to about 3.

**6**. The IC of claim 5 wherein said perovskite-type oxide is a titanate-based dielectric, a manganate-based material, a cuprate-based material, a tungsten bronze-type niobate, tantalate or titanate, or a layered bismuth-tantalate, -niobate or -titanate.

**7**. The IC of claim 3 wherein said amorphous dielectric is barium strontium titanate, barium titanate, lead zirconium titanate, tantalum titanate, lead lanthanum titanate, strontium titanate, barium strontium niobate, barium zirconium titanate or barium titanium niobate.

**8**. The IC of claim 3 wherein said amorphous dielectric is barium strontium titanate or barium zirconium titanate.

**9**. The IC of claim 1 wherein said insulator is $SiO_2$, $Si_3N_4$ or $Al_2O_3$.

**10**. The IC of claim 1 wherein said metals of said metal-insulator-metal film are composed of the same or different material selected from the group consisting of TaN, Pt, Ir, ruthenium oxide, Al, Au , Cu, Ta, TaSiN and combinations or multilayers thereof.

**11**. The IC of claim 1 wherein said metal contacts are formed above said metal-insulator-metal film stack.

**12**. The IC of claim 1 wherein said metal contacts are formed below said metal-insulator-metal film stack.

**13**. The IC of claim 1 wherein said metal contacts are composed of a conductive metallic material selected from the group consisting of Al, W, Cu, TaN, TaN/α-Ta and mixtures or alloys thereof.

**14**. The IC of claim 13 wherein said metal contacts selected from the group consisting of TaN and TaN/α-Ta.

**15**. The IC of claim 1 wherein said metal wiring level is composed of Al, W, Cu, TaN, TaN/α-Ta and mixtures or alloys thereof.

**16**. The IC of claim 15 wherein said metal wiring level is composed of Al, W or Cu.

**17**. The IC of claim 1 further comprising a capacitor formed adjacent to said resistor, said capacitor comprising the same metal-insulator-metal films as said resistor, but being electrically isolated therefrom.

**18**. The IC of claim 1 wherein said metal contacts and metal wiring are part of a damascene structure.

**19**. A method for forming an integrated circuit (IC) including at least a resistor comprising the steps of:

(a) providing a metal-insulator-metal film stack on at least a material layer of an interconnect structure;

(b) patterning said metal-insulator-metal film stack into discrete metal-insulator-metal film stacks;

(c) forming metal contacts on at least one of said discrete metal-insulator-metal film stacks; and

(d) forming a wiring region connected to said metal contacts.

**20**. The method of claim 19 wherein said insulator of said film stack is an amorphous dielectric having a dielectric constant of 10 or greater.

**21**. The method of claim 20 wherein said amorphous dielectric is formed utilizing deposition and annealing temperatures below 450° C.

**22**. A method for forming an integrated circuit (IC) including at least a resistor comprising the steps of:

(a) forming metal contacts on a surface of a metal wiring region, said metal wiring region is part of an interconnect or damascene structure; and

(b) forming a discrete metal-insulator-metal film stack on at least said metal contacts.

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