

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
2 July 2009 (02.07.2009)

PCT

(10) International Publication Number
WO 2009/082121 A2

(51) International Patent Classification:
H01L 33/00 (2006.01)

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(21) International Application Number:
PCT/KR2008/007475

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(22) International Filing Date:
17 December 2008 (17.12.2008)

(25) Filing Language: Korean

(26) Publication Language: English

(30) Priority Data:
10-2007-0133918
20 December 2007 (20.12.2007) KR

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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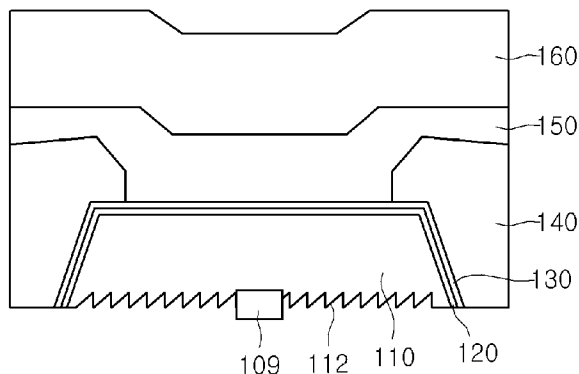
Published:

— *without international search report and to be republished upon receipt of that report*

(54) Title: SEMICONDUCTOR LIGHT EMITTING DEVICE AND METHOD OF FABRICATING THE SAME

[Fig. 1]

100



(57) Abstract: Provided are a semiconductor light emitting device and a method of fabricating the same. The semiconductor light emitting device comprises: a light emitting structure comprising a first conductive semiconductor layer, an active layer on the first conductive semiconductor layer, and a second conductive semiconductor layer on the active layer; a nitride semiconductor layer on an outer periphery of the second conductive semiconductor layer; and an ohmic layer on the second conductive semiconductor layer.

Description

SEMICONDUCTOR LIGHT EMITTING DEVICE AND METHOD OF FABRICATING THE SAME

Technical Field

- [1] The present disclosure relates to a semiconductor light emitting device and a method of fabricating the same.

Background Art

- [2] Group III-V nitride semiconductors have been variously applied to an optical device such as blue and green light emitting diodes (LED), a high speed switching device, such as a MOSFET (Metal Semiconductor Field Effect Transistor) and an HEMT (Hetero junction Field Effect Transistors), and a light source of a lighting device or a display device. In particular, light emitting devices using group III nitride semiconductors have a direct transition-type bandgap corresponding to the range from visible rays to ultraviolet rays, and can perform high-efficiency light emission.
- [3] The nitride semiconductor is mainly used for the LED (Light Emitting Diode) or an LD (laser diode), and studies have been continuously conducted to improve the fabrication process or light efficiency of the nitride semiconductor.

Disclosure of Invention

Technical Problem

- [4] Embodiments provide a semiconductor light emitting device comprising a nitride semiconductor layer around a light emitting structure, and a method of fabricating the same.
- [5] Embodiments also provide a semiconductor light emitting device comprising an active layer on an outer periphery of a light emitting structure, and a method for manufacturing the same.

Technical Solution

- [6] An embodiment provides a semiconductor light emitting device comprising: a light emitting structure comprising a first conductive semiconductor layer, an active layer on the first conductive semiconductor layer, and a second conductive semiconductor layer on the active layer; a nitride semiconductor layer on an outer periphery of the second conductive semiconductor layer; and an ohmic layer on the second conductive semiconductor layer.
- [7] An embodiment provides a semiconductor light emitting device comprising: a first conductive semiconductor layer; an active layer on top and side surfaces of the first conductive semiconductor layer; a second conductive semiconductor layer on top and side surfaces of the active layer; a nitride semiconductor layer on an outer periphery of

the second conductive semiconductor layer; and an ohmic layer on the second conductive semiconductor layer and the nitride semiconductor layer.

- [8] An embodiment provides a method of fabricating a semiconductor light emitting device comprising: forming a first conductive semiconductor layer on a substrate; sequentially forming an active layer and a second conductive semiconductor layer on the first conductive semiconductor layer; forming a nitride semiconductor layer in an outer periphery of the second conductive semiconductor layer; forming an ohmic layer on the second conductive semiconductor layer and the nitride semiconductor layer; forming a conductive support member on the ohmic layer; and removing the substrate.

Advantageous Effects

- [9] Embodiments can enhance the luminous efficiency of the semiconductor light emitting device.
- [10] Embodiments can enhance the fabrication process of the semiconductor light emitting device.
- [11] Embodiments can separate the light emitting structure from a metal material by a nitride semiconductor layer formed around an outer periphery of the light emitting structure.

Brief Description of Drawings

- [12] FIG. 1 is a side sectional view of a semiconductor light emitting device according to a first embodiment.
- [13] FIGS. 2 through 8 are sectional views illustrating a method of fabricating a semiconductor light emitting device according to a first embodiment.
- [14] FIGS. 9 through 12 are sectional views illustrating a method of fabricating a semiconductor light emitting device according to a second embodiment.

Best Mode for Carrying out the Invention

- [15] Hereinafter, a semiconductor light emitting device and a method of fabricating the same according to the embodiment will be described with reference to the accompanying drawings.
- [16] In the description of the embodiment, it will be understood that, when a layer (or film), a region, a pattern, or a structure is referred to as being "on(above/over/upper)" or "under(below/down/lower)" another substrate, another layer (or film), another region, another pad, or another pattern, it can be directly on the other substrate, layer (or film), region, pad or pattern, or intervening layers may also be present.
- [17] FIG. 1 is a side sectional view of a semiconductor light emitting device according to a first embodiment. In the description of the first embodiment, the criterion for "on" or "under" of each layer will be described with reference to the relevant drawings. The thickness of each layer is merely exemplary and is not limited by the thickness il-

lustrated in the drawings.

- [18] Referring to FIG. 1, a semiconductor light emitting device 100 comprises a first conductive semiconductor layer 110, an active layer 120, a second conductive semiconductor layer 130, a nitride semiconductor layer 140, an ohmic layer 150, and a conductive support member 160.
- [19] The first conductive semiconductor layer 110 is doped with a first conductive dopant. The first conductive semiconductor layer 110 may be formed of one of group III-V compound semiconductors, for example, GaN, InN, AlN, InGaN, AlGaN, InAlGaN, and AlInN. When the first conductive semiconductor layer 110 is an N-type semiconductor layer, the first conductive dopant is an N-type dopant, such as Si, Ge, Sn, Se, or Te.
- [20] A first electrode 109 is formed under the first conductive semiconductor layer 110. The first electrode 109 may be formed in a predetermined pattern, but the present invention is not limited thereto. Also, a roughness 112 having a predetermined shape may be formed under the first conductive semiconductor layer 110. The roughness 112 may comprise a pyramid-shaped pattern or a concave-convex pattern.
- [21] The first conductive semiconductor layer 110 may be formed to a predetermined thickness in a polyhedral shape such as a hexahedron, a polygonal prism shape, a cylinder shape, or a random shape. Furthermore, the side of the first conductive semiconductor layer 110 may be formed in a right angle shape with respect to a horizontal line or may be sloped.
- [22] The active layer 120 is formed on the first conductive semiconductor layer 110. The active layer 120 is formed along the top and side surfaces of the first conductive semiconductor layer 110. The active layer 120 may have a single quantum well structure or a multiple quantum well structure. The active layer 120 may be formed of an InGaN well layer/GaN barrier layer or an AlGaN well layer/GaN barrier layer by using group III-V compound semiconductors.
- [23] The active layer 120 is formed of a material having a bandgap energy according to a light wavelength at which light is emitted. For example, in the case of a blue light emission having a wavelength range from 460 nm to 470 nm, the active layer 120 may be formed in a single or multiple quantum well structure at a period of an InGaN well layer/GaN barrier layer. The active layer 120 may comprise a material emitting a colored light such as a blue wavelength light, a red wavelength light, and a green wavelength light. A conductive clad layer may be formed on an/or under the active layer 120. The conductive clad layer comprises an AlGaN-based layer. Furthermore, another semiconductor layer may be stacked on and/or under the active layer 120, but the present invention is not limited thereto.
- [24] At least one second conductive semiconductor layer 130 is formed on the active layer

120. The second conductive semiconductor layer 130 is formed along the top and side surfaces of the active layer 120. The second conductive semiconductor layer 130 may be formed with a semiconductor layer doped with a second conductive dopant. The second conductive semiconductor layer 130 may be formed of one of group III-V compound semiconductors, for example, GaN, InN, AlN, InGaN, AlGaIn, InAlGaIn, and AlInN. When the second conductive semiconductor layer 130 is a P-type semiconductor layer, the second conductive dopant may comprise a P-type dopant, such as Mg, Zn, Ca, Sr, or Ba.

- [25] In addition, an N-type semiconductor layer (not shown) or a P-type semiconductor layer (not shown) may be formed on the second conductive semiconductor layer 130. The first conductive semiconductor layer 110, the active layer 120, and the second conductive semiconductor layer 130 may be defined as a light emitting structure. The light emitting structure may be formed in an N-P junction structure, a P-N junction structure, an N-P-N junction structure, or a P-N-P junction structure.
- [26] The active layer 120 is disposed along the top and side surfaces of the first conductive semiconductor layer 110 and the second conductive semiconductor layer 130. Accordingly, the luminous efficiency of the semiconductor light emitting device 100 may be enhanced.
- [27] The nitride semiconductor layer 140 is formed along an outer periphery of the second conductive semiconductor layer 130. The nitride semiconductor layer 140 may be formed in a portion of the side surface of the second conductive semiconductor layer 130, or may be formed in a whole side surface of the second conductive semiconductor layer 130, or may extend from the side surface to a portion of the top surface of the second conductive semiconductor layer 130.
- [28] The nitride semiconductor layer 140 may be doped with a first conductive dopant or a second conductive dopant and may be formed of one of group III-V compound semiconductors, for example, GaN, InN, AlN, InGaIn, AlGaIn, InAlGaIn, and AlInN. Also, the nitride semiconductor layer 140 may not be doped with a conductive dopant.
- [29] The nitride semiconductor layer 140 is formed in an outer periphery of the light emitting structure 110, 120 and 130 and protects the outer periphery of the light emitting structure 110, 120 and 130.
- [30] The ohmic layer 150 may be formed on the second conductive semiconductor layer 130, or may be formed on the second conductive semiconductor layer 130 and the nitride semiconductor layer 140.
- [31] The ohmic layer 150 ohmic-contacts the second conductive semiconductor layer 130 and the nitride semiconductor layer 140, and serves as a metal seed for the conductive support member 160.
- [32] The ohmic layer 150 may be formed of at least one or selective mixture of indium tin

oxide (ITO), Pt, Ni, Au, Rh, Pd, Ag, Al, and Ir. The ohmic layer 150 may be deposited in a single layer or multi layer. The ohmic layer 150 may be formed of, but is not limited to, a material having an ohmic characteristic, a reflection characteristic, and a metal seed characteristic.

- [33] The conductive support member 160 may be selectively formed on the ohmic layer 150 by using a conductive material, for example, copper, gold, or carrier wafer (e.g., Si, Ge, GaAs, ZnO, SiC, etc.). Also, the conductive support member 160 may be formed using a copper plating or wafer bonding technology, but the present invention is not limited thereto. The top surface of the conductive support member 160 may be flattened through a planarization process.
- [34] According to the first embodiment, the surface area of the active layer 120 can be increased by forming the first conductive semiconductor layer 110 in a polyhedral shape or a prism shape. Accordingly, the luminous efficiency of the semiconductor light emitting device 100 can be enhanced.
- [35] Furthermore, end portions of the active layer 120 and the second conductive semiconductor layer 130 may be exposed in the downward direction of the first conductive semiconductor layer 110.
- [36] Moreover, the nitride semiconductor layer 140 is formed along the outer periphery of the second conductive semiconductor layer 130 and protects the outer periphery of the light emitting structure 110, 120 and 130. For example, the nitride semiconductor layer 140 separates an outside gap between the light emitting structure 110, 120 and 130 and the ohmic layer 150 or the conductive support member 160. The outside gap between the light emitting structure 110, 120 and 130 and the ohmic layer 150 or the conductive support member 160 prevents the outside of the light emitting structure 110, 120 and 130 from contacting a metal component.
- [37] FIGS. 2 through 8 are sectional views illustrating a method of fabricating a semiconductor light emitting device according to a first embodiment.
- [38] Referring to FIG. 2, first mask patterns 103 are formed in a chip boundary region on a substrate 101. The chip boundary region may be an outer region of a chip or a region between light emitting structures.
- [39] The substrate 101 may be selected from the group consisting of a sapphire substrate (Al_2O_3), GaN, SiC, ZnO, Si, GaP, InP, and GaAs. The chip boundary region may be defined as a region between chips or a region between the light emitting structures.
- [40] The first mask pattern 103 is formed along the chip boundary region. The first mask pattern 103 may be formed of, but is not limited to, SiO_2 , SiO_x , SiN_{x2} , SiN_x , or SiO_xN_y . The first mask pattern 103 is formed to a predetermined thickness (for example, 1,000 Å to 5,000 Å).
- [41] A buffer layer (not shown) and/or an undoped semiconductor layer (not shown) may

be formed on the substrate 101. The buffer layer (not shown) may be formed of group III-V compound semiconductors, for example, GaN, InN, AlN, InGaN, AlGaN, InAlGaN, or AlInN. A dopant may be doped into the buffer layer (not shown). The undoped semiconductor layer (not shown) may be implemented with an undoped GaN-based layer. In this case, the first mask pattern 103 may be formed before or after forming the buffer layer (not shown) and/or the undoped semiconductor layer (not shown). Such a structure may be modified.

- [42] A first conductive semiconductor layer 110 is formed on the substrate 101 between the first mask patterns 103. A region for the light emitting structure may be defined between the first mask patterns 103.
- [43] The first conductive semiconductor layer 110 may be doped with a first conductive dopant and may be formed of one of group III-V compound semiconductors, for example, GaN, InN, AlN, InGaN, AlGaN, InAlGaN, and AlInN. When the first conductive semiconductor layer 110 is an N-type semiconductor layer, the first conductive dopant is an N-type dopant, such as Si, Ge, Sn, Se, or Te.
- [44] The first conductive semiconductor layer 110 may be formed between the first mask patterns 103 in a predetermined shape, for example, a polyhedral shape such as a hexahedron, a cylinder shape, a polygonal prism shape, or a random shape, but the present invention is limited thereto. The first conductive semiconductor layer 110 may be formed in a thickness range of 4.0 μm to 7.0 μm .
- [45] The outer periphery of the first conductive semiconductor layer 110 may be sloped or perpendicular to the top surface of the substrate.
- [46] An active layer 120 is formed on the first conductive semiconductor layer 110. The active layer 120 is formed along the top and side surfaces of the first conductive semiconductor layer 110. The active layer 120 may have a single quantum well structure or a multiple quantum well structure. The active layer 120 may be formed of, but is not limited to, an InGaN well layer/GaN barrier layer or an AlGaN well layer/GaN barrier layer by using group III-V compound semiconductors.
- [47] A second conductive semiconductor layer 130 is formed on the active layer 120. The second conductive semiconductor layer 130 is formed along the top and side surfaces of the active layer 120. The second conductive semiconductor layer 130 may be formed with a semiconductor layer doped with a second conductive dopant. The second conductive semiconductor layer 130 may be formed of one of group III-V compound semiconductors, for example, GaN, InN, AlN, InGaN, AlGaN, InAlGaN, or AlInN. When the second conductive semiconductor layer 130 is a P-type semiconductor layer, the second conductive dopant may comprise a P-type dopant, such as Mg, Zn, Ca, Sr, or Ba.
- [48] End portions of the first conductive semiconductor layer 110, the active layer 120,

and the second conductive semiconductor layer 130 may be formed on the first mask patterns 103.

- [49] In addition, an N-type semiconductor layer (not shown) or a P-type semiconductor layer (not shown) may be formed on the second conductive semiconductor layer 130. The first conductive semiconductor layer 110, the active layer 120, and the second conductive semiconductor layer 130 may be defined as a light emitting structure. The light emitting structure may be formed in one of an N-P junction structure, a P-N junction structure, an N-P-N junction structure, and a P-N-P junction structure.
- [50] Since the light emitting structure 110, 120 and 130 has the top surface and the outer periphery, the light emitting area can be increased.
- [51] After forming the second conductive semiconductor layer 130, the first mask patterns 103 are removed by an etching process (e.g., a wet etching process). The first mask pattern 103 may be removed in a process of separating the substrate 101, and the removal order of the first mask patterns 103 may be changed.
- [52] Referring to FIGS. 2 and 3, after the first mask patterns 103 are removed, second mask patterns 135 are formed in an inner region on the second conductive semiconductor layer 130. The second mask patterns 135 may be formed in an upper inner side of the second conductive semiconductor layer 130 or regions other than the chip boundary region.
- [53] The second mask patterns 135 may be formed of, but are not limited to, SiO_2 , SiO_x , $\text{SiN}_{x/2}$, SiN_x , or SiO_xN_y .
- [54] The nitride semiconductor layer 140 is formed in a region where the second mask patterns 135 are not formed. The nitride semiconductor layer 140 is formed on the substrate 101 and may be formed up to the side of the second conductive semiconductor layer 130 and a portion of the top surface thereof. The nitride semiconductor layer 140 may be formed in a portion of the side of the second conductive semiconductor layer 130 on the substrate 101.
- [55] Furthermore, the bottom of the nitride semiconductor layer 140 may be formed in the first mask pattern region 104.
- [56] The nitride semiconductor layer 140 may be formed to a thickness equal to or greater than that of the light emitting structure 110, 120 and 130, for example, 2 μm to 8 μm . Also, the nitride semiconductor layer 140 may be formed in a range of $\pm 2\sim 8$ μm with respect to the thickness of the light emitting structure 110, 120 and 130.
- [57] The nitride semiconductor layer 140 may be doped with a first conductive dopant or a second conductive dopant and may be formed of one of group III-V compound semiconductors, for example, GaN, InN, AlN, InGaN, AlGaIn, InAlGaIn, and AlInN. Also, the nitride semiconductor layer 140 may be formed of semiconductors which are not doped with a conductive dopant.

- [58] The nitride semiconductor layer 140 is formed in an outer periphery of the light emitting structure 110, 120 and 130 and thus protects the outer periphery of the light emitting structure 110, 120 and 130.
- [59] Since the nitride semiconductor layer 140 is formed in the boundary region between the light emitting structures 110, 120 and 130, it is unnecessary to perform a process of forming and removing a separate passivation layer.
- [60] After the nitride semiconductor layer 140 is formed, the second mask patterns 135 are removed by a wet etching process and/or a dry etching process.
- [61] Referring to FIGS. 3 and 4, after the second mask patterns 135 are removed, an ohmic layer 150 is formed on the second conductive semiconductor layer 130 and the nitride semiconductor layer 140.
- [62] The ohmic layer 150 may be formed of at least one or selective mixture of indium tin oxide (ITO), Pt, Ni, Au, Rh, Pd, Ag, Al, and Ir. The ohmic layer 150 may be deposited in a single layer or multi layer. The ohmic layer 150 may be formed of, but is not limited to, a material having an ohmic characteristic, a reflection characteristic, and a metal seed characteristic.
- [63] Referring to FIGS. 4 and 5, a conductive support member 160 may be selectively formed on the ohmic layer 150. The conductive support member 160 may be formed of a conductive material, for example, copper, gold, or carrier wafer (e.g., Si, Ge, GaAs, ZnO, SiC, etc.) to a predetermined thickness (for example, 30 μm to 150 μm). The top surface of the conductive support member 160 may be flattened through a planarization process. The planarization process may be performed by a cutting or polishing process.
- [64] Referring to FIGS. 5 and 6, the substrate 101 is removed by a physical method and/or a chemical method. The physical method may separate the substrate 101 by a laser lift off (LLO) method, and the chemical method can separate the buffer layer and the substrate 101 by injecting a wet etchant into the buffer layer (not shown).
- [65] When the substrate 101 is removed, the bottoms of the first conductive semiconductor layer 110 and the nitride semiconductor layer 140 are exposed. At this point, a surface pretreatment process is performed on the first conductive semiconductor layer 110 and the nitride semiconductor layer 140. The surface pretreatment thickness may remove more than the thickness of the first mask pattern 103 of FIG. 2.
- [66] The surface pretreatment process may be performed by a wet etching process using BOE, HF, HCl or KOH solution and/or a dry etching process such as ICP and RIE. At this point, the bottom of the first conductive semiconductor layer 110 is etched to form a roughness 112. Also, a roughness (not shown) may be formed on the nitride semiconductor layer 140. The size and shape of the roughness 112 may be different according to etching degree, and the roughness 112 may not be formed.

- [67] Referring to FIGS. 7 and 8, a first electrode 109 is formed on the bottom surface of the first conductive semiconductor layer 110 in a predetermined pattern. That is, after the substrate is removed from the bottom surface of the first conductive semiconductor layer 110, the first conductive semiconductor layer 110 is arranged so that the bottom surface of the first conductive semiconductor layer 110 turn upward. The first electrode 109 may be formed on the first conductive semiconductor layer 110.
- [68] After the first electrode 109 is formed, the chip boundry region comprising the conductive support member 160 and the nitride semiconductor layer 140 is separated along a chip size by using a laser scribe. In this case, a separate dry etching may not be performed on the side of the chip. Moreover, the dry etching can be performed according to need.
- [69] The light emitting structure 110, 120 and 130 comprises the first conductive semiconductor layer 110, the active layer 120, and the second conductive semiconductor layer 130, and is disposed in an inner region defined by the nitride semiconductor layer 140 and the ohmic layer 150.
- [70] Furthermore, the surface area of the active layer 120 can be increased by forming the first conductive semiconductor layer 110 in a polyhedral shape or a prism shape. Accordingly, the luminous efficiency of the semiconductor light emitting device 100 can be enhanced.
- [71] Furthermore, end portions of the active layer 120 and the second conductive semiconductor layer 130 may be exposed in the downward direction of the first conductive semiconductor layer 110.
- [72] Moreover, the nitride semiconductor layer 140 is formed along the outer periphery of the second conductive semiconductor layer 130 and protects the outer periphery of the light emitting structure 110, 120 and 130.
- [73] FIGS. 9 through 12 are sectional views illustrating a method of fabricating a semiconductor light emitting device according to a second embodiment. In the first and second embodiments, like reference numerals refer to like elements and duplicate description will be omitted.
- [74] Referring to FIG. 9, a buffer layer 105, an undoped semiconductor layer 106, and a first conductive semiconductor layer 110 are sequentially formed on the substrate 101. The buffer layer 105, the undoped semiconductor layer 106, and the first conductive semiconductor layer 110 may be formed to a thickness of 1 μ m to 5 μ m.
- [75] The buffer layer 105 may be formed one of group III-V compound semiconductors, for example, GaN, InN, AlN, InGaN, AlGaN, InAlGaN, and AlInN and may be doped with a dopant. The undoped semiconductor layer 106 may be implemented with an undoped GaN-based layer.
- [76] Referring to FIGS. 9 and 10, a dry etching process (e.g., ICP) is performed on a chip

boundary region 108 on the substrate 101. in this case, the top surface of the substrate 101 is exposed in the chip boundary region 108. At this point, sides of the buffer layer 105, the undoped semiconductor layer 106, and the first conductive semiconductor layer 110 may be etched to be sloped or perpendicular to the top surface of the substrate 101.

- [77] A 1A conductive semiconductor layer 110A is re-grown on the first conductive semiconductor layer 110 and the substrate 101. The 1A conductive semiconductor layer 110A is doped with a first conductive dopant and may be formed of group III-V compound semiconductor. The 1A conductive semiconductor layer 110A may be implemented with an N-type semiconductor layer.
- [78] The 1A conductive semiconductor layer 110A is formed from the top surface of the substrate 101 to the top surface of the first conductive semiconductor layer 110. The 1A conductive semiconductor layer 110A may be formed to have a height difference along the chip boundary area and the first conductive semiconductor layer 110.
- [79] Referring to FIGS. 10 and 11, an active layer 121 and a second conductive semiconductor layer 131 are formed on the 1A conductive semiconductor layer 110A. The active layer 121 and the second conductive semiconductor layer 131 are formed along the curved surface of 1A conductive semiconductor layer 110A. That is, the active layer 121 and the second conductive semiconductor layer 131 may be formed along the inner upper surface, side surface and outer top surface of the 1A conductive semiconductor layer 110A.
- [80] Second mask patterns (not shown, 135 in FIG. 3) are formed on the second conductive semiconductor layer 131, and a nitride semiconductor layer 140 is formed on the second conductive semiconductor layer 131 of the chip boundary area. The second mask patterns (not shown) are removed.
- [81] An ohmic layer 150 and a conductive support member 160 are formed on the second conductive semiconductor layer 131 and the nitride semiconductor layer 140.
- [82] Referring to FIGS. 11 and 12, the substrate 101 may be removed by a physical method and/or a chemical method. A pre-treatment is performed on the surface of a resulting structure where the substrate is removed. The buffer layer (105 in FIG. 9) and the undoped semiconductor layer (106 in FIG. 9) are removed by the pre-treatment, and the bottom surface of the first conductive semiconductor layer 110 and the outer bottom surface of the 1A conductive semiconductor layer 110A are exposed.
- [83] A roughness 112 is formed on the bottom surface of the first conductive semiconductor layer 110, and a first electrode 109 is formed. That is, after the substrate is removed from the bottom surface of the first conductive semiconductor layer 110, the first conductive semiconductor layer 110 is arranged so that the bottom surface of the first conductive semiconductor layer 110 turn upward. The first electrode 109 may be

formed on the first conductive semiconductor layer 110. Accordingly, a semiconductor light emitting device 100B separated in a chip size is fabricated. The light emitting structure comprises the first conductive semiconductor layer 110, the 1A conductive semiconductor layer 110A, the active layer 121, and the second conductive semiconductor layer 131, and the outer periphery of the semiconductor light emitting structure extends up to the bottom of the nitride semiconductor layer 140.

[84] In the semiconductor light emitting device 100B according to the second embodiment, the 1A conductive semiconductor layer 110A is formed on the first conductive semiconductor layer 110, and the 1A conductive semiconductor layer 110A extends outward in a stepped shape. Accordingly, since the 1A conductive semiconductor layer 110A, the active layer 120, and the second conductive semiconductor layer 130 extend outward in the stepped shape, the luminous efficiency can be enhanced.

[85] Furthermore, since the nitride semiconductor layer is formed around the chip, it is unnecessary to form a passivation layer such as a separate insulation layer. Moreover, since the nitride semiconductor layer is formed at the outside of the light emitting structure, the fabrication process can be simplified without reducing the light emitting area.

[86] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

Industrial Applicability

[87] Embodiments can provide a semiconductor light emitting device.

[88] Embodiments can increase the light emitting area of the semiconductor light emitting device.

[89] Embodiments can enhance the fabrication process of the semiconductor light emitting device.

Claims

- [1] A semiconductor light emitting device comprising:
a light emitting structure comprising a first conductive semiconductor layer, an active layer on the first conductive semiconductor layer, and a second conductive semiconductor layer on the active layer;
a nitride semiconductor layer on an outer periphery of the second conductive semiconductor layer; and
an ohmic layer on the second conductive semiconductor layer.
- [2] The semiconductor light emitting device according to claim 1, comprising a conductive support member on the ohmic layer.
- [3] The semiconductor light emitting device according to claim 2, wherein the ohmic layer extends on the nitride semiconductor layer.
- [4] The semiconductor light emitting device according to claim 1, wherein the first conductive semiconductor layer has a thickness of 4 μm or more, and the active layer and the second conductive semiconductor layer is formed on the first conductive semiconductor layer and around an outer periphery of the first conductive semiconductor layer.
- [5] The semiconductor light emitting device according to claim 1, wherein the first conductive semiconductor layer comprises one of a polyhedral shape, a prism shape, and a random shape having a predetermined thickness.
- [6] The semiconductor light emitting device according to claim 1, wherein an upper side and lower side of the light emitting structure is formed with the other size.
- [7] The semiconductor light emitting device according to claim 1, comprising a roughness and a first electrode under the first conductive semiconductor layer.
- [8] The semiconductor light emitting device according to claim 1, wherein outer end portions of the active layer and the second conductive semiconductor layer are exposed in a downward direction of the first conductive semiconductor layer.
- [9] The semiconductor light emitting device according to claim 1, comprising a 1A conductive semiconductor layer between the first conductive semiconductor layer and the active layer.
- [10] A semiconductor light emitting device comprising:
a first conductive semiconductor layer;
an active layer on top and side surfaces of the first conductive semiconductor layer;
a second conductive semiconductor layer on top and side surfaces of the active layer;
a nitride semiconductor layer on an outer periphery of the second conductive

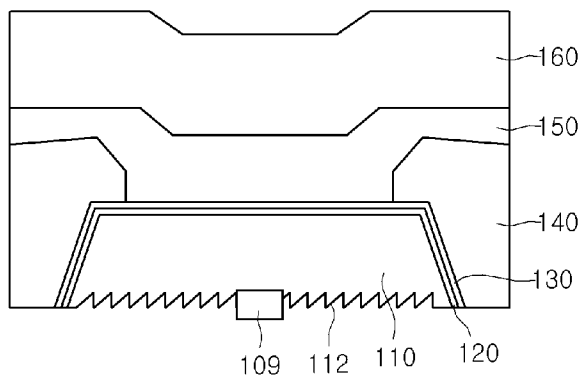
semiconductor layer; and

an ohmic layer on the second conductive semiconductor layer and the nitride semiconductor layer.

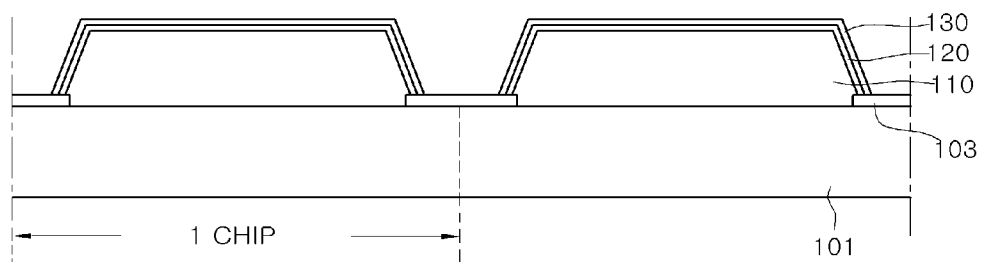
- [11] The semiconductor light emitting device according to claim 10, comprising a conductive support member on the ohmic layer, wherein the ohmic layer comprises at least one or mixture of indium tin oxide (ITO), Pt, Ni, Au, Rh, Pd, Ag, Al, and Ir.
- [12] The semiconductor light emitting device according to claim 10, wherein the first conductive semiconductor layer is formed to a thickness of 4 μm to 7 μm , and the nitride semiconductor layer is formed to a thickness of 2 μm to 8 μm .
- [13] The semiconductor light emitting device according to claim 10, comprising a 1A conductive semiconductor layer on the first conductive semiconductor layer, wherein the 1A conductive semiconductor layer, the active layer, and the second conductive semiconductor layer extend outward from the top surface of the first conductive semiconductor layer in a stepped shape.
- [14] A method of fabricating a semiconductor light emitting device, the method comprising:
forming a first conductive semiconductor layer on a substrate;
sequentially forming an active layer and a second conductive semiconductor layer on the first conductive semiconductor layer;
forming a nitride semiconductor layer in an outer periphery of the second conductive semiconductor layer;
forming an ohmic layer on the second conductive semiconductor layer and the nitride semiconductor layer;
forming a conductive support member on the ohmic layer; and
removing the substrate.
- [15] The method according to claim 14, comprising
forming a 1A conductive semiconductor layer between the first conductive semiconductor layer and the active layer.
- [16] The method according to claim 14, comprising:
performing a surface treatment on the first conductive semiconductor layer and the nitride semiconductor layer to form a roughness; and
forming a first electrode under the first conductive semiconductor layer.

[Fig. 1]

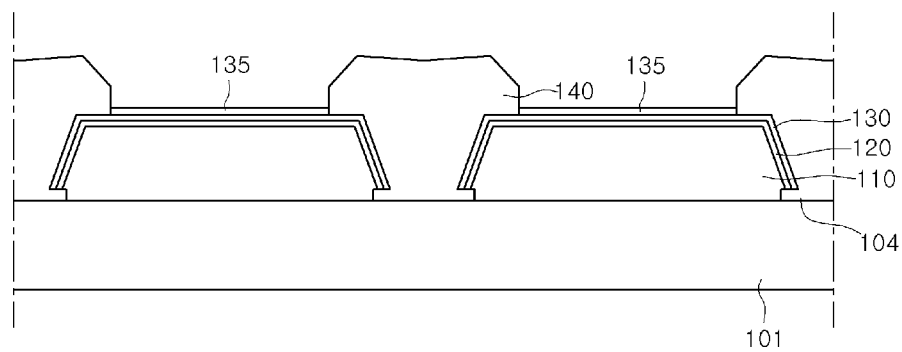
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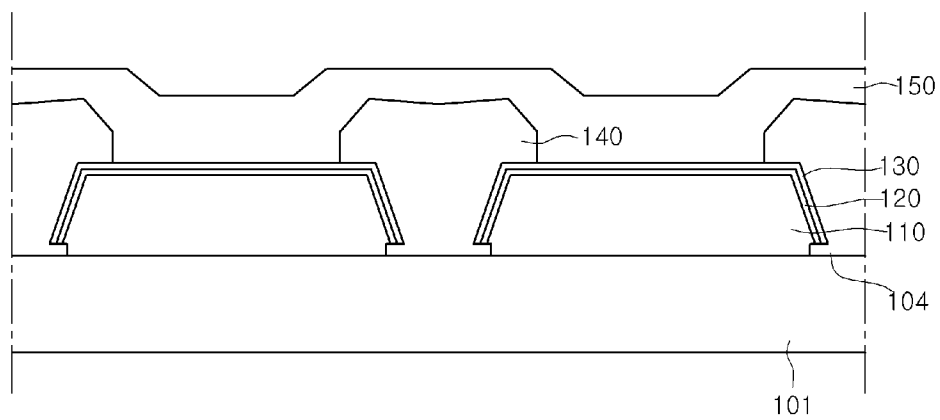
[Fig. 2]



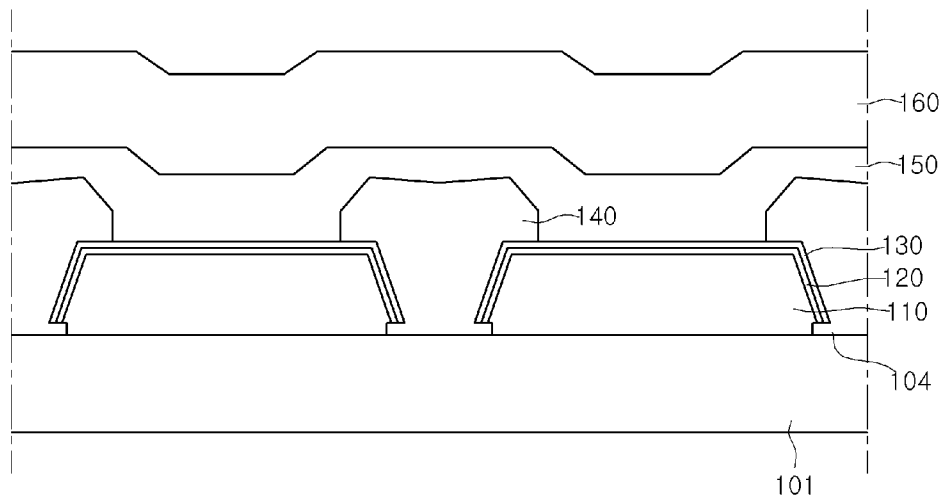
[Fig. 3]



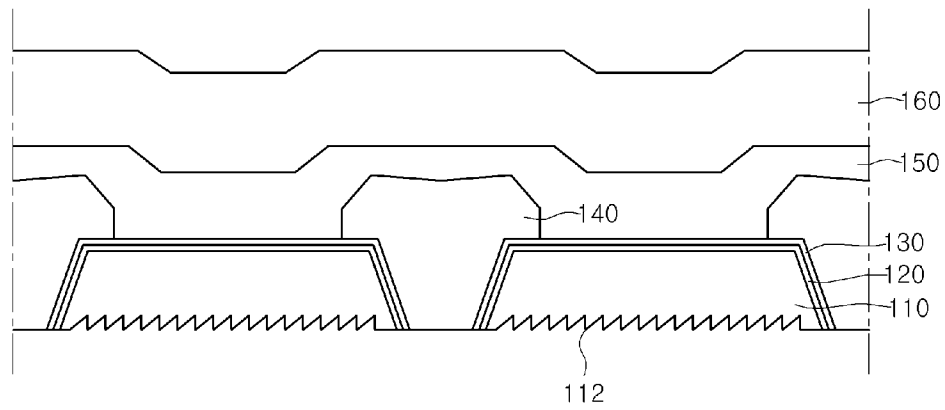
[Fig. 4]



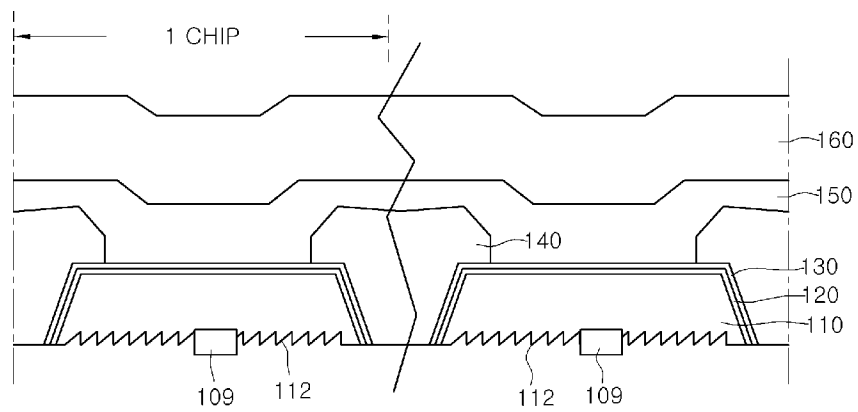
[Fig. 5]



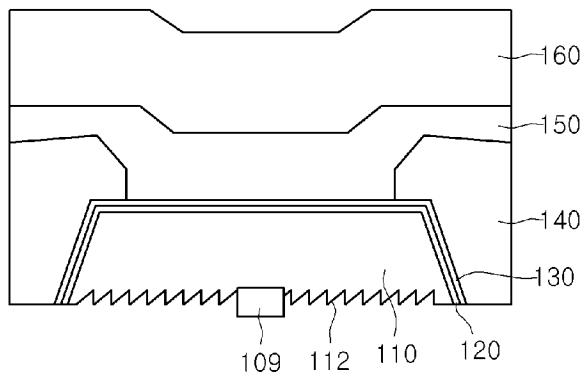
[Fig. 6]



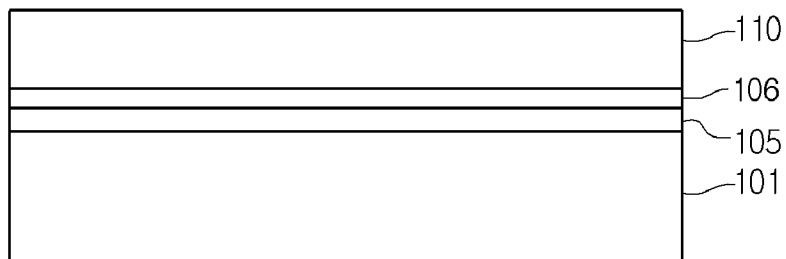
[Fig. 7]



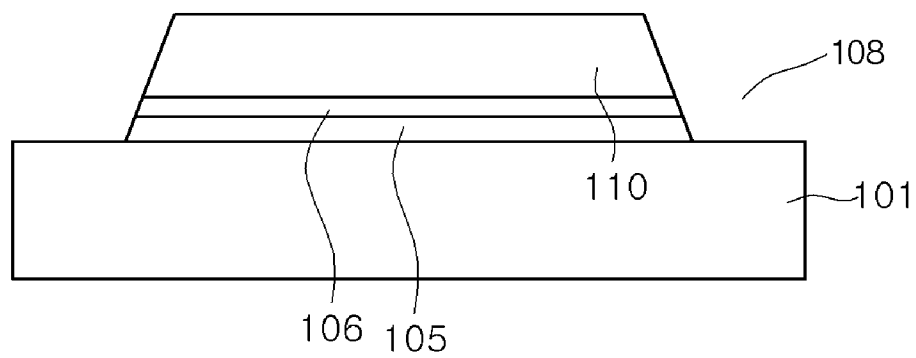
[Fig. 8]

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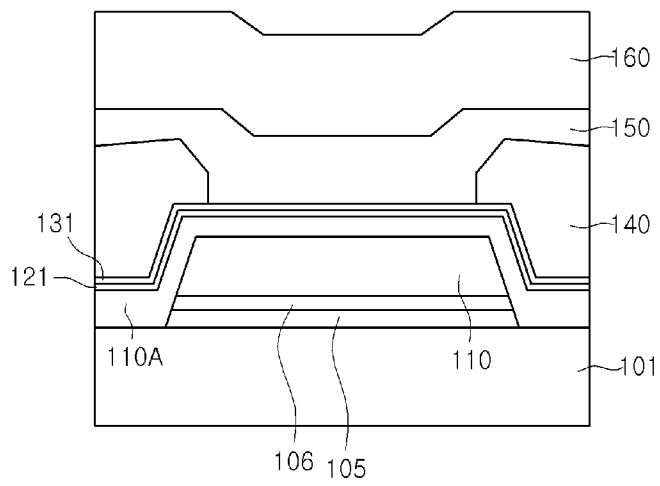
[Fig. 9]



[Fig. 10]



[Fig. 11]



[Fig. 12]

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