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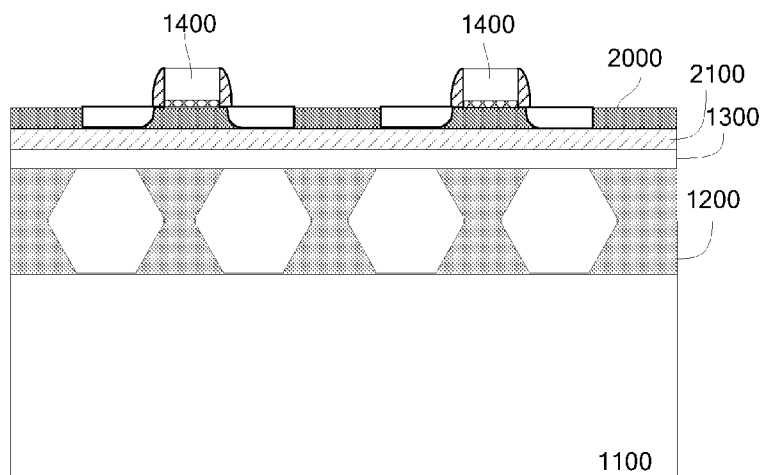


Fig. 1

(57) Abstract: A semiconductor structure and a method for forming the same are provided. The semiconductor structure comprises: a Si substrate (1100); a plurality of convex structures (1200) formed on the Si substrate (1100), in which every two adjacent convex structures (1200) are separated by a cavity in a predetermined pattern, and the cavity between every two adjacent convex structures (1200) is less than 50nm in width; a first semiconductor film (1300), in which the first semiconductor film (1300) is formed between the every two adjacent convex structures (1200) and connected with tops of the every two adjacent convex structures (1200); a buffer layer (2100) formed on the first semiconductor film (1300); and a high-mobility III-V compound semiconductor layer (2000) formed on the buffer layer (2100).



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SEMICONDUCTOR STRUCTURE AND METHOD FOR FORMING THE SAME

FIELD

The present disclosure relates to a semiconductor manufacture and design, and
5 more particularly to a semiconductor structure and a method for forming the same.

BACKGROUND

For a long time, in order to achieve a higher chip density, a faster working speed and a lower power consumption, a feature size of a MOSFET (metal-oxide-semiconductor
10 field effect transistor) is continuously scaled down according to Moore's law, and a working speed of the MOSFET is faster and faster. Currently, the feature size of the MOSFET has reached a nanometer level. However, a serious challenge is an emergence of a short-channel effect, such as a subthreshold voltage roll-off (V_t roll-off), a DIBL (drain-induced barrier lowering) and a source-drain punch through, thus increasing an
15 off-state leakage current. Therefore, a performance of the MOSFET may be deteriorated. In addition, for an III-V compound device, there is a large lattice mismatch between III-V compound materials and Si materials, so that a dislocation density may be higher. Therefore, a buffer layer, for example, a GaAs layer, may need to be formed between the III-V compound materials and the Si materials, which may not only improve an interface
20 state between the III-V compound materials and the Si materials, but also alleviate a lattice mismatch between the III-V compound materials and the Si materials. However, the conventional buffer layer is thick, and a defect density is high, thus further deteriorating the performance of the MOSFET.

25 SUMMARY

The present disclosure is aimed to solve at least one of the above mentioned technical problems.

According to an aspect of the present disclosure, a semiconductor structure is provided. The semiconductor structure comprises: a Si substrate; a plurality of convex
30 structures formed on the Si substrate, in which every two adjacent convex structures are separated by a cavity in a predetermined pattern, and the cavity between every two

adjacent convex structures is less than 50nm in width; a first semiconductor film formed on the plurality of convex structures, wherein a part of the first semiconductor film on the cavity is floated and separated from the Si substrate; a buffer layer formed on the first semiconductor film; and a high-mobility III-V compound semiconductor layer formed on the buffer layer.

In one embodiment, the semiconductor structure further comprises: a gate stack formed on the high-mobility III-V compound semiconductor layer; and a source region and a drain region formed in the high-mobility III-V compound semiconductor layer and on sides of the gate stack respectively.

In one embodiment, a width of each convex structure increases gradually from a middle part thereof to a top part thereof so that a cavity between top parts of two adjacent convex structures is less than that between middle parts of the two adjacent convex structures.

In one embodiment, a material forming each convex structure comprises $\text{Si}_{1-x}\text{C}_x$, $\text{Si}_y\text{Ge}_{1-y}$ or Ge, and the first semiconductor film is a $\text{Si}_{1-x}\text{C}_x$ layer, a $\text{Si}_y\text{Ge}_{1-y}$ layer or a Ge layer.

In one embodiment, each convex structure comprises a bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $\text{Si}_y\text{Ge}_{1-y}$ layer or a Ge layer.

In one embodiment, the first semiconductor film is formed by annealing the plurality of convex structures at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen.

In one embodiment, the material forming each convex structure comprises $\text{Si}_y\text{Ge}_{1-y}$, and the first semiconductor film is a Ge layer.

According to another aspect of the present disclosure, a method for forming a semiconductor structure is provided. The method comprises steps of: providing a Si substrate; forming a plurality of convex structures on the Si substrate, in which every two adjacent convex structures are separated by a cavity in a predetermined pattern, and the cavity size between every two adjacent convex structures is less than 50nm in width; forming a semiconductor film on tops of the plurality of convex structures, in which a first part of the semiconductor film on the cavity is spaced apart from the Si substrate; forming

a buffer layer on the first semiconductor film; and forming a high-mobility III-V compound semiconductor layer on the buffer layer.

In one embodiment, the method further comprises: forming a gate stack on the high-mobility III-V compound semiconductor layer; and forming a source region and a drain region in the high-mobility III-V compound semiconductor layer and on sides of the gate stack respectively.

In one embodiment, a material forming each convex structure comprises $\text{Si}_{1-x}\text{C}_x$, $\text{Si}_y\text{Ge}_{1-y}$ or Ge, and the first semiconductor film is a $\text{Si}_{1-x}\text{C}_x$ layer, a $\text{Si}_y\text{Ge}_{1-y}$ layer or a Ge layer.

In one embodiment, a width of each convex structure increases gradually from a middle part thereof to a top part thereof so that a cavity size between top parts of two adjacent convex structures is less than that between middle parts of the two adjacent convex structures.

In one embodiment, each convex structure comprises a bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $\text{Si}_y\text{Ge}_{1-y}$ layer or a Ge layer.

In one embodiment, the first semiconductor film is formed by annealing the plurality of convex structures at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen.

In one embodiment, the material forming each convex structure comprises Ge, and the ambient further comprises GeH_4 so that the first semiconductor film is a Ge layer.

In one embodiment, the step of forming a semiconductor film on the plurality of convex structures comprises: forming the semiconductor film on the plurality of convex structures by epitaxy.

In one embodiment, the step of forming a plurality of convex structures on the Si substrate comprises: forming a first semiconductor layer on the Si substrate; implanting Si or Ge ions into the first semiconductor layer to form an ion-implanted layer in the first semiconductor layer; and selectively etching the first semiconductor layer to form the plurality of convex structures.

In one preferred embodiment, the material forming each convex structure comprises Ge, and the first semiconductor layer is a Ge layer, so that the high-mobility III-V compound semiconductor layer may be directly formed on the Ge layer. The first

semiconductor layer is very thin, and consequently the first semiconductor layer may be relaxed during the forming of the convex structures and the subsequent high-temperature annealing. After the first semiconductor layer is relaxed, the high-mobility III-V compound semiconductor layer is formed by epitaxy, which may largely reduce the dislocation density in the buffer layer and the high-mobility III-V compound semiconductor layer so as to form a high-quality heteroepitaxial structure. In addition, because the convex structures may release a part of a thermal mismatch stress, a growth quality of the buffer layer may be ensured, and the buffer layer may be very thin. Moreover, because the high-mobility III-V compound semiconductor layer is directly formed on the first semiconductor layer, for example, a Ge layer, Ge materials may be used as a buffer layer between Si materials and III-V compound materials.

According to an embodiment of the present disclosure, the first semiconductor film are used. In this way, on one hand, dopants in the source and the drain may be prevented from diffusing into a substrate, so that an ultra-shallow junction may be easy to fabricate. On the other hand, the source and the drain may not contact with the substrate, thus inhibiting band-to-band tunneling (BTBT) leakage between the source and the substrate and between the drain and the substrate. Furthermore, parasitic junction capacitance of the source and the drain may be reduced, thus improving the performance of the device.

Additional aspects and advantages of the embodiments of the present disclosure will be given in part in the following descriptions, become apparent in part from the following descriptions, or be learned from the practice of the embodiments of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects and advantages of the disclosure will become apparent and more readily appreciated from the following descriptions taken in conjunction with the drawings in which:

Fig. 1 is a cross-sectional view of a semiconductor structure according to an embodiment of the present disclosure;

Fig. 2 is a cross-sectional view of a semiconductor structure according to another embodiment of the present disclosure;

Fig. 3 is a cross-sectional view of a semiconductor structure according to still another embodiment of the present disclosure;

5 Fig. 4 is a cross-sectional view of a semiconductor structure with a common source region or a common drain region according to an embodiment of the present disclosure;

Fig. 5 is a cross-sectional view of a semiconductor structure with a common source region or a common drain region according to another embodiment of the present disclosure; and

10 Fig. 6 is a flow chart of a method for forming a semiconductor structure according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

Embodiments of the present disclosure will be described in detail in the following
15 descriptions, examples of which are shown in the accompanying drawings, in which the same or similar elements and elements having same or similar functions are denoted by like reference numerals throughout the descriptions. The embodiments described herein with reference to the accompanying drawings are explanatory and illustrative, which are used to generally understand the present disclosure. The embodiments shall not be
20 construed to limit the present disclosure.

Various embodiments and examples are provided in the following description to implement different structures of the present disclosure. In order to simplify the present disclosure, certain elements and settings will be described. However, these elements and settings are only examples and are not intended to limit the present disclosure. In
25 addition, reference numerals may be repeated in different examples in the disclosure. This repeating is for the purpose of simplification and clarity and does not refer to relations between different embodiments and/or settings. Furthermore, examples of different processes and materials are provided in the present disclosure. However, it would be appreciated by those skilled in the art that other processes and/or materials
30 may be also applied. Moreover, a structure in which a first feature is "on" a second feature may include an embodiment in which the first feature directly contacts the second

feature and may include an embodiment in which an additional feature is prepared between the first feature and the second feature so that the first feature does not directly contact the second feature.

Fig. 1 is a cross-sectional view of a semiconductor structure according to an embodiment of the present disclosure. Fig. 2 is a cross-sectional view of a semiconductor structure according to another embodiment of the present disclosure. The semiconductor structure comprises a substrate 1100; a plurality of convex structures 1200 formed on the substrate 1100, in which every two adjacent convex structures 1200 are separated by a cavity in a predetermined pattern. In some embodiments, the cavity between every two adjacent convex structures is less than 50nm in width, preferably, 30 nm. It should be noted that, in some embodiments, the convex structures 1200 may be a vertical structure. However, in other embodiments, as shown in Figs. 1-2, a width of each convex structure 1200 increases gradually from a middle part thereof to a top part thereof so that a cavity size between top parts of two adjacent convex structures 1200 is less than that between middle parts of the two adjacent convex structures 1200. Therefore, a first semiconductor film 1300 may be formed by annealing the convex structures 1200 or by epitaxy. If the cavity size between top parts of two adjacent convex structures 1200 is less than that between middle parts of the two adjacent convex structures 1200, the cavity size between every two adjacent convex structures is the nearest cavity size between the two adjacent convex structures 1200, i.e., the cavity size between the top parts of the two adjacent convex structures 1200. The semiconductor structure according to an embodiment of the present disclosure may be applied to a small size device, particularly used for alleviating a leakage of a small size device.

The semiconductor structure further comprises a first semiconductor film 1300, in which the first semiconductor film 1300 is formed on the convex structures 1200; a buffer layer 2100 formed on the first semiconductor film; and a high-mobility III-V compound semiconductor layer 2000, for example, an InGaAs layer, a GaAs layer, an InP layer, a GaSb layer, an InSb layer or an InAs layer, formed on the buffer layer 2100. In one embodiment, the buffer layer 2100 may also be an III-V compound semiconductor layer 2000, for example, a GaAs layer or an InP layer. The semiconductor structure further comprises a gate stack 1400 formed on the high-mobility III-V compound semiconductor

layer 2000. The gate stack 1400 comprises a gate dielectric layer and a gate electrode, for example, a high k gate dielectric layer. In this embodiment, two independent semiconductor structures are shown, each semiconductor structure forms a device, and the two devices are isolated from each other.

5 The semiconductor structure further comprises a source region and a drain region formed in the high-mobility III-V compound semiconductor layer 2000 and on sides of the gate stack 1400 respectively.

10 In one embodiment, the substrate 1100 is a substrate or a $\text{Si}_y\text{Ge}_{1-y}$ substrate with low Ge content, and the first semiconductor film 1300 is a $\text{Si}_{1-x}\text{C}_x$ layer, a $\text{Si}_y\text{Ge}_{1-y}$ layer with high Ge content, or a Ge layer. In another embodiment, if the first semiconductor film 1300 is formed by epitaxy, the first semiconductor film 1300 may also be an III-V compound semiconductor layer.

15 In one embodiment, a material forming each convex structure 1200 comprises $\text{Si}_{1-x}\text{C}_x$, $\text{Si}_y\text{Ge}_{1-y}$ with high Ge content, or Ge. Therefore, the first semiconductor film may be formed by annealing the convex structures 1200 or by epitaxy.

20 In some embodiments, the first semiconductor film may be formed by annealing the plurality of convex structures 1200. In some embodiments, the annealing is performed at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen to migrate atoms on surfaces of the plurality of convex structures 1200. Since the ambient contains hydrogen, hydrogen may effectively facilitate a migration of atoms on surfaces of the plurality of convex structures 1200. Preferably, when the material forming each convex structure 1200 comprises $\text{Si}_y\text{Ge}_{1-y}$ with high Ge content or Ge, the ambient further comprises at least one gas selected from a group consisting of SiH_4 , GeH_4 , SiH_2Cl_2 , and SiHCl_3 . A small amount of Si and/or Ge atoms are deposited on the surface of the first semiconductor film 1300 by decomposing the at least one gas, so that the surface of the first semiconductor film 1300 may be flattened, and a required flatness is achieved. After the annealing, the top parts of two adjacent convex structures 1200 may be connected with each other to form the first semiconductor film 1300. In one embodiment, for different materials forming the convex structures, an annealing temperature is different. For example, for Si materials, the annealing temperature is about 1200 degrees Celsius, and for Ge

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materials, the annealing temperature is about 900 degrees Celsius. In one preferred embodiment, the material forming each convex structure comprises $\text{Si}_y\text{Ge}_{1-y}$, and the ambient further comprises GeH_4 so that the first semiconductor film is a Ge layer. In this embodiment, the higher the content of Ge in the first semiconductor film 1300, the lower the annealing temperature is. For example, if the first semiconductor film 1300 are a Ge layer, the annealing temperature may be 300 degrees Celsius.

In another embodiment, each convex structure 1200 comprises a bottom layer and a top layer. Fig. 3 is a cross-sectional view of a semiconductor structure according to still another embodiment of the present disclosure. In some embodiments, the bottom layer is a Si layer, and the top layer is a $\text{Si}_y\text{Ge}_{1-y}$ layer or a Ge layer. For example, as shown in Fig. 3, in each convex structure 1200, the bottom layer is a Si layer, and the top layer is a Ge layer. In this way, the Si layer may be used as a buffer layer between the substrate 1100 and the Ge layer.

In other embodiments, a semiconductor structure with a common source region and a common drain region may also be formed, as shown in Figs. 4-5..

Fig. 6 is a flow chart of a method for forming a semiconductor structure according to an embodiment of the present disclosure. The method comprises the following steps.

Step S601, a substrate is provided. The substrate is a Si substrate or a $\text{Si}_y\text{Ge}_{1-y}$ substrate with low Ge content.

Step S602, a plurality of convex structures are formed on the substrate, in which every two adjacent convex structures are separated by a cavity in a predetermined pattern. In some embodiments, a cavity between every two adjacent convex structures is less than 50nm in width, and preferably, 30nm. A width of each convex structure increases gradually from a middle part thereof to a top part thereof so that a cavity size between top parts of two adjacent convex structures is less than that between middle parts of the two adjacent convex structures. Therefore, a first semiconductor film may be formed by annealing the convex structures or by epitaxy. Particularly, in some embodiments, at least one first semiconductor layer is formed on the substrate by epitaxy, and then the at least one first semiconductor layer is etched to form the plurality of convex structures, in which the at least one first semiconductor layer is a Si layer, a $\text{Si}_y\text{Ge}_{1-y}$ layer or a Ge layer. Certainly, in other embodiments, a surface layer of the

substrate is used as the first semiconductor layer, that is, a surface of the substrate is directly etched to form the plurality of convex structures. Preferably, in order to form the plurality of convex structures shown in Fig. 1, the first semiconductor layer may be etched by an anisotropic wet etching.

5 Alternatively, in another preferred embodiment, Si or Ge ions are implanted into the first semiconductor layer to form an ion-implanted layer in the first semiconductor layer, and then the first semiconductor layer is selectively etched by a dry etching to form the plurality of convex structures. Because crystal structures in the ion-implanted layer are damaged seriously, an etching rate in the ion-implanted layer is greater than that in other
10 parts of the first semiconductor layer, thus forming the plurality of convex structures shown in Fig. 2.

Step S603, a first semiconductor film is formed on tops of the plurality of convex structures, in which a first part of the semiconductor film on the cavity is spaced apart from the substrate. In some embodiments, the first semiconductor film is a Si layer, a
15 $\text{Si}_y\text{Ge}_{1-y}$ layer with high Ge content, or a Ge layer.

In one embodiment, the first semiconductor film may be formed by annealing the plurality of convex structures. In some embodiments, the annealing is performed at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen to migrate atoms on surfaces of the plurality of convex structures. Preferably, the
20 ambient further comprises at least one gas selected from a group consisting of SiH_4 , GeH_4 , SiH_2Cl_2 , and SiHCl_3 . A small amount of Si and/or Ge atoms are deposited on the surface of the first semiconductor film by decomposing the at least one gas, so that the surface of the first semiconductor film may be flattened. In one embodiment, the material forming each convex structure comprises Ge, and the ambient further
25 comprises GeH_4 so that the first semiconductor film is a Ge layer.

In one embodiment, a material forming each convex structure comprises $\text{Si}_{1-x}\text{C}_x$, $\text{Si}_y\text{Ge}_{1-y}$ or Ge.

In another embodiment, each convex structure comprises a bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $\text{Si}_y\text{Ge}_{1-y}$ layer with high
30 Ge content or a Ge layer.

In another embodiment, the first semiconductor film may also be formed by epitaxy. In this embodiment, the first semiconductor film is formed on the plurality of convex structures by epitaxy. In some embodiments, the substrate may be a Si substrate, a $\text{Si}_{1-x}\text{C}_x$ substrate, a SiGe substrate or a Ge substrate with a surface of a crystal orientation (100), in which x is within a range from 0 to 0.1. Because a lateral epitaxial growth rate of the first semiconductor film with a certain crystal orientation is not less than a longitudinal growth rate thereof, a gap between top parts of two adjacent convex structures may be quickly sealed up by epitaxial materials. Therefore, the first semiconductor film may not contact with the substrate directly, so that a part of the first semiconductor film may be separated from the substrate. In another embodiment, if the first semiconductor film are formed by epitaxy, the first semiconductor film may also be an III-V compound semiconductor layer.

In one preferred embodiment, after the annealing or the epitaxy, if the first semiconductor film is thick, the first semiconductor film may be subjected to an etching or a thinning process.

Step S604, a buffer layer is formed on the first semiconductor film.

Step S605, a high-mobility III-V compound semiconductor layer is formed on the buffer layer.

In one embodiment, a gate stack is formed on the high-mobility III-V compound semiconductor layer, and a source region and a drain region are formed in the high-mobility III-V compound semiconductor layer and on sides of the gate stack respectively.

In one preferred embodiment, the material forming each convex structure comprises Ge, and the first semiconductor layer is a Ge layer, so that the high-mobility III-V compound semiconductor layer may be directly formed on the Ge layer. The first semiconductor layer is very thin, and consequently the first semiconductor layer may be relaxed during the forming of the convex structures and the subsequent high-temperature annealing. After the first semiconductor layer is relaxed, the high-mobility III-V compound semiconductor layer is formed by epitaxy, which may largely reduce the dislocation density in the buffer layer and the high-mobility III-V compound semiconductor layer so as to form a high-quality heteroepitaxial structure. In addition, because the convex

structures may release a part of a thermal mismatch stress, a growth quality of the buffer layer may be ensured, and the buffer layer may be very thin. Moreover, because the high-mobility III-V compound semiconductor layer is directly formed on the first semiconductor layer, for example, a Ge layer, Ge materials may be used as a buffer
5 layer between Si materials and III-V compound materials.

According to an embodiment of the present disclosure, the first semiconductor film is used. In this way, on one hand, dopants in the source and the drain may be prevented from diffusing into a substrate, so that an ultra-shallow junction may be easy to fabricate. On the other hand, the source and the drain may not contact with the substrate, thus
10 inhibiting BTBT leakage between the source and the substrate and between the drain and the substrate. Furthermore, parasitic junction capacitance of the source and the drain may be reduced, thus improving the performance of the device.

Although explanatory embodiments have been shown and described, it would be appreciated by those skilled in the art that changes, alternatives, and modifications all
15 falling into the scope of the claims and their equivalents may be made in the embodiments without departing from spirit and principles of the disclosure.

WHAT IS CLAIMED IS:

1. A semiconductor structure, comprising:

a Si substrate;

5 a plurality of convex structures formed on the Si substrate, wherein every two adjacent convex structures are separated by a cavity in a predetermined pattern, and the cavity between every two adjacent convex structures is less than 50nm in width;

a first semiconductor film formed on the plurality of convex structures, wherein a part of the first semiconductor film on the cavity is floated and separated from the Si
10 substrate;

a buffer layer formed on the first semiconductor film; and

a high-mobility III-V compound semiconductor layer formed on the buffer layer.

2. The semiconductor structure according to claim 1, further comprising:

15 a gate stack formed on the high-mobility III-V compound semiconductor layer; and

a source region and a drain region formed in the high-mobility III-V compound semiconductor layer and on sides of the gate stack respectively.

3. The semiconductor structure according to claim 1, wherein a width of each convex
20 structure increases gradually from a middle part thereof to a top part thereof so that a cavity size between top parts of two adjacent convex structures is less than that between middle parts of the two adjacent convex structures.

4. The semiconductor structure according to claim 1, wherein a material forming
25 each convex structure comprises $\text{Si}_{1-x}\text{C}_x$, $\text{Si}_y\text{Ge}_{1-y}$ or Ge, and the first semiconductor film is a $\text{Si}_{1-x}\text{C}_x$ layer, a $\text{Si}_y\text{Ge}_{1-y}$ layer or a Ge layer.

5. The semiconductor structure according to claim 1, wherein each convex
30 structure comprises a bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $\text{Si}_y\text{Ge}_{1-y}$ layer or a Ge layer.

6. The semiconductor structure according to claim 1, wherein the first semiconductor film is formed by annealing the plurality of convex structures at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen.

5 7. The semiconductor structure according to claim 4, wherein the material forming each convex structure comprises $\text{Si}_y\text{Ge}_{1-y}$, and the first semiconductor film is a Ge layer.

10 8. A method for forming a semiconductor structure, comprising steps of:
providing a Si substrate;
forming a plurality of convex structures on the Si substrate, wherein every two adjacent convex structures are separated by a cavity in a predetermined pattern, and the cavity between every two adjacent convex structures is less than 50nm in width;
15 forming a semiconductor film on tops of the plurality of convex structures, wherein a first part of the semiconductor film on the cavity is spaced apart from the Si substrate;
forming a buffer layer on the first semiconductor film; and
forming a high-mobility III-V compound semiconductor layer on the buffer layer.

20 9. The method according to claim 8, further comprising:
forming a gate stack on the high-mobility III-V compound semiconductor layer; and
forming a source region and a drain region in the high-mobility III-V compound semiconductor layer and on sides of the gate stack respectively.

25 10. The method according to claim 8, wherein a material forming each convex structure comprises $\text{Si}_{1-x}\text{C}_x$, $\text{Si}_y\text{Ge}_{1-y}$ or Ge, and the first semiconductor film is a $\text{Si}_{1-x}\text{C}_x$ layer, a $\text{Si}_y\text{Ge}_{1-y}$ layer or a Ge layer.

30 11. The method according to claim 8, wherein a width of each convex structure increases gradually from a middle part thereof to a top part thereof so that a cavity size

between top parts of two adjacent convex structures is less than that between middle parts of the two adjacent convex structures.

12. The method according to claim 8, wherein each convex structure comprises
5 a bottom layer and a top layer, the bottom layer is a Si layer, and the top layer is a $\text{Si}_y\text{Ge}_{1-y}$ layer or a Ge layer.

13. The method according to claim 10, wherein the first semiconductor film is
10 formed by annealing the plurality of convex structures at a temperature of 300-1350 degrees Celsius in an ambient containing hydrogen.

14. The method according to claim 13, wherein the material forming each convex
structure comprises Ge, and the ambient further comprises GeH_4 so that the first
semiconductor film is a Ge layer.

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15. The method according to claim 9, wherein the step of forming a
semiconductor film on the plurality of convex structures comprises:

forming the semiconductor film on the plurality of convex structures by epitaxy.

20 16. The method according to claim 9, wherein the step of forming a plurality of
convex structures on the Si substrate comprises:

forming a first semiconductor layer on the Si substrate;

implanting Si or Ge ions into the first semiconductor layer to form an ion-implanted
layer in the first semiconductor layer; and

25 selectively etching the first semiconductor layer to form the plurality of convex
structures.

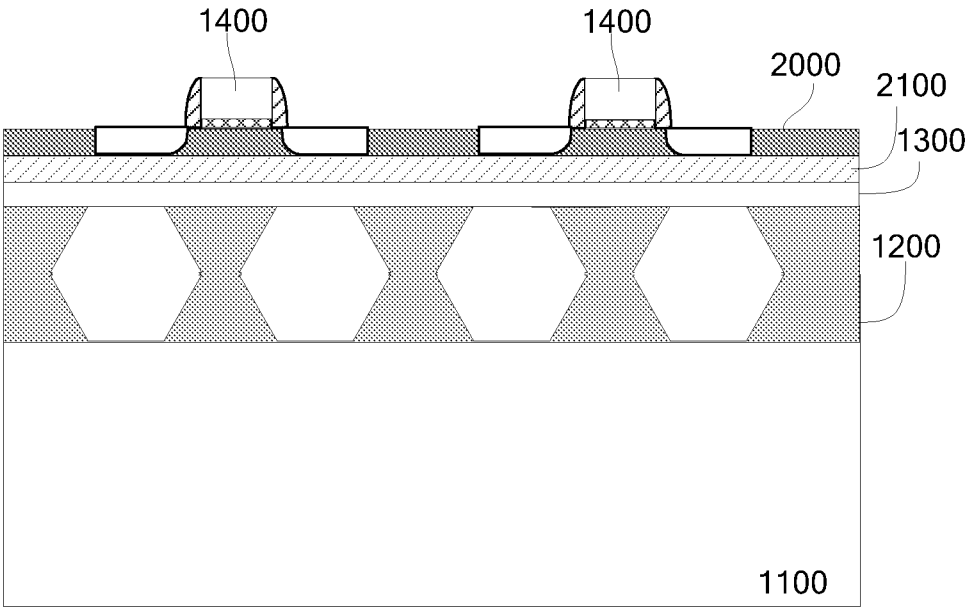


Fig. 1

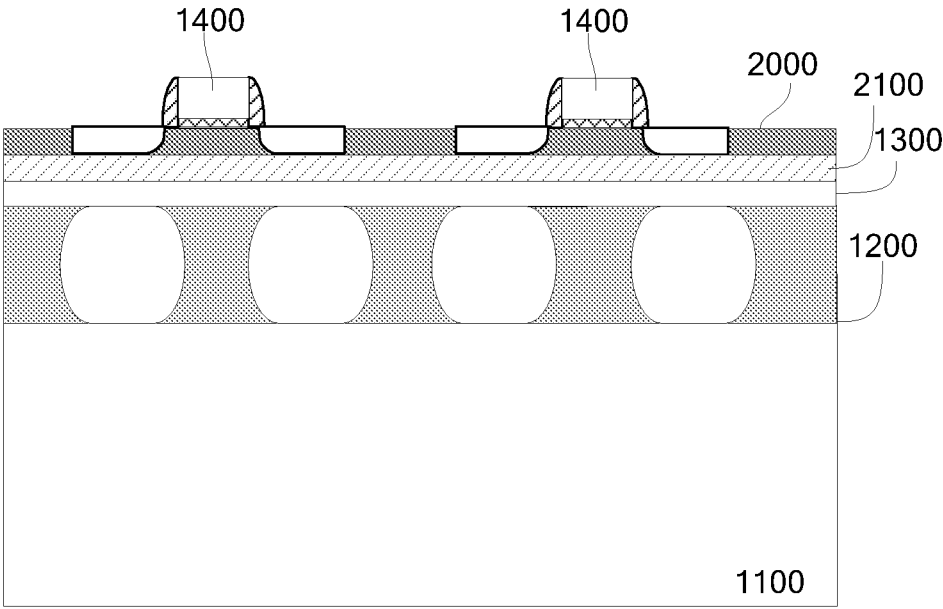


Fig. 2

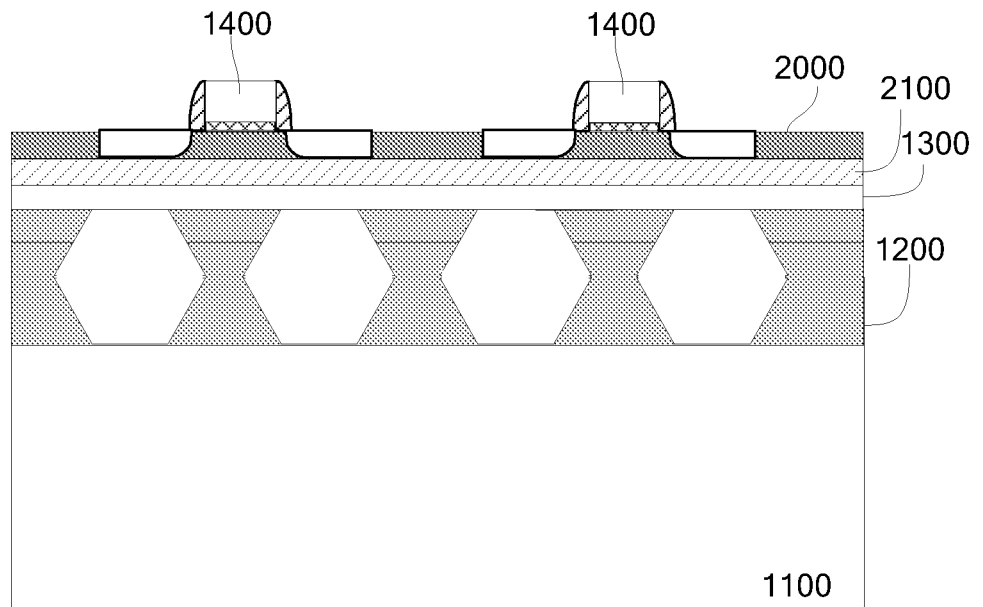


Fig. 3

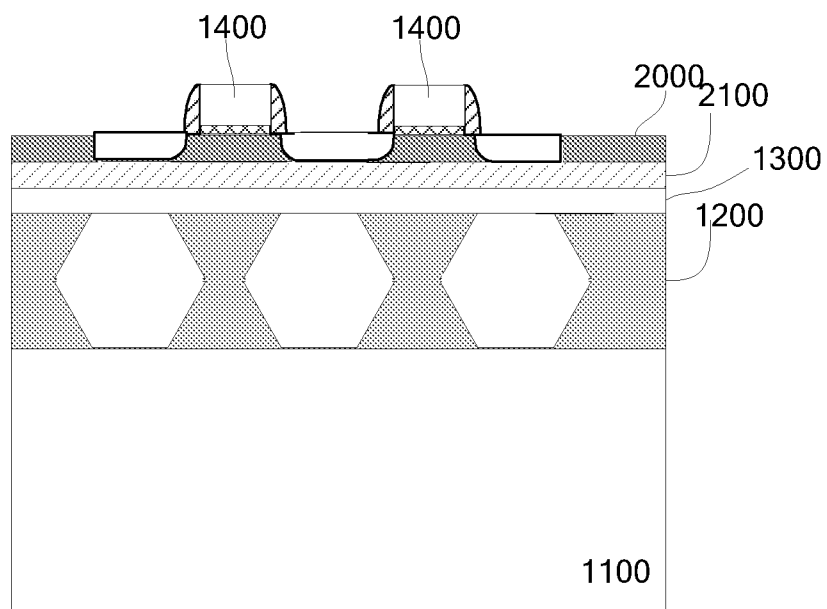


Fig. 4

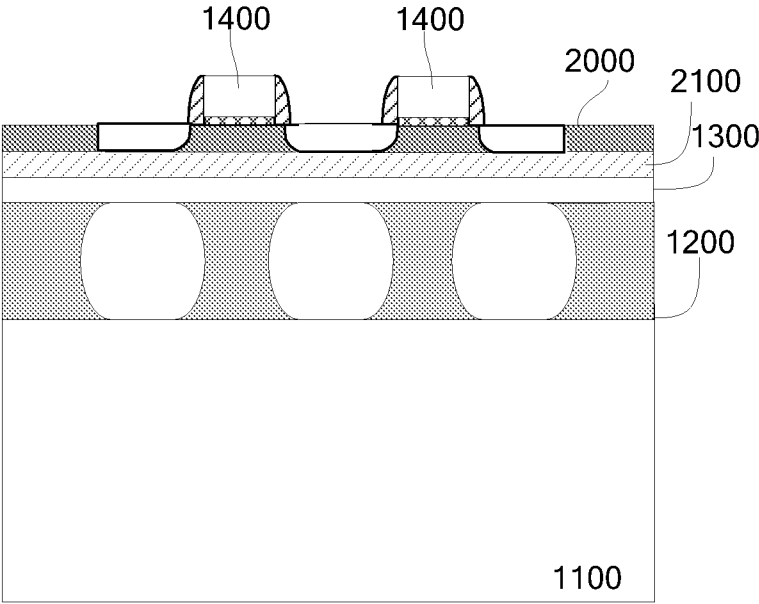


Fig. 5

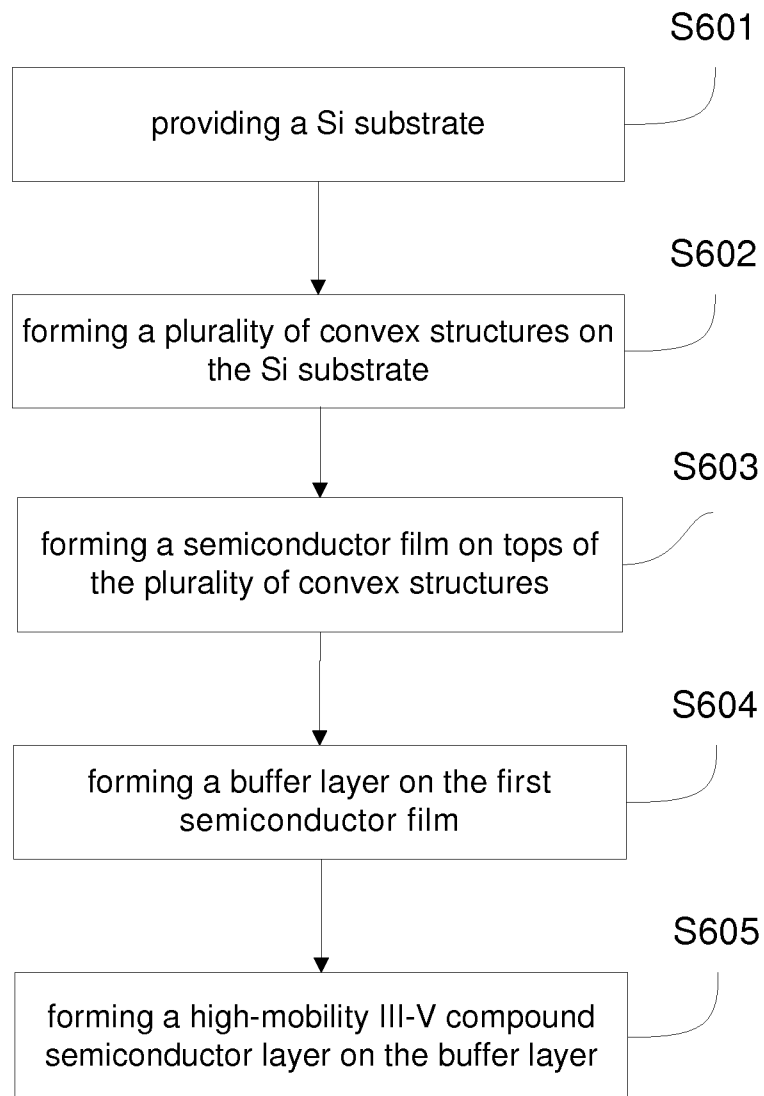


Fig. 6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/082112

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L 29/-, H01L 27/-, H01L 21/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI,CNPAT,WPI,EPODOC: float source drain substrate convex concave cavity buffer mobility gate stack

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN102214685A (TSINGHUA UNIVERSITY) 12 Oct. 2011 (12.10.2011) claims 1-16	1-5,7-12,15-16
X		6,13-14
A	CN1783512A (CHINESE ACAD SCI SEMICONDUCTOR INST) 07 Jun. 2006 (07.06.2006) the whole document	1-16
A	JP2000-323714A (TOSHIBA KK) 24 Nov. 2000 (24.11.2000) the whole document	1-16

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“A” document defining the general state of the art which is not considered to be of particular relevance	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“E” earlier application or patent but published on or after the international filing date	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“L” document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)	“&” document member of the same patent family
“O” document referring to an oral disclosure, use, exhibition or other means	
“P” document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 20 Feb. 2012 (20.02.2012)	Date of mailing of the international search report 15 Mar. 2012 (15.03.2012)
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer WANG Lin Telephone No. (86-10)6241 1816

International application No.
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INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/082112

CLASSIFICATION OF SUBJECT MATTER

H01L 29/06 (2006.01) i

H01L 29/24 (2006.01) i

H01L 21/8234 (2006.01) i

H01L 27/088 (2006.01) n