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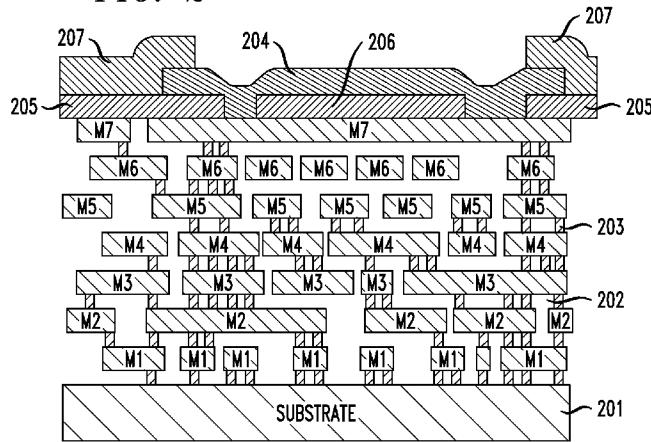
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[Continued on next page]

(54) Title: BOND PAD SUPPORT STRUCTURE FOR SEMICONDUCTOR DEVICE

FIG. 2



(57) **Abstract:** According to certain embodiments, integrated circuits are fabricated using brittle low-k dielectric material to reduce undesired capacitances between conductive structures. To avoid permanent damage to such dielectric material, bond pads are fabricated with support structures that shield the dielectric material from destructive forces during wire bonding. In one implementation, the support structure includes a passivation structure between the bond pad and the topmost metallization layer. In another implementation, the support structure includes metal features between the topmost metallization layer and the next-topmost metallization layer. In both cases, the region of the next-topmost metallization layer under the bond pad can have multiple metal lines corresponding to different signal routing paths. As such, restrictions on the use of the next-topmost metallization layer for routing purposes are reduced compared to prior-art bond-pad support structures that require the region of the next-topmost metallization layer under the bond pad to be a single metal structure.

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GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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BOND PAD SUPPORT STRUCTURE FOR SEMICONDUCTOR DEVICEBACKGROUND OF THE INVENTION5 Field of the Invention

[0001] The present invention relates to bond pads for integrated circuit dies, and in particular to the metallization layers supporting a bond pad.

Description of the Related Art

10 [0002] The manufacture of a semiconductor device is a multi-step process that includes a wafer-fabrication step and an assembly step. Wafer fabrication includes adding layers of precisely-formed materials on a semiconductor substrate. The layers are patterned by photo-masking and etching. Typically, the topmost layers include several metallization layers that contain metal lines connecting various components on lower layers. Direct connections between metal layers are accomplished 15 using metal vias, *i.e.*, vertical lines, between metal layers. Wafer fabrication produces a wafer that comprises multiple integrated circuits (ICs). Assembly typically includes (i) cutting the wafer into individual IC dies, (ii) attaching each die to a corresponding lead frame, (iii) wire bonding pads on each die to leads on the corresponding lead frame, and (iv) encapsulating each die, bond wires, and corresponding lead frame in a plastic or ceramic package. Alternative assembly processes are used 20 for particular chip types. For example, assembly of ball grid array (BGA) type chips typically involves the electrical connection of the die to a non-lead-frame base, referred to as a substrate, that provides electrical connectivity to a circuit board, and encapsulation in a polymer material.

[0003] Engineering advances over time lead to reductions in the size of the components in ICs along with increases in the operational clock speeds of the ICs. The reduction in size and increase in 25 speed introduce new challenges. Parasitic capacitive coupling between elements, *e.g.*, metal lines, increases as element device dimensions decrease and its effects can be magnified at higher operating frequencies. The capacitive coupling increases because the capacitance between two elements is inversely-proportional to the distance between them. This relationship can be seen from the formula for C, the capacitance of a parallel-plate capacitor, wherein the capacitance can be represented as:

$$30 \quad C = \frac{\epsilon_0 k A}{d} \quad (1)$$

wherein ϵ_0 is the permittivity of vacuum, k is the dielectric constant of the dielectric, *i.e.*, the material separating the capacitor plates, A is the area of each of the plates, and d is the distance between the plates.

[0004] Metal lines in an IC are typically separated by silicon dioxide (SiO_2), whose dielectric 35 constant k is approximately 4.3. Reducing the dielectric constant would operate to reduce the capacitance between two elements, as can be seen from equation (1). Techniques have been

developed to fabricate ICs with low-k dielectrics. Dielectric materials having a *k* below approximately 3.0 are considered low-k dielectrics. Low-k dielectrics can be formed, for example, by introducing hollow spaces, *i.e.*, porosity, and/or impurities, *e.g.*, certain hydrocarbons, into regular SiO₂ dielectric material.

5 [0005] Low-k SiO₂ dielectrics tend to be structurally weaker than regular SiO₂. The relative weakness is exemplified, *e.g.*, by having a lower elastic modulus. For example, a piece of regular SiO₂ can have a Young's modulus of between 50 and 150GPa, depending on the technique used to fabricate it, while a corresponding piece of a low-k dielectric can have a Young's modulus of less than 20GPa. Weaker dielectrics are more easily damaged and are more likely to suffer destructive
10 fractures during assembly, *e.g.*, during the wire bonding process when a wire is attached to a bond pad on the die. The attachment of a wire to a bond pad generally includes the application of pressure, ultrasonic energy, and/or heat, which impose mechanical stress onto the bond pad as well as the structure underneath the bond pad. This mechanical stress can potentially damage those underlying structures. The likelihood of damage increases as the strength of the bond pad and underlying
15 structure decreases. In addition, since the mechanical stress on a bond pad is inversely proportional to the area of the bond pad, the likelihood of damage increases as the silicon technology dimensions, and consequently, the bond pad sizes, decrease.

20 [0006] FIG. 1 shows a cross-sectional view of a bond pad area of semiconductor device 100 in accordance with U.S. Patent No. 7,115,985 B2 ("the '985 Patent") issued to Antol et al., which describes one prior-art reinforced bond pad that helps reduce damage to device components subjacent to the bonding pad. Semiconductor device 100 comprises substrate 101 at the bottom. Overlaying substrate 101 are seven metallization layers M1-M7. The metallization layers comprise metallic lines that are routed to connect components on substrate 101. The metallic lines and metallization layers are separated by dielectric 102. Select metallic lines in adjoining metallization layers are directly
25 connected by metallic vias such as via 103.

20 [0007] Topmost metal layer M7 is partially overlaid with first passivation layer 104, which has an opening, or window, to allow the formation of bond pad 105 using, *e.g.*, aluminum. Passivation layers can be made of, *e.g.*, silicon nitride (Si₃N₄). Bond pad 105 is conductively connected to a portion of metallization layer M7, and, via the other metallization layers and intermediary vias, to one
30 or more appropriate components on substrate 101. Exposed areas of first passivation layer 104 and the perimeter of bond pad 105 are topped by second passivation layer 106. In the volume substantially beneath bond pad 105, metal layers M6 and M7 are substantially continuous planar structures interconnected by an array of metal-filled recesses arranged to intersect one another to form a mesh-like pattern containing a plurality of discrete sections of dielectric 102. This two-layer array-
35 interconnected metallic structure underneath bond pad 105 provides (i) structural reinforcement to the

volume underneath bond pad **105**, as well as (ii) a conductive path from bond pad **105** to appropriate components on substrate **101**.

[0008] Because of the substantially-planar natures of, and the mesh of metallic interconnects between, the sections of metal layers **M6** and **M7** underneath bond pad **105**, those areas of metal layers **M6** and **M7** have comprehensive routing restrictions and are largely unusable for routing regular metal lines for component interconnection.

SUMMARY OF THE INVENTION

[0009] In one embodiment, the invention can be an integrated circuit (IC) comprising: (i) a bond pad, (ii) a passivation structure directly underneath and in direct contact with a portion of the bond pad, and (iii) a first metallization layer under the bond pad and the passivation structure, wherein an other portion of the bond pad is in direct contact with the first metallization layer.

[0010] In another embodiment, the invention can be an integrated circuit (IC) comprising: (i) a bond pad, (ii) a first metallization layer under and in direct contact with the bond pad, (iii) a second metallization layer under the first metallization layer, and (iv) first low-k dielectric material between the first and second metallization layers. A portion of the second metallization layer under the bond pad comprises two or more metal lines that are (i) part of two more distinct routing paths in the IC and (ii) separated by second low-k dielectric material. At least one of the metal lines in the portion of the second metallization layer under the bond pad is directly connected to the first metallization layer by one or more metal features in the first low-k dielectric material. At least one of the metal lines in the portion of the second metallization layer under the bond pad is not directly connected to the first metallization layer by any metal feature in the first low-k dielectric material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Other aspects, features, and advantages of the present invention will become more fully apparent from the following detailed description, the appended claims, and the accompanying drawings in which like reference numerals identify similar or identical elements.

[0012] **FIG. 1** shows a cross-sectional view of a bond pad of a prior-art semiconductor device.

[0013] **FIG. 2** shows a cross-sectional view of a semiconductor-device bond pad in accordance with an embodiment of the present invention.

[0014] **FIG. 3** shows a cutaway top view of one implementation of the bond pad of **FIG. 2**.

[0015] **FIG. 4** shows a cutaway top view of another implementation of the bond pad of **FIG. 2**.

[0016] **FIG. 5** shows a cross-sectional view of a semiconductor-device bond pad in accordance with another embodiment of the present invention.

[0017] **FIG. 6** shows a cutaway top view of one implementation of the bond pad of **FIG. 5**.

DETAILED DESCRIPTION

[0018] **FIG. 2** shows a cross-sectional view of a section of semiconductor device **200** corresponding to bond pad **204**. Semiconductor device **200** comprises substrate **201** at the bottom.

5 Overlaying substrate **201** are seven metallization layers **M1-M7**. The metallization layers comprise metallic lines that are routed to connect components on substrate **201**. The metallic lines and metallization layers are separated by dielectric **202**. Particular metallic lines in adjoining metallization layers are directly connected by metallic vias such as via **203**.

[0019] Topmost metal layer **M7** is partially overlaid with first passivation layer **205**, which has an opening to allow the formation of bond pad **204** using, *e.g.*, aluminum. The opening for bond pad **204** in first passivation layer **205** is a frame or outline opening, *i.e.*, only a framing part is removed from the first passivation layer **205** section that is coincident with bond pad **204**, thereby, leaving behind passivation structure **206**. Bond pad **204** is conductively connected to a portion of metallization layer **M7**, and, via the other metallization layers and intermediary vias, to one or more appropriate components on substrate **201**. Exposed areas of first passivation layer **205** and the perimeter of bond pad **204** are topped by second passivation layer **207**. In the volume substantially beneath bond pad **204**, metal layer **M7** is substantially a continuous planar structure, while metal layers **M1-M6** in that volume comprise routed metal lines, as metal layers **M1-M6** generally do in other areas. Specifically, the portion of metallization layer **M6** underneath bond pad **204** comprises 10 two or more metal lines that are parts of distinct routing paths in semiconductor device **200**. Distinct routing paths are not directly connected, but may be coupled through other components.

[0020] Passivation structure **206** and the substantially-continuous planar portion of metallization layer **M7** underneath bond pad **204** provide structural support for the area of semiconductor device **200** underneath bond pad **204**. During wire bonding, passivation structure **206** helps mitigate the 15 stresses from the bonding process on the underlying volume. The area of metallization layer **M6** substantially underneath bond pad **204** is not a substantially-continuous planar structure and does not have the comprehensive routing restrictions of the corresponding section of metallization layer **M6** of **FIG. 1**, *i.e.*, that area as well as the rest of metallization layer **M6** are not subject to any routing 20 restrictions directly related to the location of bond pad **204**. Rather, that area can be used to route metal lines, which allows for more efficient utilization of the volume substantially underneath bond pad **204**.

[0021] **FIG. 3** shows a cutaway top view of one implementation of the bond pad section of **FIG. 2**. First passivation layer **205** and passivation structure **206** are shown using a diagonal cross-hatch pattern. It should be noted that passivation layer **205** extends beyond the area shown in **FIG. 3**. Bond 25 pad **204** is substantially square in shape. Passivation structure **206** is substantially (i) centered within the area of bond pad **204** and (ii) square in shape. Exemplary dimensions for bond pad **204** and

passivation structure **206** are 60x60 μm and 40x40 μm , respectively. Interface region **301**, shown in white, is the area between passivation structure **206** and first passivation layer **205**. Interface region **301** provides electrical connectivity for bond pad **204** to topmost metallization layer **M7** of **FIG. 2**.

[0022] **FIG. 4** shows a cutaway top view of an alternative implementation of the bond pad section of **FIG. 2**. First passivation layer **205** and passivation structure **206** are shown using a diagonal cross-hatch pattern, wherein passivation layer **205** extends beyond the area shown. Bond pad **204** is substantially rectangular. Passivation structure **206** is substantially (i) centered within the area of bond pad **204** and (ii) circular in shape. Note that circle is a particular type of ellipse. Exemplary dimensions for bond pad **204** and passivation structure **206** are 60x40 μm and 40 μm diameter, respectively. Interface region **401**, shown in white, is the area between passivation structure **206** and first passivation layer **205**. Interface region **401** provides electrical connectivity for bond pad **204** to topmost metallization layer **M7** of **FIG. 2**.

[0023] **FIG. 5** shows a cross-sectional view of a bond pad of semiconductor device **500**, in accordance with another embodiment of the present invention. Elements in **FIG. 5** that are substantially similar to elements in **FIG. 2** have been similarly numbered, but with a different prefix. Bond pad **504** of semiconductor device **500** does not include a passivation structure analogous to passivation structure **206** of **FIG. 2**. Rather, structural reinforcement is provided using supporting vias, such as vias **508**, between metallization layers **M6** and **M7**. The area of metallization layer **M6** underneath bond pad **504** is partially routing restricted, wherein some parts can be used for routing metal lines, while other parts comprise dedicated metal lines connected to metallization layer **M7** to provide structural support to bond pad **504**. It should be noted that the dedicated metal lines can nevertheless be used as part of a conductive path connecting bond pad **504** to appropriate components on substrate **501**.

[0024] **FIG. 6** shows a cutaway top view of one implementation of the bond pad section of **FIG. 5**. First passivation layer **505** is shown using a diagonal cross-hatch pattern, wherein passivation layer **505** extends beyond the area shown. Bond pad **504** is substantially square. Routing-restricted areas **601** of metallization layer **M6** correspond to structural-support vias, such as vias **508** of **FIG. 5**, and are shown using an orthogonal cross-hatch pattern. Routing-restricted areas **601** of **FIG. 6** form a partial frame and are substantially symmetrical about the center of bond pad **504**.

[0025] In an alternative implementation of the bond pad section of **FIG. 5**, routing-restricted areas **601** of metallization layer **M6** and the corresponding structure-supporting vias form a shape other than that shown in **FIG. 6**. The fill density for the vias between metallization layers **M6** and **M7**, *i.e.*, the percentage of the top-view cross-sectional area that is metal vias, in the area underneath bond pad **504** should be at least 30%, with a preferred fill density of approximately 60-80%. The fill density can be achieved either by particular routing of the dedicated metal lines of metallization layer **M6** or by use of a particular fill pattern for the interconnecting metal features.

[0026] In an alternative embodiment of bond pad 204 of **FIG. 4**, passivation structure 206 has a diameter lesser than the smaller dimension of bond pad 204. In an alternative implementation of bond pad 204 of **FIG. 2**, passivation structure 206 is in the shape of a non-circular ellipse. In an alternative implementation of bond pad 204 of **FIG. 2**, passivation structure 206 is a shape other than a square or an ellipse. In designing a specific shape for passivation structure 206, factors to be considered include design rules for the semiconductor device, the need to maximize the area of the passivation structure to provide maximal structural support, and the need to maximize the contact area to provide maximal signal transmittal from bond pad to topmost metallization layer.

5 [0027] In one alternative implementation of semiconductor device 200 of **FIG. 2**, there are no metal vias between metallization layers M6 and M7 in the volume underneath bond pad 204.

10 [0028] Embodiments of semiconductor devices have been described having seven metallization layers. That number is exemplary. As would be appreciated by one of ordinary skill in the art, alternative embodiments can have different numbers of metallization layers, as determined by the designer of the particular semiconductor device.

15 [0029] Embodiments of semiconductor devices have been described employing a second passivation layer. An alternative embodiment has only the first passivation layer. Another alternative embodiment has three or more passivation layers.

20 [0030] Some integrated circuits comprise one or more metal structures having a bond pad directly connected to a probe region. As used in this specification, the term “bond pad” does not include the probe region of such a metal structure.

25 [0031] In one alternative implementation of semiconductor device 200 of **FIG. 2**, the routing-restricted portion of metallization layer M7 that forms a contact structure with bond pad 204 is shaped substantially similar to the interface region, such as interface region 301 of **FIG. 3** or interface region 401 of **FIG. 4**. Thus, some of the area of metallization layer M7 that is underneath the passivation structure can be used for routing metal lines. For example, in one implementation, the area of metallization layer M7 that corresponds to passivation structure 206 of **FIG. 3** can be used for regular routing of metal lines.

30 [0032] It will be further understood that various changes in the details, materials, and arrangements of the parts which have been described and illustrated in order to explain the nature of this invention may be made by those skilled in the art without departing from the scope of the invention as expressed in the following claims.

35 [0033] Reference herein to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment can be included in at least one embodiment of the invention. The appearances of the phrase “in one embodiment” in various places in the specification are not necessarily all referring to the same embodiment, nor are

separate or alternative embodiments necessarily mutually exclusive of other embodiments. The same applies to the term “implementation.”

[0034] Unless explicitly stated otherwise, each numerical value and range should be interpreted as being approximate as if the word “about” or “approximately” preceded the value of the value or 5 range. As used in this application, unless otherwise explicitly indicated, the term “connected” is intended to cover both direct and indirect connections between elements.

[0035] For purposes of this description, the terms “couple,” “coupling,” “coupled,” “connect,” “connecting,” or “connected” refer to any manner known in the art or later developed in which energy 10 is allowed to be transferred between two or more elements, and the interposition of one or more additional elements is contemplated, although not required. The terms “directly coupled,” “directly connected,” etc., imply that the connected elements are either contiguous or connected via a conductor for the transferred energy.

[0036] The use of figure numbers and/or figure reference labels in the claims is intended to 15 identify one or more possible embodiments of the claimed subject matter in order to facilitate the interpretation of the claims. Such use is not to be construed as limiting the scope of those claims to the embodiments shown in the corresponding figures.

CLAIMS**We claim:**

1. An integrated circuit (IC) comprising:

a bond pad (e.g., 204);

5 a passivation structure (e.g., 206) directly underneath and in direct contact with a portion of the bond pad; and

a first metallization layer (e.g., M7) under the bond pad and the passivation structure, wherein an other portion of the bond pad is in direct contact with the first metallization layer.

10 2. The invention of claim 1, further comprising:

a second metallization layer (e.g., M6) under the first metallization layer; and

first dielectric material between the first and second metallization layers, wherein:

the portion of the second metallization layer under the bond pad comprises two or more metal lines separated by second dielectric material.

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3. The invention of claim 2, wherein the two or more metal lines are part of two or more distinct routing paths in the IC.

20 4. The invention of claim 2, wherein the first and second dielectric materials are low-k dielectric materials.

5. The invention of claim 4, wherein the low-k dielectric materials have a dielectric constant k of less than 3.

25 6. The invention of claim 4, wherein the low-k dielectric materials have a Young's modulus of less than 40GPa.

7. The invention of claim 2, wherein there are no metal vias between the first and second metallization layers in the volume underneath the bond pad.

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8. The invention of claim 1, wherein the bond pad does not include a probe region.

9. The IC of claim 1, wherein the passivation structure helps prevent permanent damage to the IC during wire-bonding to the bond pad.

10. The invention of claim 1, wherein the first metallization layer comprises a first portion that is a substantially continuous planar metal structure having substantially the same area as the bond pad, located underneath and directly connected to the bond pad.

5 11. The invention of claim 10, wherein the first metallization layer comprises a second portion comprising one or more metal lines not directly connected to the first portion.

12. The invention of claim 1, further comprising a first passivation layer (e.g., 205) above the first metallization layer.

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13. The invention of claim 12, wherein the passivation structure is separated from the first passivation layer by the other portion of the bond pad that is in direct contact with the first metallization layer.

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14. The invention of claim 13, wherein the passivation structure is substantially in the shape of a square substantially centered in an opening in the first passivation layer.

15. The invention of claim 13, wherein the passivation structure is substantially in the shape of an ellipse substantially centered in an opening in the first passivation layer.

20

16. The invention of claim 12, wherein the first passivation layer and the passivation structure are made of substantially identical passivation material.

17. An integrated circuit (IC) comprising:

a bond pad (e.g., 504);

25

a first metallization layer (e.g., M7) under and in direct contact with the bond pad;

a second metallization layer (e.g., M6) under the first metallization layer;

30

first low-k dielectric material between the first and second metallization layers, wherein:

a portion of the second metallization layer under the bond pad comprises two or more metal lines that are (i) part of two more distinct routing paths in the IC and (ii) separated by second low-k dielectric material;

at least one of the metal lines in the portion of the second metallization layer under the bond pad is directly connected to the first metallization layer by one or more metal features in the first low-k dielectric material; and

35

at least one of the metal lines in the portion of the second metallization layer under the bond pad is not directly connected to the first metallization layer by any metal feature in the first low-k dielectric material.

18. The invention of claim 17, wherein the fill density of metal features in the first low-k dielectric material in the volume underneath the bond pad is at least 30%.

5 19. The invention of claim 18, wherein the fill density of metal features in the first low-k dielectric material in the volume underneath the bond pad is 60-80%.

20. The invention of claim 17, wherein the one or more metal features helps prevent permanent damage to the IC during wire-bonding to the bond pad.

FIG. 1 1/3
PRIOR ART

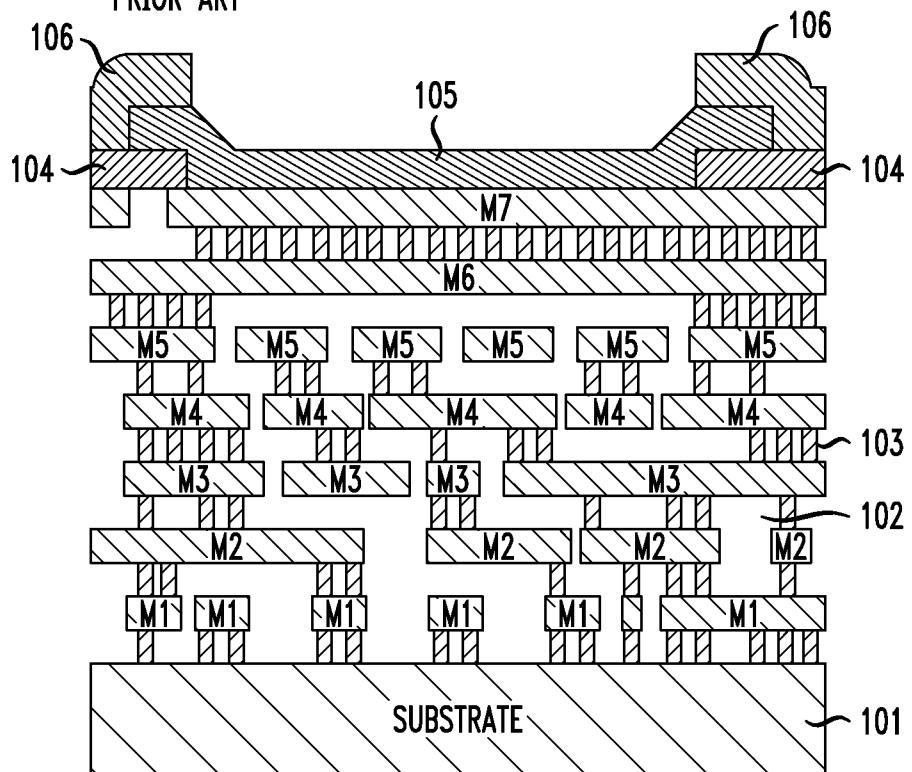
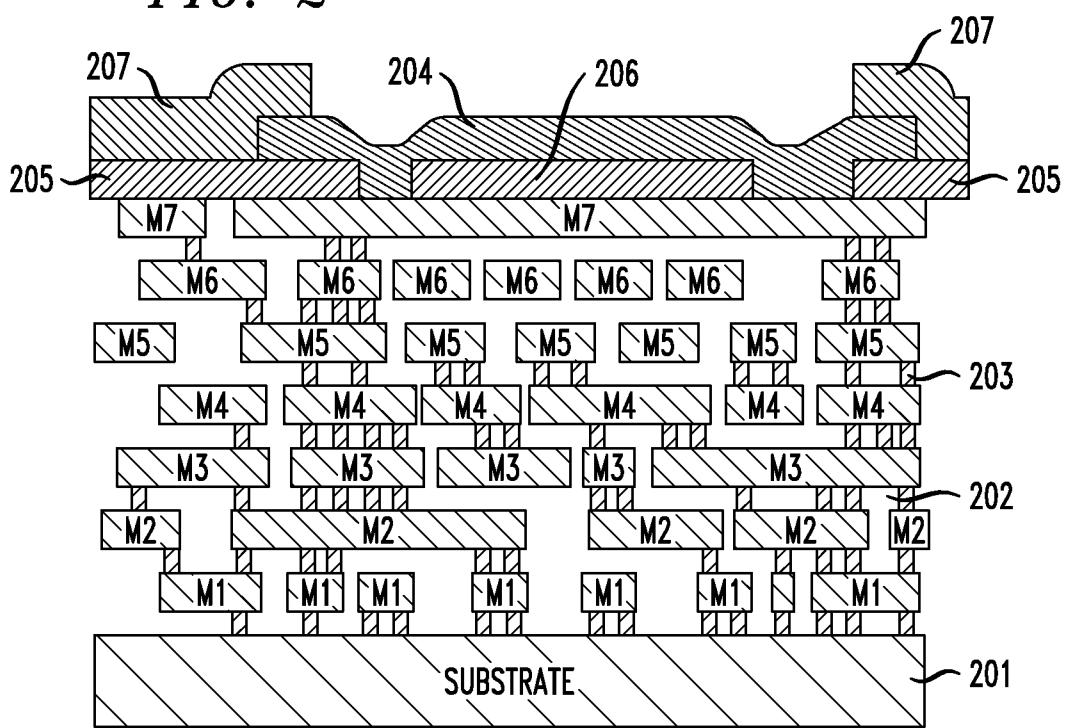


FIG. 2



2/3

FIG. 3

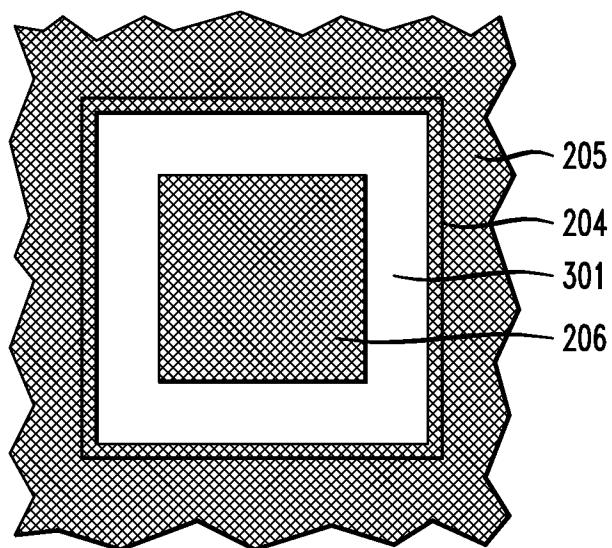
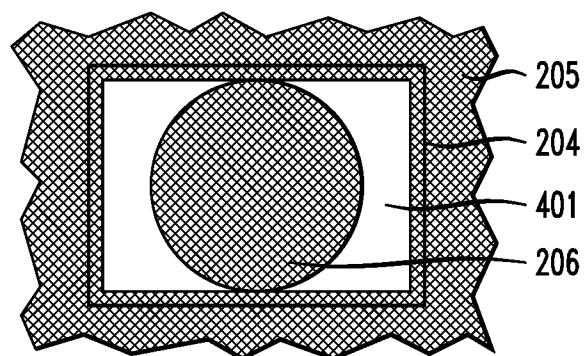


FIG. 4



3/3

FIG. 5

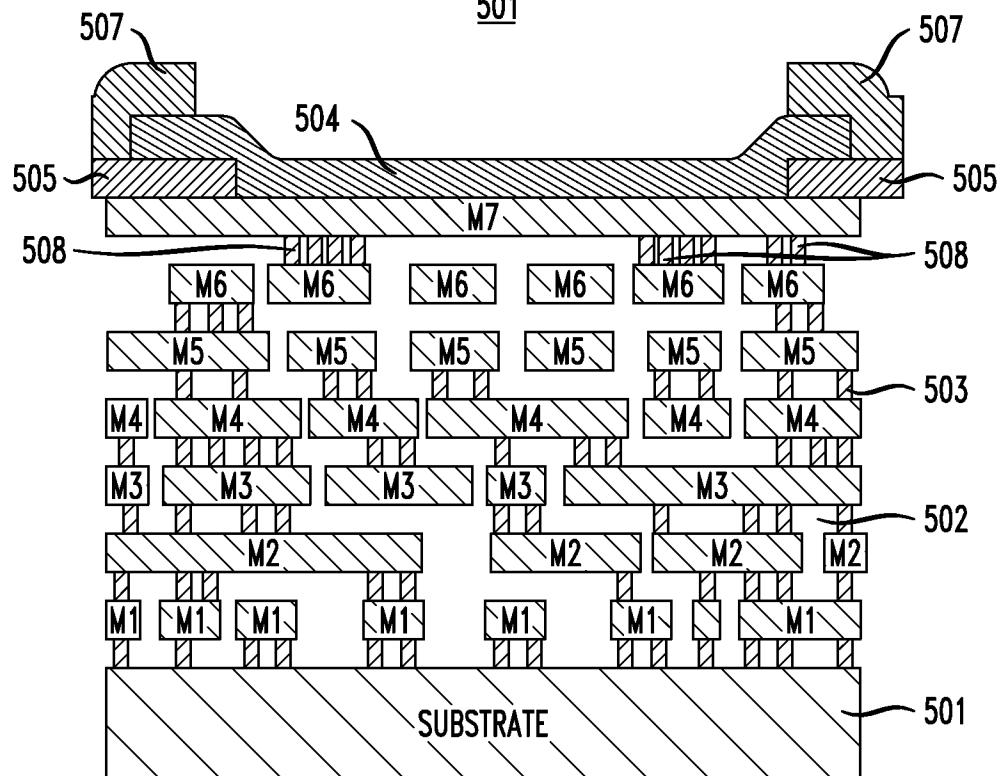
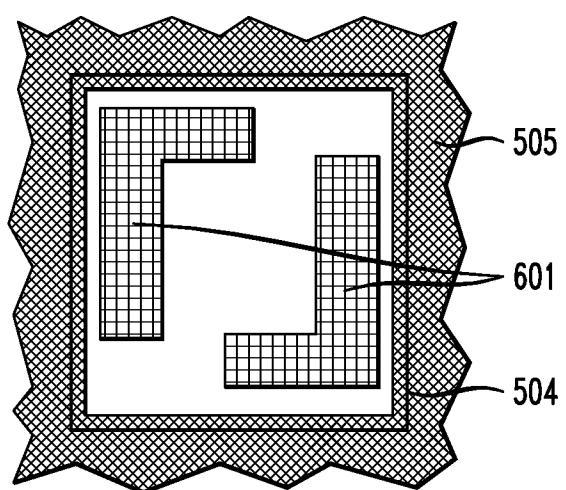
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FIG. 6



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/083183

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/485 H01L23/528

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/173637 A1 (DOWNEY SUSAN H [US] ET AL) 18 September 2003 (2003-09-18) paragraphs [0010] - [0018]; figure 3	1-6,8,9, 12-16
X	JP 2004 207509 A (MATSUSHITA ELECTRIC IND CO LTD) 22 July 2004 (2004-07-22) abstract	1-6, 8-12, 17-20
X	US 2003/173667 A1 (YONG LOIS E [US] ET AL) 18 September 2003 (2003-09-18) paragraphs [0010] - [0018]; figure 3	17-20
X	US 6 222 270 B1 (LEE HYAE-RYOUNG [KR]) 24 April 2001 (2001-04-24) column 3, line 34 - column 5, line 25; figures 1-4	1,8-16
		-/-

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

- *A* document defining the general state of the art which is not considered to be of particular relevance
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Date of the actual completion of the international search

2 July 2008

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18/07/2008

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2007/083183

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 198 170 B1 (ZHAO BIN [US]) 6 March 2001 (2001-03-06) column 8, line 35 - column 11, line 24; figures 3B,4 ----- JP 2007 227815 A (CONSORTIUM FOR ADVANCED SEMICO) 6 September 2007 (2007-09-06) abstract -----	4-6 18,19
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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