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(54) Title: A CMOS METHOD OF FABRICATING A COMBINATION OF AN ION SENSITIVE FIELD EFFECT TRANSISTOR (ISFET) AND MOSFET DEVICE

ISFET gate is sensing membrane

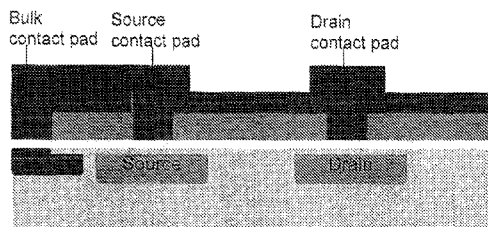


Figure 2: ISFET complete device

MOSFET gate is metal on silicon nitride

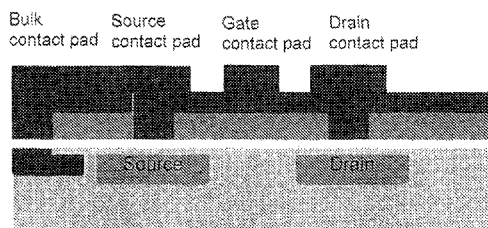


Figure 3: MOSFET complete device

(57) Abstract: A method of fabricating ion-sensitive field-effect transistor (ISFET) device by using Complementary metal-oxide-semiconductor (CMOS) compatible is provided, the method includes the steps of marking and etching a silicon layer (101), depositing an oxide layer (102), as well as implanting doping patterns on the silicon and oxide layers (101, 102), depositing a silicon nitride layer (104), sputtering and etching metal.





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A CMOS METHOD OF FABRICATING A COMBINATION OF AN ION SENSITIVE FIELD EFFECT TRANSISTOR (ISFET) AND MOSFET DEVICE

FIELD OF INVENTION

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The present invention relates to a method of fabricating ion-sensitive field-effect transistor (ISFET) device by using Complementary metal-oxide-semiconductor (CMOS) compatible.

BACKGROUND OF INVENTION

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Chemical sensors are micro devices that connect chemical and electrical domains (i.e. transduction of the chemical information into electric signal). The response of the sensors should be fast and selective and sensitive for the analyte. The construction of chemical sensors requires the integration of a sensing receptor and a transducing element into a defined chemical system. Field effect transistors (FETs) are very interesting because they can be made very small with current planar IC technology and have the advantage of a fast response time.

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ISFET was first explored by P. Bergveld in 1972 (Bergveld, 1972). In recent years, many researchers have done to characterize ISFET based on MOSFET technology up until now. ISFET is an integrated device that is similar to Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) except the gate part. Unlike MOSFET, metal gate of MOSFET is replaced by a pH sensing membrane which is Silicon Nitride (Si_3N_4) in ISFET design. Si_3N_4 as a sensing membrane is use to detect ion response in pH buffer solution by exposing the membrane layer to the solution.

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The pH sensitivity is one of the most important characteristic parameters of ISFET devices. The response of an ISFET is generally determined by the type of the sensing membrane used. Therefore the sensing membrane material plays a significant role.

- 5 The pH sensitivity can be determined by extracting the threshold voltage (V_{TH}) of ISFET device in various pH solutions. The V_{TH} of MOSFET is usually defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. As for ISFET device, V_{TH} refer to the minimum gate voltage required to induce a conducting channel at the surface of ISFET.

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The standard fabrication process produces an unstable threshold voltage that can affect yield of wafer fabrication. There is also a large metal etch process variation between center and edge of wafer that would also affect the yield of fabrication. It is also not possible to determine performance at wafer level testing.

15

US 7,019,343 B2 describes an ISFET device, manufacturing method. However, this solution is only partially CMOS compatible.

Therefore, there is a need for an improvement over the existing fabrication process of
20 ISFET.

SUMMARY OF INVENTION

Accordingly, there is provided a method of fabricating ion-sensitive field-effect transistor (ISFET) device by using Complementary metal–oxide–semiconductor (CMOS) compatible, the method includes the steps of marking and etching a silicon layer, depositing an oxide layer, implanting a p-well pattern on the silicon and oxide layers, implanting a channel pattern onto the silicon and oxide layers, implanting N+ source and drain pattern onto the silicon and oxide layers, implanting P+ diffusion pattern onto the silicon and oxide layers, removing the oxide layer, adding a bottom oxidation layer, depositing a silicon nitride layer, adding a contact hole pattern, sputtering metal 1 onto contact hole pattern, silicon nitride layer and the bottom oxidation layer and etching a metal 1 pattern on the sputtered metal such that the method forms a mask design includes a combination of ISFET and metal–oxide–semiconductor field-effect transistor (MOSFET) dice on a single site. .

The present invention consists of several novel features and a combination of parts hereinafter fully described and illustrated in the accompanying description and drawings, it being understood that various changes in the details may be made without departing from the scope of the invention or sacrificing any of the advantages of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be fully understood from the detailed description given herein below and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, wherein:

Figure 1 shows a block diagram of a method of method of fabricating ion-sensitive field-effect transistor (ISFET) device by using Complementary metal-oxide-semiconductor (CMOS) compatible in the present embodiment of the invention;

Figure 2 shows a cross section of a device fabricated using the method in the present embodiment of the invention;

Figure 3 shows a cross section of a MOSFET device to be used as test structure in the method;

Figure 4 shows a cross section of a die including 14 ISFET devices and 1 MOSFET device;

Figure 5 shows contact points of ISFET and MOSFET devices;

Figure 6 shows a layout design of an ISFET device with a window opening for sensing area;

Figure 7 shows an enlarged view of an ISFET sensing area; and

Figure 8 shows a wafer map with 125 dice.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention relates to a method of fabricating ion-sensitive field-effect transistor (ISFET) device by using Complementary metal-oxide-semiconductor (CMOS) compatible. Hereinafter, this specification will describe the present invention according to the preferred embodiment of the present invention. However, it is to be understood that limiting the description to the preferred embodiment of the invention is merely to facilitate discussion of the present invention and it is envisioned that those skilled in the art may devise various modifications and equivalents without departing from the scope of the appended claims.

The following detailed description of the preferred embodiment will now be described in accordance with the attached drawings, either individually or in combination.

Figure 1 illustrates a method of fabricating ion-sensitive field-effect transistor (ISFET) device by using Complementary metal-oxide-semiconductor (CMOS) compatible. The method includes the steps of marking and etching a silicon layer (101), depositing an oxide layer (102), implanting a p-well pattern on the silicon and oxide layers (101, 102), implanting a channel pattern onto the silicon and oxide layers (101, 102), implanting N+ source and drain pattern onto the silicon and oxide layers (101, 102), implanting P+ diffusion pattern onto the silicon and oxide layers (101, 102), removing the oxide layer (102), adding a bottom oxidation layer (103), depositing a silicon nitride layer (104), adding a contact hole pattern (105), sputtering metal 1 onto contact hole pattern (105), silicon nitride layer (104) and the bottom oxidation layer (103) and etching a metal 1 pattern on the sputtered metal such that the method forms a mask design includes a combination of ISFET and metal-oxide-semiconductor field-effect transistor (MOSFET) dice on a single site. .

The fabrication method uses 6 lithography mask layers which include silicon mark etch pattern, P-well implant pattern, N+ source and drain pattern, P+ diffusion pattern, contact hole pattern and Metal 1 pattern.

- 5 The method as described above uses a CMOS compatible process flow. The additional steps of low pressure chemical vapor deposition (LPCVD) bottom oxidation and LPCVD silicon nitride deposition together with post nitride deposition with nitrogen annealing ensures that the fabrication is CMOS compatible.

10 An ISFET sensing membrane includes a thin layer film less than 1000 Angstrom deposited by low pressure chemical vapour deposition (LPCVD) high temperature silicon nitride and a thin layer film less than 1000 Angstrom deposited by LPCVD high temperature bottom silicon oxide.

The metal etching process is done on the silicon nitride sensing membrane which is done in a reactive ion etcher. The metal is etched at a pressure between 6 and 18 mT in a plasma
15 containing Cl_2 gas at a flow rate about 50 and 120 sccm, BCl_3 gas at flow rate about 30 and 50 sccm, CHF_4 gas at flow rate about 5 sccm and Argon gas at flow rate about 50 sccm.

The method as described above uses MOSFET as a test structure in each image lithography shot.

20 In ISFET devices, electric current (I_d) flows from source to drain via channel. Like in MOSFET, channel resistance depends on electric field perpendicular to the direction of the current. Channel resistance also depends on potential difference over silicon nitride gate. Therefore, source-drain current, I_d , is influenced by the interface potential at the silicon nitride/aqueous solution. Although the electric resistance of the channel provides a measure
25 for the silicon nitride potential, the direct measurement of this resistance gives no indication of the absolute value of this potential. However at a fixed source-drain potential (V_{ds}),

changes in the gate potential can be compensated by modulation of the V_{gs} . This adjustment should be carried out in such a way that the changes in V_{gs} applied to the reference electrode are exactly opposite to the changes in the gate oxide potential. This is automatically performed by ISFET amplifier with feedback which allows obtaining constant
5 source-drain current. In this particular case, the gate-source potential is determined by the surface potential at the insulator/electrolyte interface. The selectivity and chemical sensitivity of the ISFET are completely controlled by the properties of the electrolyte/insulator interface.

Figure 2 shows a complete ISFET device as fabricated by the method described above in comparison to Figure 3 that shows a complete MOSFET device.

10 Figure 4 shows a mask design which is a combination of ISFET and metal-oxide-semiconductor field-effect transistor (MOSFET) dice on a single site. In this example in Figure 4, there are 14 ISFET and 1 MOSFET die on a single site. Figure 5 shows contact points of ISFET and MOSFET devices.

15 Figure 6 shows a layout design of ISFET which has a window opening for sensing area after encapsulation to facilitate sensing process. Figure 7 specifically points to an ISFET sensing area. Figure 8 shows an example of a wafer map that includes 125 dice.

20 It is to be appreciated that the method as described herein improves existing fabrication process flow of ISFET devices by using CMOS compatible by optimizing metal etch recipe and including MOSFET test structures.

CLAIMS

1. A method of fabricating ion-sensitive field-effect transistor (ISFET) device by using Complementary metal–oxide–semiconductor (CMOS) compatible, the method includes the steps of:

- i. marking and etching a silicon layer (101);
 - ii. depositing an oxide layer (102);
 - iii. implanting a p-well pattern on the silicon and oxide layers (101, 102);
 - iv. implanting a channel pattern onto the silicon and oxide layers (101, 102);
 - v. implanting N+ source and drain pattern onto the silicon and oxide layers (101, 102);
 - vi. implanting P+ diffusion pattern onto the silicon and oxide layers (101, 102);
 - vii. removing the oxide layer (102);
 - viii. adding a bottom oxidation layer (103);
 - ix. depositing a silicon nitride layer (104);
 - x. adding a contact hole pattern (105);
 - xi. sputtering metal 1 onto contact hole pattern (105), silicon nitride layer (104) and the bottom oxidation layer (103); and
 - xii. etching a metal 1 pattern on the sputtered metal;
- such that the method forms a mask design includes a combination of ISFET and metal–oxide–semiconductor field-effect transistor (MOSFET) dice on a single site.

2. The method as claimed in claim 1, wherein the method uses 6 lithography mask layers which include silicon mark etch pattern, P-well implant pattern, N+ source and drain pattern, P+ diffusion pattern, contact hole pattern and Metal 1 pattern.

3. The method as claimed in claim 1, wherein the method further includes steps of low pressure chemical vapor deposition (LPCVD) bottom oxidation and LPCVD silicon nitride

deposition together with post nitride deposition with nitrogen annealing ensures that fabrication is CMOS compatible.

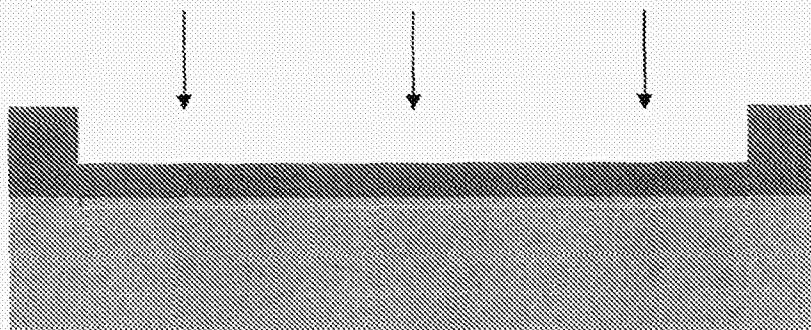
4. The method as claimed in claim 1, wherein the metal etching step is done on the silicon
5 nitride sensing membrane which is done in a reactive ion etcher.
5. The method as claimed in claim 1, wherein MOSFET is used as a test structure in each image lithography shot.
- 10 6. The method as claimed in claim 1, wherein selectivity and chemical sensitivity of the ISFET are completely controlled by properties of electrolyte/insulator interface.
7. The method as claimed in claim 1, wherein the method further includes adding a window opening for sensing area after encapsulation.



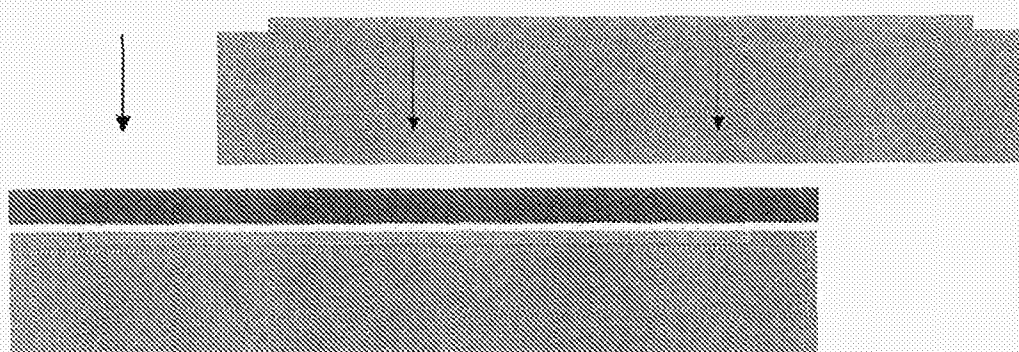
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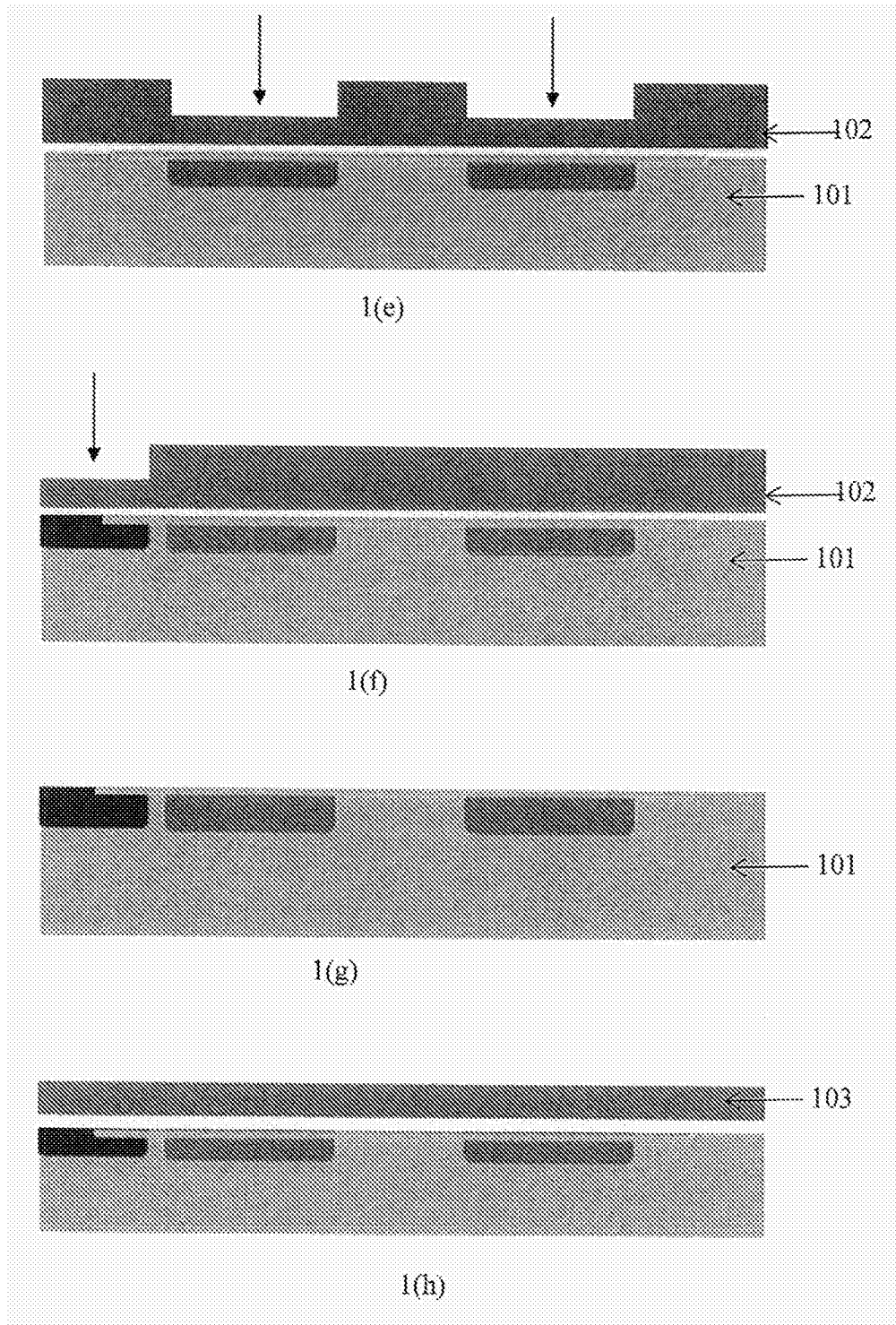
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1(c)

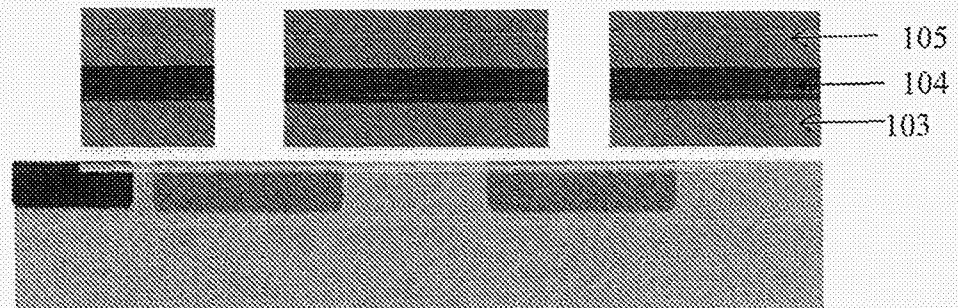


1(d)

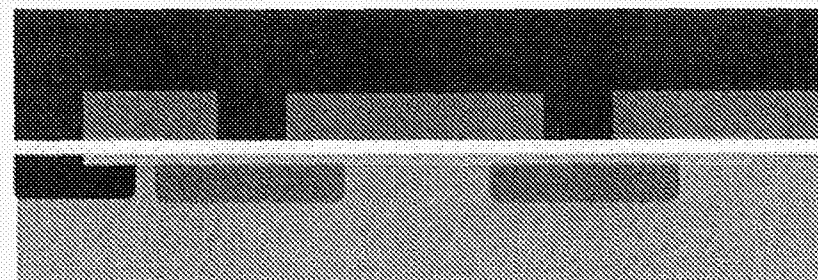




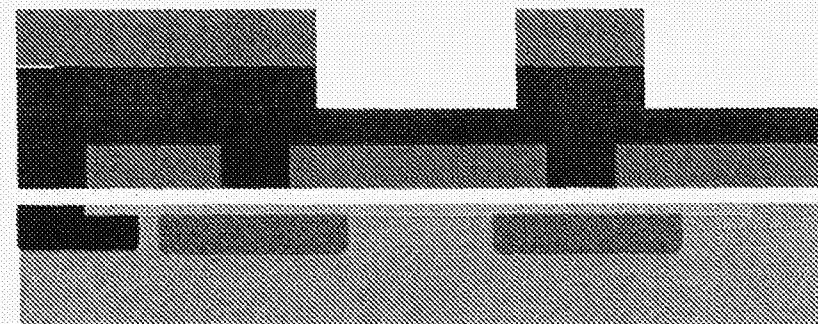
1(i)



1(j)



1(k)



1(l)

Figure 1

ISFET gate is sensing membrane

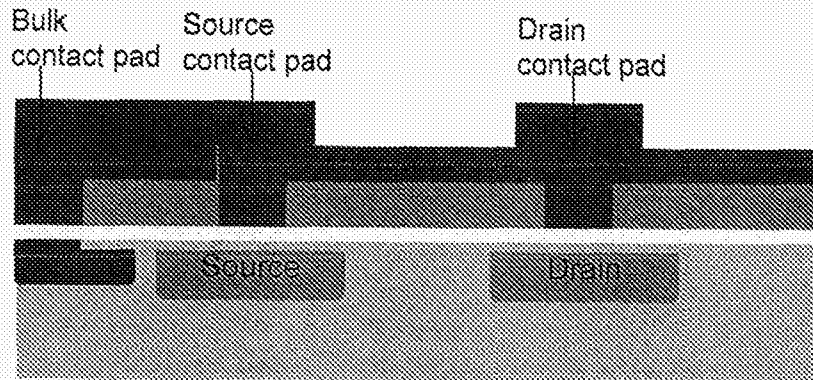


Figure 2: ISFET complete device

MOSFET gate is metal on silicon nitride

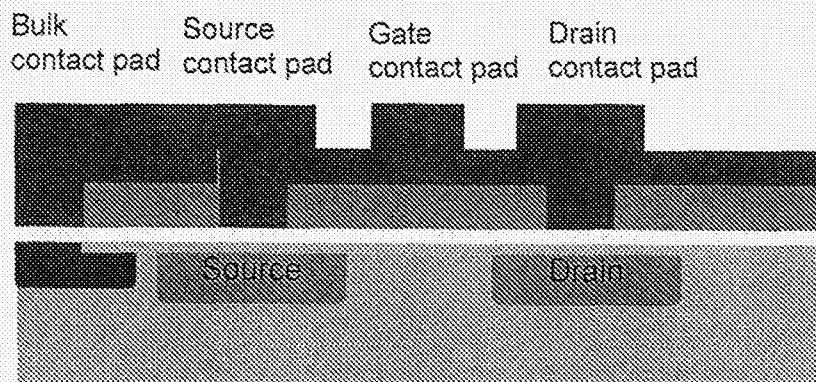


Figure 3: MOSFET complete device

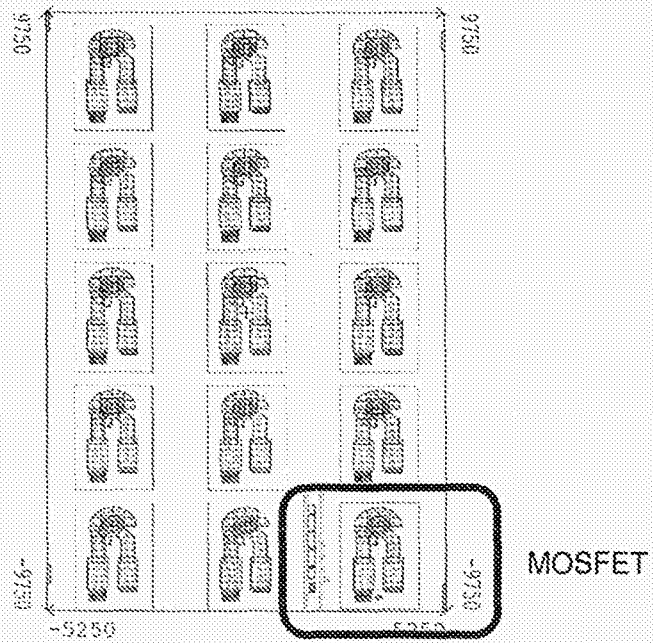


Figure 4: Die comprise of 14 ISFET and 1 MOSFET

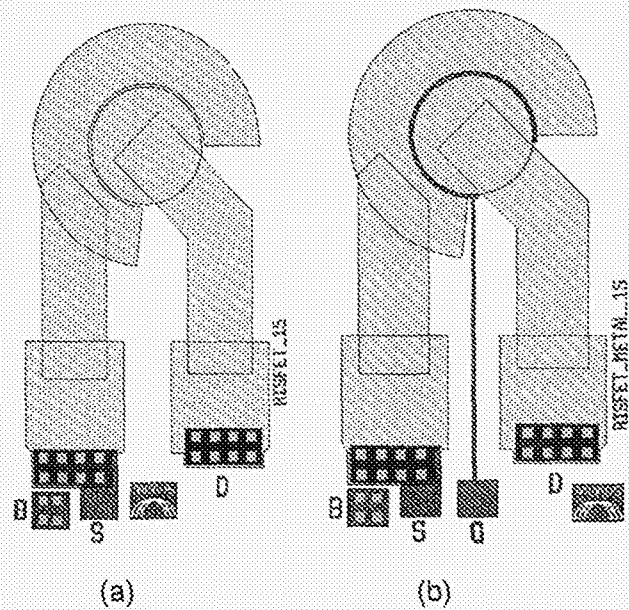


Figure 5: (a) ISFET pH sensor; B=bulk (ground), S=source and D=drain
(b) MOSFET pH sensor; B=bulk (ground), S=source, G=gate, D=drain

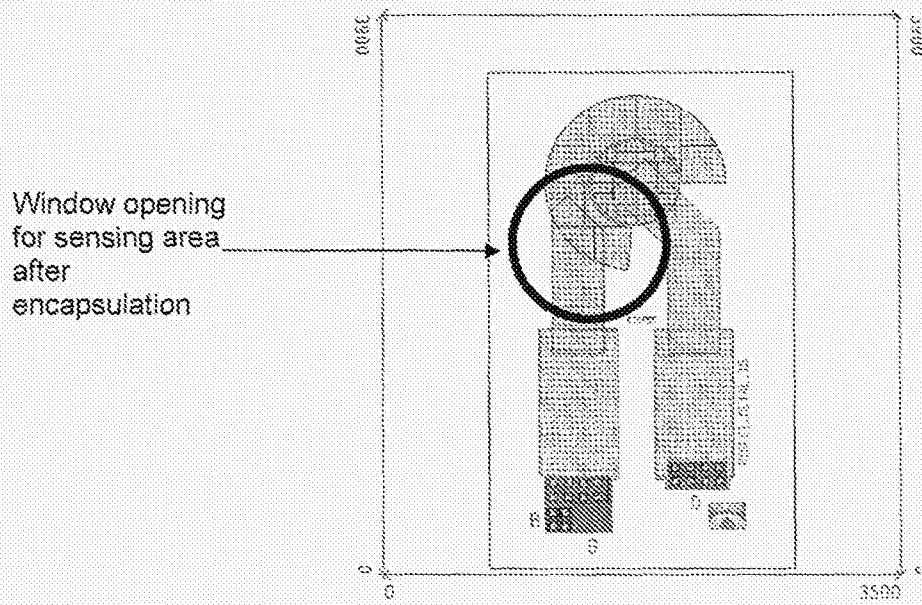


Figure 6: ISFET Layout Design

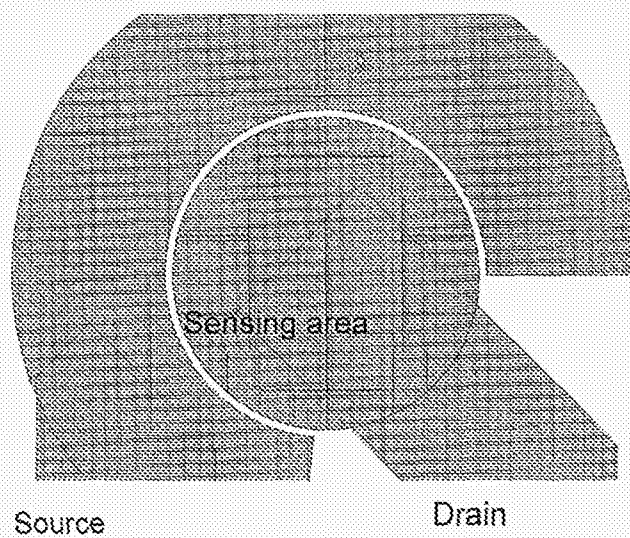


Figure 7: ISFET Sensing Area

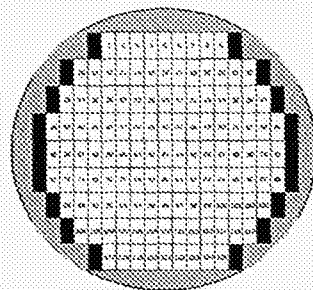


Figure 8: Wafer map comprise 125 dice

INTERNATIONAL SEARCH REPORT

International application No
PCT/MY2014/000091

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01N27/414
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	HASHIM U ET AL: "Silicon nitride gate ISFET fabrication based on four mask layers using standard MOSFET technology", SEMICONDUCTOR ELECTRONICS, 2008. ICSE 2008. IEEE INTERNATIONAL CONFERENCE ON, IEEE, PISCATAWAY, NJ, USA, 25 November 2008 (2008-11-25), pages 626-628, XP031415503, ISBN: 978-1-4244-3873-0 the whole document ----- -/--	1-7



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

9 October 2014

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17/10/2014

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INTERNATIONAL SEARCH REPORT

International application No

PCT/MY2014/000091

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CANE C ET AL: "Compatibility of ISFET and CMOS technologies for smart sensors", TRANSDUCERS. SAN FRANCISCO, JUNE 24 - 27, 1991; [PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON SOLID STATE SENSORS AND ACTUATORS], NEW YORK, IEEE, US, vol. CONF. 6, 24 June 1991 (1991-06-24), pages 225-228, XP010037246, DOI: 10.1109/SENSOR.1991.148843 ISBN: 978-0-87942-585-2 the whole document -----	1-7
A	BOUSSE L ET AL: "A process for the combined fabrication of ion sensors and CMOS circuits", IEEE ELECTRON DEVICE LETTERS, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. 9, no. 1, 1 January 1988 (1988-01-01), pages 44-46, XP011406588, ISSN: 0741-3106, DOI: 10.1109/55.20408 the whole document -----	1-7
A	KWON D H ET AL: "A very large integrated pH-ISFET sensor array chip compatible with standard CMOS processes", SENSORS AND ACTUATORS B: CHEMICAL: INTERNATIONAL JOURNAL DEVOTED TO RESEARCH AND DEVELOPMENT OF PHYSICAL AND CHEMICAL TRANSDUCERS, ELSEVIER S.A, CH, vol. 44, no. 1-3, 1 October 1997 (1997-10-01), pages 434-440, XP004117157, ISSN: 0925-4005, DOI: 10.1016/S0925-4005(97)00207-4 the whole document -----	1-7