United States Patent

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[54] CONSTANT WRITING RATE DISPLAY CONTROL APPARATUS
4 Claims, 10 Drawing Figs.

[73] Assignee Honeywell Inc., Minneapolis, Minn., a corporation of Delaware

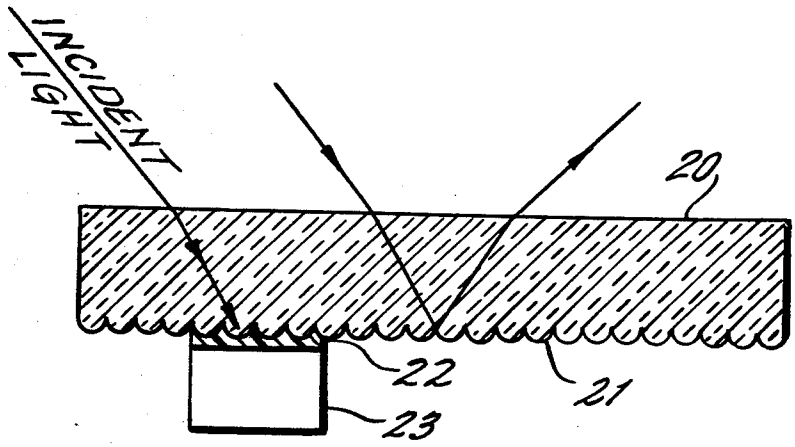
[52] U.S. Cl. 340/324A
[51] Int. Cl. H03k 13/04
G06f 3/14
[50] Field of Search 340/347D/A; 324.1; 315/18; 235/151

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ABSTRACT: A function generator for converting digital signal indicative of quadrature components of a vector into analog signals indicative of the components. The function generator produces a time varied ramp, the time of which is a function of the approximate vector addition of the digital input signals. The ramp always varies between the same two voltages so that when it is applied to a pair of digital to analog converters having the digital signal inputs, the resulting outputs will produce constant writing rate vector signals.



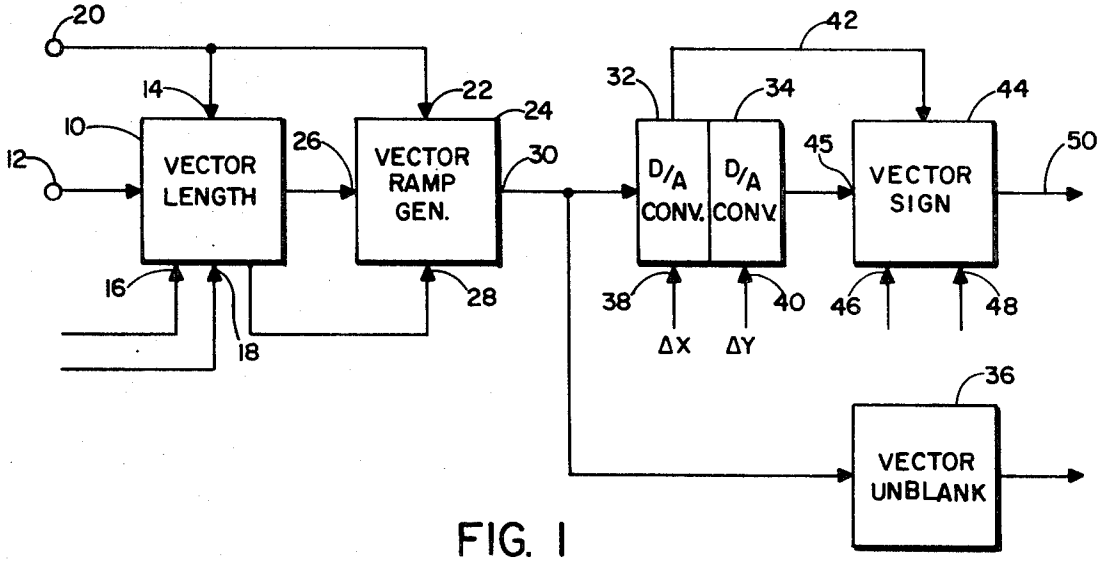


FIG. 1

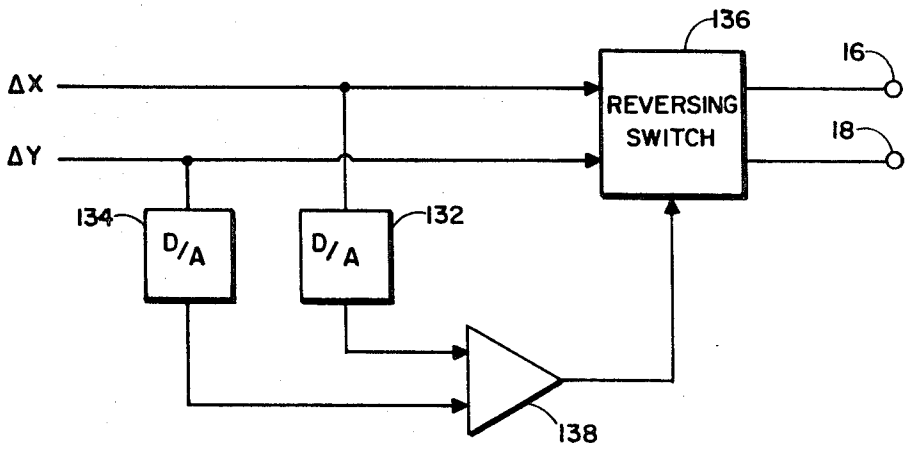


FIG. 6

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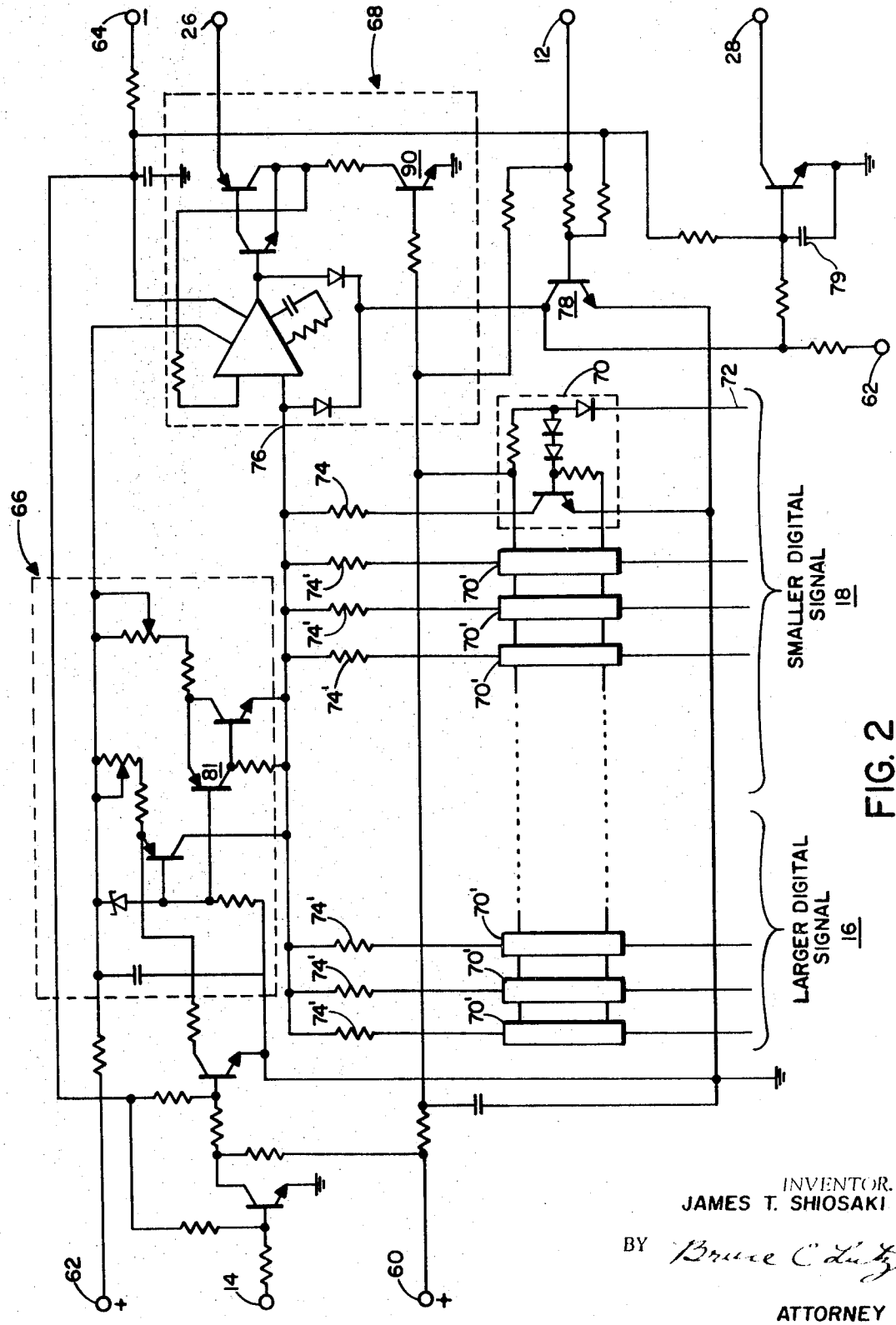


FIG. 2

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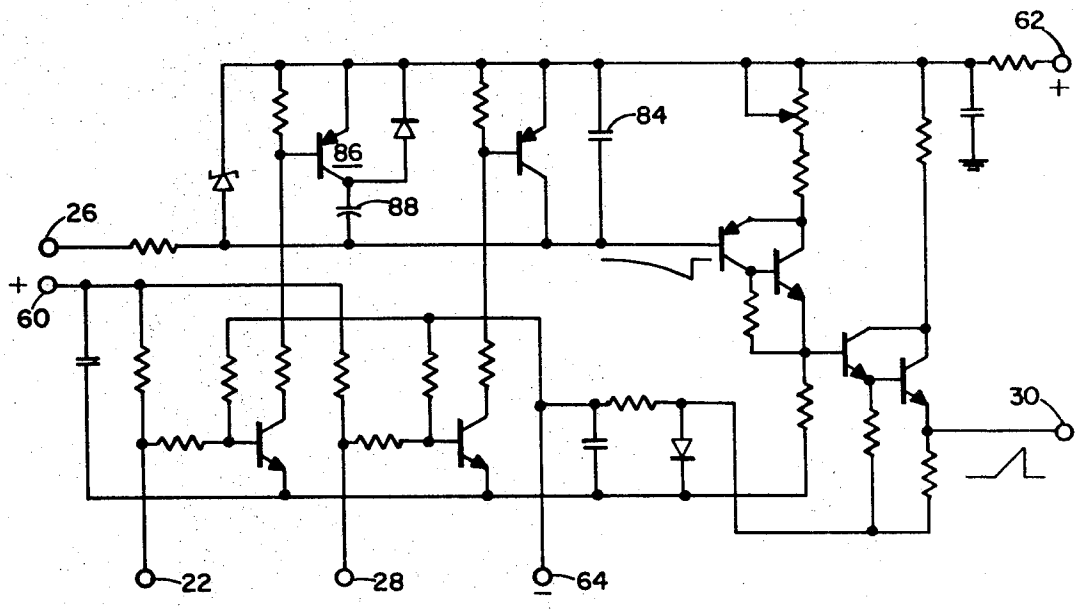


FIG. 3

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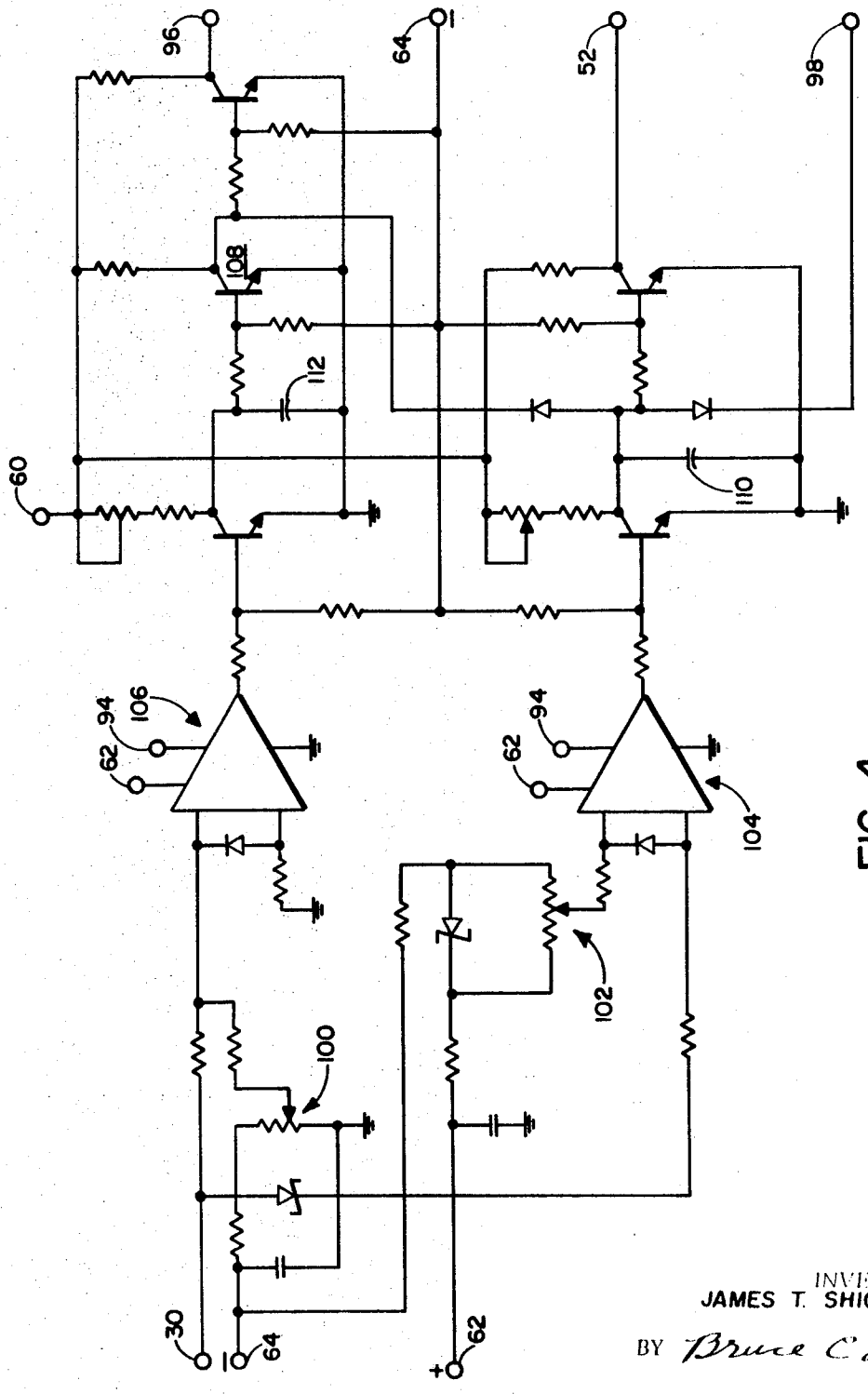


FIG. 4

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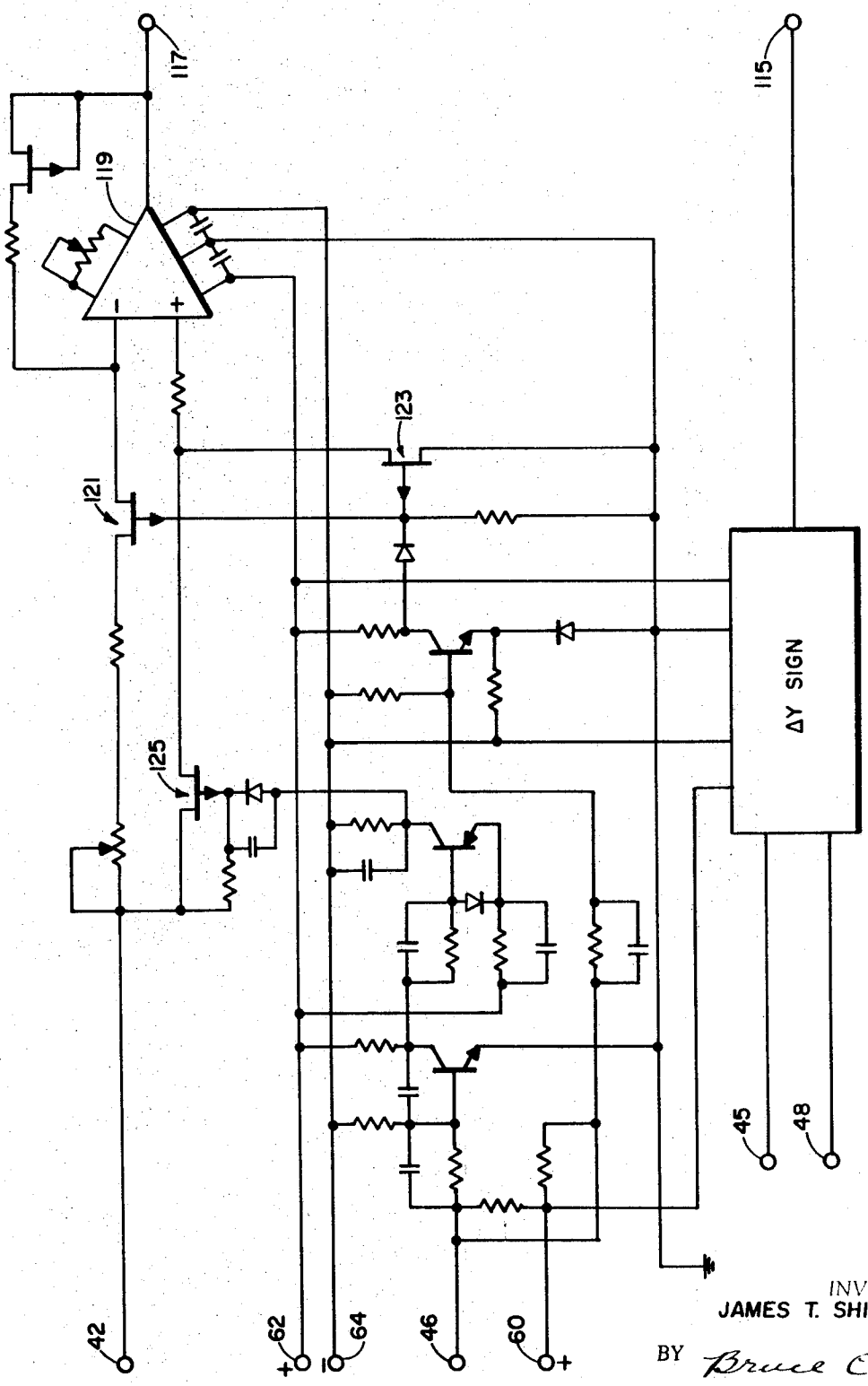


FIG. 5

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THE INVENTION

The present invention is directed mainly toward electronics and more specifically toward a function generator.

The prior art has many function generators, and indeed has many function generators for converting digital signals to be useful in analog displays. Such function generators typically produce variable writing rates, certain effects of which must be overcome by changing the brightness of the display for different vector lengths or by making the brightness high enough for the fastest writing rate, thereby producing an excessively bright signal for low writing rates. The latter solution tends to cause degeneration of the luminescent material on display devices such as cathode ray tubes.

The present invention on the other hand operates to produce a substantially constant writing rate through the use of a time varied ramp whose time is adjusted in accordance with the approximate length of the resulting vector. This ramp always varies between the same two voltages but changes in length in accordance with its generation time. By applying this time varied ramp to a pair of D to A converters, two ramp outputs can be produced which are scaled to be indicative of digital inputs thereto. There is, of course, apparatus for changing the slope sense indicated by the ramp in accordance with the sign of the digital inputs, and further apparatus for blanking the electron gun until such time as unblanking is required. As will be apparent to those skilled in the art, the time that the present invention takes to generate a long vector is proportionately longer than the time it takes to generate a short vector. Thus the brightness of the display is uniform without adjustment of the brightness signal.

It is therefore an object of the present invention to produce better vector generating apparatus.

Further objects and advantages of the present invention will be apparent from a reading of the specification and appended claims in conjunction with the drawings wherein:

FIG. 1 is a block diagram of a complete vector function generator system;

FIGS. 2–5 are schematic diagrams of various blocks in FIG. 1; and

FIG. 6 is a logic system for detecting and selectively applying the larger of two sets of digital signals to appropriate outputs thereof.

Referring now to FIG. 1, a vector length block **10** is shown with a vector start input terminal **12**, a long vector signal input **14** and two sets of digital signal inputs **16** and **18**. The digital input **16** receives the greater of the ΔX and ΔY inputs while input **18** receives the lesser of the ΔX and ΔY inputs. An input terminal **20** supplies the long vector input to input **14** of vector length block **10** and also to an input **22** of a vector ramp generator **24**. Vector ramp generator **24** receives a first input at **26** from vector length block **10** which is indicative of the reciprocal of the approximate vector addition of the two digital inputs and also receives an input at **28** to provide a delayed start for the vector generation. An output **30** of generator **24** supplies an input to a pair of vector digital to analog converters **32** and **34** which are shown in one large block, and also supplies an input to a vector unblank circuit **36**.

Each of the digital to analog converters **32** and **34** may be any type of converter capable of accepting a reference voltage varying from −1 V. to +10 V. One example is one of the AN 1,000 Series variable reference digital to analog converters sold by Analogic Company of Waltham, Massachusetts. However, any of many types may be utilized.

The digital to analog converters **32** and **34** have respectively ΔX and ΔY digital inputs **38** and **40** which receive the same digital input signals supplied to vector length block **10**. An output **42** of converter **32** is supplied to a vector sign block **44** which is also supplied with an input **45** from converter **34**. The sign portion of the ΔX and ΔY digital inputs are supplied to vector sign block **44** as inputs **46** and **48** respectively. The vector sign block **44** produces a pair of signals shown at output **50** which are supplied to summing amplifiers of appropriate display equipment, while vector unblank **36** has an output **52** which is supplied to a brightness control of the display.

The vector length block **10** receives the two digital inputs and combines these in a digital to analog converter to produce an output at **26** which is indicative of the vector addition. It has been determined experimentally and proven mathematically that a vector can be generated according to formula

$$L = 0.96U + 0.4V$$

where

L = vector length
U = ΔX or ΔY which ever is greater and
V = ΔX or ΔY which ever is lesser.

The vector length unit L which results from this approximation is never in error by more than 4 percent.

In one embodiment of the invention the vector ramp generator always varied between −1 and 10 volts. However, the time necessary for generation of this signal is varied by the input **26**. In the embodiment shown, the input **26** is a current whose magnitude is controlled by the vector approximation signal generated in vector length block **10**. Thus, the current regulates the charging time necessary to obtain the 10 volt maximum amplitude.

The writing rate on the display will, of course, be determined by the voltage change per unit time. As will be further determined, a quickly generated ramp in generator **24** will have a faster or higher voltage change per unit time than will a long ramp.

These ramps are supplied to the two converters **32** and **34** and the outputs from the two converters are scaled in proportion to the ΔX and ΔY input signals. Thus, the outputs on **42** and **45** are normally of lesser amplitude than the input signal supplied from terminal **30**. These signals on **42** and **45** are supplied to the sign block **44** for correction as to sign in accordance with the sign portion of the digital signals. The corrected ramps are then summed with positioning signals and supplied to the CRT or other display equipment. The vector unblank circuit block **36** used to blank out the display until such time as a ramp is which has reached its zero crossover point is received.

The present invention is designed for use with a master deflection system whereby incremental changes in the electron beam position may be produced. The vector generator of the present invention is useful in such a system for purposes such as writing letters or producing figures on a display. While the circuitry of the present invention can be used to deflect an electron beam to any point on a CRT face, it can normally be more profitably utilized to merely make incremental changes in the display while leaving the major deflections of the electron beam to a master control system.

Reference will now be made to FIG. 2 which illustrates the vector length block **10**. The digital signals are supplied to a weighted resistor network to change the digital signals into an analog signal indicative of the inverse of 0.96 times the larger vector component plus 0.4 times the smaller vector component. Power is supplied to a terminal **60** while the long vector signal is supplied to terminal **14** as shown in FIG. **1**. Further positive power is supplied to a terminal **62** while negative power is supplied to a terminal **64**. The vector start terminal **12** is also shown as well as output **28** for providing the delayed start signal. The circuits shown within blocks **66** and **68** function as current sources. Block **70** illustrates in detail one step of the weighted resistor network digital to analog converter. Signals supplied to an input **72** actuate or leave unactuated a transistor switch within the block **70**, depending upon the value of digital input such signals. In other words, if the signal represents a one, the transistor will be actuated and complete a current path through a resistor

74. If it represents a zero, resistor 74 will remain in an unused condition. Each of the other blocks 70' in the circuit contain circuitry similar to that of circuit 70. Specifically, each of these blocks 70' contains a switch which determines whether or not a resistor 74' is used. The switch is actuated in response to a particular digital signal. The selection of the greater or lesser digital signal 16 or 18 can be performed with exclusive OR gating or alternatively by the apparatus shown in FIG. 6.

Normally, current is supplied to the resistor network from current source 66. The larger the digital input signals, the more resistors connected in parallel to ground, thus reducing the resistance and lowering the voltage supplied at an input 76 to current source 68. Transistor 78 is normally in an ON condition due to the bias current from input 60. However, when a vector start signal is received at terminal 12, transistor 78 is turned OFF, thus disconnecting the operational amplifier in current source 68 from ground. The switching action of transistor 78 is transmitted to output 28 after a capacitor 79 is charged sufficiently to cause a transistor associated therewith to turn ON. At this time the analog signal at input 76 will operate the operational amplifier to produce a current signal at terminal 26 which is inversely proportional to the approximate vector length of the vectorally combined digital inputs. Transistor 90 within current charging circuit 68 operates for temperature compensation only and is not affected by the vector start signal.

An input supplied to long vector input 14 will change the current output of block 66 by altering the bias to transistor 81 contained therein. In other words, with a long vector signal at input 14, the current generator 66 current output is increased. The higher current provides a more accurate output since it is less subject to errors due to noise signals. Of course, compensation has to be made for the higher current output at a later portion in the circuit. This is accomplished in the vector ramp generator shown in FIG. 3.

The vector ramp generator of FIG. 3 has a vector current input 26, a long vector input 22, a vector start input 28, and a ramp output 30 as shown in FIG. 1. In addition, there are positive input terminals 60 and 62 and a negative power input 64 as shown in FIG. 2. The capacitor 84 is the regular charging capacitor and it produces a negative going ramp such as shown in the diagram. This is reversed to produce a positive going ramp at output 30 through the action of the associated transistors. A long vector signal at input 22 operates to turn ON a transistor generally designated as 86 to connect in the circuit a capacitor 88 which, in the long vector, operates in parallel with capacitor 84. Thus, compensation for the increased current due to the change in bias in current generator 66 is by the increased capacitance added by capacitor 88 to make the charging rate the same as it would be without the long vector signal, while operating to overcome the effects of noise, etc., which occur with small current charging rates. A positive signal at input 28 is utilized to discharge capacitor 84 and/or 88 to zero for proper operation. A ground input at 28 will allow the capacitor 84 to charge.

FIG. 4 is the vector unblank circuit of block 36 in FIG. 1. Negative power inputs 64 are again shown as well as power terminals 60 and 62. Reference numeral 94 identifies an additional negative power terminal. Also shown is terminal 30 representing the input to the vector unblank circuit and an output terminal 52. Normally, the signal at terminal 52 is a positive signal to blank out the electron beam. However, during generation of a ramp, the output at 52 drops to a zero value so that the electron beam may be displayed. An output 96 is utilized to signal the computer or other digital generator that the vector generation is complete, while an input 98 is used to indicate a border limit of the display so that an overrun outside the display face is not produced. In one embodiment of the invention a potentiometer generally designated as 100, is set to establish a −10 volt reference while a further potentiometer designated as 102 is set to establish a 0 volt reference. When the input signal rises to 0 volts, it will overcome the input at an operational amplifier 104 to change the output from a positive to a negative signal. The negative signal will operate through two phase inverting transistors to produce a negative going signal at output 52. Capacitor 110 provides a compensating delay in the response. As the input further rises it will eventually reach 10 volts at which time it will overcome the negative signal from potentiometer 100 and produce a negative going output at the output of an operational amplifier 106. A negative going output at this point will produce a positive going output at terminal 96. When the output of amplifier 106 goes negative, the collector of a transistor 108 in the string of output transistors will also go negative and discharge a capacitor 110 in the lower string of transistors to reset the circuit and allow terminal 52 to rise to a positive voltage again. A capacitor 112 is momentarily charged by the change in output potential from amplifier 106 to provide a compensating delayed output at 96.

FIG. 5 illustrates a vector sign control circuit such as used in block 44. This circuit adjusts the polarity of the output ramp with respect to the input in accordance with the sign of the digital signals. Terminals 46, 48, as well as 42 and 45 are shown. In addition there are power terminals such as 62, 64, and 60 as previously mentioned. The schematic diagram in the upper portion of FIG. 5 is duplicated in the block in the lower portion which is designated as "ΔY sign". In other words, there are two identical circuits. However, for purposes of simplicity, only one is shown in detail. An output terminal 115 produces the ΔY ramp output while an output terminal 117 produces the ΔX ramp output.

The ΔX ramp input signal is supplied at terminal 42 and applied to an operational amplifier 119 at either an upper or a lower input, designated as "—" and "+" respectively. The circuitry is designed such that the amplifier will not receive inputs at both places at once. In normal operation, an input is supplied through the upper input through an FET 121, while the noninverting (+) input is grounded through an FET 123. If the sign is to be changed from the normal condition, a positive signal is applied at terminal 46 to turn an FET 125 ON and turn FETs 121 and 123 OFF. While it is necessary to ground the noninverting input of operational amplifier 119 when an input is supplied to the inverting input, it is undesirable to ground the inverting input when a signal is supplied to the noninverting input because doing so will change the gain of the amplifier. The circuit as shown will produce a gain of one for a signal supplied to either input. Thus the sense of the input ramp is inverted or left unaltered in accordance with the input signals at terminal 46.

While the circuit of FIG. 5 has been described and discussed in detail as means for determining the sense of a ramp signal, there are also other satisfactory methods for performing this function. For example bipolar transistors may be used to connect the input signal to either the inverting or non-inverting input of the differential operational amplifier to obtain polarity reversal. In other words, FET 121 can be replaced with a bipolar transistor having one electrode connected to ground and another connected through a resistor to the minus input of the amplifier; FET 125 can be replaced with a resistor, and FET 123 can be replaced with a bipolar transistor.

FIG. 6 illustrates one means of choosing the greater or lesser of two digital inputs. The ΔX input is supplied to a D to A converter 132 while the ΔY input is supplied to a D to A converter 134. Both inputs are also supplied to an exclusive OR circuit or reversing switch means 136. The larger of the two digital input signals will operate to switch a differential amplifier 138 and thus affect the position of reversing switch 136. The result will be that the larger of the two signals is always supplied to the same output, such as output 16, of the reversing switch 136. The components 132, 134 and 138 comprise a sensing circuit which may be designated as an replaced by a digital subtractor. Such a subtractor would provide the same function.

In summary, while I believe there is invention in the overall system, I further believe that there are several subcom-

binations in the specific circuitry which are inventive. Examples of these are the polarity inverting amplifier as shown in FIG. 5. and a circuitry of FIG. 2 for providing an analog output which is the inverse of a digital input and for providing vector addition of digital signals representing quadrature vector components.

The specific schematic diagrams utilized to show the contents of the various blocks of FIG. 1 have been very sketchily illustrated since the schematic diagrams other than those in Vector Length block 10 and Vector Sign block 44 are not believed to contain inventive circuitry, but represent implementations which are obvious to those skilled in the art basic. It is apparent that other implementations of the block diagram will be realized by those skilled in the art. I wish to be limited only to a function generator which will produce constant writing rates on a display as the result of operations on digital input signals.

I claim:

1. In apparatus of the type which provides a visual display formed of a succession of line segments produced at predetermined substantially identical writing rates, each line segment being produced in response to a pair of digital signals indicative of quadrature components thereof, the improvement which comprises:

approximation means for converting a first digital signal into a first analog signal continuously representing 0.96 times the first digital signal, converting a second digital signal into a second analog signal continuously representing 0.40 times the second digital signal, and adding the first and second analog signals to produce an output signal;

means for supplying a pair of digital signals indicative ot quadrature components of a line segment to said approximation means so that the larger of said pair of digital signals is always supplied as said first digital signal and the smaller of said pair of digital signals is always supplied as said second digital signal, whereby the magnitude of the analog output signal produced by said approximation means is approximately proportional to the length of the line segment indicated by the pair of digital signals;

ramp generation means for producing an output signal whose magnitude varies linearly from a first value to a second value in response to a constant input signal at a rate dependent on the magnitude of the input signal;

means for supplying the output signal of said approximation means as the input signal of said ramp generation means;

digital to analog conversion means for producing third and fourth analog signals whose magnitudes are proportional to the magnitude of an analog input signal, the constants of proportionality being determined by third and fourth digital signals respectively;

means for supplying the output signal of said ramp generation means as the analog input signal of said digital to analog conversion means; and

means for supplying said pair of digital signals indicative of quadrature components of the line segment as the third and fourth digital input signals to said digital to analog conversion means, the third and fourth analog signals being adapted to cause formation of a visual display on display apparatus at a predetermined writing rate regardless of the length of the line segment to be formed.

2. The apparatus of claim 1 wherein the third and fourth analog signals produced by said digital to analog conversion means always have the same polarity as the output signal from said ramp generation means; and wherein is further included sign determination means connected to receive the third and fourth analog signals and operable to produce fifth and sixth analog signals whose magnitudes correspond to the magnitudes of the third and fourth analog signals, but whose polarities are determined by third and fourth digital signals.

3. The apparatus of claim 2 further including:

means for producing a characteristic output signal in response to an input signal having greater than a predetermined magnitude; and

means for supplying the output signal of said ramp generation means as the input signal of said last named means, the characteristic signal produced by said last named means comprising a blanking signal adapted to permit formation of a visual display on display apparatus only when the output signal of said ramp generation means exceeds said predetermined magnitude.

4. The apparatus of claim 3 wherein the output signal of said approximation means comprises a current signal whose magnitude is determined by said pair of digital signals, said approximation means further including means for stepping up the output signal current from said approximation means in response to an additional input signal; and

said ramp generation means comprises capacitor means which is charged by the current produced by said approximation means, said ramp generation means further including means for increasing the capacitance of said capacitor means in response to said additional signal.

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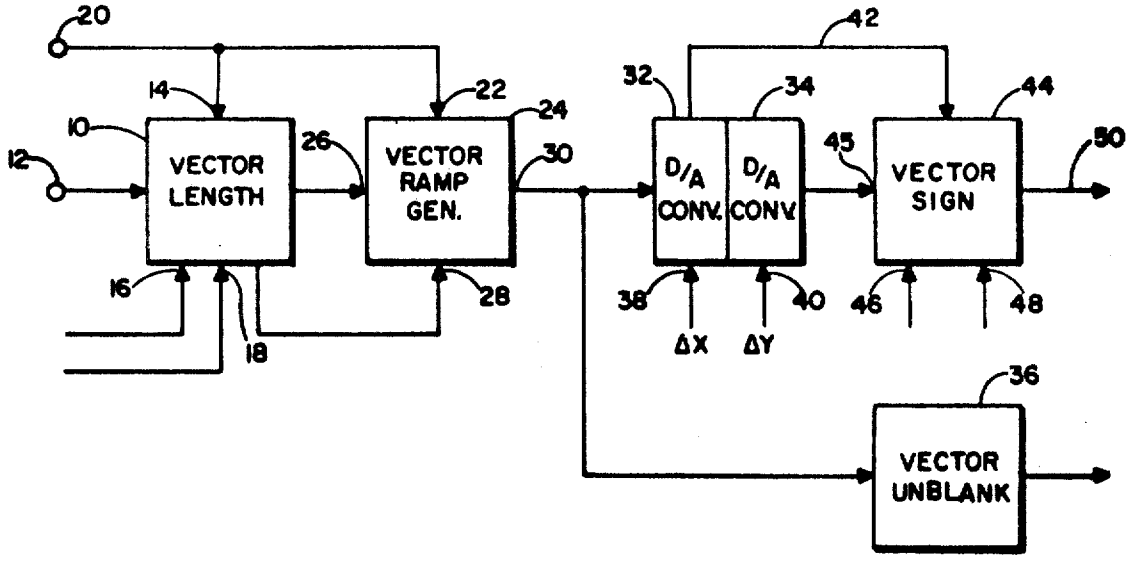
CERTIFICATE OF CORRECTION

Patent No. 3,588,871 Dated June 28, 1971

Inventor(s) James T. Shiosaki

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

On the Abstract page cancel the illustrative drawing and insert the drawing shown below:



Signed and sealed this 22nd day of August 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents

USCOMM-DC 60376-P69
* U.S. GOVERNMENT PRINTING OFFICE : 1969 O—366-334.