

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization

International Bureau



WIPO | PCT



(10) International Publication Number

WO 2013/094772 A1

(43) International Publication Date

27 June 2013 (27.06.2013)

(51) International Patent Classification:

*H01L 29/786* (2006.01)    *H01L 21/8244* (2006.01)  
*G02F 1/1368* (2006.01)    *H01L 27/105* (2006.01)  
*H01L 21/336* (2006.01)    *H01L 27/108* (2006.01)  
*H01L 21/8242* (2006.01)    *H01L 27/11* (2006.01)

(21) International Application Number:

PCT/JP2012/083764

(22) International Filing Date:

19 December 2012 (19.12.2012)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

2011-282509 23 December 2011 (23.12.2011)    JP

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))



WO 2013/094772 A1

(54) Title: SEMICONDUCTOR DEVICE

(57) **Abstract:** Provided is a transistor which includes an oxide semiconductor film and has stable electrical characteristics. In the transistor, over an oxide film which can release oxygen by being heated, a first oxide semiconductor film which can suppress oxygen release at least from the oxide film is formed. Over the first oxide semiconductor film, a second oxide semiconductor film is formed. With such a structure in which the oxide semiconductor films are stacked, the oxygen release from the oxide film can be suppressed at the time of the formation of the second oxide semiconductor film, and oxygen can be released from the oxide film in later-performed heat treatment. Thus, oxygen can pass through the first oxide semiconductor film to be favorably supplied to the second oxide semiconductor film. Oxygen supplied to the second oxide semiconductor film can suppress the generation of oxygen deficiency, resulting in stable electrical characteristics.

## DESCRIPTION

## SEMICONDUCTOR DEVICE

## 5 TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device including an oxide semiconductor.

[0002]

10 In this specification, a semiconductor device refers to a device which can function by utilizing semiconductor characteristics; a transistor, an electro-optical device, a semiconductor circuit, and an electronic device are all included in the category of the semiconductor device.

## 15 BACKGROUND ART

[0003]

20 A technique by which transistors are formed using semiconductor thin films formed over a substrate having an insulating surface has been attracting attention. The transistor is applied to a wide range of electronic devices such as an integrated circuit (IC) or an image display device (display device). A silicon-based semiconductor material is widely known as a material for a semiconductor thin film applicable to a transistor. As another material, an oxide semiconductor has been attracting attention.

[0004]

25 For example, a transistor including an amorphous oxide semiconductor film containing indium (In), gallium (Ga), and zinc (Zn) as an active layer is disclosed (see Patent Document 1).

[Reference]

[Patent Document]

[0005]

30 [Patent Document 1] Japanese Published Patent Application No. 2006-165528

## DISCLOSURE OF INVENTION

[0006]

A transistor including an oxide semiconductor film operates faster (it can also be said that the field effect mobility is higher) than a transistor including an amorphous silicon film and is manufactured more easily than a transistor including a polycrystalline silicon film.

[0007]

However, some problems of the transistor including an oxide semiconductor film have been pointed out. One of the problems is unstable electrical characteristics of the transistor. Specifically, a problem that the threshold voltage of the transistor is negatively shifted by a bias-temperature stress test (also referred to as a BT stress test) or irradiation with visible light or ultraviolet light, so that the transistor tends to be normally on has been pointed out. As one of factors of the problem, oxygen deficiency in the oxide semiconductor film can be given.

[0008]

When the oxide semiconductor film is amorphous, for example, the bonding state of metal atoms and oxygen atoms in the oxide semiconductor film is not ordered; thus, oxygen deficiency is likely to be generated. For this reason, the electrical characteristics (e.g., electrical conductivity) of the oxide semiconductor film might be changed. Such a change can cause variations in the electrical characteristics of a transistor, which leads to a reduction in reliability of a semiconductor device including the transistor.

[0009]

One example of a method for reducing oxygen deficiency generated in an oxide semiconductor film is to supply oxygen to the oxide semiconductor film from an oxide film or the like formed in the vicinity of the oxide semiconductor film so that the oxygen deficiency can be repaired. However, before the formation of the oxide semiconductor film (in other words, before the oxygen supply to the oxide semiconductor film), heat treatment or the like in a manufacturing process might cause oxygen to be released from the oxide film or the like formed in the vicinity of the oxide semiconductor film, which would result in insufficient supply of oxygen to the oxide semiconductor film.

[0010]

In view of the above problem, an object of one embodiment of the present invention is to provide a transistor which includes an oxide semiconductor film and has stable electrical characteristics.

[001 1]

5 Over an oxide film which can release oxygen by being heated, a first oxide semiconductor film which can suppress the oxygen release at least from the oxide film is formed. Over the first oxide semiconductor film, a second oxide semiconductor film is formed. With such a structure in which the oxide semiconductor films are stacked, the oxygen release from the oxide film can be suppressed at the time of the formation of  
10 the second oxide semiconductor film, and oxygen can be released from the oxide film in later-performed heat treatment. Thus, oxygen can pass through the first oxide semiconductor film to be favorably supplied to the second oxide semiconductor film. Oxygen supplied to the second oxide semiconductor film can suppress the generation of oxygen deficiency, resulting in stable electrical characteristics.

15 [0012]

The first oxide semiconductor film and the second oxide semiconductor film are each an oxide film containing at least indium, gallium, and zinc; the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film. Being formed over  
20 the first oxide semiconductor film containing the same kinds of materials, the second oxide semiconductor film can have a crystal that grows from the interface with the first oxide semiconductor film. More details will be described below.

[0013]

One embodiment of the present invention is a semiconductor device including  
25 a first oxide semiconductor film; and a second oxide semiconductor film formed over the first oxide semiconductor film. The first oxide semiconductor film and the second oxide semiconductor film are each an oxide film containing at least indium, gallium, and zinc, and the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor  
30 film.

[0014]

Another embodiment of the present invention is a semiconductor device

including a first oxide semiconductor film formed over an oxide film; a second oxide semiconductor film formed over the first oxide semiconductor film; a gate insulating film formed over the second oxide semiconductor film; and a gate electrode which is in contact with the gate insulating film and formed in a region overlapping with the second oxide semiconductor film. The first oxide semiconductor film and the second oxide semiconductor film are each an oxide film containing at least indium, gallium, and zinc, and the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film.

[0015]

10 In this specification and the like, the term content percentage means the proportion of a component in a film, and is particularly often referred to for the first oxide semiconductor film and the second oxide semiconductor film.

[0016]

15 Another embodiment of the present invention is a semiconductor device including a first oxide semiconductor film formed over an oxide film; a second oxide semiconductor film formed over the first oxide semiconductor film; a gate insulating film formed over the second oxide semiconductor film; a gate electrode which is in contact with the gate insulating film and formed in a region overlapping with the second oxide semiconductor film; a protective insulating film formed over the gate electrode; 20 an interlayer insulating film formed over the protective insulating film; and a source electrode and a drain electrode which are formed over the interlayer insulating film and electrically connected to the second oxide semiconductor film. The first oxide semiconductor film and the second oxide semiconductor film are each an oxide film containing at least indium, gallium, and zinc, and the first oxide semiconductor film has 25 a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film.

[0017]

30 Another embodiment of the present invention is a semiconductor device including a first oxide semiconductor film formed over an oxide film; a second oxide semiconductor film formed over the first oxide semiconductor film; a gate insulating film formed over the second oxide semiconductor film; a gate electrode which is in contact with the gate insulating film and formed in a region overlapping with the second

oxide semiconductor film; a protective insulating film formed over the gate electrode; an interlayer insulating film formed over the protective insulating film; a first opening and a second opening which are formed in the gate insulating film, the protective insulating film, and the interlayer insulating film; and a source electrode and a drain electrode which are embedded in the first opening and the second opening and electrically connected to the second oxide semiconductor film. The first oxide semiconductor film and the second oxide semiconductor film are each an oxide film containing at least indium, gallium, and zinc, and the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film.

[0018]

Another embodiment of the present invention is a semiconductor device including a first oxide semiconductor film formed over an oxide film; a second oxide semiconductor film formed over the first oxide semiconductor film; a gate insulating film formed over the second oxide semiconductor film; a gate electrode which is in contact with the gate insulating film and formed in a region overlapping with the second oxide semiconductor film; an insulating film formed in a region overlapping with the gate electrode; a sidewall insulating film formed along a side surface of the gate electrode and a side surface of the insulating film in a cross section taken along a channel length; a source electrode and a drain electrode which are in contact with the sidewall insulating film and electrically connected to the second oxide semiconductor film; and a protective insulating film and an interlayer insulating film which are formed at least over the source electrode and the drain electrode. The first oxide semiconductor film and the second oxide semiconductor film are each an oxide film containing at least indium, gallium, and zinc, and the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film.

[0019]

Another embodiment of the present invention is a semiconductor device including a first oxide semiconductor film formed over an oxide film; a second oxide semiconductor film formed over the first oxide semiconductor film; a gate insulating film formed over the second oxide semiconductor film; a gate electrode which is in

contact with the gate insulating film and formed in a region overlapping with the second oxide semiconductor film; a source electrode which is in contact with one side surface of the second oxide semiconductor film and a drain electrode which is in contact with the other side surface of the second oxide semiconductor film in a cross section taken 5 along a channel length; a first conductive film formed along one side surface of the gate electrode; a second conductive film formed along the other side surface of the gate electrode; a sidewall insulating film formed along a side surface of the first conductive film and a side surface of the second conductive film; and a protective insulating film and an interlayer insulating film which are formed at least over the gate electrode, the 10 source electrode, and the drain electrode. The first oxide semiconductor film and the second oxide semiconductor film are each an oxide film containing at least indium, gallium, and zinc, and the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film.

15 [0020]

In any of the above structures, at least part of the first conductive film is formed over the source electrode with the gate insulating film interposed therebetween, and at least part of the second conductive film is formed over the drain electrode with the gate insulating film interposed therebetween.

20 [0021]

The first conductive film and the second conductive film formed in this manner to be in contact with the gate electrode can have the regions (also referred to as Lov regions) that overlap with the source electrode and the drain electrode with the gate insulating film interposed therebetween. Accordingly, a reduction in on-state current 25 due to miniaturization can be suppressed.

[0022]

Another embodiment of the present invention is a semiconductor device including a first oxide semiconductor film formed over an oxide film; a second oxide semiconductor film formed over the first oxide semiconductor film; a gate insulating film formed over the second oxide semiconductor film; a gate electrode which is in contact with the gate insulating film and covers a top surface and a side surface of the second oxide semiconductor film; a protective insulating film and an interlayer 30

insulating film which are formed over the gate electrode; a source electrode and a drain electrode each of which is in contact with a side surface of the second oxide semiconductor film in an opening penetrating through the interlayer insulating film, the protective insulating film, the gate insulating film, and the second oxide semiconductor film in a cross section taken along a channel length. The first oxide semiconductor film and the second oxide semiconductor film are each an oxide film containing at least indium, gallium, and zinc, and the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film.

10 [0023]

In any of the above structures, it is preferable that the source electrode and the drain electrode each have a surface which is planarized by chemical mechanical polishing treatment.

[0024]

15 Formation of the source electrode and the drain electrode each of which has the surface planarized by chemical mechanical polishing treatment does not require etching treatment using a resist mask, enabling precise processing accurately even in the case where the widths of the source electrode and the drain electrode in the channel length direction are scaled-down.

20 [0025]

In any of the above structures, it is preferable that the first oxide semiconductor film include a low-resistance region and a high-resistance region, the high-resistance region being located at least outside the second oxide semiconductor film.

[0026]

25 The high-resistance region of the first oxide semiconductor film is formed outside the second oxide semiconductor film to serve as a separation layer between transistors. Such a structure can prevent electrical connection between adjacent transistors.

[0027]

30 In any of the above structures, the second oxide semiconductor film preferably includes a channel region and a pair of low-resistance regions which are in contact with the channel region. The formation of the pair of low-resistance regions which are in

contact with the channel region in the second oxide semiconductor film can lower contact resistances between the second oxide semiconductor film and the source electrode, and between the second oxide semiconductor film and the drain electrode.

[0028]

5 In any of the above structures, the second oxide semiconductor film preferably includes a high-resistance region on either end thereof in the channel width direction. The formation of the high-resistance region on either side of the second oxide semiconductor film in the channel width direction can suppress the generation of a parasitic channel in the second oxide semiconductor film.

10 [0029]

In any of the above structures, the content percentage of gallium is preferably higher than or equal to that of indium in the first oxide semiconductor film, and the content percentage of indium is higher than that of gallium in the second oxide semiconductor film. When the content percentage of indium is higher than gallium in 15 the second oxide semiconductor film, the second oxide semiconductor film can have higher crystallinity.

[0030]

20 In any of the above structures, it is preferable that the first oxide semiconductor film be formed using an oxide having an atomic ratio of In:Ga:Zn = 1:1:1 or 1:3:2, and the second oxide semiconductor film be formed using an oxide having an atomic ratio of In:Ga:Zn = 3:1:2.

[0031]

25 In any of the above structures, the second oxide semiconductor film preferably includes a crystal portion where a c-axis is aligned in a direction parallel to a normal vector of a surface where the second oxide semiconductor film is formed. With the crystal portion included in the second oxide semiconductor film, the bonding state of metal atoms and oxygen atoms can be ordered and the generation of oxygen deficiency can be suppressed.

[0032]

30 In any of the above structures, the protective insulating film is preferably an aluminum oxide film having a film density of higher than or equal to 3.2 g/cm<sup>3</sup>. The

use of such an aluminum oxide film has a shielding effect of preventing the protective insulating film from transmitting both oxygen and an impurity such as hydrogen or moisture which might enter the second oxide semiconductor film.

[0033]

5 It is possible to provide a transistor which includes an oxide semiconductor film and has stable electrical characteristics.

#### BRIEF DESCRIPTION OF DRAWINGS

[0034]

10 FIG. 1A is a plan view illustrating one embodiment of a semiconductor device and FIGS. 1B and 1C are cross-sectional views thereof.

FIGS. 2A to 2D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

15 FIGS. 3A to 3D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIG. 4A is a plan view illustrating one embodiment of a semiconductor device and FIGS. 4B and 4C are cross-sectional views thereof.

FIGS. 5A to 5D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

20 FIGS. 6A to 6C are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIG. 7A is a plan view illustrating one embodiment of a semiconductor device and FIGS. 7B and 7C are cross-sectional views thereof.

25 FIGS. 8A to 8D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIG. 9A is a plan view illustrating an example of a manufacturing process of a semiconductor device and FIGS. 9B and 9C are cross-sectional views thereof.

FIG. 10A is a plan view illustrating an example of a manufacturing process of a semiconductor device and FIGS. 10B and 10C are cross-sectional views thereof.

30 FIGS. 11A to 11D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 12A to 12C are cross-sectional views illustrating an example of a

manufacturing process of a semiconductor device.

FIG. 13A is a plan view illustrating one embodiment of a semiconductor device and FIGS. 13B and 13C are cross-sectional views thereof.

FIGS. 14A to 14D are cross-sectional views illustrating an example of a 5 manufacturing process of a semiconductor device.

FIGS. 15A to 15D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 16A to 16D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

10 FIGS. 17A and 17B are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIG. 18A is a plan view illustrating one embodiment of a semiconductor device and FIGS. 18B and 18C are cross-sectional views thereof.

15 FIGS. 19A to 19D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 20A to 20D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 21A to 21C are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

20 FIGS. 22A to 22C are a cross-sectional view, a plan view, and a circuit diagram illustrating one embodiment of a semiconductor device.

FIGS. 23A and 23B are a circuit diagram and a perspective view illustrating one embodiment of a semiconductor device.

25 FIG. 24A is a cross-sectional view illustrating one embodiment of a semiconductor device and FIG. 24B is a plan view thereof.

FIGS. 25A and 25B are circuit diagrams illustrating one embodiment of a semiconductor device.

FIG. 26 is a block diagram illustrating one embodiment of a semiconductor device.

30 FIG. 27 is a block diagram illustrating one embodiment of a semiconductor device.

FIG. 28 is a block diagram illustrating one embodiment of a semiconductor

device.

FIG. 29 is a flowchart illustrating manufacturing processes of sputtering targets.

#### BEST MODE FOR CARRYING OUT THE INVENTION

5 [0035]

Hereinafter, embodiments of the invention disclosed in this specification will be described in detail with reference to the accompanying drawings. Note that the present invention is not limited to the following description and it will be readily appreciated by those skilled in the art that modes and details can be modified in various 10 ways without departing from the spirit and the scope of the present invention. Therefore, the invention should not be construed as being limited to the description in the following embodiments.

[0036]

Note that the position, size, range, or the like of each structure illustrated in 15 drawings and the like is not accurately represented in some cases for easy understanding. Therefore, the disclosed invention is not necessarily limited to the position, size, range, or the like as disclosed in the drawings and the like.

[0037]

In this specification and the like, ordinal numbers such as "first", "second", and 20 "third" are used in order to avoid confusion among components, and the terms do not limit the components numerically.

[0038]

Note that in this specification and the like, the term such as "over" or "below" does not necessarily mean that a component is placed "directly on" or "directly under" 25 another component. For example, the expression "a gate electrode over a gate insulating film" can mean the case where there is an additional component between the gate insulating film and the gate electrode.

[0039]

In addition, in this specification and the like, the term such as "electrode" or 30 "wiring" does not limit a function of a component. For example, an "electrode" is sometimes used as part of a "wiring", and vice versa. Furthermore, the term "electrode" or "wiring" can include the case where a plurality of "electrodes" or

"wirings" is formed in an integrated manner.

[0040]

Functions of a "source" and a "drain" are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flowing is 5 changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be replaced with each other in this specification and the like.

[0041]

Note that in this specification and the like, the term "electrically connected" includes the case where components are connected through an object having any electric 10 function. There is no particular limitation on an "object having any electric function" as long as electric signals can be transmitted and received between components that are connected through the object. Examples of an "object having any electric function" are a switching element such as a transistor, a resistor, an inductor, a capacitor, and an element with a variety of functions as well as an electrode and a wiring.

15 [0042]

(Embodiment 1)

In this embodiment, one embodiment of a semiconductor device and a method for manufacturing the semiconductor device will be described with reference to FIGS. 1A to 1C, FIGS. 2A to 2D, and FIGS. 3A to 3D.

20 [0043]

[Structural Example 1 of Semiconductor Device]

A plan view and cross-sectional views of a top-gate transistor as an example of the semiconductor device are illustrated in FIGS. 1A to 1C. FIG. 1A is the plan view, FIG. 1B corresponds to a cross-sectional view taken along line X1-Y1 in FIG. 1A, and 25 FIG. 1C corresponds to a cross-sectional view taken along line V1-W1 in FIG. 1A. Note that in FIG. 1A, some components of the semiconductor device (e.g., a gate insulating film 110) are omitted for simplicity.

[0044]

The semiconductor device illustrated in FIGS. 1A to 1C includes an oxide film 30 104; a first oxide semiconductor film 106 formed over the oxide film 104; a second oxide semiconductor film 108 formed over the first oxide semiconductor film 106; the gate insulating film 110 formed over the second oxide semiconductor film 108; and a

gate electrode 112 which is in contact with the gate insulating film 110 and formed in a region overlapping with the second oxide semiconductor film 108.

[0045]

5 The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are each formed using an oxide film containing at least indium, gallium, and zinc, and the content percentage of gallium in the first oxide semiconductor film 106 is higher than in the second oxide semiconductor film 108.

[0046]

10 Further, in the first oxide semiconductor film 106, the content percentage of gallium is higher than or equal to that of indium. Furthermore, in the second oxide semiconductor film 108, the content percentage of indium is higher than that of gallium. The high content percentage of indium in the second oxide semiconductor film 108 can lead to higher crystallinity of the second oxide semiconductor film 108.

[0047]

15 The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are stacked and have different compositions as described above. Further, the first oxide semiconductor film 106 can suppress oxygen release from the oxide film 104 at the time of the formation of the second oxide semiconductor film 108.

[0048]

20 The following will discuss a structure without the first oxide semiconductor film 106. In this case, the second oxide semiconductor film 108 is to be formed directly on the oxide film 104. To deposit the second oxide semiconductor film 108 while heating it at 400 °C for example, oxygen would be released from the oxide film 104 before the formation of the second oxide semiconductor film 108. Therefore, after 25 the formation of second oxide semiconductor film 108, the amount of oxygen released from the oxide film 104 becomes small, resulting in insufficient oxygen supply to the second oxide semiconductor film 108. Further, in the case where the material of the oxide film 104 is different from that of the second oxide semiconductor 108, e.g., silicon oxide, silicon that is contained in the oxide film 104 might be mixed into the 30 second oxide semiconductor film 108 to interfere with the crystallization of the second oxide semiconductor film 108.

[0049]

In contrast, in a structure described in this embodiment in which, for example, after the oxide film 104 is formed, the first oxide semiconductor film 106 is formed at a low temperature (e.g., higher than or equal to room temperature and lower than or equal to 200 °C) and the second oxide semiconductor film 108 is formed at a high temperature (e.g., higher than or equal to 250 °C to lower than or equal to 500 °C, preferably higher than or equal to 300 °C and lower than or equal to 400 °C), the first oxide semiconductor film 106 can suppress oxygen release from the oxide film 104. Further, the second oxide semiconductor film 108 is formed over the first oxide semiconductor film 106 which is formed using the same kinds of materials as the second oxide semiconductor film 108, whereby no impurities or very few impurities, if any, are mixed into the second oxide semiconductor film 108. Accordingly, the second oxide semiconductor film 108 can have a crystal portion that grows from the interface with the first oxide semiconductor film 106.

[0050]

That is, the first oxide semiconductor film 106 suppresses oxygen release from the oxide film 104 at least at the time of the deposition of the second oxide semiconductor film 108, and also serves as a base film for the second oxide semiconductor film 108, resulting in higher crystallinity of the second oxide semiconductor film 108. After the second oxide semiconductor film 108 is formed, oxygen is released from the oxide film 104 by heat treatment or the like, and then the oxygen can pass through the first oxide semiconductor film 106 to be supplied to the second oxide semiconductor film 108.

[0051]

A structure in which the first oxide semiconductor film 106 and the second oxide semiconductor film 108 are thus stacked has an excellent effect of suppressing the generation of oxygen deficiency in the second oxide semiconductor film 108 and of facilitating the crystallinity of the second oxide semiconductor film 108.

[0052]

High crystallinity of the second oxide semiconductor film 108 can make the bonding state of metal atoms and oxygen atoms therein ordered, thereby suppressing the generation of oxygen deficiency. Even though oxygen deficiency is generated, it

would be repaired by oxygen supply from the oxide film 104.

[0053]

Note that in the first oxide semiconductor film 106, high-resistance regions 106a are formed in a region overlapping with the gate electrode 112 and regions outside the second oxide semiconductor film 108, and a pair of low-resistance regions 106b is formed adjacent to the region overlapping with the gate electrode 112. Further, in the second oxide semiconductor film 108, a channel region 108a is formed in a region overlapping with the gate electrode 112, and a pair of low-resistance regions 108b is formed adjacent to the region overlapping with the gate electrode 112.

10 [0054]

The high-resistance region 106a formed outside the second oxide semiconductor film 108 serves as a separation layer between transistors. This is to prevent electrical connection between adjacent transistors, for example, which would occur in the case where the high-resistance region 106a is not provided outside the 15 second oxide semiconductor film 108.

[0055]

The semiconductor device may also include a protective insulating film 114 formed over the gate electrode 112, an interlayer insulating film 116 formed over the protective insulating film 114, and a source electrode 118a and a drain electrode 118b which are formed over the interlayer insulating film 116 and electrically connected to the second oxide semiconductor film 108. Note that since the source electrode 118a and the drain electrode 118b are in contact with the pair of low-resistance regions 108b formed in the second oxide semiconductor film 108, the contact resistance can be low.

[0056]

25 The following will show each component that can be included in the semiconductor device of one embodiment of the present invention in detail.

[0057]

[Detailed Description of Substrate]

Although there is no particular limitation on a substrate that can be used as a 30 substrate 102, it is necessary that the substrate have heat resistance to withstand at least heat treatment performed later. For example, a glass substrate of barium borosilicate glass, aluminoborosilicate glass, or the like, a ceramic substrate, a quartz substrate, or a

sapphire substrate can be used. Alternatively, a single-crystal semiconductor substrate of silicon, silicon carbide, or the like, a polycrystalline semiconductor substrate, a compound semiconductor substrate of silicon germanium or the like, an SOI substrate, or the like can be used.

5 [0058]

[Detailed Description of Oxide Film]

The oxide film 104 has the effect of preventing diffusion of an impurity element such as hydrogen or moisture from the substrate 102, and can be formed with a single-layer structure or a stacked structure using one or more of a silicon oxide film, a 10 silicon nitride oxide film, and a silicon oxynitride film. In addition, the oxide film 104 preferably has another effect to supply oxygen to the first oxide semiconductor film 106 and the second oxide semiconductor film 108, which are to be formed later. In the case where a silicon oxide film is used as the oxide film 104 for example, part of oxygen therein can be released by heating the oxide film 104, so that oxygen can be 15 supplied to the first oxide semiconductor film 106 and the second oxide semiconductor film 108 to repair oxygen deficiency in the first oxide semiconductor film 106 and the second oxide semiconductor film 108.

[0059]

In particular, the oxide film 104 preferably contains oxygen at an amount that 20 exceeds at least the stoichiometry. For example, a silicon oxide film of  $\text{SiO}_{2+\alpha}$  ( $\alpha > 0$ ) is preferably used as the oxide film 104. With the use of such a silicon oxide film as the oxide film 104, oxygen can be supplied to the first oxide semiconductor film 106 and the second oxide semiconductor film 108.

[0060]

25 [Detailed Description of First Oxide Semiconductor Film]

The first oxide semiconductor film 106 is an oxide film containing at least indium, gallium, and zinc, and can be formed using an In-Ga-Zn-based oxide (also expressed as IGZO). Note that the In-Ga-Zn-based oxide means an oxide containing In, Ga, and Zn, and may contain a metal element other than In, Ga, or Zn. For 30 example, it is possible to use an In-Sn-Ga-Zn-based oxide, an In-Hf-Ga-Zn-based oxide, or an In-Al-Ga-Zn-based oxide.

[0061]

The first oxide semiconductor film 106 has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film 108. Further, in the first oxide semiconductor film 106, the content percentage of gallium is higher than or equal to that of indium. That is, it is preferable to use an oxide in which content percentages can be expressed as  $\text{In} \leq \text{Ga}$ . For example, it is preferable to use an In-Ga-Zn-based oxide having an atomic ratio of  $\text{In}:\text{Ga}:\text{Zn} = 1:1:1$  or  $1:3:2$ , or an oxide having a composition in the neighborhood of the above composition.

5 [0062]

Further, the first oxide semiconductor film 106 can be formed by a sputtering method, an atomic layer deposition (ALD) method, an evaporation method, a coating method, or the like. The thickness of the first oxide semiconductor film 106 is greater than 5 nm and less than or equal to 200 nm, preferably greater than or equal to 10 nm and less than or equal to 30 nm. The first oxide semiconductor film 106 is in a single crystal state, a polycrystalline (also referred to as polycrystal) state, an amorphous state,

10 or the like.

15 [0063]

#### [Detailed Description of Second Oxide Semiconductor Film]

The second oxide semiconductor film 108 is an oxide film containing at least indium, gallium, and zinc, and can be formed using an In-Ga-Zn-based oxide (also expressed as IGZO). Note that the In-Ga-Zn-based oxide means an oxide containing In, Ga, and Zn, and may contain a metal element other than In, Ga, or Zn. For example, it is possible to use an In-Sn-Ga-Zn-based oxide, an In-Hf-Ga-Zn-based oxide, or an In-Al-Ga-Zn-based oxide.

[0064]

25 The second oxide semiconductor film 108 has a higher content percentage of indium and a lower content percentage of gallium than the first oxide semiconductor film 106. Further, in the second oxide semiconductor film 108, the content percentage of indium is higher than that of gallium. That is, it is preferable to use an oxide in which content percentages can be expressed as  $\text{In} > \text{Ga}$ . For example, it is preferable to use an In-Ga-Zn-based oxide having an atomic ratio of  $\text{In}:\text{Ga}:\text{Zn} = 3:1:2$  or  $2:1:3$ , or an oxide having a composition in the neighborhood of the above composition.

30

[0065]

Further, the second oxide semiconductor film 108 can be formed by a sputtering method, an ALD method, an evaporation method, a coating method, or the like. The thickness of the second oxide semiconductor film 108 is greater than 5 nm and less than or equal to 200 nm, preferably greater than or equal to 10 nm and less than or equal to 30 nm. The second oxide semiconductor film 108 preferably has crystallinity, such as a single crystal state, a polycrystalline (also referred to as polycrystal) state, or a microcrystalline state.

[0066]

10 Further, the second oxide semiconductor film 108 is preferably a CAAC-OS (c-axis aligned crystalline oxide semiconductor) film. The CAAC-OS film is not completely single crystal nor completely amorphous. The CAAC-OS film is an oxide semiconductor film with a crystal-amorphous mixed phase structure where crystal parts are included in an amorphous phase. Note that in most cases, the crystal part fits 15 inside a cube whose one side is less than 100 nm. From an observation image obtained with a transmission electron microscope (TEM), a boundary between an amorphous part and a crystal part in the CAAC-OS film is not clear. Further, with the TEM, a grain boundary in the CAAC-OS film is not found. Thus, in the CAAC-OS film, a reduction in electron mobility, due to the grain boundary, is suppressed.

20 [0067]

In each of the crystal parts included in the CAAC-OS film, a c-axis is aligned in a direction parallel to a normal vector of a surface where the CAAC-OS film is formed or a normal vector of a surface of the CAAC-OS film, triangular or hexagonal atomic arrangement which is seen from the direction perpendicular to the a-b plane is 25 formed, and metal atoms are arranged in a layered manner or metal atoms and oxygen atoms are arranged in a layered manner when seen from the direction perpendicular to the c-axis. Note that, among crystal parts, the directions of the a-axis and the b-axis of one crystal part may be different from those of another crystal part. In this specification, a simple term "perpendicular" includes a range from 85° to 95°. In 30 addition, a simple term "parallel" includes a range from -5° to 5°.

[0068]

In the CAAC-OS film, distribution of crystal parts is not necessarily uniform. For example, in the formation process of the CAAC-OS film, in the case where crystal growth occurs from a surface side of the oxide semiconductor film, the proportion of crystal portions in the vicinity of the surface of the oxide semiconductor film is higher 5 than that in the vicinity of the surface where the oxide semiconductor film is formed in some cases. Further, when an impurity is added to the CAAC-OS film, the crystal part in a region to which the impurity is added becomes amorphous in some cases.

[0069]

Since the c-axes of the crystal parts included in the CAAC-OS film are aligned 10 in the direction parallel to a normal vector of a surface where the CAAC-OS film is formed or a normal vector of a surface of the CAAC-OS film, the directions of the c-axes may be different from each other depending on the shape of the CAAC-OS film (the cross-sectional shape of the surface where the CAAC-OS film is formed or the cross-sectional shape of the surface of the CAAC-OS film). Note that when the 15 CAAC-OS film is formed, the direction of c-axis of the crystal part is the direction parallel to a normal vector of the surface where the CAAC-OS film is formed or a normal vector of the surface of the CAAC-OS film. The crystal part is formed by film formation or by performing treatment for crystallization such as heat treatment after film formation.

20 [0070]

With the use of the CAAC-OS film in a transistor, change in electrical characteristics of the transistor due to irradiation with visible light or ultraviolet light can be reduced. Change and variation in threshold voltages can be suppressed. Thus, the transistor has high reliability.

25 [0071]

In a crystal portion or a crystalline oxide semiconductor film, defects in the bulk can be further reduced. Further, when the surface planarity of the crystal portion or the crystalline oxide semiconductor film is enhanced, a transistor including the oxide semiconductor can have higher field-effect mobility than a transistor including an 30 amorphous oxide semiconductor. In order to enhance the surface planarity of the oxide semiconductor film, the oxide semiconductor is preferably formed over a flat surface. Specifically, the oxide semiconductor is preferably formed over a surface with an

average surface roughness ( $R_a$ ) less than or equal to 0.15 nm, preferably less than or equal to 0.1 nm.

[0072]

5 Note that  $R_a$  is obtained by expanding arithmetic mean deviation, which is defined by JIS B 0601, into three dimensions so as to be applicable to a surface. Moreover,  $R_a$  can be expressed as an average value of the absolute values of deviations from a reference surface to a specific surface and is defined by the following formula.

[0073]

[FORMULA 1]

$$10 Ra = \frac{1}{S_0} \int_{y_1}^{y_2} \int_{x_1}^{x_2} |f(x, y) - Z_0| dx dy$$

[0074]

Here, the specific surface is a surface which is a target of roughness measurement, and is a quadrilateral region which is specified by four points represented by the coordinates  $(x_1, y_1, f(x_1, y_1))$ ,  $(x_1, y_2, f(x_1, y_2))$ ,  $(x_2, y_1, f(x_2, y_1))$ , and  $(x_2, y_2, f(x_2, y_2))$ .  $S_0$  represents the area of a rectangle which is obtained by projecting the specific surface on the  $xy$  plane, and  $Z_0$  represents the height of the reference surface (the average height of the specific surface).  $R_a$  can be measured using an atomic force microscope (AFM).

[0075]

20 There are three methods for forming a CAAC-OS film when the CAAC-OS film is used as the second oxide semiconductor film 108. The first method is to form an oxide semiconductor film at a temperature higher than or equal to 200 °C and lower than or equal to 450 °C to form, in the oxide semiconductor film, crystal parts in which the c-axes are aligned in the direction parallel to a normal vector of a surface where the 25 oxide semiconductor film is formed or a normal vector of a surface of the oxide semiconductor film. The second method is to form an oxide semiconductor film with a small thickness and then heat it at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, to form, in the oxide semiconductor film, crystal parts in which the c-axes are aligned in the direction parallel to a normal vector of a surface

where the oxide semiconductor film is formed or a normal vector of a surface of the oxide semiconductor film. The third method is to form one oxide semiconductor film with a small thickness, then heat it at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, and form another oxide semiconductor film, to form, in the oxide semiconductor film, crystal parts in which the c-axes are aligned in the direction parallel to a normal vector of a surface where the oxide semiconductor film is formed or a normal vector of a surface of the oxide semiconductor film.

[0076]

By heating the substrate 102 during deposition, the concentration of an impurity such as hydrogen or water in the second oxide semiconductor film 108 can be reduced. In addition, damage by sputtering can be reduced, which is preferable. The second oxide semiconductor film 108 may be formed by an ALD method, an evaporation method, a coating method, or the like.

[0077]

Note that when an oxide semiconductor film (single crystal or microcrystalline) having crystallinity different from the CAAC-OS film is formed as the second oxide semiconductor film 108, the deposition temperature is not particularly limited.

[0078]

The energy gap of the second oxide semiconductor film 108 is 2.8 eV to 3.2 eV, and is greater than that of silicon (1.1 eV). The minor carrier density of the second oxide semiconductor film 108 is  $1 \times 10^{19} / \text{cm}^3$ , which is much smaller than the intrinsic carrier density of silicon ( $1 \times 10^{15} / \text{cm}^3$ ).

[0079]

Majority carriers (electrons) of the second oxide semiconductor film 108 flow only from a source of a transistor. Further, a channel formation region can be depleted completely. Thus, an off-state current of the transistor can be extremely small. The off-state current of the transistor including the second oxide semiconductor film 108 is as small as  $10 \text{ yA}/\mu\text{A}$  or less at room temperature, or  $1 \text{ yA}/\mu\text{A}$  or less at 85 °C to 95 °C.

[0080]

In the case of an n-channel transistor, the off-state current in this specification is current that flows between a source electrode and a drain electrode when the potential

of a gate electrode is less than or equal to 0 V with the potential of the source electrode as a reference potential while the potential of the drain electrode is higher than those of the source electrode and the gate electrode. Alternatively, in the case of a p-channel transistor, the off-state current in this specification is current that flows between a 5 source electrode and a drain electrode when the potential of a gate electrode is greater than or equal to 0 V with the potential of the source electrode as a reference potential while the potential of the drain electrode is lower than those of the source electrode and the gate electrode.

[0081]

10 Further, a transistor including the second oxide semiconductor film 108 has an ideally low S value. The transistor also has high reliability.

[0082]

[Detailed Description of Gate Insulating Film]

The gate insulating film 110 can be formed using a silicon oxide film, a gallium 15 oxide film, an aluminum oxide film, a silicon nitride film, a silicon oxynitride film, an aluminum oxynitride film, a silicon nitride oxide film, or the like. It is preferable that the gate insulating film 110 contain oxygen in a portion which is in contact with the second oxide semiconductor film 108. In particular, the gate insulating film 110 preferably contains oxygen at an amount that exceeds at least the stoichiometry. For 20 example, in the case where a silicon oxide film is used as the gate insulating film 110, a film of  $\text{SiO}_{2+\alpha}$  ( $\alpha > 0$ ) is preferably used. With the use of the silicon oxide film as the gate insulating film 110, oxygen can be supplied to the second oxide semiconductor film 108 and excellent electric characteristics can be obtained.

[0083]

25 The gate insulating film 110 can be formed using a high-k material such as hafnium oxide, yttrium oxide, hafnium silicate ( $\text{HfSi}_x\text{O}_y$  ( $x > 0, y > 0$ ))), hafnium silicate to which nitrogen is added ( $\text{HfSiO}^N_y$  ( $x > 0, y > 0$ ))), hafnium aluminate ( $\text{HfAlO}_y$  ( $x > 0, y > 0$ ))), or lanthanum oxide. With the use of such a material, gate leakage current can be reduced. Further, the gate insulating film 110 may have a single-layer structure 30 or a stacked structure.

[0084]

Further, the gate insulating film 110 can have a thickness greater than or equal to 1 nm and less than or equal to 500 nm. There is no particular limitation on a method for forming the gate insulating film 110; for example, a sputtering method, an MBE method, a PE-CVD method, a pulse laser deposition method, an ALD method, or the like can be employed as appropriate.

5 [0085]

[Detailed Description of Gate Electrode]

For the gate electrode 112, it is possible to use a metal material such as molybdenum, titanium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material containing any of these materials, for example. Alternatively, the gate electrode 112 may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide ( $In_2O_3$ ), tin oxide ( $SnO_2$ ), zinc oxide ( $ZnO$ ), indium tin oxide ( $In_2O_3-SnO_2$ , which is abbreviated to ITO in some cases), indium zinc oxide ( $In_2O_3-ZnO$ ), or any of these metal oxide materials containing silicon or silicon oxide can be used. The gate electrode 112 can be formed to have a single-layer structure or a stacked structure using any of the above materials. There is no particular limitation on the method for forming the gate electrode 112, and a variety of deposition methods such as an evaporation method, a PE-CVD method, a sputtering method, or a spin coating method can be employed.

10 20 [0086]

[Detailed Description of Protective Insulating Film]

The protective insulating film 114 is preferably formed using an inorganic insulating film and may be formed as a single layer or a stacked layer using any of oxide insulating films such as a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, a gallium oxide film, and a hafnium oxide film. Further, over the above oxide insulating film, a single layer or a stacked layer using any of nitride insulating films such as a silicon nitride film, a silicon nitride oxide film, an aluminum nitride film, and an aluminum nitride oxide film may be formed. For example, as a stacked layer, a silicon oxide film and an aluminum oxide film can be formed in this order over the gate electrode 112 by a sputtering method. There is no particular limitation on a method for forming the protective insulating film 114; for example, a sputtering method, an MBE method, a PE-CVD method, a pulse

laser deposition method, an ALD method, or the like can be employed as appropriate.

[0087]

Alternatively, in particular, a dense inorganic insulating film is preferably formed as the protective insulating film 114. For example, an aluminum oxide film 5 can be formed by a sputtering method. By forming an aluminum oxide film having high density (a film density of 3.2 g/cm<sup>3</sup> or higher, preferably 3.6 g/cm<sup>3</sup> or higher), a high shielding effect (blocking effect) of preventing the protective insulating film 114 from transmitting both oxygen and an impurity such as hydrogen or moisture which might enter the second oxide semiconductor film 108 can be obtained. Therefore, in 10 and after the manufacturing process, the aluminum oxide film functions as a protective film to prevent an impurity such as hydrogen or moisture, which causes a change of the second oxide semiconductor film 108, from being mixed into the second oxide semiconductor film 108 and to prevent oxygen from being released, which is a main 15 constituent material of the second oxide semiconductor film 108. Note that the film density can be measured by Rutherford backscattering spectrometry (RBS) or X-ray reflection (XRR).

[0088]

[Detailed Description of Interlayer Insulating Film]

The interlayer insulating film 116 is preferably formed using an inorganic 20 insulating film and may be formed as a single layer or a stacked layer using any of a silicon oxide film, a silicon oxynitride film, a silicon nitride film, and a silicon nitride oxide film. There is no particular limitation on a method for forming the interlayer insulating film 116; for example, a sputtering method, an MBE method, a PE-CVD method, a pulse laser deposition method, an ALD method, or the like can be employed 25 as appropriate.

[0089]

[Detailed Description of Source Electrode and Drain Electrode]

As each of the source electrode 118a and the drain electrode 118b, for example, 30 a metal film containing an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten, or a metal nitride film containing any of the above elements as its component (e.g., a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film) can be used. Alternatively, each of the source

electrode 118a and the drain electrode 118b may have a structure in which a film of a high-melting-point metal such as titanium, molybdenum, or tungsten, or a nitride film of any of these metals (e.g., a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film) is stacked on either or both of the bottom surface and the top 5 surface of a metal film of aluminum, copper, or the like. Further, a conductive film used for the source electrode 118a and the drain electrode 118b may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide ( $In_2O_3$ ), tin oxide ( $SnO_2$ ), zinc oxide ( $ZnO$ ), indium tin oxide ( $In_2O_3-SnO_2$ , abbreviated to ITO), or indium zinc oxide ( $In_2O_3-ZnO$ ) can be used. The conductive film used for the source 10 electrode and the drain electrode can be formed with a single-layer structure or a stacked structure using any of the above materials. There is no particular limitation on the method for forming the conductive film, and a variety of deposition methods such as an evaporation method, a PE-CVD method, a sputtering method, or a spin coating method can be employed.

15 [0090]

Note that details of the other components will be described in [Method 1 for Manufacturing Semiconductor Device] below, with reference to FIGS. 2A to 2D and FIGS. 3A to 3D.

[0091]

20 [Method 1 for Manufacturing Semiconductor Device]

An example of a method for manufacturing the semiconductor device illustrated in FIGS. 1A to 1C of this embodiment will be described below with reference to FIGS. 2A to 2D and FIGS. 3A to 3D.

[0092]

25 First, the substrate 102 is prepared, and then the oxide film 104, the first oxide semiconductor film 106, and the second oxide semiconductor film 108 are formed over the substrate 102 (see FIG. 2A).

[0093]

30 The substrate 102 may be subjected to plasma treatment or the like before the oxide film 104 is formed. As plasma treatment, reverse sputtering in which an argon gas is introduced and plasma is generated can be performed. The reverse sputtering refers to a method in which an RF power source is used for application of a voltage to

the substrate 102 side in an argon atmosphere so that plasma is generated in the vicinity of the substrate 102 to modify a surface of the substrate. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used. The reverse sputtering can remove particle substances (also referred 5 to as particles or dust) attached to the surface of the substrate 102.

[0094]

As a method for forming the second oxide semiconductor film 108, the oxide semiconductor film is etched by a dry etching method. As an etching gas,  $BCl_3$ ,  $Cl_2$ ,  $O_2$ , or the like can be used. A dry etching apparatus using a high-density plasma 10 source such as ECR or ICP can be used to improve an etching rate. Etching conditions of the second oxide semiconductor film 108 may be selected as appropriate by a practitioner such that the first oxide semiconductor film 106 is not processed into an island shape in a step for forming the second oxide semiconductor film 108. An end portion of the second oxide semiconductor film 108 is preferably tapered at an angle of 15  $20^\circ$  to  $50^\circ$ .

[0095]

Note that the oxide film 104, the first oxide semiconductor film 106, and the second oxide semiconductor film 108 are preferably deposited successively without being exposed to the air; in particular, the first oxide semiconductor film 106 and the 20 second oxide semiconductor film 108 are preferably deposited successively. In this manner, by depositing the oxide film 104, the first oxide semiconductor film 106, and the second oxide semiconductor film 108 successively without being exposed to the air, it is possible to suppress mixing of an impurity element such as moisture or hydrogen contained in the air into each interface.

25 [0096]

In a step for depositing the first oxide semiconductor film 106 and the second oxide semiconductor film 108, it is preferable that the first oxide semiconductor film 106 and the second oxide semiconductor film 108 do not contain hydrogen or water as much as possible. Thus, as pretreatment of the step for depositing the first oxide 30 semiconductor film 106 and the second oxide semiconductor film 108, for example, it is preferable that the substrate 102 provided with the oxide film 104 be preheated in a preheating chamber of a sputtering apparatus to remove and exhaust an impurity such as

hydrogen or moisture adsorbed to the substrate 102 and the oxide film 104. Note that the temperature of the pretreatment is set such that no oxygen, or little oxygen, if any, is released from the oxide film 104. The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are preferably deposited in a deposition station 5 (also referred to as a deposition chamber) from which remaining moisture is exhausted, and are more preferably deposited successively in vacuum with the use of a multi-chamber sputtering apparatus with a plurality of deposition stations.

[0097]

To remove the moisture in a preheating chamber and the deposition chamber, 10 an entrapment vacuum pump, for example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an exhaustion unit may be a turbo pump provided with a cold trap. From the preheating chamber and the deposition chamber which are exhausted with a cryopump, a hydrogen atom, a compound containing a hydrogen atom such as water (H<sub>2</sub>O) (more preferably, also a compound containing a 15 carbon atom), and the like are exhausted, whereby the concentration of an impurity such as hydrogen or moisture in the first oxide semiconductor film 106 and the second oxide semiconductor film 108 can be reduced.

[0098]

Note that in this embodiment, the first oxide semiconductor film 106 and the 20 second oxide semiconductor film 108 are deposited by a sputtering method using a metal oxide target with an atomic ratio of In:Ga:Zn = 1:1:1 and a metal oxide target with an atomic ratio of In:Ga:Zn = 3:1:2, respectively. Note that the targets that can be used for forming the first oxide semiconductor film 106 and the second oxide semiconductor film 108 are not limited to the targets including the above materials with 25 the above ratios. Further, the targets that can be used for forming the first oxide semiconductor film 106 and the second oxide semiconductor film 108 preferably have crystallinity; that is, a single crystalline target, a polycrystalline target, or the like are preferably used. With the use of the target having crystallinity, formed thin films also have crystallinity; specifically, the formed thin films tend to have a c-axis-aligned 30 crystal.

[0099]

Here, methods for manufacturing sputtering targets each including an oxide semiconductor having a crystal region in which the direction of the c-axis is parallel to a normal vector of the top surface of the oxide semiconductor will be described (see FIG. 29).

5 [0100]

First, raw materials for the sputtering target are weighed (step SI01).

[0101]

Here, an  $InO^X$  raw material (a raw material containing In), a  $GaOy$  raw material (a raw material containing Ga), and a  $ZnOz$  raw material (a raw material containing Zn) 10 are prepared as raw materials for the sputtering target. Note that  $X$ ,  $Y$ , and  $Z$  are each a given positive number; for example,  $X$ ,  $Y$ , and  $Z$  are 1.5, 1.5, and 1, respectively. It is needless to say that the above raw materials are an example, and raw materials can be selected as appropriate in order to obtain a desired compound. For example, a  $MOy$  raw material may be used instead of the  $GaOy$  raw material. Note that Sn, Hf, or Al 15 can be used as  $M$ . Alternatively, the following lanthanoid may be used as  $M$ : La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, or Lu. Although the case where three kinds of raw materials are used is shown as an example in this embodiment, one embodiment of the present invention is not limited thereto. For example, this embodiment may be applied to the case where four or more kinds of raw materials are 20 used.

[0102]

Next, the  $InOy$  raw material, the  $GaOy$  raw material, and the  $ZnOz$  raw material are mixed in a predetermined ratio.

[0103]

25 For example, the predetermined ratio of the  $InOy$  raw material, the  $GaOy$  raw material, and the  $ZnOz$  raw material is 2:2:1, 8:4:3, 3:1:1, 1:1:1, 4:2:3, 1:1:2, 3:1:4, or 3:1:2 in a molar ratio. With the use of a mixed material having such a ratio, a sputtering target including an oxide semiconductor having a crystal region in which the direction of the c-axis is parallel to a normal vector of the top surface of the oxide 30 semiconductor can be easily obtained.

[0104]

More specifically, in the case of forming a sputtering target of In-Ga-Zn-based

oxide having a composition of In:Ga:Zn = 1:1:1 [atomic ratio], the raw materials are weighed so that **Ir<sub>2</sub>O<sub>3</sub>:Ga<sub>2</sub>O<sub>3</sub>:ZnO** = 1:1:2 [molar ratio].

[0105]

5 Note that also in the case where the  $MO_Y$  raw material is used instead of the  $GaO_Y$  raw material, the ratio of the  $InO_X$  raw material, the  $MO_Y$  raw material, and the  $ZnO_Z$  raw material is 2:2:1, 8:4:3, 3:1:1, 1:1:1, 4:2:3, 1:1:2, 3:1:4, or 3:1:2 in a molar ratio.

[0106]

10 A method for forming the sputtering target using a wet method is described. The raw materials for the sputtering target are weighed, and then, the raw materials are ground and mixed with a ball mill or the like to obtain compound powder. Ion-exchange water, an organic additive, and the like are further mixed into the compound powder to form slurry (step S11).

[0107]

15 Then, the slurry is poured into a mold provided with a moisture-permeable filter, so that moisture is removed. The mold may be formed using a metal or an oxide and the upper shape thereof is rectangular or rounded. The mold can be provided with one or more holes at the bottom. With the plural holes, moisture of the slurry can be removed rapidly. A porous resin, cloth, or the like may be used for the filter.

20 [0108]

Moisture is removed from the slurry in such a manner that water is removed under reduced pressure through the hole provided at the bottom of the mold into which the slurry is poured. Next, the slurry from which moisture has been removed under reduced pressure is naturally dried. Thus, the slurry from which moisture has been removed is molded into the internal shape of the mold (step S113).

[0109]

25 Then, the molded body is baked in an oxygen ( $O_2$ ) atmosphere at 1400 °C (step S114). Through the above-described steps, the sputtering target can be obtained using a wet method.

30 [0110]

Next, a method for forming the sputtering target using a dry method will be

described. The raw materials for the sputtering target are weighed, and then, the raw materials are ground and mixed with a ball mill or the like to obtain compound powder (step S121).

[01 11]

5 The compound powder obtained is spread over a mold, and pressure is applied thereto with a pressing machine, whereby the compound powder is molded to obtain a molded body (step S122).

[01 12]

10 The molded body is placed in a heating apparatus such as an electric furnace and baked in an oxygen ( $O_2$ ) atmosphere at a temperature of 1400 °C (step S123). Note that in this embodiment, a method in which a molding step and a baking step are separated as in step S122 and step S123 is referred to as a cold press method. As a comparison example of a cold press method, a hot press method in which a molding step and a baking step are concurrently performed will be described below.

15 [0113]

First, the above-described steps up to and including step S121 are performed. The compound powder obtained is spread over the mold, and pressure is applied with a pressing machine to the compound powder provided on the inner side of the mold while the mold is heated in an argon (Ar) atmosphere at a temperature of 1000 °C. In this manner, pressure is applied to the compound powder with the compound powder baked, whereby the compound powder can be molded to obtain a molded body (step S125). Through the above-described steps, the sputtering target can be obtained using a dry method.

[0114]

25 Further, the first oxide semiconductor film 106 and the second oxide semiconductor film 108 can be formed by a sputtering method in a rare gas (typically argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere of a rare gas and oxygen.

[0115]

30 The temperature for depositing the first oxide semiconductor film 106 is preferably higher than or equal to room temperature and lower than or equal to 200 °C,

and the temperature for depositing the second oxide semiconductor film 108 is preferably higher than or equal to 250 °C and lower than or equal to 500 °C, more preferably higher than or equal to 300 °C and lower than or equal to 400 °C.

[01 16]

5 In this manner, by depositing the first oxide semiconductor film 106 at a low temperature (higher than or equal to room temperature and lower than or equal to 200 °C) and the second oxide semiconductor film 108 at a high temperature (higher than or equal to 250 °C and lower than or equal to 500 °C), oxygen release from the oxide film 104 can be suppressed and the second oxide semiconductor film 108 can have higher 10 crystallinity.

[0117]

In addition, shortly after the first oxide semiconductor film 106 and the second oxide semiconductor film 108 are deposited, it is preferable that the oxide semiconductor films contain oxygen at an amount that exceeds at least the stoichiometry, 15 i.e., the oxide semiconductor films be supersaturated. As an example, in the case where the first oxide semiconductor film 106 and the second oxide semiconductor film 108 are deposited by a sputtering method, the deposition is preferably performed under the condition where the proportion of oxygen in a deposition gas is large, and in particular, the deposition is preferably performed in an oxygen atmosphere (an oxygen 20 gas: 100 %). For example, in the case where an In-Ga-Zn-based oxide (IGZO) is to be used for the first oxide semiconductor film 106 and the second oxide semiconductor film 108, and the deposition is performed under the condition where the proportion of oxygen in the deposition gas is large (in particular, in an atmosphere of an oxygen gas of 100 %), Zn release from the films can be suppressed even when the deposition 25 temperature is 300 °C or higher.

[01 18]

Further, when the first oxide semiconductor film 106 is formed using the above-described metal oxide target, the composition of the target is different from that of the thin film formed over the substrate in some cases. For example, when the metal 30 oxide target of In:Ga:Zn = 1:1:1 [atomic ratio] is used, the composition of the first oxide semiconductor film 106, which is a thin film, becomes In:Ga:Zn = 1:1:0.6 to 1:1:0.8

[atomic ratio] in some cases, although it depends on the deposition conditions. This is because in deposition of the first oxide semiconductor film 106 and the second oxide semiconductor film 108, ZnO is sublimed, or because a sputtering rate differs between the components of  $In_2O_3$ ,  $Ga_2O_3$ , and ZnO.

5 [0119]

Accordingly, in order to form a thin film having a desired composition ratio, the composition of the metal oxide target needs to be adjusted in advance. For example, in order to make the composition of the first oxide semiconductor film 106, which is a thin film, be  $In:Ga:Zn = 1:1:1$  [atomic ratio], the composition of the metal oxide target is preferably  $In:Ga:Zn = 1:1:1.5$  [atomic ratio]. In other words, the content percentage of ZnO in the metal oxide target is preferably made higher in advance. The composition of the target is not limited to the above value, and can be adjusted as appropriate depending on the deposition conditions or the composition of the thin film to be formed. Further, it is preferable to increase the content percentage of ZnO in the metal oxide target because in that case, the obtained thin film can have higher crystallinity. The above description has been about the first oxide semiconductor film 106; in a similar manner, to form a thin film having a desired composition as the second oxide semiconductor film 108, the composition of the metal oxide target may be adjusted.

10 [0120]

The relative density of the metal oxide target is 90 % to 100 % inclusive, preferably, 95 % to 99.9 % inclusive. With the use of the metal oxide target having high relative density, the first oxide semiconductor film 106 and the second oxide semiconductor film 108, which are deposited, can be dense.

15 [0121]

As a sputtering gas used for depositing the first oxide semiconductor film 106 and the second oxide semiconductor film 108, it is preferable to use a high-purity gas from which an impurity such as hydrogen, water, a hydroxyl group, or hydride is removed.

20 [0122]

After the second oxide semiconductor film 108 is formed, the second oxide

semiconductor film 108 may be subjected to heat treatment. The temperature of the heat treatment is higher than or equal to 300 °C and lower than or equal to 700 °C, or lower than the strain point of the substrate. The heat treatment can remove excess hydrogen (including water and a hydroxyl group) from the second oxide semiconductor film 108. Note that the heat treatment is also referred to as dehydration treatment (dehydrogenation treatment) in this specification and the like in some cases.

[0123]

Oxygen might be released from the oxide film 104 during the dehydration treatment. To prevent this, the temperature of the dehydration treatment may be selected as appropriate by a practitioner such that excess hydrogen (including water and a hydroxyl group) can be removed from the second oxide semiconductor film 108 and oxygen release from the oxide film 104 can be suppressed. Note that the dehydration treatment might cause oxygen release from the oxide film 104; however, since the first oxide semiconductor film 106 is formed, the oxygen release from the oxide film 104 can be suppressed and the dehydration treatment can be performed effectively.

[0124]

The heat treatment can be performed in such a manner that, for example, an object to be processed is introduced into an electric furnace in which a resistance heater or the like is used and heated at 450 °C in a nitrogen atmosphere for one hour. The second oxide semiconductor film 108 is not exposed to the air during the heat treatment so that the entry of water and hydrogen can be prevented.

[0125]

A heat treatment apparatus is not limited to the electric furnace and may be an apparatus for heating an object to be processed by thermal conduction or thermal radiation from a medium such as a heated gas. For example, an RTA (rapid thermal anneal) apparatus such as a GRTA (gas rapid thermal anneal) apparatus or an LRTA (lamp rapid thermal anneal) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for performing heat treatment using a

high-temperature gas. As the gas, an inert gas which does not react with an object to be processed by heat treatment, such as nitrogen or a rare gas such as argon is used.

[0126]

As the heat treatment, for example, a GRTA process may be performed as follows. The object is put in a heated inert gas atmosphere, heated for several minutes, and taken out of the inert gas atmosphere. The GRTA process enables high-temperature heat treatment for a short time. Moreover, the GRTA process can be employed even when the temperature exceeds the upper temperature limit of the object. Note that the inert gas may be switched to a gas containing oxygen during the process.

10 [0127]

Note that as the inert gas atmosphere, an atmosphere that contains nitrogen or a rare gas (e.g., helium, neon, or argon) as its main component and does not contain water, hydrogen, or the like is preferably used. The purity of nitrogen or a rare gas such as helium, neon, or argon introduced into a heat treatment apparatus is, for example, 6N (99.9999 %) or higher, preferably 7N (99.99999 %) or higher (that is, the concentration of an impurity is 1 ppm or lower, preferably 0.1 ppm or lower).

[0128]

The dehydration treatment (dehydrogenation treatment) might be accompanied by release of oxygen which is a main constituent material of the second oxide semiconductor film 108 to lead to a reduction in oxygen. Oxygen deficiency exists in a portion where oxygen is released in the second oxide semiconductor film 108, and a donor level which leads to a change in the electrical characteristics of a transistor is formed owing to the oxygen deficiency. Therefore, in the case where the dehydration treatment (dehydrogenation treatment) is performed, oxygen is preferably supplied to the second oxide semiconductor film 108. By supply of oxygen to the second oxide semiconductor film 108, oxygen deficiency in the second oxide semiconductor film 108 can be repaired.

[0129]

The oxygen deficiency in the second oxide semiconductor film 108 may be repaired in the following manner for example: after the second oxide semiconductor film 108 is subjected to the dehydration treatment (dehydrogenation treatment), a high-purity oxygen gas, a high-purity nitrous oxide gas, or ultra dry air (the moisture

amount is less than or equal to 20 ppm (-55 °C by conversion into a dew point), preferably less than or equal to 1 ppm, more preferably less than or equal to 10 ppb, in the measurement with the use of a dew point meter of a cavity ring down laser spectroscopy (CRDS) system is introduced into the same furnace. It is preferable that  
5 water, hydrogen, or the like not be contained in the oxygen gas or the nitrous oxide gas. The purity of the oxygen gas or the nitrous oxide gas which is introduced into the heat treatment apparatus is preferably 6N (99.9999 %) or higher, more preferably 7N (99.99999 %) or higher (i.e., the impurity concentration in the oxygen gas or the nitrous oxide gas is preferably 1 ppm or lower, more preferably 0.1 ppm or lower).

10 [0130]

As an example of a method for supplying oxygen to the second oxide semiconductor film 108, oxygen (including at least any one of oxygen radicals, oxygen atoms, and oxygen ions) is added to the second oxide semiconductor film 108 in order to supply oxygen to the second oxide semiconductor film 108. An ion implantation  
15 method, an ion doping method, a plasma immersion ion implantation method, plasma treatment, or the like can be employed as a method for adding oxygen.

[0131]

As another example of a method for supplying oxygen to the second oxide semiconductor film 108, oxygen is supplied to the second oxide semiconductor film 108  
20 in such a manner that the oxide film 104, the gate insulating film 110 to be formed later, or the like is heated and part of oxygen is released. In particular, in this embodiment, oxygen that is released from the oxide film 104 is preferably transmitted through the first oxide semiconductor film 106 to be supplied to the second oxide semiconductor film 108.

25 [0132]

As described above, after the second oxide semiconductor film 108 is formed, the dehydration treatment (dehydrogenation treatment) is preferably performed to remove hydrogen or moisture from the second oxide semiconductor film 108, so that the second oxide semiconductor film 108 is highly purified and does not contain an  
30 impurity as much as possible. Further, oxygen whose amount is reduced in the dehydration treatment (dehydrogenation treatment) is preferably added to the second

oxide semiconductor film 108 or supplied to repair oxygen deficiency in the second oxide semiconductor film 108. In this specification and the like, supplying oxygen to the second oxide semiconductor film 108 may be expressed as oxygen adding treatment. Alternatively, making the second oxide semiconductor film 108 contain oxygen at an 5 amount that exceeds the stoichiometry may be expressed as treatment for making an oxygen-excess state.

[0133]

Note that in the above-described case, the dehydration treatment (dehydrogenation treatment) and the oxygen adding treatment are performed after the 10 second oxide semiconductor film 108 is processed into an island shape; however, one embodiment of the disclosed invention is not construed as being limited to the case. Such treatment may be performed before the second oxide semiconductor film 108 is processed into an island shape. Alternatively, after the interlayer insulating film 116 is formed, which is to be formed later, heat treatment may be performed so that oxygen is 15 supplied from the oxide film 104, the gate insulating film 110, or the like to the second oxide semiconductor film 108.

[0134]

In this manner, hydrogen or moisture is removed from the second oxide semiconductor film 108 by the dehydration treatment (dehydrogenation treatment) and 20 oxygen deficiency therein are repaired by the oxygen adding treatment, whereby the oxide semiconductor film can be turned into an electrically i-type (intrinsic) or substantially i-type oxide semiconductor film. The oxide semiconductor film formed in such a manner contains extremely few (close to zero) carriers derived from a donor, and the carrier concentration thereof is lower than  $1 \times 10^{14} /cm^3$ , preferably lower than 1 25  $1 \times 10^{12} /cm^3$ , more preferably lower than  $1 \times 10^{11} /cm^3$ .

[0135]

It is preferable that the second oxide semiconductor film 108 be highly purified and hardly contain an impurity such as copper, aluminum, or chlorine. In a process for manufacturing a transistor, it is preferable to select steps as appropriate where such an 30 impurity might not be mixed into the second oxide semiconductor film 108 or be attached onto a surface thereof. In the case where such an impurity is attached onto

the surface of the second oxide semiconductor film 108, the second oxide semiconductor film 108 is preferably exposed to oxalic acid or dilute hydrofluoric acid or subjected to plasma (e.g., N<sub>2</sub>O plasma), for example, so that the impurity on the surface of the second oxide semiconductor film 108 can be removed. Specifically, the 5 second oxide semiconductor film 108 has a copper concentration of  $1 \times 10^{18}$  atoms/cm<sup>3</sup> or lower, preferably  $1 \times 10^{17}$  atoms/cm<sup>3</sup> or lower, an aluminum concentration of  $1 \times 10^{18}$  atoms/cm<sup>3</sup> or lower, and a chlorine concentration of  $2 \times 10^{18}$  atoms/cm<sup>3</sup> or lower.

[0136]

The second oxide semiconductor film 108 is preferably highly purified by 10 sufficient removal of an impurity such as hydrogen or sufficient supply of oxygen so as to be supersaturated with oxygen. Specifically, the second oxide semiconductor film 108 has a hydrogen concentration of  $5 \times 10^{19}$  atoms/cm<sup>3</sup> or lower, preferably  $5 \times 10^{18}$  atoms/cm<sup>3</sup> or lower, more preferably  $5 \times 10^{17}$  atoms/cm<sup>3</sup> or lower. Note that the 15 concentration of hydrogen in the second oxide semiconductor film 108 is measured by secondary ion mass spectrometry (SIMS). In order that the second oxide semiconductor film 108 is supersaturated with oxygen by sufficient supply of oxygen, it is preferable that an insulating film containing excess oxygen (e.g., a SiO\* film) be provided so as to cover and be in contact with the second oxide semiconductor film 108.

[0137]

20 The insulating film containing excess oxygen is formed using, for example, a SiO\* film or a silicon oxynitride film by a PE-CVD method or a sputtering method such as to contain much oxygen by setting its deposition conditions as appropriate. To make excess oxygen be further contained in the insulating film, oxygen is added to the insulating film by an ion implantation method, an ion doping method, or plasma 25 treatment.

[0138]

Further, in the case where the hydrogen concentration in an insulating film containing excess oxygen is  $7.2 \times 10^{20}$  atoms/cm<sup>3</sup> or higher, variations in initial 30 characteristics of transistors are increased, a channel length dependence of electrical characteristics of a transistor is increased, and a transistor is significantly degraded in the BT stress test; therefore, the hydrogen concentration in the insulating film

containing excess oxygen is preferably less than  $7.2 \times 10^{20}$  atoms/cm<sup>3</sup>. In other words, the hydrogen concentration in the second oxide semiconductor film 108 is preferably less than or equal to  $5 \times 10^{19}$  atoms/cm<sup>3</sup>, and the hydrogen concentration in the insulating film containing excess oxygen is preferably less than  $7.2 \times 10^{20}$  atoms/cm<sup>3</sup>.

5 [0139]

Further, a blocking film (e.g., an  $A10_x$  film) that suppresses oxygen release from the second oxide semiconductor film 108 is preferably formed to cover the second oxide semiconductor film 108 and to be provided outside the insulating film containing excess oxygen.

10 [0140]

By being covered with the insulating film containing excess oxygen or the blocking film, the second oxide semiconductor film 108 can be kept in a state that is substantially the same as the stoichiometry or in a supersaturated state in which the amount of oxygen exceeds the stoichiometry.

15 [0141]

Next, the gate insulating film 110 and a conductive film 111 are formed over the first oxide semiconductor film 106 and the second oxide semiconductor film 108 (see FIG. 2B).

[0142]

20 Next, through a photolithography step, a resist mask is formed over the conductive film 111, and selective etching is performed to form the gate electrode 112, and then the resist mask is removed (see FIG. 2C).

[0143]

25 Note that a resist mask for forming the gate electrode 112 may be formed by an inkjet method, in which case manufacturing costs can be reduced because a photomask is not used. The gate electrode 112 may be etched by either dry etching or wet etching, or by both of them.

[0144]

Then, a resist mask 132 is formed over the gate insulating film 110 and the gate 30 electrode 112 (see FIG. 2D).

[0145]

Next, the resist mask 132 is selectively subjected to light exposure and development through a photolithography step to form a resist mask 132a. After that, with the use of the gate electrode 112 and the resist mask 132a as masks, a dopant 142 is introduced into the first oxide semiconductor film 106 and the second oxide semiconductor film 108. The introduction of the dopant 142 makes the first oxide semiconductor film 106 have the high-resistance regions 106a and the pair of low-resistance regions 106b which are adjacent to a region overlapping with the gate electrode 112. The introduction of the dopant 142 also makes the second oxide semiconductor film 108 have the channel region 108a and the pair of low-resistance regions 108b which are adjacent to a region overlapping with the gate electrode 112 (see FIG. 3A).

[0146]

The dopant 142 is an impurity that changes the conductivity of the first oxide semiconductor film 106 and the second oxide semiconductor film 108. One or more selected from the following can be used as the dopant 142: Group 15 elements (typical examples thereof are nitrogen (N), phosphorus (P), arsenic (As), and antimony (Sb)), boron (B), aluminum (Al), argon (Ar), helium (He), neon (Ne), indium (In), fluorine (F), chlorine (Cl), titanium (Ti), and zinc (Zn).

[0147]

Alternatively, the dopant 142 can be introduced into the first oxide semiconductor film 106 and the second oxide semiconductor film 108 through another film (e.g., the gate insulating film 110) by an implantation method. As the method for introducing the dopant 142, an ion implantation method, an ion doping method, a plasma immersion ion implantation method, or the like can be used. In that case, it is preferable to use a single ion of the dopant 142, or a fluoride ion or chloride ion thereof.

[0148]

The introduction of the dopant 142 may be controlled by setting as appropriate the implantation conditions such as the acceleration voltage and the dosage, or the thickness of the film through which the dopant passes. In this embodiment, phosphorus is used as the dopant 142, whose ion is implanted by an ion implantation method. Note that the dosage of the dopant 142 may be greater than or equal to 1 x

$10^{13}$  ions/cm<sup>2</sup> and less than or equal to  $5 \times 10^{16}$  ions/cm<sup>2</sup>.

[0149]

The concentration of the dopant 142 in the low-resistance regions 108b is preferably higher than or equal to  $5 \times 10^{18}$  /cm<sup>3</sup> and lower than or equal to  $1 \times 10^{22}$  /cm<sup>3</sup>.

[0150]

The dopant 142 may be introduced with the substrate 102 heated.

[0151]

The introduction of the dopant 142 into the first oxide semiconductor film 106 and the second oxide semiconductor film 108 may be performed plural times, and the number of kinds of dopant may be plural.

[0152]

Further, heat treatment may be performed after the introduction of the dopant 142. The heat treatment is preferably performed at a temperature higher than or equal to 300 °C and lower than or equal to 700 °C (more preferably higher than or equal to 300 °C and lower than or equal to 450 °C) for one hour in an oxygen atmosphere. The heat treatment may be performed in a nitrogen atmosphere, reduced pressure, or the air (ultra-dry air).

[0153]

In the case where the second oxide semiconductor film 108 is a crystalline oxide semiconductor film or a CAAC-OS film, part of the second oxide semiconductor film 108 becomes amorphous owing to the introduction of the dopant 142 in some cases. In this case, the crystallinity of the second oxide semiconductor film 108 can be recovered by performing heat treatment thereon after the introduction of the dopant 142.

[0154]

Next, the resist mask 132a is removed and the protective insulating film 114 and the interlayer insulating film 116 are formed over the gate insulating film 110 and the gate electrode 112 (see FIG. 3B).

[0155]

Then, through a photolithography step, a resist mask is formed over the interlayer insulating film 116, and then the gate insulating film 110, the protective

insulating film 114, and the interlayer insulating film 116 are selectively etched, so that openings reaching the second oxide semiconductor film 108 (more specifically, the low-resistance regions 108b formed in the second oxide semiconductor film 108) are formed, and then the resist mask is removed (see FIG. 3C).

5 [0156]

Then, a conductive film is deposited in the openings, followed by a photolithography step through which a resist mask is formed over the conductive film and etching is selectively performed to form the source electrode 118a and the drain electrode 118b (see FIG. 3D).

10 [0157]

Note that in this embodiment, as illustrated in FIG. 3D, in a cross section taken along the channel length direction, the distance between the gate electrode 112 and the opening where the source electrode 118a is formed and the distance between the gate electrode 112 and the opening where the drain electrode 118b is formed are different.

15 Such a structure enables suppression of off-state current.

[0158]

Through the above manufacturing steps, the semiconductor device illustrated in FIGS. 1A to 1C can be manufactured.

[0159]

20 As described in this embodiment, a technical idea of the present invention is as follows. By forming the first oxide semiconductor film over the oxide film and the second oxide semiconductor film to be stacked over the first oxide semiconductor film, at least during the deposition of the second oxide semiconductor film, oxygen release from the oxide film can be suppressed. Further, since the first oxide semiconductor film serves as a base film for the second oxide semiconductor film, the second oxide semiconductor film can have higher crystallinity. The high crystallinity of the second oxide semiconductor film can suppress the generation of oxygen deficiency in the second oxide semiconductor film, and a transistor with stable electrical characteristics can be provided.

25

30 [0160]

The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

[0161]

(Embodiment 2)

In this embodiment, a modification example of the semiconductor device in Embodiment 1 and a method for manufacturing a semiconductor device, which is different from that in Embodiment 1, will be described with reference to FIGS. 4A to 4C, FIGS. 5A to 5D, and FIGS. 6A to 6C. Note that portions similar to those in FIGS. 1A to 1C, FIGS. 2A to 2D, and FIGS. 3A to 3D are denoted by the same reference numerals, and description thereof is omitted. In addition, detailed description of the same portions is not repeated, either.

10 [0162]

[Structural Example 2 of Semiconductor Device]

A plan view and cross-sectional views of a top-gate transistor as an example of the semiconductor device are illustrated in FIGS. 4A to 4C. FIG. 4A is the plan view, FIG. 4B corresponds to a cross-sectional view taken along line X2-Y2 in FIG. 4A, and FIG. 4C corresponds to a cross-sectional view taken along line V2-W2 in FIG. 4A. Note that in FIG. 4A, some components of the semiconductor device (e.g., a gate insulating film 110) are omitted for simplicity.

[0163]

The semiconductor device illustrated in FIGS. 4A to 4C include an oxide film 104; a first oxide semiconductor film 106 formed over the oxide film 104; a second oxide semiconductor film 108 formed over the first oxide semiconductor film 106; the gate insulating film 110 formed over the second oxide semiconductor film 108; and a gate electrode 112 which is in contact with the gate insulating film 110 and formed in a region overlapping with the second oxide semiconductor film 108.

25 [0164]

The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are each formed using an oxide film containing at least indium, gallium, and zinc, and the content percentage of gallium in the first oxide semiconductor film 106 is higher than in the second oxide semiconductor film 108.

30 [0165]

Further, in the first oxide semiconductor film 106, the content percentage of gallium is higher than or equal to that of indium. Furthermore, in the second oxide

semiconductor film 108, the content percentage of indium is higher than that of gallium. The high content percentage of indium in the second oxide semiconductor film 108 can lead to higher crystallinity of the second oxide semiconductor film 108.

[0166]

5 The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are stacked and have different compositions as described above. Further, the first oxide semiconductor film 106 can suppress oxygen release from the oxide film 104 at the time of the formation of the second oxide semiconductor film 108.

[0167]

10 Further, the second oxide semiconductor film 108 is formed over the first oxide semiconductor film 106 which is formed using the same kinds of materials as the second oxide semiconductor film 108. Accordingly, the second oxide semiconductor film 108 can have a crystal portion that grows from the interface with the first oxide semiconductor film 106.

15 [0168]

That is, the first oxide semiconductor film 106 suppresses oxygen release from the oxide film 104 at least at the time of the deposition of the second oxide semiconductor film 108, and also serves as a base film for the second oxide semiconductor film 108, resulting in higher crystallinity of the second oxide semiconductor film 108. After the second oxide semiconductor film 108 is formed, oxygen is released from the oxide film 104 by heat treatment or the like, and then the oxygen can pass through the first oxide semiconductor film 106 to be supplied to the second oxide semiconductor film 108.

[0169]

25 A structure in which the first oxide semiconductor film 106 and the second oxide semiconductor film 108 are thus stacked has an excellent effect of suppressing the generation of oxygen deficiency in the second oxide semiconductor film 108 and of facilitating the crystallinity of the second oxide semiconductor film 108.

[0170]

30 Note that in the first oxide semiconductor film 106, high-resistance regions 106a are formed in a region overlapping with the gate electrode 112 and regions outside the second oxide semiconductor film 108, and a pair of low-resistance regions 106b is

formed adjacent to the region overlapping with the gate electrode 112. Further, in the second oxide semiconductor film 108, a channel region 108a is formed in a region overlapping with the gate electrode 112, and a pair of low-resistance regions 108b is formed adjacent to the region overlapping with the gate electrode 112.

5 [0171]

The high-resistance region 106a formed outside the second oxide semiconductor film 108 serves as a separation layer between transistors. This is to prevent electrical connection between adjacent transistors, for example, which would occur in the case where the high-resistance region 106a is not provided outside the 10 second oxide semiconductor film 108.

[0172]

The semiconductor device may also include a protective insulating film 114 formed over the gate electrode 112; an interlayer insulating film 116 formed over the protective insulating film 114; a source electrode 118a and a drain electrode 118b which 15 are embedded in a first opening 151a and a second opening 151b, respectively, formed in the gate insulating film 110, the protective insulating film 114, and the interlayer insulating film 116, and are electrically connected to the second oxide semiconductor film 108; and a wiring 119a and a wiring 119b which are electrically connected to the source electrode 118a and the drain electrode 118b, respectively. Note that since the 20 source electrode 118a and the drain electrode 118b are in contact with the pair of low-resistance regions 108b formed in the second oxide semiconductor film 108, the contact resistance can be low.

[0173]

A structure of the semiconductor device in this embodiment differs from that of the semiconductor device in Embodiment 1 in that the source electrode 118a is 25 embedded in the first opening 151a formed in the gate insulating film 110, the protective insulating film 114, and the interlayer insulating film 116; the drain electrode 118b is embedded in the second opening 151b formed in the gate insulating film 110, the protective insulating film 114, and the interlayer insulating film 116; and the wiring 119a and the wiring 119b are formed, which are electrically connected to the source 30 electrode 118a and the drain electrode 118b, respectively.

[0174]

The openings (the first opening 151a and the second opening 151b) of the semiconductor device in this embodiment, in which the source electrode 118a and the drain electrode 118b are embedded, are formed through two steps described later in [Method 2 for Manufacturing the Semiconductor Device]. Further, the source 5 electrode 118a and the drain electrode 118b are formed by division of a conductive film 118 by CMP treatment. Thus, it is unnecessary to employ a photolithography step to form the source electrode 118a and the drain electrode 118b, and accordingly, the source electrode 118a and the drain electrode 118b can be formed without any concerns about the accuracy of a light-exposure machine and misalignment of a photomask(s). Thus, 10 the semiconductor device in this embodiment has a structure suitable for miniaturization. Further, with such a structure, the distance between the gate electrode 112 and a source side contact region or a drain side contact region can be reduced to, for example, 0.05  $\mu\text{m}$  to 0.1  $\mu\text{m}$ . Accordingly, the resistance between the source and the drain can be reduced, resulting in more excellent electrical characteristics of the semiconductor 15 device (e.g., higher on-state current characteristics of a transistor).

[0175]

Note that each component that can be used for the semiconductor device in this embodiment can be similar to that in Embodiment 1; therefore, detailed description thereof is omitted and components that are not employed in Embodiment 1 will be 20 described below.

[0176]

#### [Detailed Description of Wirings]

As each of the wiring 119a and the wiring 119b, for example, a metal film containing an element selected from aluminum, chromium, copper, tantalum, titanium, 25 molybdenum, or tungsten, or a metal nitride film containing any of the above elements as its component (e.g., a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film) can be used. Alternatively, each of the wiring 119a and the wiring 119b may have a structure in which a film of a high-melting-point metal such as titanium, molybdenum, or tungsten, or a nitride film of any of these metals (e.g., a titanium 30 nitride film, a molybdenum nitride film, or a tungsten nitride film) is stacked on either or both of the bottom surface and the top surface of a metal film of aluminum, copper, or the like. Further, a conductive film used for the wiring 119a and the wiring 119b

may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide ( $In_2O_3$ ), tin oxide ( $SnO_2$ ), zinc oxide ( $ZnO$ ), indium tin oxide ( $In_2O_3-SnO_2$ , abbreviated to ITO), or indium zinc oxide ( $In_2O_3-ZnO$ ) can be used. The conductive film used for the wiring 119a and the wiring 119b can be formed with a single-layer structure or a stacked structure using any of the above materials. There is no particular limitation on the method for forming the conductive film, and a variety of deposition methods such as an evaporation method, a PE-CVD method, a sputtering method, or a spin coating method can be employed.

[0177]

10 Note that details of the other components will be described in [Method 2 for Manufacturing Semiconductor Device] below, with reference to FIGS. 5A to 5D and FIGS. 6A to 6C.

[0178]

[Method 2 for Manufacturing Semiconductor Device]

15 An example of a method for manufacturing the semiconductor device illustrated in FIGS. 4A to 4C of this embodiment will be described below with reference to FIGS. 5A to 5D and FIGS. 6A to 6C.

[0179]

20 First, referring to the manufacturing method in Embodiment 1, a semiconductor device in a state illustrated in FIG. 5A can be manufactured. Note that a cross-sectional view illustrated in FIG. 5A is the same as the cross-sectional view illustrated in FIG. 3B.

[0180]

25 Then, through a photolithography step, a resist mask is formed over the interlayer insulating film 116, and then the gate insulating film 110, the protective insulating film 114, and the interlayer insulating film 116 are selectively etched, so that a first opening 151a reaching the second oxide semiconductor film 108 (more specifically, the low-resistance region 108b) is formed, and then the resist mask is removed (see FIG. 5B).

30 [0181]

For light exposure at the above photolithography step, extreme ultraviolet light having a wavelength as short as several nanometers to several tens of nanometers is

preferably used. In the light exposure with extreme ultraviolet light, the resolution is high and the focus depth is large. Thus, a fine pattern can be formed. As long as it is possible to form a resist mask having a sufficiently fine pattern, a different method such as an inkjet method may be used to form the resist mask. In this case, it is unnecessary to use a material having a photosensitivity, as a material of the resist mask.

5 [0182]

Then, a resist mask is formed over the first opening 151a and the interlayer insulating film 116, and then the gate insulating film 110, the protective insulating film 114, and the interlayer insulating film 116 are selectively etched, so that a second opening 151b reaching the second oxide semiconductor film 108 (more specifically, the low-resistance region 108b) is formed, and then the resist mask is removed (see FIG. 5C). Thus, a pair of openings with the gate electrode 112 interposed therebetween is formed in the gate insulating film 110, the protective insulating film 114, and the interlayer insulating film 116.

10 15 [0183]

Next, the conductive film 118 is formed over the interlayer insulating film 116 to be embedded in the first opening 151a and the second opening 151b (see FIG. 5D).

[0184]

Next, CMP (chemical mechanical polishing) treatment is performed on the conductive film 118 in order to remove the conductive film 118 provided over the interlayer insulating film 116 (at least a region overlapping with the gate electrode 112); thus, the source electrode 118a and the drain electrode 118b embedded in the first opening 151a and the second opening 151b, respectively, are formed (see FIG. 6A).

[0185]

25 In this embodiment, through the CMP treatment performed on the conductive film 118 under such conditions that a surface of the interlayer insulating film 116 can be exposed, the source electrode 118a and the drain electrode 118b are formed. Note that the surface of the protective insulating film 114 may also be polished depending on conditions of the CMP treatment.

30 [0186]

The CMP treatment is a method for planarizing a surface of an object to be processed by a combination of chemical and mechanical actions. More specifically,

the CMP treatment is a method in which a polishing cloth is attached to a polishing stage, the polishing stage and an object to be processed are each rotated or swung while slurry (abrasive) is supplied between the object to be processed and the polishing cloth, and the surface of the object to be processed is polished by a chemical reaction between 5 the slurry and the surface of the object to be processed and by a mechanical polishing action of the polishing cloth on the object to be processed.

[0187]

Note that the CMP treatment may be performed only once or plural times. When the CMP treatment is performed plural times, first polishing is preferably 10 performed with a high polishing rate followed by final polishing with a low polishing rate. By performing polishing at different polishing rates, the planarity of the surfaces of the source electrode 118a, the drain electrode 118b, and the interlayer insulating film 116 can be further improved.

[0188]

15 Note that in this embodiment, the CMP treatment is employed to remove the conductive film 118; however, another polishing (grinding or cutting) treatment may be employed. Alternatively, the polishing treatment such as the CMP treatment may be combined with etching (dry etching or wet etching) treatment or plasma treatment. For example, after the CMP treatment, dry etching treatment or plasma treatment (e.g., 20 reverse sputtering) may be performed in order to improve the planarity of a surface to be processed. In the case where the polishing treatment is combined with etching treatment, plasma treatment, or the like, the order of the steps may be set as appropriate, without particular limitation, depending on the material, thickness, and roughness of the surface of the conductive film 118.

25 [0189]

As described above, the source electrode 118a and the drain electrode 118b are formed to be embedded in the openings (the first opening 151a and the second opening 151b) provided in the interlayer insulating film 116, the protective insulating film 114, and the gate insulating film 110. Therefore, the distance ( $L_{sG}$  in FIG. 6A) between the 30 gate electrode 112 and a region (a source side contact region) where the source electrode 118a is in contact with the second oxide semiconductor film 108 is determined by the width from the gate electrode 112 to an edge of the first opening 151a. In a

similar manner, the distance (LDG in FIG. 6A) between the gate electrode 112 and a region (a drain side contact region) where the drain electrode 118b is in contact with the second oxide semiconductor film 108 is determined by the width from the gate electrode 112 to an edge of the second opening 151b.

5 [0190]

In the case of forming the first opening 151a for providing the source electrode 118a and the second opening 151b for providing the drain electrode 118b by one-time treatment, the minimum feature size of the width between the first opening 151a and the second opening 151b in the channel length direction is restricted by the resolution limit 10 of a light-exposure machine used for forming a mask. Therefore, it is difficult to scale down the distance between the first opening 151a and the second opening 151b sufficiently, so that it is also difficult to scale down the distance (LSG) between the gate electrode 112 and the source side contact region, and the distance (LDG) between the gate electrode 112 and the drain side contact region.

15 [0191]

However, according to the manufacturing method in this embodiment, the first opening 151a and the second opening 151b are formed with the use of two masks; therefore, the positions of the openings can be set freely without depending on the resolution limit of the light-exposure machine. Thus, the distance (LSG or LDG) 20 between the gate electrode 112 and the source side contact region or the drain side contact region can be reduced to 0.05  $\mu\text{m}$  to 0.1  $\mu\text{m}$ , for example. By reducing LSG and LDG, the resistance between the source and the drain can be reduced, so that the electrical characteristics of the semiconductor device (e.g., on-state current characteristics of the transistor) can be improved.

25 [0192]

Further, since etching treatment using a resist mask is not performed in a step for removing the conductive film 118 over the interlayer insulating film 116 in order to form the source electrode 118a and the drain electrode 118b, fine processing can be performed accurately even in the case where the width between the source electrode 30 118a and the drain electrode 118b in the channel length direction is scaled-down. Thus, in a process for manufacturing the semiconductor device, a miniaturized structure having little variation in shapes and characteristics can be manufactured with a high

yield.

[0193]

Next, a conductive film 119 is deposited over the interlayer insulating film 116, the source electrode 118a, and the drain electrode 118b (see FIG. 6B).

5 [0194]

After that, through a photolithography step, a resist mask is formed over the conductive film 119, and a wiring 119a which is electrically connected to the source electrode 118a and a wiring 119b which is electrically connected the drain electrode 118b are formed (see FIG. 6C).

10 [0195]

Through the above manufacturing steps, the semiconductor device illustrated in FIGS. 4A to 4C can be manufactured.

[0196]

As described in this embodiment, a technical idea of the present invention is as follows. By forming the first oxide semiconductor film over the oxide film and the second oxide semiconductor film to be stacked over the first oxide semiconductor film, at least during the deposition of the second oxide semiconductor film, oxygen release from the oxide film can be suppressed. Further, since the first oxide semiconductor film serves as a base film for the second oxide semiconductor film, the second oxide semiconductor film can have higher crystallinity. The high crystallinity of the second oxide semiconductor film can suppress the generation of oxygen deficiency in the second oxide semiconductor film, and a transistor with stable electrical characteristics can be provided.

[0197]

25 The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

[0198]

(Embodiment 3)

In this embodiment, a modification example of the semiconductor device in Embodiment 1 or Embodiment 2 and a method for manufacturing a semiconductor device, which is different from that in Embodiment 1 or Embodiment 2, will be described with reference to FIGS. 7A to 7C, FIGS. 8A to 8D, FIGS. 9A to 9C, FIGS.

10A to 10C, FIGS. 11A to 11D, and FIGS. 12A to 12C. Note that portions similar to those in FIGS. 1A to 1C, FIGS. 2A to 2D, FIGS. 3A to 3D, FIGS. 4A to 4C, FIGS. 5A to 5D, and FIGS. 6A to 6C are denoted by the same reference numerals, and description thereof is omitted. In addition, detailed description of the same portions is not 5 repeated, either.

[0199]

[Structural Example 3 of Semiconductor Device]

A plan view and cross-sectional views of a top-gate transistor as an example of the semiconductor device are illustrated in FIGS. 7A to 7C. FIG. 7A is the plan view, FIG. 7B corresponds to a cross-sectional view taken along line X3-Y3 in FIG. 7A, and FIG. 7C corresponds to a cross-sectional view taken along line V3-W3 in FIG. 7A. Note that in FIG. 7A, some components of the semiconductor device (e.g., a gate insulating film 110) are omitted for simplicity.

[0200]

15 The semiconductor device illustrated in FIGS. 7A to 7C include an oxide film 104; a first oxide semiconductor film 106 formed over the oxide film 104; a second oxide semiconductor film 108 formed over the first oxide semiconductor film 106; the gate insulating film 110 formed over the second oxide semiconductor film 108; and a gate electrode 112 which is in contact with the gate insulating film 110 and formed in a 20 region overlapping with the second oxide semiconductor film 108.

[0201]

The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are each formed using an oxide film containing at least indium, gallium, and zinc, and the content percentage of gallium in the first oxide semiconductor film 106 is 25 higher than in the second oxide semiconductor film 108.

[0202]

Further, in the first oxide semiconductor film 106, the content percentage of gallium is higher than or equal to that of indium. Furthermore, in the second oxide semiconductor film 108, the content percentage of indium is higher than that of gallium.

30 The high content percentage of indium in the second oxide semiconductor film 108 can lead to higher crystallinity of the second oxide semiconductor film 108.

[0203]

The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are stacked and have different compositions as described above. Further, the first oxide semiconductor film 106 can suppress oxygen release from the oxide film 104 at the time of the formation of the second oxide semiconductor film 108.

5 [0204]

Further, the second oxide semiconductor film 108 is formed over the first oxide semiconductor film 106 which is formed using the same kinds of materials as the second oxide semiconductor film 108. Accordingly, the second oxide semiconductor film 108 can have a crystal portion that grows from the interface with the first oxide 10 semiconductor film 106.

[0205]

That is, the first oxide semiconductor film 106 suppresses oxygen release from the oxide film 104 at least at the time of the deposition of the second oxide semiconductor film 108, and also serves as a base film for the second oxide 15 semiconductor film 108, resulting in higher crystallinity of the second oxide semiconductor film 108. After the second oxide semiconductor film 108 is formed, oxygen is released from the oxide film 104 by heat treatment or the like, and then the oxygen can pass through the first oxide semiconductor film 106 to be supplied to the second oxide semiconductor film 108.

20 [0206]

A structure in which the first oxide semiconductor film 106 and the second oxide semiconductor film 108 are thus stacked has an excellent effect of suppressing the generation of oxygen deficiency in the second oxide semiconductor film 108 and of facilitating the crystallinity of the second oxide semiconductor film 108.

25 [0207]

Note that in the first oxide semiconductor film 106, high-resistance regions 106a are formed in a region overlapping with the gate electrode 112 and regions outside the second oxide semiconductor film 108, and a pair of low-resistance regions 106b is formed adjacent to the region overlapping with the gate electrode 112. Further, in the 30 second oxide semiconductor film 108, a channel region 108a is formed in a region overlapping with the gate electrode 112, and a pair of low-resistance regions 108b is formed adjacent to the region overlapping with the gate electrode 112.

[0208]

The high-resistance region 106a formed outside the second oxide semiconductor film 108 serves as a separation layer between transistors. This is to prevent electrical connection between adjacent transistors, for example, which would 5 occur in the case where the high-resistance region 106a is not provided outside the second oxide semiconductor film 108.

[0209]

The semiconductor device may also include an insulating film 113 formed in a region overlapping with the gate electrode 112; sidewall insulating films 115 which are 10 formed along side surfaces of the gate electrode 112 and the insulating film 113; a source electrode 118a and a drain electrode 118b which are formed in contact with the sidewall insulating films 115 and electrically connected to the second oxide semiconductor film 108; a protective insulating film 114 and an interlayer insulating film 116 which are formed at least over the source electrode 118a and the drain 15 electrode 118b; an insulating film 120 formed over the interlayer insulating film 116; and a wiring 119a and a wiring 119b which are electrically connected to the source electrode 118a and the drain electrode 118b, respectively, through openings formed in the insulating film 120, the interlayer insulating film 116, and the protective insulating film 114. Note that since the source electrode 118a and the drain electrode 118b are in 20 contact with the pair of low-resistance regions 108b formed in the second oxide semiconductor film 108, the contact resistance can be low.

[0210]

The structure of the semiconductor device in this embodiment differs from that of the semiconductor device in Embodiment 1 in that the insulating film 113 over the 25 gate electrode 112 is formed, the sidewall insulating films 115 along the side surfaces of the gate electrode 112 are formed, the source electrode 118a and the drain electrode 118b are formed in contact with the sidewall insulating films 115, and the insulating film 120 is formed.

[0211]

30 Further, in the semiconductor device in this embodiment, a conductive film to be used for the source electrode 118a and the drain electrode 118b is formed over the insulating film 113 and the sidewall insulating films 115, and then is subjected to

planarization treatment (also referred to as polishing treatment) so as to be partly removed, whereby the source electrode 118a and the drain electrode 118b are formed. Thus, it is unnecessary to employ a photolithography step to form the source electrode 118a and the drain electrode 118b, and accordingly, the source electrode 118a and the drain electrode 118b can be formed without any concerns about the accuracy of a light-exposure machine and misalignment of a photomask(s). Thus, the semiconductor device in this embodiment has a structure suitable for miniaturization.

[0212]

10 Note that each component that can be used for the semiconductor device in this embodiment can be similar to that in Embodiment 1 or Embodiment 2; therefore, detailed description thereof is omitted and components that are not employed in Embodiment 1 or Embodiment 2 will be described below.

[0213]

[Detailed Description of Insulating Film and Sidewall Insulating Films]

15 The insulating film 113, the sidewall insulating films 115, and the insulating film 120 are each preferably formed using an inorganic insulating film and may be formed as a single layer or a stacked layer using any of a silicon oxide film, a silicon oxynitride film, a silicon nitride film, and a silicon nitride oxide film. There is no particular limitation on a method for forming the insulating film 113, the sidewall insulating films 115, and the insulating film 120; for example, a sputtering method, an MBE method, a PE-CVD method, a pulse laser deposition method, an ALD method, or the like can be employed as appropriate.

[0214]

25 Note that details of the other components will be described in [Method 3 for Manufacturing Semiconductor Device] below, with reference to FIGS. 8A to 8D, FIGS. 9A to 9C, FIGS. 10A to 10C, FIGS. 11A to 11D, and FIGS. 12A to 12C.

[0215]

[Method 3 for Manufacturing Semiconductor Device]

30 An example of a method for manufacturing the semiconductor device illustrated in FIGS. 7A to 7C of this embodiment will be described below with reference to FIGS. 8A to 8D, FIGS. 9A to 9C, FIGS. 10A to 10C, FIGS. 11A to 11D, and FIGS. 12A to 12C.

[0216]

First, referring to the manufacturing method in Embodiment 1, a semiconductor device in a state illustrated in FIG. 8A can be manufactured. Note that a cross-sectional view illustrated in FIG. 8A is the same as the cross-sectional view 5 illustrated in FIG. 2B.

[0217]

Next, an insulating film 113a is formed over a conductive film 111 (see FIG. 8B).

[0218]

10 Next, through a photolithography step, a resist mask is formed over the insulating film 113a, and selective etching is performed on the insulating film 113a and the conductive film 111 to form the insulating film 113 and the gate electrode 112 (see FIG. 8C).

[0219]

15 Then, a resist mask 134 is formed over the gate insulating film 110 and the insulating film 113 (see FIG. 8D).

[0220]

20 Next, the resist mask 134 is selectively subjected to light exposure and development through a photolithography step to form a resist mask 134a or a resist mask 134b. After that, with the use of the gate electrode 112, the insulating film 113, and the resist mask (the resist mask 134a or the resist mask 134b) as masks, a dopant 142 is introduced into the first oxide semiconductor film 106 and the second oxide semiconductor film 108. The introduction of the dopant 142 makes the first oxide semiconductor film 106 have the high-resistance regions 106a and the pair of low-resistance regions 106b which are adjacent to a region overlapping with the gate electrode 112. The introduction of the dopant 142 also makes the second oxide semiconductor film 108 have the channel region 108a and the pair of low-resistance regions 108b which are adjacent to a region overlapping with the gate electrode 112 (see FIG. 9B and 10B).

25 [0221]

To clearly show the positions where the dopant 142 is introduced and the low-resistance regions 106b and the low-resistance regions 108b are formed, this

embodiment will be described with reference to cross-sectional views and plan views in FIGS. 9A to 9C and FIGS. 10A to 10C.

[0222]

FIG. 9A is the plan view, FIG. 9B corresponds to a cross-sectional view taken 5 along line X3-Y3 in FIG. 9A, and FIG. 9C corresponds to a cross-sectional view taken along line V3-W3 in FIG. 9A. Note that in FIG. 9A, some components of the semiconductor device (e.g., the gate insulating film 110) are omitted for simplicity. Further, FIG. 10A is the plan view, FIG. 10B corresponds to a cross-sectional view taken along line X3-Y3 in FIG. 10A, and FIG. 10C corresponds to a cross-sectional view 10 taken along line V3-W3 in FIG. 10A. Note that in FIG. 10A, some components of the semiconductor device (e.g., the gate insulating film 110) are omitted for simplicity.

[0223]

Further, two kinds of manufacturing methods about the positions where the low-resistance regions 106b and the low-resistance regions 108b are formed will be 15 described with reference to FIGS. 9A to 9C and FIGS. 10A to 10C. Note that the method shown in FIGS. 9A to 9C and the method shown in FIGS. 10A to 10C are each one embodiment of the present invention.

[0224]

The following will show a difference between the manufacturing methods 20 shown in FIGS. 9A to 9C and FIGS. 10A to 10C.

[0225]

In accordance with the manufacturing method shown in FIGS. 9A to 9C, the resist mask 134a is formed outside the second oxide semiconductor film 108 (see FIGS. 9A to 9C).

25 [0226]

In contrast, in accordance with the manufacturing method shown in FIGS. 10A to 10C, the resist mask 134b is formed also a region between the long sides of the second oxide semiconductor film 108 (see FIGS. 10A to 10C).

[0227]

30 In accordance with the manufacturing method shown in FIGS. 9A to 9C, the entire surface except the channel region 108a becomes the low-resistance region 108b; accordingly, contact regions with the source electrode 118a and the drain electrode 118b,

which are formed later, can be large. In contrast, in accordance with the manufacturing method shown in FIGS. 10A to IOC, the region between the long sides of the second oxide semiconductor film 108 is made to have higher resistance than the low-resistance region 108b as in the channel region 108a; thus, the generation of a 5 parasitic channel (also referred to as a parasitic transistor) that can occur in the long-side direction of the second oxide semiconductor film 108 can be suppressed.

[0228]

By changing the shape of the resist mask 134a and the shape of the resist mask 134b in the above manner, semiconductor devices having different effects can be 10 manufactured.

[0229]

Next, the resist mask (the resist mask 134a or the resist mask 134b) is removed, and then an insulating film 115a is formed over the gate insulating film 110 and the insulating film 113 (see FIG. 11A).

15 [0230]

Then, the sidewall insulating films 115 are formed by etching the insulating film 115a. The sidewall insulating films 115 can be formed in a self-aligned manner by performing a highly anisotropic etching step on the insulating film 115a. As an example of an etching method, a dry etching method is preferably employed. As an 20 example of an etching gas used for the dry etching method, a gas containing fluorine such as trifluoromethane, octafluorocyclobutane, or tetrafluoromethane can be used. A rare gas or hydrogen may be added to the etching gas. As the dry etching method, a reactive ion etching (RIE) method in which high-frequency voltage is applied to a substrate is preferably employed. After the sidewall insulating films 115 are formed, 25 the gate insulating film 110 is processed with the use of the gate electrode 112, the insulating film 113, and the sidewall insulating films 115 as masks, whereby the first oxide semiconductor film 106 and the second oxide semiconductor film 108 are exposed (see FIG. 11B). Note that the gate insulating film 110 may be processed at the time of the formation of the sidewall insulating films 115.

30 [0231]

Note that in this embodiment, in a step shortly after the formation of the gate electrode 112 and the insulating film 113, the dopant 142 is introduced into the first

oxide semiconductor film 106 and the second oxide semiconductor film 108 with the use of the gate electrode 112, the insulating film 113, and the resist mask (the resist mask 134a or the resist mask 134b) as masks. However, after the sidewall insulating films 115 are formed, the dopant 142 may be introduced into the first oxide semiconductor film 106 and the second oxide semiconductor film 108 with the use of the gate electrode 112, the insulating film 113, and the sidewall insulating films 115, and a resist mask as masks. In such a manner, regions of the first oxide semiconductor film 106 and the second oxide semiconductor film 108, which overlap with the sidewall insulating films 115, can be included in the high-resistance regions.

10 [0232]

Next, a conductive film is formed to cover the first oxide semiconductor film 106, the second oxide semiconductor film 108, the insulating film 113, and the sidewall insulating film 115. The conductive film is subjected to a photolithography step and an etching step to form a conductive film 118 (see FIG. 11C).

15 [0233]

Then, an insulating film 114a and an insulating film 116a are formed over the first oxide semiconductor film 106 and the conductive film 118 (see FIG. 11D).

[0234]

Next, in order to remove the conductive film 118 provided over the insulating film 113 (at least in a region overlapping with the gate electrode 112), CMP treatment is performed on the insulating film 114a, the insulating film 116a, and the conductive film 118. Thus, the insulating film 114a, the insulating film 116a, and the conductive film 118 are divided, and the protective insulating film 114, the interlayer insulating film 116, the source electrode 118a, and the drain electrode 118b are formed in the state where the gate electrode 112 is interposed between divided parts of the protective insulating film 114, divided parts of the interlayer insulating film 116, and the source electrode 118a and the drain electrode 118b (see FIG. 12A).

[0235]

Note that surfaces of the source electrode 118a and the drain electrode 118b are flush with surfaces of the insulating film 113 and the interlayer insulating film 116 in FIG. 12A. However, in the case where the surfaces of the source electrode 118a and the drain electrode 118b, the insulating film 113, and the interlayer insulating film 116

are polished with a CMP apparatus and polishing speeds (or polishing rates) are different among the source electrode 118a, the drain electrode 118b, the insulating film 113, and the interlayer insulating film 116, the surfaces of the source electrode 118a and the drain electrode 118b might not be flush with the surfaces of the insulating film 113 or the interlayer insulating film 116, generating steps. For example, the surfaces of the source electrode 118a and the drain electrode 118b become lower than the surface of the insulating film 113 (a depression is formed) in some cases. Depending on CMP treatment conditions, the sidewall insulating films 115 might be polished too.

[0236]

10 Note that for the CMP treatment here, the description of the CMP treatment performed on the conductive film 118 in Embodiment 2 can be referred to.

[0237]

15 Next, the insulating film 120 is formed over the protective insulating film 114, the interlayer insulating film 116, the source electrode 118a, and the drain electrode 118b (see FIG. 12B).

[0238]

20 Then, through a photolithography step, a resist mask is formed over the insulating film 120, and the protective insulating film 114, the interlayer insulating film 116, and the insulating film 120 are selectively etched so that openings reaching the source electrode 118a and the drain electrode 118b are formed, and then the resist mask is removed. Then, a conductive film is deposited to cover the openings, followed by a photolithography step through which a resist mask is formed over the conductive film and etching is selectively performed on the conductive film to form the wiring 119a and wiring 119b (see FIG. 12C).

25 [0239]

Through the above manufacturing steps, the semiconductor device illustrated in FIGS. 7A to 7C can be manufactured.

[0240]

30 As described in this embodiment, a technical idea of the present invention is as follows. By forming the first oxide semiconductor film over the oxide film and the second oxide semiconductor film to be stacked over the first oxide semiconductor film, at least during the deposition of the second oxide semiconductor film, oxygen release

from the oxide film can be suppressed. Further, since the first oxide semiconductor film serves as a base film for the second oxide semiconductor film, the second oxide semiconductor film can have higher crystallinity. The high crystallinity of the second oxide semiconductor film can suppress the generation of oxygen deficiency in the 5 second oxide semiconductor film, and a transistor with stable electrical characteristics can be provided.

[0241]

The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

10 [0242]

(Embodiment 4)

In this embodiment, a modification example of the semiconductor device in any of Embodiments 1 to 3 and a method for manufacturing a semiconductor device, which is different from that in any of Embodiments 1 to 3, will be described with 15 reference to FIGS. 13A to 13C, FIGS. 14A to 14D, FIGS. 15A to 15D, FIGS. 16A to 16D, and FIGS. 17A and 17B. Note that portions similar to those in FIGS. 1A to 1C, FIGS. 2A to 2D, FIGS. 3A to 3D, FIGS. 4A to 4C, FIGS. 5A to 5D, FIGS. 6A to 6C, FIGS. 7A to 7C, FIGS. 8A to 8D, FIGS. 9A to 9C, FIGS. 10A to 10C, FIGS. 11A to 11D, and FIGS. 12A to 12C are denoted by the same reference numerals, and description 20 thereof is omitted. In addition, detailed description of the same portions is not repeated, either.

[0243]

[Structural Example 4 of Semiconductor Device]

A plan view and cross-sectional views of a top-gate transistor as an example of 25 the semiconductor device are illustrated in FIGS. 13A to 13C. FIG. 13A is the plan view, FIG. 13B corresponds to a cross-sectional view taken along line X4-Y4 in FIG. 13A, and FIG. 13C corresponds to a cross-sectional view taken along line V4-W4 in FIG. 13A. Note that in FIG. 13A, some components of the semiconductor device (e.g., a gate insulating film 110) are omitted for simplicity.

30 [0244]

The semiconductor device illustrated in FIGS. 13 to 13C include an oxide film 104; a first oxide semiconductor film 106 formed over the oxide film 104; a second

oxide semiconductor film 108 formed over the first oxide semiconductor film 106; the gate insulating film 110 formed over the second oxide semiconductor film 108; and a gate electrode 112 which is in contact with the gate insulating film 110 and formed in a region overlapping with the second oxide semiconductor film 108.

5 [0245]

The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are each formed using an oxide film containing at least indium, gallium, and zinc, and the content percentage of gallium in the first oxide semiconductor film 106 is higher than in the second oxide semiconductor film 108.

10 [0246]

Further, in the first oxide semiconductor film 106, the content percentage of gallium is higher than or equal to that of indium. Furthermore, in the second oxide semiconductor film 108, the content percentage of indium is higher than that of gallium. The high content percentage of indium in the second oxide semiconductor film 108 can 15 lead to higher crystallinity of the second oxide semiconductor film 108.

[0247]

The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are stacked and have different compositions as described above. Further, the first oxide semiconductor film 106 can suppress oxygen release from the oxide film 104 20 at the time of the formation of the second oxide semiconductor film 108.

[0248]

Further, the second oxide semiconductor film 108 is formed over the first oxide semiconductor film 106 which is formed using the same kinds of materials as the second oxide semiconductor film 108, whereby the second oxide semiconductor film 25 108 can have a crystal portion that grows from the interface with the first oxide semiconductor film 106.

[0249]

That is, the first oxide semiconductor film 106 suppresses oxygen release from the oxide film 104 at least at the time of the deposition of the second oxide 30 semiconductor film 108, and also serves as a base film for the second oxide semiconductor film 108, resulting in higher crystallinity of the second oxide semiconductor film 108. After the second oxide semiconductor film 108 is formed,

oxygen is released from the oxide film 104 by heat treatment or the like, and then the oxygen can pass through the first oxide semiconductor film 106 to be supplied to the second oxide semiconductor film 108.

[0250]

5 A structure in which the first oxide semiconductor film 106 and the second oxide semiconductor film 108 are thus stacked has an excellent effect of suppressing the generation of oxygen deficiency in the second oxide semiconductor film 108 and of facilitating the crystallinity of the second oxide semiconductor film 108.

[0251]

10 Note that in the first oxide semiconductor film 106, high-resistance regions 106a are formed in a region overlapping with the gate electrode 112 and regions outside the second oxide semiconductor film 108, and a pair of low-resistance regions 106b is formed adjacent to the region overlapping with the gate electrode 112. Further, in the second oxide semiconductor film 108, a channel region 108a is formed in a region 15 overlapping with the gate electrode 112, and a pair of low-resistance regions 108b is formed adjacent to the region overlapping with the gate electrode 112.

[0252]

20 The high-resistance region 106a formed outside the second oxide semiconductor film 108 serves as a separation layer between transistors. This is to prevent electrical connection between adjacent transistors, for example, which would occur in the case where the high-resistance region 106a is not provided outside the second oxide semiconductor film 108.

[0253]

25 The semiconductor device may also include, in a cross section taken along the channel length, a source electrode 118a in contact with one side surface of the second oxide semiconductor film 108; a drain electrode 118b in contact with the other side surface of the second oxide semiconductor film 108; a first conductive film 121a formed along one side surface of the gate electrode 112; a second conductive film 121b formed along the other side surface of the gate electrode 112; sidewall insulating films 30 115 which are formed on side surfaces of the first conductive film 121a and the second conductive films 121b; a protective insulating film 114 formed over the first oxide semiconductor film 106, the source electrode 118a, the drain electrode 118b, the

sidewall insulating films 115, and the gate electrode 112; an interlayer insulating film 116 formed over the protective insulating film 114; a wiring 119a and a wiring 119b which are electrically connected to the source electrode 118a and the drain electrode 118b, respectively. Note that since the source electrode 118a and the drain electrode 5 118b are in contact with the pair of low-resistance regions 108b formed in the second oxide semiconductor film 108, the contact resistance can be low.

[0254]

The structure of the semiconductor device in this embodiment differs from that of the semiconductor device in Embodiment 1 in that the first conductive film 121a, the 10 second conductive film 121b, and the sidewall insulating films 115 are formed along both side surfaces of the gate electrode 112, and the source electrode 118a and the drain electrode 118b are in contact with one side surface and the other side surface of the second oxide semiconductor film 108, respectively, in a cross section taken along the channel length.

15 [0255]

Further, in the semiconductor device in this embodiment, at least part of the first conductive film 121a formed along the one side surface of the gate electrode 112 is formed over the source electrode 118a with the gate insulating film 110 interposed therebetween, and at least part of the second conductive film 121b formed along the 20 other side surface of the gate electrode 112 is formed over the drain electrode 118b with the gate insulating film 110 interposed therebetween. In this manner, it is possible to provide a region (also referred to as an Lov region) in which part of the gate electrode 112 (more specifically, the gate electrode 112, the first conductive film 121a, and the second conductive film 121b) overlaps with the source electrode 118a and the drain 25 electrode 118b with the gate insulating film 110 interposed therebetween. Thus, the semiconductor device in this embodiment has a structure suitable for miniaturization and can suitably suppress a reduction in on-state current due to miniaturization.

[0256]

Note that each component that can be used for the semiconductor device in this 30 embodiment can be similar to that in any of Embodiments 1 to 3; therefore, detailed description thereof is omitted and components that are not employed in any of Embodiment 1 to 3 will be described below.

[0257]

[Detailed Description of First Conductive Film and Second Conductive Film]

The first conductive film 121a and the second conductive film 121b can be formed, for example, by processing a metal film of tungsten, titanium, or the like or a 5 silicon film or the like containing an impurity element such as phosphorus or boron as long as the first conductive film 121a and the second conductive film 121b have conductivity. Alternatively, the first conductive film 121a and the second conductive film 121b which have conductivity may be provided by forming a polycrystalline silicon film over the gate electrode 112, forming a conductive film in contact with the 10 gate electrode 112 by etching, introducing an impurity element such as phosphorus or boron into the conductive film by doping, and performing heat treatment.

[0258]

Note that details of the other components will be described in [Method 4 for Manufacturing Semiconductor Device] below, with reference to FIGS. 14A to 14D, 15 FIGS. 15A to 15D, FIGS. 16A to 16D, and FIGS. 17A and 17B.

[0259]

[Method 4 for Manufacturing Semiconductor Device]

An example of a method for manufacturing the semiconductor device illustrated in FIGS. 13A to 13C of this embodiment will be described below with 20 reference to FIGS. 14A to 14D, FIGS. 15A to 15D, FIGS. 16A to 16D, and FIGS. 17A and 17B.

[0260]

First, referring to the manufacturing method in Embodiment 1, a semiconductor device in a state illustrated in FIG. 14A can be manufactured. Note that 25 a cross section in FIG. 14A is a modulation example of the semiconductor device in FIG. 2B, and is different only in the area of the second oxide semiconductor film 108.

[0261]

Then, a conductive film is deposited over the first oxide semiconductor film 106 and the second oxide semiconductor film 108, followed by a photolithography step 30 through which a resist mask is formed over the conductive film and etching is selectively performed on the conductive film to form a conductive film 118 (see FIG. 14B).

[0262]

Next, CMP treatment is performed on the conductive film 118 to remove part of the conductive film 118, so that the second semiconductor film 108 is exposed. The CMP treatment can remove a region of the conductive film 118, which overlaps with the 5 second oxide semiconductor film 108, whereby the source electrode 118a and the drain electrode 118b are formed (see FIG. 14C).

[0263]

Note that for the CMP treatment here, the description of the CMP treatment performed on the conductive film 118 in Embodiment 2 can be referred to.

10 [0264]

Next, the gate insulating film 110 and a conductive film 111 are formed over the first oxide semiconductor film 106, the second oxide semiconductor film 108, the source electrode 118a, and the drain electrode 118b (see FIG. 14D).

[0265]

15 Next, through a photolithography step, a resist mask is formed over the conductive film 111, and selective etching is performed on the conductive film 111 to form the gate electrode 112 (see FIG. 15A).

[0266]

Then, a resist mask 136 is formed over the gate insulating film 110 and the gate 20 electrode 112 (see FIG. 15B).

[0267]

Next, the resist mask 136 is selectively subjected to light exposure and development through a photolithography step to form a resist mask 136a. After that, with the use of the gate electrode 112 and the resist mask 136a as masks, a dopant 142 is 25 introduced into the first oxide semiconductor film 106 and the second oxide semiconductor film 108. The introduction of the dopant 142 makes the first oxide semiconductor film 106 have the high-resistance regions 106a and the pair of low-resistance regions 106b which are adjacent to a region overlapping with the gate electrode 112. The introduction of the dopant 142 also makes the second oxide 30 semiconductor film 108 have the channel region 108a and the pair of low-resistance regions 108b which are adjacent to a region overlapping with the gate electrode 112 (see FIG. 15C).

[0268]

Note that this embodiment has shown a structure in which the dopant 142 is introduced into the first oxide semiconductor film 106 through the source electrode 118a and the drain electrode 118b to form the low-resistance region 106b; however, the 5 present invention is not limited thereto. Regions of the first oxide semiconductor film 106, which overlap with the source electrode 118a and the drain electrode 118b, may have the same impurity concentration as the high-resistance region 106a.

[0269]

Next, the resist mask 136a is removed and a conductive film 121 is formed 10 over the gate insulating film 110 and the gate electrode 112 (see FIG. 15D).

[0270]

Next, an insulating film 115a is formed over a conductive film 121 (see FIG. 16A).

[0271]

15 Then, the sidewall insulating films 115 are formed by etching the insulating film 115a. The sidewall insulating films 115 can be formed in a self-aligned manner by performing a highly anisotropic etching step on the insulating film 115a. As an example of an etching method, a dry etching method is preferably employed. As an example of an etching gas used for the dry etching method, a gas containing fluorine 20 such as trifluoromethane, octafluorocyclobutane, or tetrafluoromethane can be used. A rare gas or hydrogen may be added to the etching gas. As the dry etching method, a reactive ion etching (RIE) method in which high-frequency voltage is applied to a substrate is preferably employed. After the sidewall insulating films 115 are formed, the conductive film 121 and the gate insulating film 110 are processed with the use of 25 the gate electrode 112 and the sidewall insulating films 115 as masks, whereby the first oxide semiconductor film 106, the source electrode 118a, and the drain electrode 118b are exposed (see FIG. 16B). Note that the conductive film 121 and the gate insulating film 110 may be processed at the time of the formation of the sidewall insulating films 115. In this embodiment, the conductive film 121 is divided into the first conductive 30 film 121a and the second conductive film 121b, part of the gate insulating film 110 is removed, and part of surfaces of the source electrode 118a and the drain electrode 118b is exposed.

[0272]

Next, the protective insulating film 114 and the interlayer insulating film 116 are formed to cover the first oxide semiconductor film 106, the gate electrode 112, the sidewall insulating films 115, the first conductive film 121a, the second conductive film 5 121b, the source electrode 118a, and the drain electrode 118b (see FIG. 16C).

[0273]

Then, through a photolithography step, a resist mask is formed over the interlayer insulating film 116, and the protective insulating film 114 and the interlayer insulating film 116 are selectively etched so that openings reaching the source electrode 10 118a and the drain electrode 118b are formed, and then the resist mask is removed (see FIG. 16D).

[0274]

Next, the conductive film 119 is formed over the interlayer insulating film 116 to be embedded in the openings (see FIG. 17A).

15 [0275]

Then, through a photolithography step, a resist mask is formed over the conductive film 119, and the conductive film 119 is selectively etched, so that the wiring 119a and wiring 119b are formed (see FIG. 17B).

[0276]

20 Through the above manufacturing steps, the semiconductor device illustrated in FIGS. 13A to 13C can be manufactured.

[0277]

As described in this embodiment, a technical idea of the present invention is as follows. By forming the first oxide semiconductor film over the oxide film and the 25 second oxide semiconductor film to be stacked over the first oxide semiconductor film, at least during the deposition of the second oxide semiconductor film, oxygen release from the oxide film can be suppressed. Further, since the first oxide semiconductor film serves as a base film for the second oxide semiconductor film, the second oxide semiconductor film can have higher crystallinity. The high crystallinity of the second 30 oxide semiconductor film can suppress the generation of oxygen deficiency in the second oxide semiconductor film, and a transistor with stable electrical characteristics can be provided.

[0278]

The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

[0279]

5 (Embodiment 5)

In this embodiment, a modification example of the semiconductor device in any of Embodiments 1 to 4 and a method for manufacturing a semiconductor device, which is different from that in any of Embodiments 1 to 4, will be described with reference to FIGS. 18A to 18C, FIGS. 19A to 19D, FIGS. 20A to 20D, and FIGS. 21A to 21C. Note that portions similar to those in FIGS. 1A to 1C, FIGS. 2A to 2D, FIGS. 3A to 3D, FIGS. 4A to 4C, FIGS. 5A to 5D, FIGS. 6A to 6C, FIGS. 7A to 7C, FIGS. 8A to 8D, FIGS. 9A to 9C, FIGS. 10A to 10C, FIGS. 11A to 11D, FIGS. 12A to 12C, FIGS. 13A to 13C, FIGS. 14A to 14D, FIGS. 15A to 15D, FIGS. 16A to 16D, and FIGS. 17A and 17B are denoted by the same reference numerals, and description thereof is omitted.

10 In addition, detailed description of the same portions is not repeated, either.

[0280]

[Structural Example 5 of Semiconductor Device]

A plan view and cross-sectional views of a top-gate transistor as an example of the semiconductor device are illustrated in FIGS. 18A to 18C. FIG. 18A is the plan view, FIG. 18B corresponds to a cross-sectional view taken along line X5-Y5 in FIG. 18A, and FIG. 18C corresponds to a cross-sectional view taken along line V5-W5 in FIG. 18A. Note that in FIG. 18A, some components of the semiconductor device (e.g., a gate insulating film 110) are omitted for simplicity.

[0281]

25 The semiconductor device illustrated in FIGS. 18A to 18C include an oxide film 104; a first oxide semiconductor film 106 formed over the oxide film 104; a second oxide semiconductor film 108 formed over the first oxide semiconductor film 106; the gate insulating film 110 formed over the second oxide semiconductor film 108; and a gate electrode 112 which is in contact with the gate insulating film 110 and formed in a 30 region overlapping with the second oxide semiconductor film 108.

[0282]

The first oxide semiconductor film 106 and the second oxide semiconductor

film 108 are each formed using an oxide film containing at least indium, gallium, and zinc, and the content percentage of gallium in the first oxide semiconductor film 106 is higher than in the second oxide semiconductor film 108.

[0283]

5 Further, in the first oxide semiconductor film 106, the content percentage of gallium is higher than or equal to that of indium. Furthermore, in the second oxide semiconductor film 108, the content percentage of indium is higher than that of gallium. The high content percentage of indium in the second oxide semiconductor film 108 can lead to higher crystallinity of the second oxide semiconductor film 108.

10 [0284]

The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are stacked and have different compositions as described above. Further, the first oxide semiconductor film 106 can suppress oxygen release from the oxide film 104 at the time of the formation of the second oxide semiconductor film 108.

15 [0285]

Further, the second oxide semiconductor film 108 is formed over the first oxide semiconductor film 106 which is formed using the same kinds of materials as the second oxide semiconductor film 108, whereby the second oxide semiconductor film 108 can have a crystal portion that grows from the interface with the first oxide 20 semiconductor film 106.

[0286]

That is, the first oxide semiconductor film 106 suppresses oxygen release from the oxide film 104 at least at the time of the deposition of the second oxide semiconductor film 108, and also serves as a base film for the second oxide 25 semiconductor film 108, resulting in higher crystallinity of the second oxide semiconductor film 108. After the second oxide semiconductor film 108 is formed, oxygen is released from the oxide film 104 by heat treatment or the like, and then the oxygen can pass through the first oxide semiconductor film 106 to be supplied to the second oxide semiconductor film 108.

30 [0287]

A structure in which the first oxide semiconductor film 106 and the second oxide semiconductor film 108 are thus stacked has an excellent effect of suppressing the

generation of oxygen deficiency in the second oxide semiconductor film 108 and of facilitating the crystallinity of the second oxide semiconductor film 108.

[0288]

Note that in the first oxide semiconductor film 106, high-resistance regions 106a are formed in a region overlapping with the gate electrode 112 and regions outside the second oxide semiconductor film 108, and a pair of low-resistance regions 106b is formed adjacent to the region overlapping with the gate electrode 112. Further, in the second oxide semiconductor film 108, a channel region 108a is formed in a region overlapping with the gate electrode 112, and a pair of low-resistance regions 108b is formed adjacent to the region overlapping with the gate electrode 112.

[0289]

The high-resistance region 106a formed outside the second oxide semiconductor film 108 serves as a separation layer between transistors. This is to prevent electrical connection between adjacent transistors, for example, which would occur in the case where the high-resistance region 106a is not provided outside the second oxide semiconductor film 108.

[0290]

The semiconductor device may also include a protective insulating film 114 formed over the gate electrode 112; an interlayer insulating film 116 formed over the protective insulating film 114; a source electrode 118a and a drain electrode 118b which are, in a cross section in the channel length direction, in contact with side surfaces of the second oxide semiconductor film 108 in openings penetrating through the interlayer insulating film 116, the protective insulating film 114, the gate insulating film 110, and the second oxide semiconductor film 108; and a wiring 119a and a wiring 119b which are electrically connected to the source electrode 118a and the drain electrode 118b, respectively. Note that since the source electrode 118a and the drain electrode 118b are in contact with the pair of low-resistance regions 108b formed in the second oxide semiconductor film 108, the contact resistance can be low.

[0291]

A structure of the semiconductor device in this embodiment differs from that of the semiconductor device in Embodiment 1 in that the source electrode 118a and the drain electrode 118b are embedded in the openings formed in the gate insulating film

110, the protective insulating film 114, the interlayer insulating film 116, and the second oxide semiconductor film 108; and the wiring 119a and the wiring 119b are formed, which are electrically connected to the source electrode 118a and the drain electrode 118b, respectively.

5 [0292]

The structure of the semiconductor device in this embodiment differs from that of the semiconductor device in Embodiment 1 also in the shapes of the second oxide semiconductor film 108, the gate insulating film 110 which cover the top surface and side surfaces of the channel region 108a in the second oxide semiconductor film 108, and the gate electrode 112.

10 [0293]

Note that in the semiconductor device in this embodiment, a channel is formed in the top surface and side surfaces of the second oxide semiconductor film 108 (more specifically, in the channel region 108a).

15 [0294]

In this manner, in the semiconductor device in this embodiment, the second oxide semiconductor film 108 in a thick state (so-called a plate shape) is formed, the gate insulating film 110 is formed to cover the top surface and side surfaces of the second oxide semiconductor film 108, and the gate electrode 112 is formed over the gate insulating film 110. Thus, the channel width corresponds to the total length of the top surface and side surfaces of the second oxide semiconductor film 108 (more specifically, the channel region 108a); therefore, the substantial channel width can be larger without increasing a width of the top surface of the second oxide semiconductor film 108. The increase in the channel width can suppress a reduction in the on-state current of the transistor and variations in electrical characteristics of transistors.

20 [0295]

Note that each component that can be used for the semiconductor device in this embodiment can be similar to that in any of Embodiments 1 to 4; therefore, detailed description thereof is omitted and components that are not employed in any of 25 Embodiments 1 to 4 will be described below.

[0296]

[Detailed Description of Second Oxide Semiconductor Film]

The second oxide semiconductor film 108 can be formed in the same manner as in Embodiment 1 except for a difference in the thickness. The thickness of the second oxide semiconductor film 108 in this embodiment is greater than 5 nm and less than or equal to 500 nm, preferably greater than or equal to 100 nm and less than or 5 equal to 300 nm.

[0297]

Note that details of the other components will be described in [Method 5 for Manufacturing Semiconductor Device] below, with reference to FIGS. 19A to 19D, FIGS. 20A to 20C, and FIGS. 21A to 21C.

10 [0298]

[Method 5 for Manufacturing Semiconductor Device]

An example of a method for manufacturing the semiconductor device illustrated in FIGS. 18A to 18C of this embodiment will be described below with reference to FIGS. 19A to 19D, FIGS. 20A to 20C, and FIGS. 21A to 21C.

15 [0299]

First, referring to the manufacturing method in Embodiment 1, a semiconductor device in a state illustrated in FIG. 19A can be manufactured. Note that a cross section in FIG. 19A is a modulation example of the semiconductor device in FIG. 2A, and is different only in the thickness of the second oxide semiconductor film 108.

20 [0300]

Next, the gate insulating film 110 and a conductive film 111 are formed over the first oxide semiconductor film 106 and the second oxide semiconductor film 108 (see FIG. 19B).

[0301]

25 Next, through a photolithography step, a resist mask is formed over the conductive film 111, and selective etching is performed on the conductive film 111 to form the gate electrode 112 (see FIG. 19C).

[0302]

Then, a resist mask 138 is formed over the gate insulating film 110 and the gate 30 electrode 112 (see FIG. 19D).

[0303]

Next, the resist mask 138 is selectively subjected to light exposure and

development through a photolithography step to form a resist mask 138a. After that, with the use of the gate electrode 112 and the resist mask 138a as masks, a dopant 142 is introduced into the first oxide semiconductor film 106 and the second oxide semiconductor film 108. The introduction of the dopant 142 makes the first oxide 5 semiconductor film 106 have the high-resistance regions 106a and the pair of low-resistance regions 106b which are adjacent to a region overlapping with the gate electrode 112. The introduction of the dopant 142 also makes the second oxide semiconductor film 108 have the channel region 108a and the pair of low-resistance regions 108b which are adjacent to a region overlapping with the gate electrode 112 (see 10 FIG. 20A).

[0304]

Note that this embodiment has shown a structure in which the dopant 142 is introduced into the first oxide semiconductor film 106 through the second oxide semiconductor film 108 to form the low-resistance region 106b; however, the present 15 invention is not limited thereto. Regions of the first oxide semiconductor film 106, which overlap with the second oxide semiconductor film 108, may have the same impurity concentration as the high-resistance region 106a.

[0305]

Next, the resist mask 138a is removed and the protective insulating film 114 20 and the interlayer insulating film 116 are formed over the gate insulating film 110 and the gate electrode 112 (see FIG. 20B).

[0306]

Then, through a photolithography step, a resist mask is formed over the interlayer insulating film 116, and then the interlayer insulating film 116, the protective insulating film 114, and the second oxide semiconductor film 108 are selectively etched, 25 so that an openings 153a reaching the first oxide semiconductor film 106 is formed, and then the resist mask is removed (see FIG. 20C).

[0307]

Then, through a photolithography step, a resist mask is formed over the 30 opening 153a and the interlayer insulating film 116, and then the interlayer insulating film 116, the protective insulating film 114, and the second oxide semiconductor film 108 are selectively etched, so that an openings 153b reaching the first oxide

semiconductor film 106 is formed, and then the resist mask is removed (see FIG. 20D). Thus, a pair of openings with the gate electrode 112 and the channel region 108a interposed therebetween is formed.

[0308]

5 Note that this embodiment has shown a structure in which the opening 153a and the opening 153b reach the first oxide semiconductor film 106; however, the present invention is not limited thereto. For example, the opening 153a and the opening 153b may reach the oxide film 104.

[0309]

10 However, according to the manufacturing method in this embodiment, as in the manufacturing method in Embodiment 2, the opening 153a and the opening 153b are formed with the use of two masks; therefore, the positions of the openings can be set freely without depending on the resolution limit of the light-exposure machine. Thus, the distance between the gate electrode 112 and the source side contact region or the 15 drain side contact region can be reduced to 0.05  $\mu\text{m}$  to 0.1  $\mu\text{m}$ , for example. By reducing the distance between the gate electrode 112 and the source side contact region or the drain side contact region, the resistance between the source and the drain can be reduced, so that the electrical characteristics of the semiconductor device (e.g., on-state current characteristics of the transistor) can be improved.

15 [0310]

Next, the conductive film 118 is formed over the interlayer insulating film 116 to be embedded in the opening 153a and the opening 153b (see FIG. 21A).

[0311]

20 Next, CMP treatment is performed on the conductive film 118 in order to remove the conductive film 118 provided over the interlayer insulating film 116 (at least a region overlapping with the gate electrode 112); thus, the source electrode 118a and the drain electrode 118b embedded in the opening 153a and the opening 153b, respectively, are formed (see FIG. 21B).

[0312]

25 Note that in this embodiment, contact regions between the source electrode 118a and the second oxide semiconductor film 108 and between the drain electrode 118b and the second oxide semiconductor film 108 are side surfaces of the second oxide

semiconductor film 108 in the openings penetrating through the interlayer insulating film 116, the protective insulating film 114, the gate insulating film 110, and the second oxide semiconductor film 108.

[0313]

5 After that, a conductive film is formed over the interlayer insulating film 116, the source electrode 118a, and the drain electrode 118b, and then, through a photolithography step, a resist mask is formed over the conductive film, and a wiring 119a which is electrically connected to the source electrode 118a and a wiring 119b which is electrically connected the drain electrode 118b are formed (see FIG. 21C).

10 [0314]

Through the above manufacturing steps, the semiconductor device illustrated in FIGS. 18A to 18C can be manufactured.

[0315]

15 As described in this embodiment, a technical idea of the present invention is as follows. By forming the first oxide semiconductor film over the oxide film and the second oxide semiconductor film to be stacked over the first oxide semiconductor film, at least during the deposition of the second oxide semiconductor film, oxygen release from the oxide film can be suppressed. Further, since the first oxide semiconductor film serves as a base film for the second oxide semiconductor film, the second oxide 20 semiconductor film can have higher crystallinity. The high crystallinity of the second oxide semiconductor film can suppress the generation of oxygen deficiency in the second oxide semiconductor film, and a transistor with stable electrical characteristics can be provided.

[0316]

25 The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

[0317]

(Embodiment 6)

30 In this embodiment, an example of a structure which includes a semiconductor device described in this specification, which can hold stored data even when not powered, and which has an unlimited number of write cycles will be described with reference to drawings.

[0318]

FIGS. 22A to 22C illustrate an example of a structure of the semiconductor device. FIGS. 22A to 22C illustrate a cross-sectional view, a plan view, and a circuit diagram, respectively, of the semiconductor device. Here, FIG. 22A corresponds to a cross section along line C1-C2 and line D1-D2 in FIG. 22B.

[0319]

The semiconductor device illustrated in FIGS. 22A and 22B includes a transistor 260 including a first semiconductor material in a lower portion, and a transistor 300 including a second semiconductor material in an upper portion. As the transistor 300 including the second semiconductor material, any of the structures of the semiconductor devices described in Embodiment 3 can be employed. Although not described in this embodiment, any of the structures of the semiconductor devices described in Embodiment 1, Embodiment 2, Embodiment 4, and Embodiment 5 can also be employed.

15 [0320]

Here, the first semiconductor material and the second semiconductor material are preferably materials having different band gaps. For example, the first semiconductor material can be a semiconductor material other than an oxide semiconductor (e.g., crystalline silicon) and the second semiconductor material can be an oxide semiconductor. A transistor including a material other than an oxide semiconductor, such as crystalline silicon, can operate at high speed easily. On the other hand, a transistor including an oxide semiconductor can hold charge for a long time owing to its characteristics.

[0321]

25 Although all the transistors are n-channel transistors here, it is needless to say that p-channel transistors can be used.

[0322]

The transistor 260 illustrated in FIG. 22A includes a channel formation region 216 provided in a substrate 200 including a semiconductor material (e.g., crystalline silicon), impurity regions 220 with the channel formation region 216 provided therebetween, intermetallic compound regions 224 in contact with the impurity regions 220, a gate insulating film 208 provided over the channel formation region 216, and a

gate electrode 210 provided over the gate insulating film 208. Note that a transistor whose source electrode and drain electrode are not illustrated in a drawing may be referred to as a transistor for the sake of convenience. Further, in such a case, in description of a connection of a transistor, a source region and a source electrode are 5 collectively referred to as a "source electrode", and a drain region and a drain electrode are collectively referred to as a "drain electrode". That is, in this specification, the term "source electrode" may include a source region.

[0323]

10 An element isolation insulating film 206 is provided over the substrate 200 so as to surround the transistor 260, and an insulating film 228 and an oxide film 230 are provided to cover the transistor 260. Note that for high integration, it is preferable that, as illustrated in FIG. 22A, the transistor 260 does not have a sidewall insulating film. On the other hand, when the characteristics of the transistor 260 have priority, the sidewall insulating film may be formed along a side surface of the gate electrode 210 15 and the impurity regions 220 may include a region having different impurity concentrations.

[0324]

20 The transistor 260 formed using a crystalline semiconductor substrate can operate at high speed. Thus, when the transistor is used as a reading transistor, data can be read at a high speed. An insulating film and an oxide film are formed so as to cover the transistor 260. As treatment prior to formation of the transistor 300 and a capacitor 264, CMP treatment is performed on the insulating film and the oxide film, whereby the insulating film 228 and the oxide film 230 which are planarized are formed and, at the same time, an upper surface of the gate electrode 210 is exposed.

25 [0325]

As the insulating film 228, an inorganic insulating film such as a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, a silicon nitride film, an aluminum nitride film, a silicon nitride oxide film, or an aluminum nitride oxide film can be used typically. As the oxide film 230, an oxide 30 film such as a silicon oxide film, a silicon oxynitride film, or a silicon nitride oxide film can be used. The insulating film 228 and the oxide film 230 can be formed by a plasma CVD method, a sputtering method, or the like.

[0326]

Alternatively, an organic material such as a polyimide-based resin, an acrylic-based resin, or a benzocyclobutene-based resin can be used for the insulating film 228. Other than such organic materials, it is also possible to use a low-dielectric constant material (a low-k material) or the like. In the case of using an organic material, the insulating film 228 may be formed by a wet method such as a spin coating method or a printing method.

[0327]

10 Note that in this embodiment, a silicon nitride film is used as the insulating film 228, and a silicon oxide film is used as the oxide film 230.

[0328]

15 A first oxide semiconductor film 106 and a second oxide semiconductor film 108 are formed over the oxide film 230 which is sufficiently planarized by polishing treatment (such as CMP treatment). Note that the average plane roughness of a surface of the oxide film 230 is preferably less than or equal to 0.15 nm.

[0329]

20 The transistor 300 illustrated in FIG. 22A includes an oxide semiconductor in the channel formation region. Here, the second oxide semiconductor film 108 included in the transistor 300 is preferably highly purified. By using a highly purified oxide semiconductor, the transistor 300 which has extremely favorable off-state current characteristics can be obtained.

[0330]

25 Since the off-state current of the transistor 300 is small, stored data can be held for a long time by using this transistor. In other words, power consumption can be sufficiently reduced because a semiconductor memory device in which refresh operation is unnecessary or the frequency of refresh operation is extremely low can be provided.

[0331]

30 An insulating film 302 and an insulating film 304 each having a single-layer structure or a stacked-layer structure are provided over the transistor 300. In this embodiment, a stack in which a silicon oxide film and an aluminum oxide film are stacked from the transistor 300 side is used as the insulating film 302 and the insulating film 304. Note that when the aluminum oxide film has high density (e.g., a film

density higher than or equal to 3.2 g/cm<sup>3</sup>, preferably higher than or equal to 3.6 g/cm<sup>3</sup>), the transistor 300 can have stable electrical characteristics.

[0332]

In addition, a conductive film 306 is provided in a region overlapping with a 5 wiring 119a which is connected to a source electrode 118a of the transistor 300 with the insulating film 302 provided therebetween, and the wiring 119a, the insulating film 302, and the conductive film 306 form a capacitor 364. That is, the source electrode 118a of the transistor 300 functions as one electrode of the capacitor 364, and the conductive film 306 functions as the other electrode of the capacitor 364. Note that in the case 10 where a capacitor is not needed, the capacitor 364 may be omitted. Alternatively, the capacitor 364 may be separately provided above the transistor 300.

[0333]

The insulating film 304 is provided over the transistor 300 and the capacitor 364. Further, a wiring 308 for connecting the transistor 300 to another transistor is 15 provided over the insulating layer 304. The wiring 308 is formed to be embedded in an opening formed in the insulating film 302, the insulating film 304, and the like, and to be electrically connected to a drain electrode 118b.

[0334]

In FIGS. 22A and 22B, the transistor 260 and the transistor 300 are provided so 20 as to at least partly overlap with each other. The source region or the drain region of the transistor 260 is preferably provided so as to overlap with part of the second oxide semiconductor film 108. Further, the transistor 300 and the capacitor 364 are provided so as to overlap with at least part of the transistor 260. For example, the conductive film 306 of the capacitor 364 is provided so as to overlap with at least part of the gate 25 electrode 210 of the transistor 260. With such a planar layout, the area occupied by the semiconductor device can be reduced; thus, higher integration can be achieved.

[0335]

Next, an example of a circuit configuration corresponding to FIGS. 22A and 22B is illustrated in FIG. 22C.

30 [0336]

In FIG. 22C, a first wiring (1st Line) is electrically connected to one of the source electrode and the drain electrode of the transistor 260, and a second wiring (2nd

Line) is electrically connected to the other of the source electrode and the drain electrode of the transistor 260. A third line (3rd line) is electrically connected to one of the source electrode and a drain electrode of the transistor 300, and a fourth line (4th line) is electrically connected to a gate electrode of the transistor 300. The gate electrode of the transistor 260 and the other of the source electrode and the drain electrode of the transistor 300 are electrically connected to one electrode of the capacitor 364. A fifth wiring (5th Line) is electrically connected to the other electrode of the capacitor 364.

[0337]

10 The semiconductor device in FIG. 22C utilizes a characteristic in which the potential of the gate electrode of the transistor 260 can be held, and can thus write, hold, and read data as follows.

[0338]

15 Writing and holding of data will be described. The potential of the fourth wiring is set to a potential at which the transistor 300 is turned on, whereby the transistor 300 is turned on. Thus, the potential of the third wiring is supplied to the gate electrode of the transistor 260 and the capacitor 365. In other words, a predetermined charge is supplied to the gate electrode of the transistor 260 (i.e., writing of data). Here, charge for supply of a potential level or charge for supply of a different 20 potential level (hereinafter referred to as Low level charge and High level charge) is given. After that, the potential of the fourth wiring is set to a potential at which the transistor 300 is turned off, so that the transistor 300 is turned off. Thus, the charge given to the gate electrode of the transistor 260 is held (holding).

[0339]

25 Since the amount of off-state current of the transistor 300 is significantly small, the charge of the gate electrode of the transistor 260 is held for a long time.

[0340]

30 Next, reading of data is described. By supplying an appropriate potential (reading potential) to the fifth wiring while a predetermined potential (constant potential) is supplied to the first wiring, the potential of the second wiring varies depending on the amount of charge retained in the gate electrode of the transistor 260. This is because in general, when the transistor 260 is an n-channel transistor, an

apparent threshold voltage  $V_{th\_H}$  in the case where High level charge is given to the gate electrode of the transistor 260 is lower than an apparent threshold voltage  $V_{th\_L}$  in the case where Low level charge is given to the gate electrode of the transistor 260. Here, an apparent threshold voltage refers to the potential of the fifth wiring, which is needed 5 to turn on the transistor 260. Thus, the potential of the fifth wiring is set to a potential  $V_0$  existing between  $V_{th\_H}$  and  $V_{th\_L}$ , whereby charge given to the gate electrode of the transistor 260 can be determined. For example, in the case where High level charge is given in writing, when the potential of the fifth wiring is set to  $V_0$  ( $> V_{th\_H}$ ), the transistor 260 is turned on. In the case where Low level charge is given in writing, 10 even when the potential of the fifth wiring is set to  $V_0$  ( $< V_{th\_L}$ ), the transistor 260 remains in an off state. Therefore, the stored data can be read by the potential of the second line.

15 [0341]

Note that in the case where memory cells are arrayed to be used, only data of 20 desired memory cells needs to be read. In the case where data is not read, a potential at which the transistor 260 is turned off regardless of the state of the gate electrode, that is, a potential lower than  $V_{th\_H}$  may be supplied to the fifth wiring. Alternatively, a potential at which the transistor 260 is turned on, that is, a potential higher than  $V_{th\_L}$  may be supplied to the fifth wiring regardless of the state of the gate electrode.

[0342]

When a transistor having a channel formation region formed using an oxide semiconductor and having extremely small off-state current is used in the semiconductor device in this embodiment, the semiconductor device can store data for an extremely long time. In other words, power consumption can be adequately 25 reduced because refresh operation becomes unnecessary or the frequency of refresh operation can be extremely low. Moreover, stored data can be held for a long time even when power is not supplied (note that a potential is preferably fixed).

[0343]

Further, in the semiconductor device in this embodiment, a high voltage is not 30 needed for writing data and there is no problem of deterioration of elements. For example, unlike in a conventional non-volatile memory, it is not necessary to inject and

extract electrons into and from a floating gate, and thus a problem such as deterioration of a gate insulating layer does not occur at all. In other words, the semiconductor device according to one embodiment of the present invention does not have a limit on the number of times of writing, which is a problem in a conventional nonvolatile 5 memory, and reliability thereof is drastically improved. Furthermore, data is written depending on the on state and the off state of the transistor, whereby high-speed operation can be easily achieved.

[0344]

The transistor 300 includes the first oxide semiconductor film 106 formed over 10 the oxide film 230; the second oxide semiconductor film 108 formed over the first oxide semiconductor film 106; a gate insulating film 110 formed over the second oxide semiconductor film 108; and a gate electrode 112 which is in contact with the gate insulating film 110 and formed in a region overlapping with the second oxide semiconductor film 108.

15 [0345]

The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are each formed using an oxide film containing at least indium, gallium, and zinc, and the content percentage of gallium in the first oxide semiconductor film 106 is higher than in the second oxide semiconductor film 108.

20 [0346]

Further, in the first oxide semiconductor film 106, the content percentage of gallium is higher than or equal to that of indium. Furthermore, in the second oxide semiconductor film 108, the content percentage of indium is higher than that of gallium. The high content percentage of indium in the second oxide semiconductor film 108 can 25 lead to higher crystallinity of the second oxide semiconductor film 108.

[0347]

The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are stacked and have different compositions as described above. Further, the first oxide semiconductor film 106 can suppress oxygen release from the oxide film 104 30 at the time of the formation of the second oxide semiconductor film 108.

[0348]

Further, the second oxide semiconductor film 108 is formed over the first oxide

semiconductor film 106 which is formed using the same kinds of materials as the second oxide semiconductor film 108, whereby the second oxide semiconductor film 108 can have a crystal portion that grows from the interface with the first oxide semiconductor film 106.

5 [0349]

That is, the first oxide semiconductor film 106 suppresses oxygen release from the oxide film 104 at least at the time of the deposition of the second oxide semiconductor film 108, and also serves as a base film for the second oxide semiconductor film 108, resulting in higher crystallinity of the second oxide 10 semiconductor film 108. After the second oxide semiconductor film 108 is formed, oxygen is released from the oxide film 104 by heat treatment or the like, and then the oxygen can pass through the first oxide semiconductor film 106 to be supplied to the second oxide semiconductor film 108.

[0350]

15 A structure in which the first oxide semiconductor film 106 and the second oxide semiconductor film 108 are thus stacked has an excellent effect of suppressing the generation of oxygen deficiency in the second oxide semiconductor film 108 and of facilitating the crystallinity of the second oxide semiconductor film 108.

[0351]

20 As described in this embodiment, a technical idea of the present invention is as follows. By forming the first oxide semiconductor film over the oxide film and the second oxide semiconductor film to be stacked over the first oxide semiconductor film, at least during the deposition of the second oxide semiconductor film, oxygen release from the oxide film can be suppressed. Further, since the first oxide semiconductor 25 film serves as a base film for the second oxide semiconductor film, the second oxide semiconductor film can have higher crystallinity. The high crystallinity of the second oxide semiconductor film can suppress the generation of oxygen deficiency in the second oxide semiconductor film, and a transistor with stable electrical characteristics can be provided.

30 [0352]

The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

[0353]

(Embodiment 7)

In this embodiment, a structure which includes the semiconductor device described in any of Embodiments 1 to 5, which can hold stored data even when not 5 powered, and which does not have a limitation on the number of write cycles, and which has a structure different from the structure described in Embodiment 6 will be described with reference to FIGS. 23A and 23B and FIGS. 24A and 24B.

[0354]

10 FIG. 23A illustrates an example of a circuit configuration of a semiconductor device, and FIG. 23B is a conceptual diagram illustrating an example of a semiconductor device. First, the semiconductor device illustrated in FIG. 23A will be described, and then, the semiconductor device illustrated in FIG. 23B will be described.

[0355]

15 In the semiconductor device illustrated in FIG. 23A, a bit line BL is electrically connected to a source electrode or a drain electrode of a transistor 300, a word line WL is electrically connected to a gate electrode of the transistor 300, and the source electrode or the drain electrode of the transistor 300 is electrically connected to a first terminal of a capacitor 354.

[0356]

20 The transistor 300 including an oxide semiconductor has extremely small off-state current. For that reason, the potential of the first terminal of the capacitor 354 (or a charge accumulated in the capacitor 354) can be held for an extremely long time by turning off the transistor 300.

[0357]

25 Next, writing and holding of data in the semiconductor device (a memory cell 350) illustrated in FIG. 23A will be described.

[0358]

30 First, the potential of the word line WL is set to a potential at which the transistor 300 is turned on, so that the transistor 300 is turned on. Accordingly, the potential of the bit line BL is supplied to the first terminal of the capacitor 354 (writing). After that, the potential of the word line WL is set to a potential at which the transistor 300 is turned off, so that the transistor 300 is turned off. Thus, the potential of the first

terminal of the capacitor 354 is held (holding).

[0359]

Because the off-state current of the transistor 300 is extremely small, the potential of the first terminal of the capacitor 354 (or the charge accumulated in the capacitor) can be held for a long time.

[0360]

Secondly, reading of data will be described. When the transistor 300 is turned on, the bit line BL which is in a floating state and the capacitor 354 are electrically connected to each other, and the charge is redistributed between the bit line BL and the capacitor 354. As a result, the potential of the bit line BL is changed. The amount of change in potential of the bit line BL fluctuates depending on the potential of the first terminal of the capacitor 354 (or the charge accumulated in the capacitor 354).

[0361]

For example, the potential of the bit line BL after charge redistribution is  $(C_B \times V_{B0} + C \times V) / (C_B + C)$ , where  $V$  is the potential of the first terminal of the capacitor 354,  $C$  is the capacitance of the capacitor 354,  $C_B$  is the capacitance of the bit line BL (hereinafter also referred to as bit line capacitance), and  $V_{B0}$  is the potential of the bit line BL before the charge redistribution. Therefore, it can be found that assuming that the memory cell 350 is in either of two states in which the potentials of the first terminal of the capacitor 354 are  $V_1$  and  $V_0$  ( $V_1 > V_0$ ), the potential of the bit line BL in the case of holding the potential  $V_1$  ( $= (C_B \times V_{B0} + C \times V_1) / (C_B + C)$ ) is higher than the potential of the bit line BL in the case of holding the potential  $V_0$  ( $= (C_B \times V_0 + C \times V_0) / (C_B + C)$ ).

[0362]

By comparing the potential of the bit line BL with a predetermined potential, data can be read.

[0363]

As described above, the semiconductor device illustrated in FIG. 23A can hold charge that is accumulated in the capacitor 354 for a long time because the off-state current of the transistor 300 is extremely small. In other words, power consumption can be adequately reduced because refresh operation becomes unnecessary or the

frequency of refresh operation can be extremely low. Moreover, stored data can be stored for a long time even when power is not supplied.

[0364]

Next, the semiconductor device illustrated in FIG. 23B will be described.

5 [0365]

The semiconductor device illustrated in FIG. 23B includes memory cell arrays 351a and 351b including a plurality of memory cells 350 illustrated in FIG. 23A as a memory circuit in an upper portion, and a peripheral circuit 353 in a lower portion which is necessary for operation of the memory cell arrays 351a and 351b. Note that 10 the peripheral circuit 353 is electrically connected to the memory cell arrays 351a and 351b.

[0366]

In the structure illustrated in FIG. 23B, the peripheral circuit 353 can be provided under the memory cell arrays 351a and 351b. Thus, the size of the 15 semiconductor device can be decreased.

[0367]

It is preferable that a semiconductor material of the transistor provided in the peripheral circuit 353 be different from that of the transistor 300. For example, silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, or the like can be 20 used, and a single crystal semiconductor is preferably used. Alternatively, an organic semiconductor material or the like may be used. A transistor including such a semiconductor material can operate at sufficiently high speed. Therefore, a variety of circuits (e.g., a logic circuit or a driver circuit) which needs to operate at high speed can be favorably achieved by the transistor.

25 [0368]

Note that FIG. 23B illustrates, as an example, the semiconductor device in which two memory cell arrays of the memory cell arrays 351a and 351b are stacked; however, the number of memory cells to be stacked is not limited thereto. Three or more memory cell arrays may be stacked.

30 [0369]

Next, a specific structure of the memory cell 350 illustrated in FIG. 23A will be described with reference to FIGS. 24A and 24B.

[0370]

FIGS. 24A and 24B illustrate an example of a structure of the memory cell 350. FIG. 24A is a cross-sectional view of the memory cell 350, and FIG. 24B is a plan view of the memory cell 350. Here, FIG. 24A illustrates cross sections taken along chain line F1-F2 and chain line G1-G2 in FIG. 24B.

[0371]

The transistor 300 illustrated in FIGS. 24A and 24B can have the same structure as the transistor in Embodiment 3 or Embodiment 6. Note that any of the structures of the transistors described in the other Embodiments may be employed.

10 [0372]

The transistor 300 includes a first oxide semiconductor film 106 formed over an oxide film 274; a second oxide semiconductor film 108 formed over the first oxide semiconductor film 106; a gate insulating film 110 formed over the second oxide semiconductor film 108; and a gate electrode 112 which is in contact with the gate insulating film 110 and formed in a region overlapping with the second oxide semiconductor film 108.

15 [0373]

The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are each formed using an oxide film containing at least indium, gallium, and zinc, and the content percentage of gallium in the first oxide semiconductor film 106 is higher than in the second oxide semiconductor film 108.

20 [0374]

Further, in the first oxide semiconductor film 106, the content percentage of gallium is higher than or equal to that of indium. Furthermore, in the second oxide semiconductor film 108, the content percentage of indium is higher than that of gallium. The high content percentage of indium in the second oxide semiconductor film 108 can lead to higher crystallinity of the second oxide semiconductor film 108.

25 [0375]

The first oxide semiconductor film 106 and the second oxide semiconductor film 108 are stacked and have different compositions as described above. Further, the first oxide semiconductor film 106 can suppress oxygen release from the oxide film 104 at the time of the formation of the second oxide semiconductor film 108.

[0376]

Further, the second oxide semiconductor film 108 is formed over the first oxide semiconductor film 106 which is formed using the same kinds of materials as the second oxide semiconductor film 108, whereby the second oxide semiconductor film 108 can have a crystal portion that grows from the interface with the first oxide semiconductor film 106.

[0377]

That is, the first oxide semiconductor film 106 suppresses oxygen release from the oxide film 104 at least at the time of the deposition of the second oxide semiconductor film 108, and also serves as a base film for the second oxide semiconductor film 108, resulting in higher crystallinity of the second oxide semiconductor film 108. After the second oxide semiconductor film 108 is formed, oxygen is released from the oxide film 104 by heat treatment or the like, and then the oxygen can pass through the first oxide semiconductor film 106 to be supplied to the second oxide semiconductor film 108.

[0378]

A structure in which the first oxide semiconductor film 106 and the second oxide semiconductor film 108 are thus stacked has an excellent effect of suppressing the generation of oxygen deficiency in the second oxide semiconductor film 108 and of facilitating the crystallinity of the second oxide semiconductor film 108.

[0379]

Note that in the first oxide semiconductor film 106, high-resistance regions 106a are formed in a region overlapping with the gate electrode 112 and regions outside the second oxide semiconductor film 108, and a pair of low-resistance regions 106b is formed adjacent to the region overlapping with the gate electrode 112. Further, in the second oxide semiconductor film 108, a channel region 108a is formed in a region overlapping with the gate electrode 112, and a pair of low-resistance regions 108b is formed adjacent to the region overlapping with the gate electrode 112.

[0380]

The high-resistance region 106a formed outside the second oxide semiconductor film 108 serves as a separation layer between transistors. This is to prevent electrical connection between adjacent transistors, for example, which would

occur in the case where the high-resistance region 106a is not provided outside the second oxide semiconductor film 108.

[0381]

The semiconductor device may also include an insulating film 113 formed in a 5 region overlapping with the gate electrode 112; sidewall insulating films 115 which are formed along side surfaces of the gate electrode 112 and the insulating film 113; a source electrode 118a and a drain electrode 118b which are electrically connected to the second oxide semiconductor film 108; an insulating film 120 formed over an interlayer insulating film 116; and a wiring 119a and a wiring 119b which are electrically 10 connected to the source electrode 118a and the drain electrode 118b, respectively, through openings formed in the insulating film 120, the interlayer insulating film 116, and a protective insulating film 114. Note that since the source electrode 118a and the drain electrode 118b are in contact with the pair of low-resistance regions 108b formed in the second oxide semiconductor film 108, the contact resistance can be low.

15 [0382]

In addition, an insulating film 258 is formed over the transistor 300, and a conductive film 262 is provided in a region overlapping with a wiring 119a which is connected to a source electrode 118a of the transistor 300 with the insulating film 258 provided therebetween, and the wiring 119a, the insulating film 258, and the conductive 20 film 262 form the capacitor 354. That is, the source electrode 118a of the transistor 300 functions as one electrode of the capacitor 354, and the conductive film 262 functions as the other electrode of the capacitor 354.

[0383]

An insulating film 256 having a single-layer structure or a stacked-layer 25 structure is provided over the transistor 300 and the capacitor 354. In addition, a wiring 272 for connecting the memory cell to an adjacent memory cell is provided over the insulating film 256. The wiring 272 is electrically connected to the drain electrode 118b of the transistor 300 through an opening which is provided in the insulating film 256, the insulating film 258, and the like and the wiring 119b. Note that the wiring 30 272 and the drain electrode 118b may be directly connected to each other. The wiring 272 corresponds to the bit line BL in the circuit configuration of FIG. 23A.

[0384]

In FIGS. 24A and 24B, the drain electrode 118b of the transistor 300 can also function as a source electrode of a transistor included in the adjacent memory cell.

[0385]

In this manner, when the planar layout in FIG. 24B is employed, the area 5 occupied by the semiconductor device can be reduced; thus, the degree of integration can be increased.

[0386]

As described above, the plurality of memory cells formed in multiple layers 10 each include a transistor including an oxide semiconductor. Since the off-state current of the transistor including an oxide semiconductor is small, stored data can be held for a long time by using this transistor. In other words, the frequency of refresh operation can be extremely lowered, which leads to a sufficient reduction in power consumption.

[0387]

A semiconductor device having a novel feature can be obtained by being 15 provided with both a peripheral circuit including the transistor including a material other than an oxide semiconductor (in other words, a transistor capable of operating at sufficiently high speed) and a memory circuit including the transistor including an oxide semiconductor (in a broader sense, a transistor whose off-state current is sufficiently small). In addition, with a structure where the peripheral circuit and the memory 20 circuit are stacked, the degree of integration of the semiconductor device can be increased.

[0388]

As described above, a miniaturized and highly integrated semiconductor device 25 having high electric characteristics and a method for manufacturing the semiconductor device can be provided.

[0389]

As described in this embodiment, a technical idea of the present invention is as follows. By forming the first oxide semiconductor film over the oxide film and the 30 second oxide semiconductor film to be stacked over the first oxide semiconductor film, at least during the deposition of the second oxide semiconductor film, oxygen release from the oxide film can be suppressed. Further, since the first oxide semiconductor film serves as a base film for the second oxide semiconductor film, the second oxide

semiconductor film can have higher crystal Unity. The high crystallinity of the second oxide semiconductor film can suppress the generation of oxygen deficiency in the second oxide semiconductor film, and a transistor with stable electrical characteristics can be provided.

5 [0390]

This embodiment can be implemented in appropriate combination with any of the structures described in the other embodiments.

[0391]

(Embodiment 8)

10 In this embodiment, examples of application of the semiconductor device described in any of the above embodiments to portable devices such as a mobile phone, a smartphone, or an e-book reader will be described with reference to FIGS. 25A and 25B, FIG. 26, FIG. 27, and FIG. 28.

[0392]

15 In portable devices such as a mobile phone, a smartphone, and an e-book reader, an SRAM or a DRAM is used to store image data temporarily. This is because response speed of a flash memory is low and thus a flash memory is not suitable for image processing. On the other hand, an SRAM or a DRAM has the following characteristics when used for temporary storage of image data.

20 [0393]

In an ordinary SRAM, as illustrated in FIG. 25A, one memory cell includes six transistors, that is, transistors 801 to 806, which are driven with an X decoder 807 and a Y decoder 808. The transistors 803 and 805 and the transistors 804 and 806 each serve as an inverter, and high-speed driving can be performed therewith. However, an SRAM has a disadvantage of large cell area because one memory cell includes six transistors. Provided that the minimum feature size of a design rule is F, the area of a memory cell in an SRAM is generally  $100 F^2$  to  $150 F^2$ . Therefore, a price per bit of an SRAM is the most expensive among a variety of memory devices.

25 [0394]

30 In contrast, in a DRAM, as illustrated in FIG. 25B, a memory cell includes a transistor 811 and a storage capacitor 812, which are driven with an X decoder 813 and a Y decoder 814. One cell includes one transistor and one capacitor and thus the area

of a memory cell is small. The area of a memory cell of a DRAM is generally less than or equal to  $10 \text{ F}^2$ . Note that in the case of a DRAM, a refresh operation is always necessary and power is consumed even when a rewriting operation is not performed.

[0395]

5 However, the area of the memory cell of the semiconductor device described in any of the above embodiments is about  $10 \text{ F}^2$  and frequent refreshing is not needed. Therefore, the area of the memory cell is reduced, and the power consumption can be reduced.

[0396]

10 Next, FIG. 26 illustrates a block diagram of a portable device. A portable device shown in FIG. 26 includes an RF circuit 901, an analog baseband circuit 902, a digital baseband circuit 903, a battery 904, a power supply circuit 905, an application processor 906, a flash memory 910, a display controller 911, a memory circuit 912, a display 913, a touch sensor 919, an audio circuit 917, a keyboard 918, and the like.  
15 The display 913 includes a display portion 914, a source driver 915, and a gate driver 916. The application processor 906 includes a CPU 907, a DSP 908, and an IF 909. In general, the memory circuit 912 includes an SRAM or a DRAM; by employing the semiconductor device described in any of the above embodiments for the memory circuit 912, writing and reading of data can be performed at high speed, data can be held  
20 for a long time, and power consumption can be sufficiently reduced.

[0397]

Next, FIG. 27 illustrates an example in which the semiconductor device described in any of the above embodiments is used for a memory circuit 950 in a display. The memory circuit 950 illustrated in FIG. 27 includes a memory 952, a memory 953, a  
25 switch 954, a switch 955, and a memory controller 951. Further, the memory circuit is connected to a display controller 956 which reads and controls image data input through a signal line (input image data) and data stored in the memory 952 and the memory 953 (stored image data), and is also connected to a display 957 which displays an image based on a signal from the display controller 956.

30 [0398]

First, image data (input image data A) is formed by an application processor (not shown). The input image data A is stored in the memory 952 through the switch

954. The image data (stored image data A) stored in the memory 952 is transmitted and displayed to the display 957 through the switch 955 and the display controller 956. [0399]

5 In the case where the input image data A is not changed, the stored image data A is read from the memory 952 through the switch 955 by the display controller 956 normally at a frequency of approximately 30 Hz to 60 Hz.

[0400]

10 Next, for example, when data displayed on the screen is rewritten by a user (that is, in the case where the input image data A is changed), new image data (input image data B) is formed by the application processor. The input image data B is held in the memory 953 through the switch 954. The stored image data A is read periodically from the memory 952 through the switch 955 even during that time. After the completion of storing the new image data (the stored image data B) in the memory 953, from the next frame for the display 957, the stored image data B starts to be read, 15 transmitted to the display 957 through the switch 955 and the display controller 956, and displayed on the display 957. This reading operation is continued until another new image data is stored in the memory 952.

[0401]

20 Accordingly, image data is alternately written and read in the memories 952 and 953 so as to be displayed on the display 957. The memories 952 and 953 are not necessarily different memories, and a memory region included in one memory may be divided to be used. By employing the semiconductor device described in any of the above embodiments for the memory 952 and the memory 953, data can be written and read at high speed and held for a long time, and power consumption can be sufficiently 25 reduced.

[0402]

30 Next, FIG. 28 illustrates a block diagram of an e-book reader. FIG. 28 includes a battery 1001, a power supply circuit 1002, a microprocessor 1003, a flash memory 1004, an audio circuit 1005, a keyboard 1006, a memory circuit 1007, a touch panel 1008, a display 1009, and a display controller 1010.

[0403]

Here, the semiconductor device described in any of the above embodiments can

be used for the memory circuit 1007 in FIG. 28. The memory circuit 1007 has a function of temporarily storing the contents of a book. For example, users use a highlight function in some cases. When users read an e-book reader, they sometimes want to mark a specified place. This marking refers to a highlight function, and users 5 can make difference from other places by, for example, changing the color of a letter displayed, underlining a word, making a letter bold, or changing the font type of a letter. That is, there is a function of storing and holding information of a place specified by users. In order to save information for a long time, the information may be copied into 10 the flash memory 1004. Even in such a case, by employing the semiconductor device described in any of the above embodiments, writing and reading of data can be performed at high speed, data can be held for a long time, and power consumption can be sufficiently reduced.

[0404]

As described above, the semiconductor device in any of the above 15 embodiments is mounted on each of the portable devices described in this embodiment. Therefore, it is possible to obtain a portable device which is capable of writing and reading data at high speed, storing data for a long time, and reducing power consumption.

[0405]

20 The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

#### EXPLANATION OF REFERENCE

[0406]

25 102: substrate, 104: oxide film, 106: first oxide semiconductor film, 106a: high-resistance region, 106b: low-resistance region, 108: second oxide semiconductor film, 108a: channel region, 108b: low-resistance region, 110: gate insulating film, 111: conductive film, 112: gate electrode, 113: insulating film, 113a: insulating film, 114: protective insulating film, 114a: insulating film, 115: sidewall insulating film, 115a: insulating film, 116: interlayer insulating film, 116a: insulating film, 118: conductive film, 118a: source electrode, 118b: drain electrode, 119: conductive film, 119a: wiring, 30 119b: wiring, 120: insulating film, 121: conductive film, 121a: first conductive film,

121b: second conductive film, 132: resist mask, 132a: resist mask, 134: resist mask, 134a: resist mask, 134b: resist mask, 136: resist mask, 136a: resist mask, 138: resist mask, 138a: resist mask, 142: dopant, 151a: first opening, 151b: second opening, 153a: opening, 153b: opening, 200: substrate, 206: element isolation insulating film, 208: gate 5 insulating film, 210: gate electrode, 216: channel formation region, 220: impurity region, 224: intermetallic compound region, 228: insulating film, 230: oxide film, 256: insulating film, 258: insulating film, 260: transistor, 262: conductive film, 264: capacitor, 272: wiring, 274: oxide film, 300: transistor, 302: insulating film, 304: insulating film, 306: conductive film, 308: wiring, 350: memory cell, 351a: memory cell 10 array, 351b: memory cell arrays, 353: peripheral circuit, 354: capacitor, 364: capacitor, 801: transistor, 802: transistor, 803: transistor, 804: transistor, 805: transistor, 806: transistor, 807: X decoder, 808: Y decoder, 811: transistor, 812: storage capacitor, 813: 15 X decoder, 814: Y decoder, 901: RF circuit, 902: analog baseband circuit, 903: digital baseband circuit, 904: battery, 905: power supply circuit, 906: application processor, 907: CPU, 908: DSP, 909: IF, 910: flash memory, 911: display controller, 912: memory circuit, 913: display, 914: display portion, 915: source driver, 916: gate driver, 917: audio circuit, 918: keyboard, 919: touch sensor, 950: memory circuit, 951: memory controller, 952: memory, 953: memory, 954: switch, 955: switch, 956: display controller, 957: display, 1001: battery, 1002: power supply circuit, 1003: microprocessor, 1004: 20 flash memory, 1005: audio circuit, 1006: keyboard, 1007: memory circuit, 1008: touch panel, 1009: display, 1010: display controller.

This application is based on Japanese Patent Application serial no. 2011-282509 filed with Japan Patent Office on December 23, in 2011, the entire 25 contents of which are hereby incorporated by reference.

## CLAIMS

1. A semiconductor device comprising:

a first oxide semiconductor film; and

5 a second oxide semiconductor film over the first oxide semiconductor film,

wherein the first oxide semiconductor film and the second oxide semiconductor

film each comprises indium, gallium, and zinc, and

wherein the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor

10 film.

2. The semiconductor device according to claim 1, wherein the first oxide semiconductor film comprises a low-resistance region and a high-resistance region, the high-resistance region being located outside the second oxide semiconductor film.

15

3. The semiconductor device according to claim 1, wherein the second oxide semiconductor film comprises a channel region and a pair of low-resistance regions in contact with the channel region.

20

4. The semiconductor device according to claim 1, wherein either end of the second oxide semiconductor film in a channel width direction comprises a high-resistance region.

25

5. The semiconductor device according to claim 1, wherein a content percentage of gallium is higher than or equal to a content percentage of indium in the first oxide semiconductor film.

30

6. The semiconductor device according to claim 1, wherein a content percentage of indium is higher than a content percentage of gallium in the second oxide semiconductor film.

7. The semiconductor device according to claim 1, wherein the second oxide

semiconductor film comprises a crystal portion having a c-axis aligned in a direction parallel to a normal vector of a surface where the second oxide semiconductor film is formed.

- 5 8. A semiconductor device comprising:  
a first oxide semiconductor film over an oxide film;  
a second oxide semiconductor film over the first oxide semiconductor film;  
a gate insulating film over the second oxide semiconductor film; and  
a gate electrode over the second oxide semiconductor film with the gate  
10 insulating film interposed therebetween,

wherein the first oxide semiconductor film and the second oxide semiconductor film each comprises indium, gallium, and zinc, and

wherein the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor  
15 film.

9. The semiconductor device according to claim 8, further comprising:

a protective insulating film over the gate electrode;  
an interlayer insulating film over the protective insulating film; and

20 a source electrode and a drain electrode which are over the interlayer insulating film and electrically connected to the second oxide semiconductor film.

10. The semiconductor device according to claim 8, further comprising:

a protective insulating film over the gate electrode;  
an interlayer insulating film over the protective insulating film;  
a first opening and a second opening which are provided in the gate insulating film, the protective insulating film, and the interlayer insulating film; and  
a source electrode and a drain electrode which are embedded in the first opening and the second opening and electrically connected to the second oxide  
30 semiconductor film.

11. The semiconductor device according to claim 8, further comprising:

a protective insulating film and an interlayer insulating film which are over the gate electrode;

5 a first opening and a second opening which are formed in the gate insulating film, the protective insulating film, the interlayer insulating film, and the second oxide semiconductor film; and

a source electrode and a drain electrode which are embedded in the first opening and the second opening and electrically connected to the second oxide semiconductor film,

10 wherein the gate electrode covers a top surface and a side surface of the second oxide semiconductor film with the gate insulating film interposed therebetween.

12. The semiconductor device according to claim 9, wherein the source electrode and the drain electrode each have a surface which is planarized by chemical mechanical polishing treatment.

15

13. The semiconductor device according to claim 10, wherein the source electrode and the drain electrode each have a surface which is planarized by chemical mechanical polishing treatment.

20

14. The semiconductor device according to claim 11, wherein the source electrode and the drain electrode each have a surface which is planarized by chemical mechanical polishing treatment.

25

15. The semiconductor device according to claim 8, wherein the first oxide semiconductor film comprises a low-resistance region and a high-resistance region, the high-resistance region being located outside the second oxide semiconductor film.

30

16. The semiconductor device according to claim 8, wherein the second oxide semiconductor film comprises a channel region and a pair of low-resistance regions in contact with the channel region.

17. The semiconductor device according to claim 8, wherein either end of the

second oxide semiconductor film in a channel width direction comprises a high-resistance region.

18. The semiconductor device according to claim 8, wherein a content 5 percentage of gallium is higher than or equal to a content percentage of indium in the first oxide semiconductor film.

19. The semiconductor device according to claim 8, wherein a content 10 percentage of indium is higher than a content percentage of gallium in the second oxide semiconductor film.

20. The semiconductor device according to claim 8, wherein the second oxide 15 semiconductor film comprises a crystal portion having a c-axis aligned in a direction parallel to a normal vector of a surface where the second oxide semiconductor film is formed.

21. The semiconductor device according to claim 9, wherein the protective 20 insulating film is an aluminum oxide film having a film density of higher than or equal to 3.2 g/cm<sup>3</sup>.

22. The semiconductor device according to claim 10, wherein the protective 25 insulating film is an aluminum oxide film having a film density of higher than or equal to 3.2 g/cm<sup>3</sup>.

23. The semiconductor device according to claim 11, wherein the protective 30 insulating film is an aluminum oxide film having a film density of higher than or equal to 3.2 g/cm<sup>3</sup>.

24. A semiconductor device comprising:

30 a first oxide semiconductor film over an oxide film;  
a second oxide semiconductor film over the first oxide semiconductor film;  
a gate insulating film over the second oxide semiconductor film;

a gate electrode over the second oxide semiconductor film with the gate insulating film interposed therebetween;

an insulating film over the gate electrode;

5 a sidewall insulating film along a side surface of the gate electrode and a side surface of the insulating film;

a source electrode and a drain electrode which are on the sidewall insulating film and electrically connected to the second oxide semiconductor film; and

a protective insulating film and an interlayer insulating film which are over the source electrode and the drain electrode,

10 wherein the first oxide semiconductor film and the second oxide semiconductor film each comprises indium, gallium, and zinc, and

wherein the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film.

15

25. A semiconductor device comprising:

a first oxide semiconductor film over an oxide film;

a second oxide semiconductor film over the first oxide semiconductor film;

20 a source electrode and a drain electrode on a top surface of the first oxide semiconductor film;

a gate insulating film over the second oxide semiconductor film; and

a gate electrode over the second oxide semiconductor film with the gate insulating film interposed therebetween,

25 wherein the second oxide semiconductor film is between the source electrode and the drain electrode, and electrically connected to the source electrode and the drain electrode,

wherein the first oxide semiconductor film and the second oxide semiconductor film each comprises indium, gallium, and zinc, and

30 wherein the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film.

26. The semiconductor device according to claim 25, wherein the second oxide semiconductor film is flush with the source electrode and the drain electrode.

27. The semiconductor device according to claim 25, further comprising:  
5 a first conductive film along one side surface of the gate electrode;  
a second conductive film along the other side surface of the gate electrode;  
a sidewall insulating film on the first conductive film and the second conductive film; and

10 a protective insulating film and an interlayer insulating film which are over the gate electrode, the source electrode, and the drain electrode.

28. The semiconductor device according to claim 27,  
wherein the first conductive film is over the source electrode with the gate insulating film interposed therebetween, and

15 wherein the second conductive film is over the drain electrode with the gate insulating film interposed therebetween.

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FIG. 1A

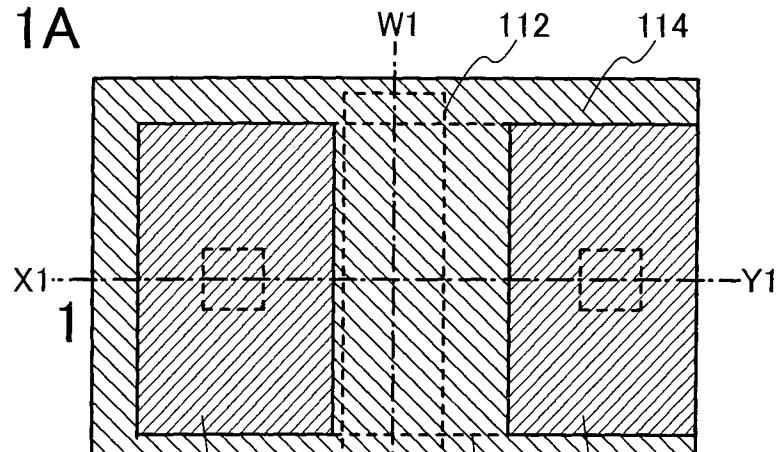


FIG. 1B

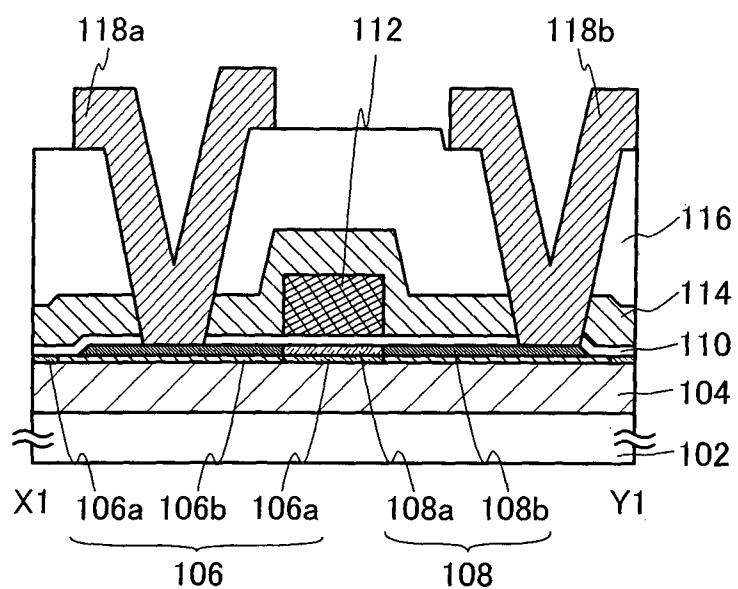
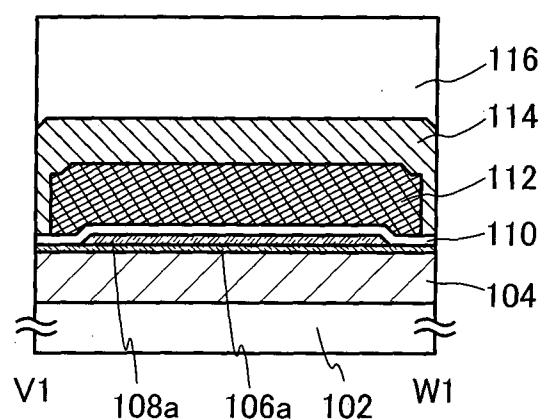


FIG. 1C



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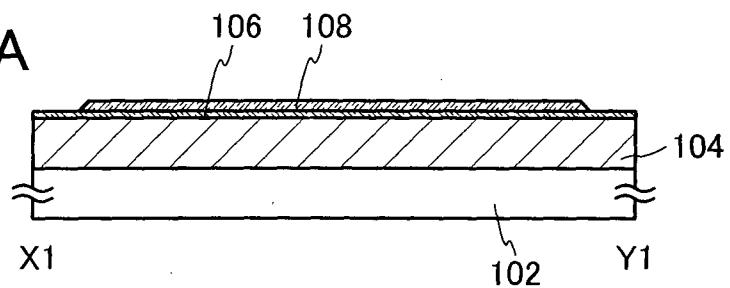
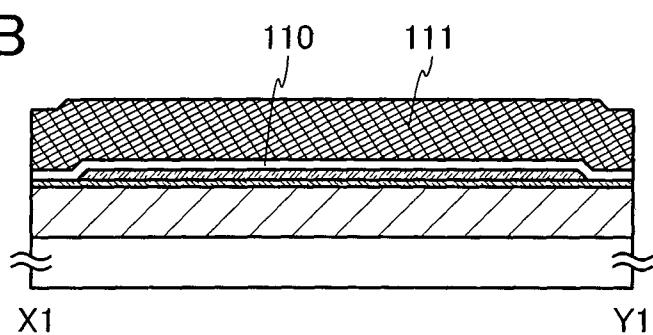
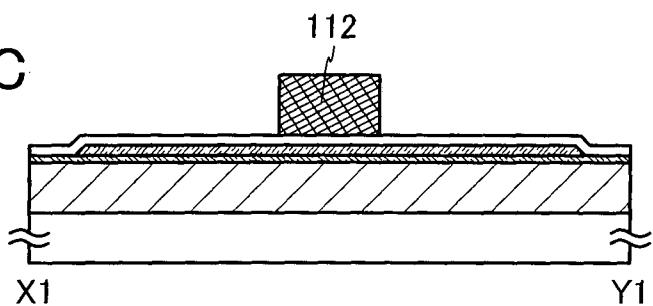
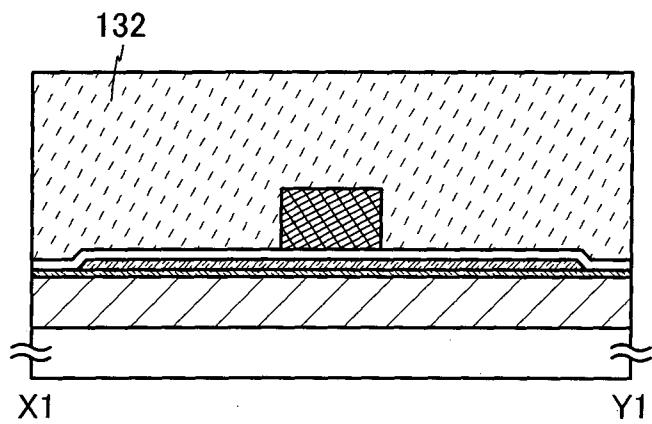
**FIG. 2A****FIG. 2B****FIG. 2C****FIG. 2D**

FIG. 3A

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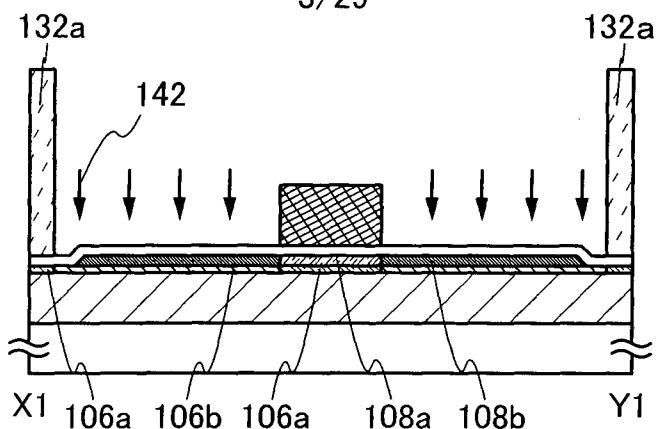


FIG. 3B

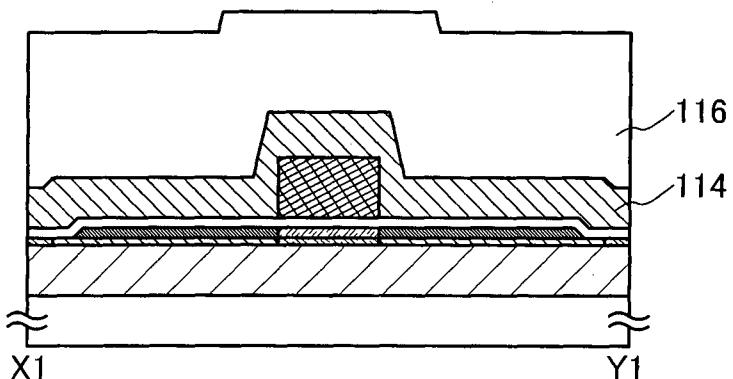


FIG. 3C

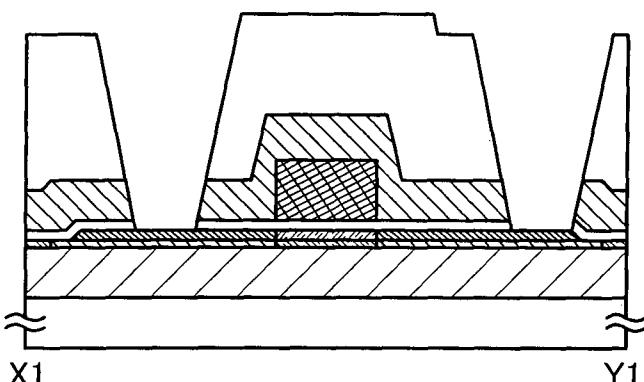


FIG. 3D

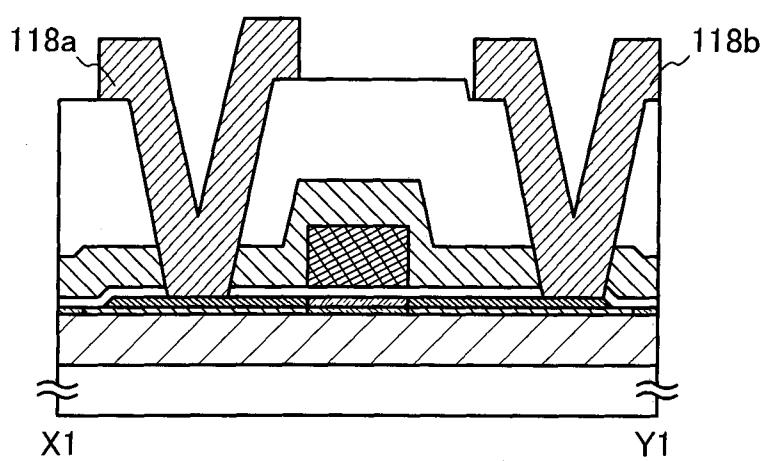


FIG. 4A

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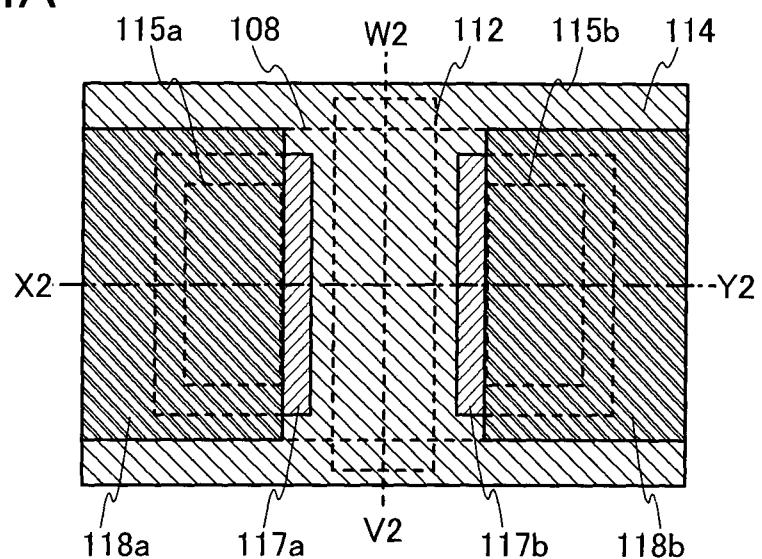


FIG. 4B

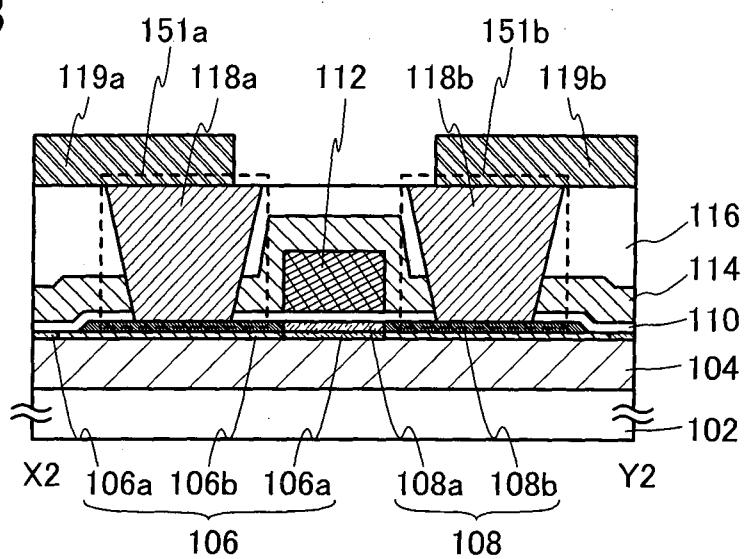


FIG. 4C

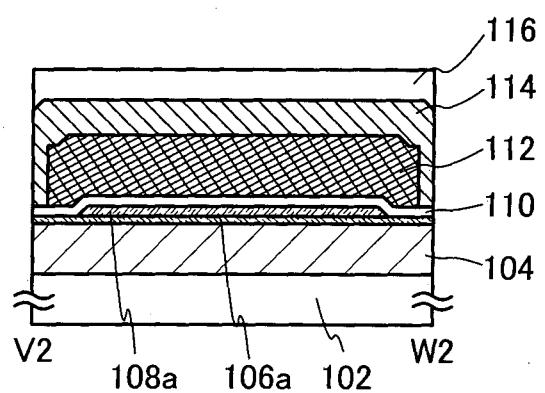


FIG. 5A

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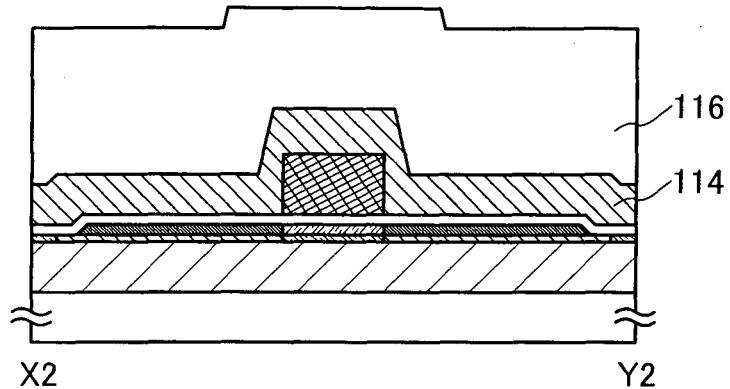


FIG. 5B

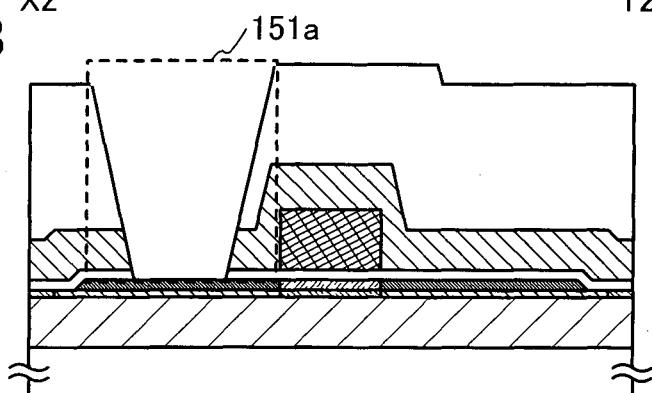


FIG. 5C

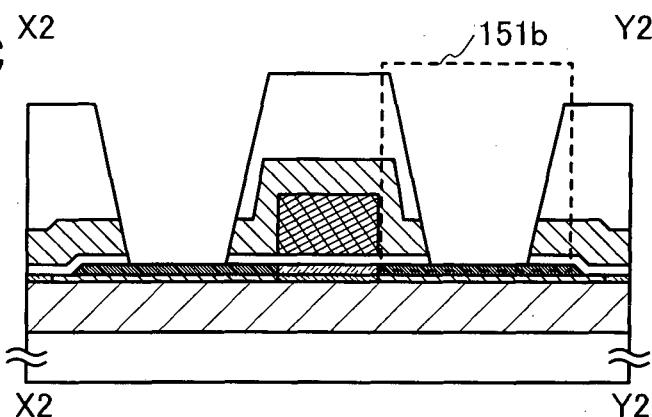
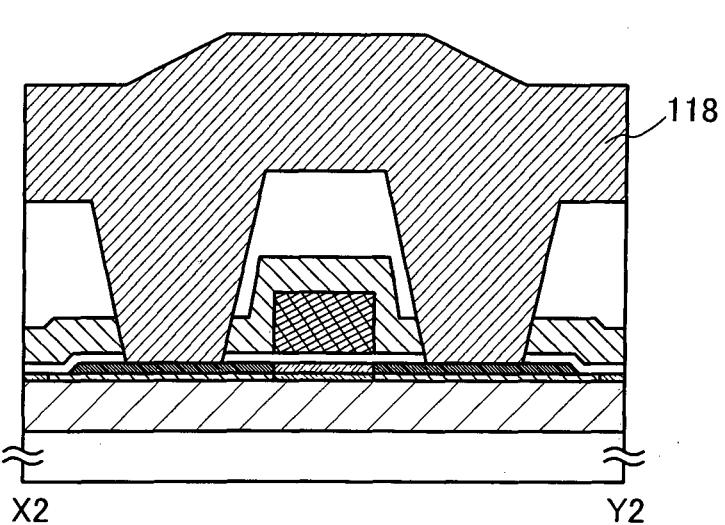
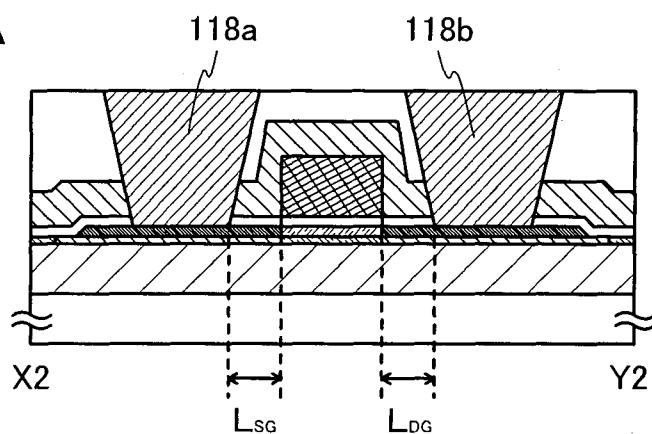
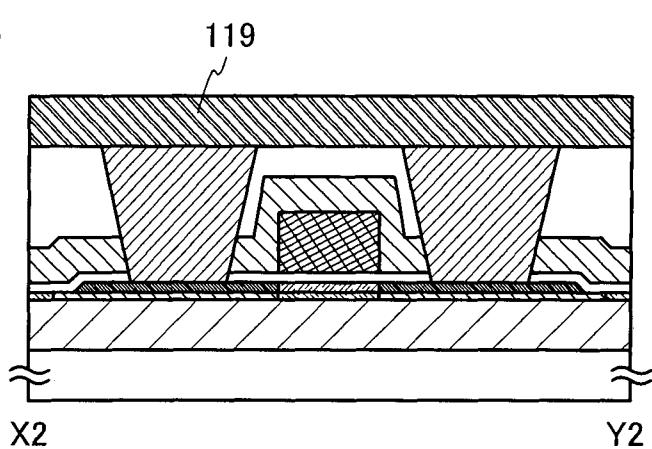
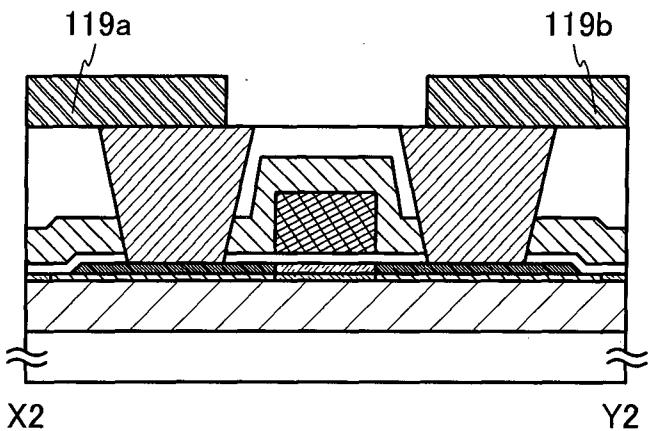


FIG. 5D



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**FIG. 6A****FIG. 6B****FIG. 6C**

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FIG. 7A

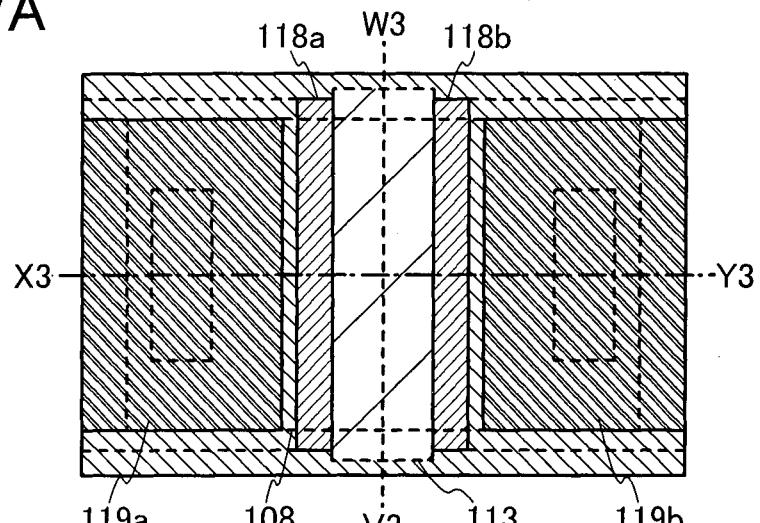


FIG. 7B

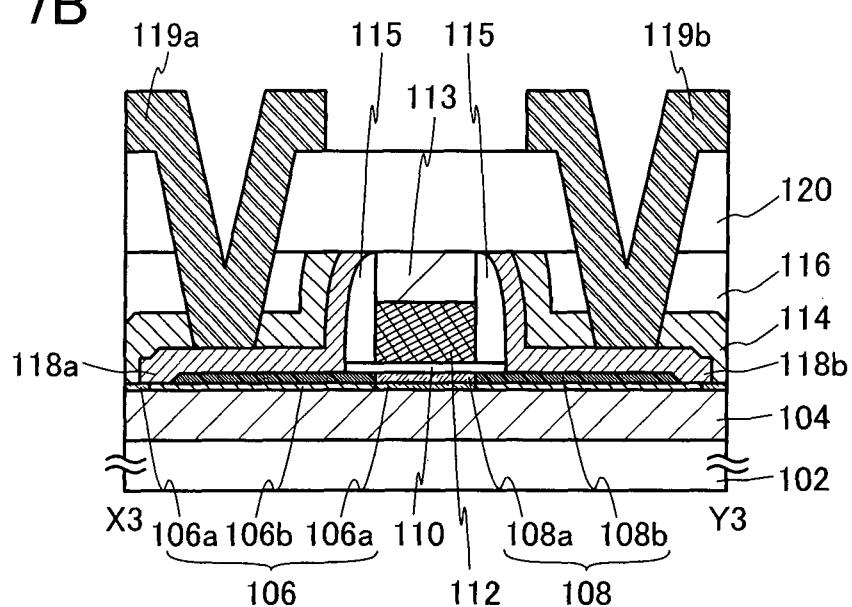
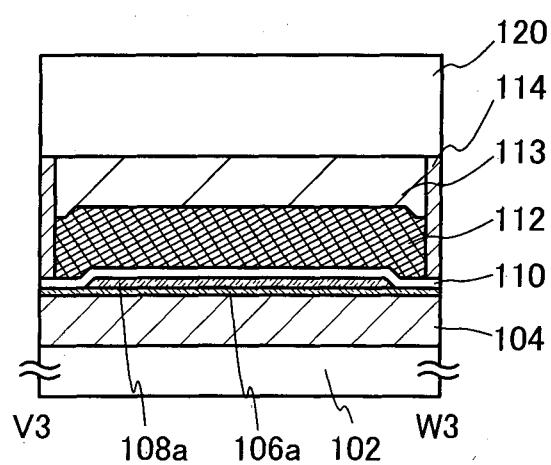


FIG. 7C



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FIG. 8A

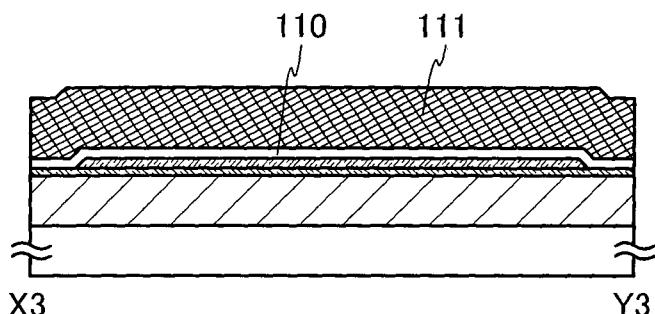


FIG. 8B

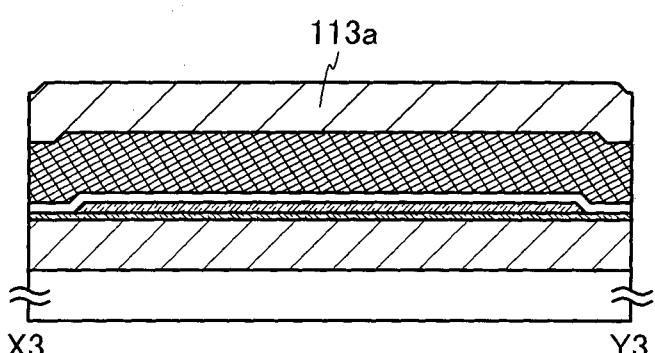


FIG. 8C

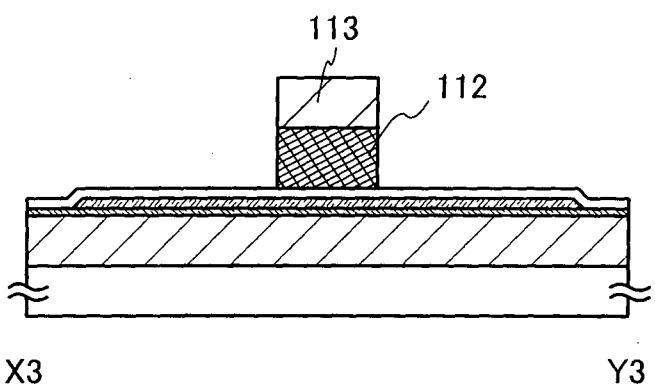
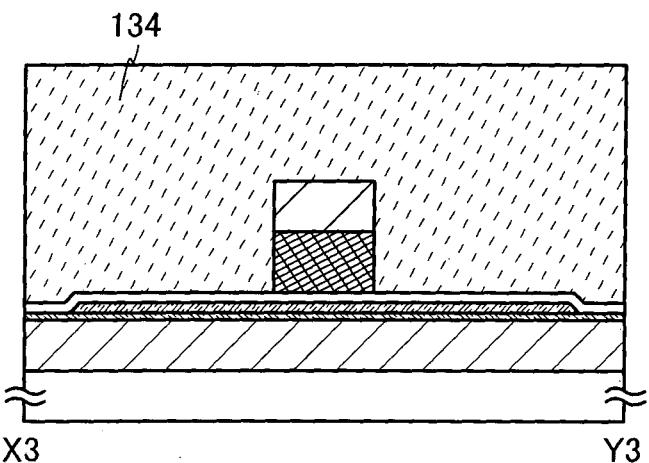


FIG. 8D



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FIG. 9A

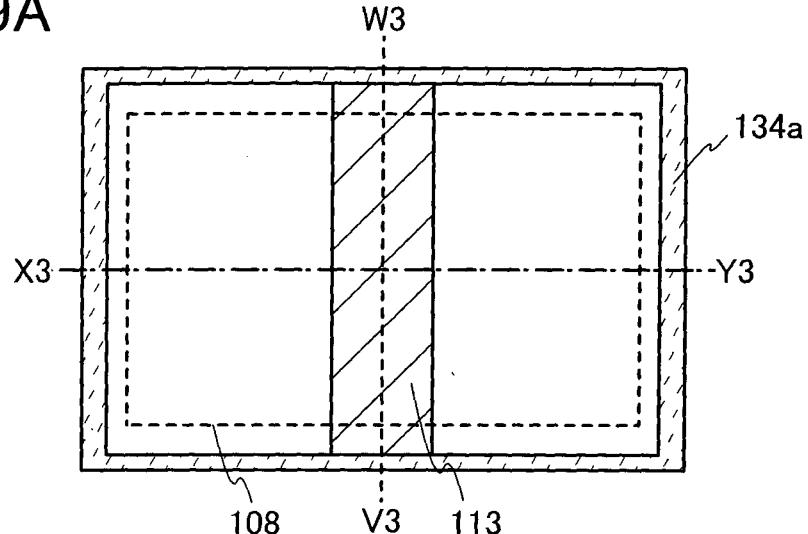


FIG. 9B

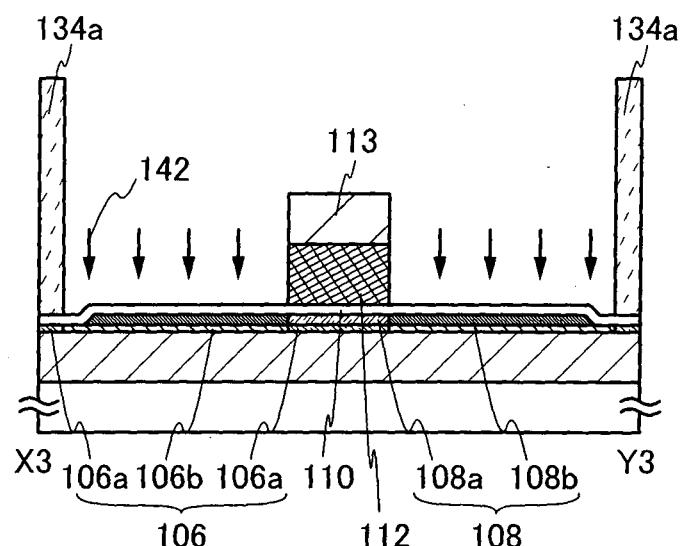
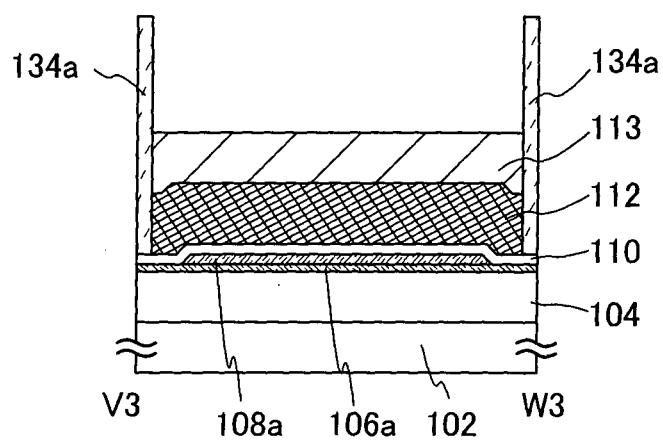


FIG. 9C



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FIG. 10A

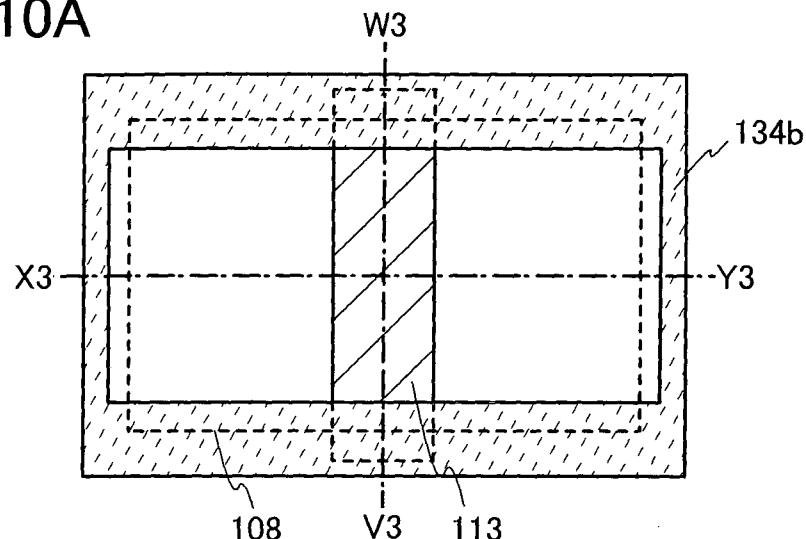


FIG. 10B

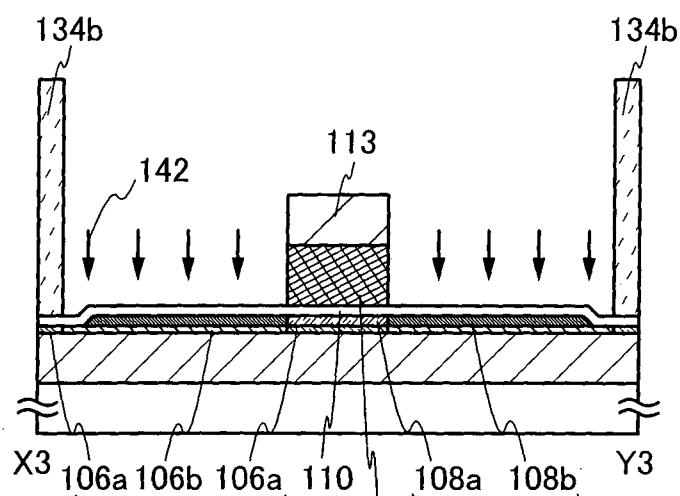
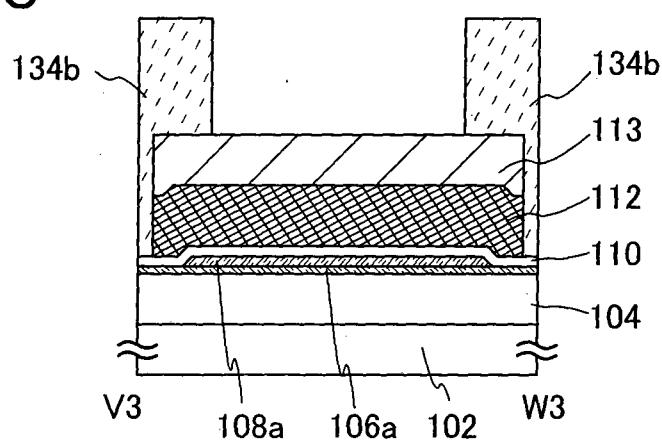


FIG. 10C



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FIG. 11A

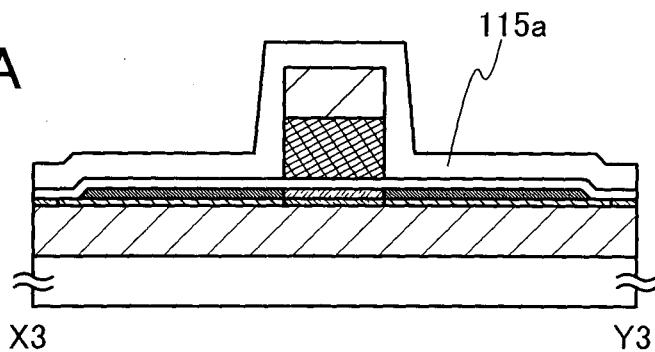


FIG. 11B

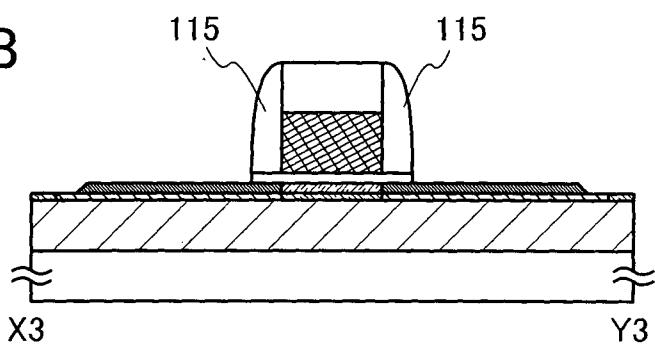


FIG. 11C

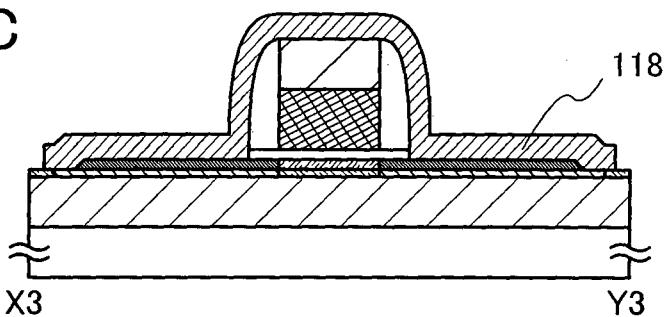
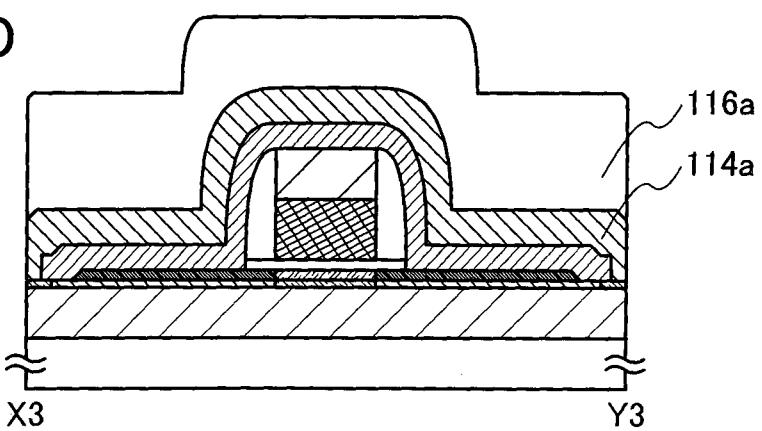


FIG. 11D



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FIG. 12A

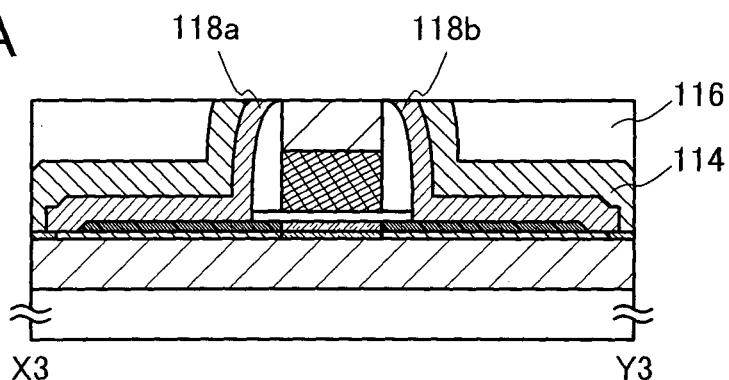


FIG. 12B

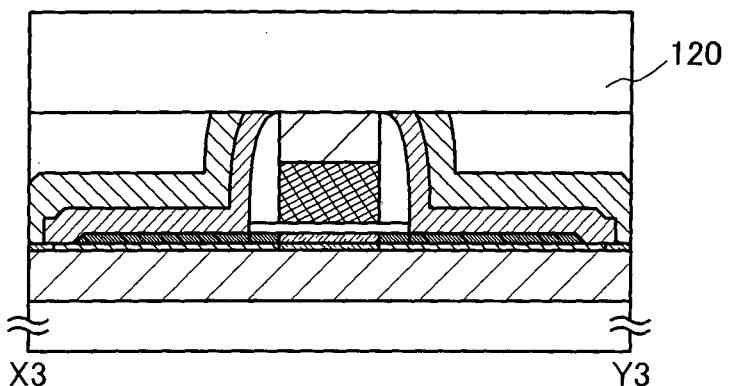
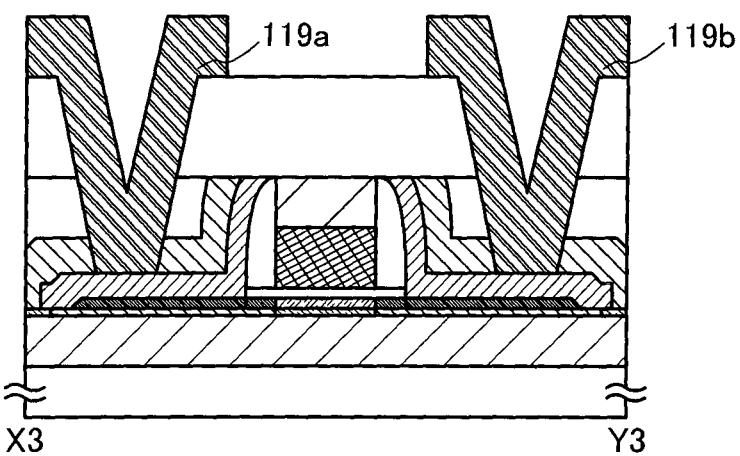


FIG. 12C



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FIG. 13A

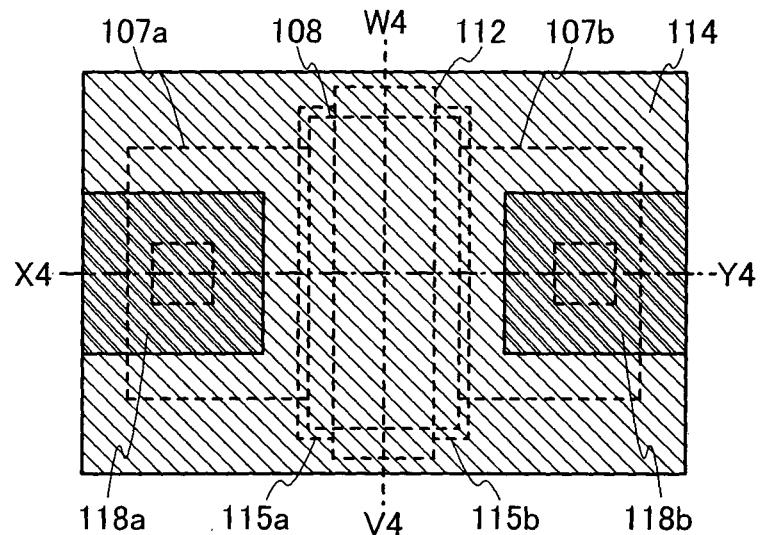


FIG. 13B

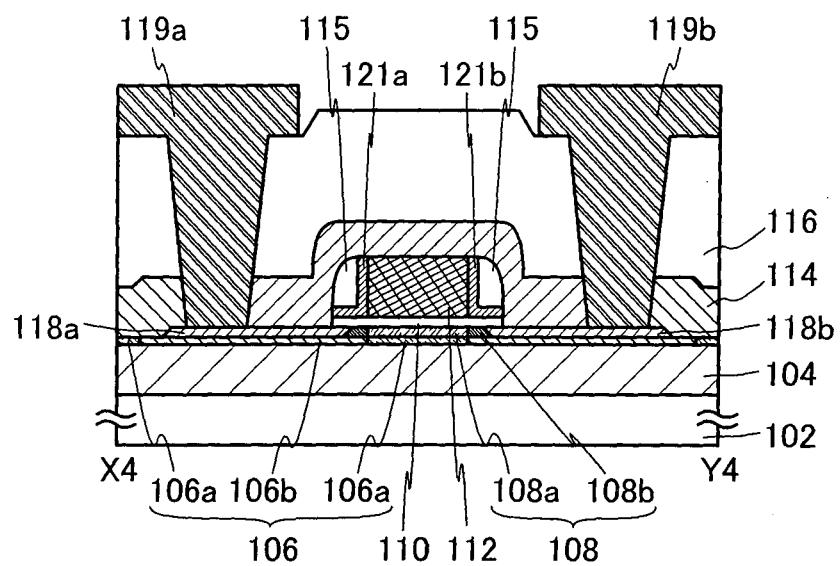
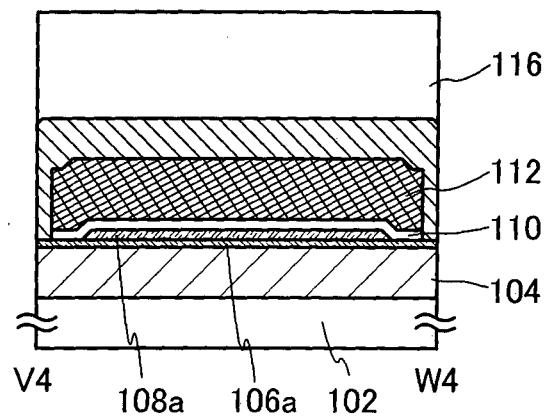


FIG. 13C



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FIG. 14A

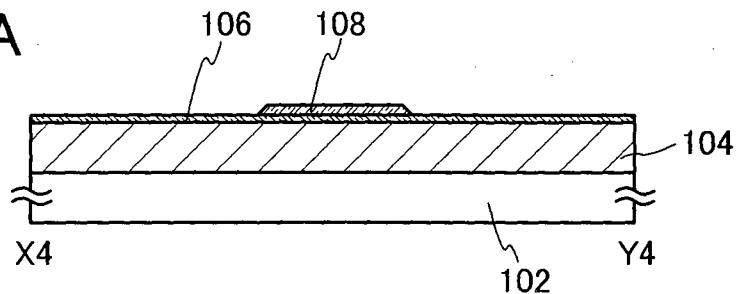


FIG. 14B

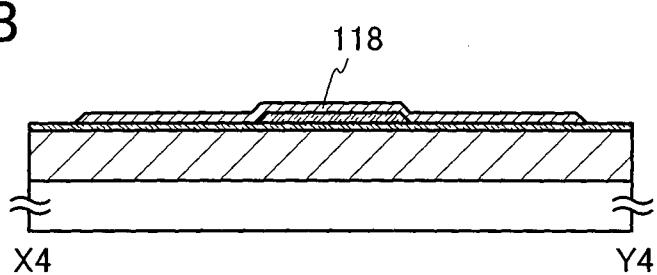


FIG. 14C

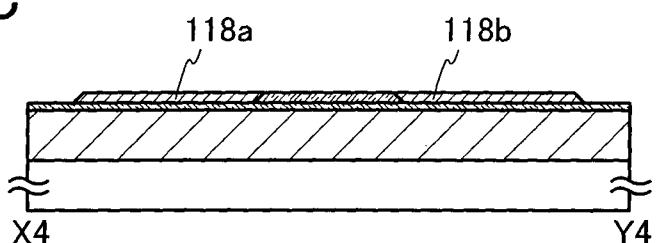
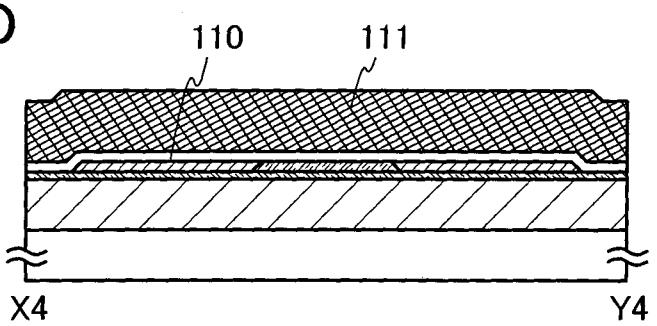


FIG. 14D



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FIG. 15A

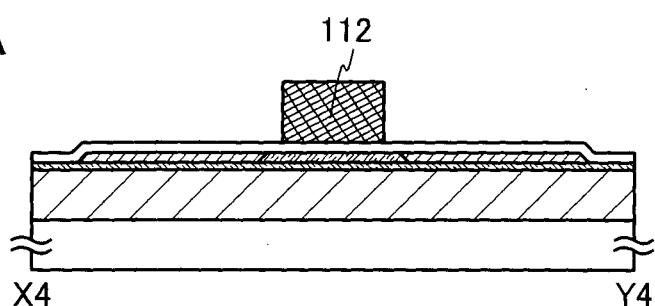


FIG. 15B

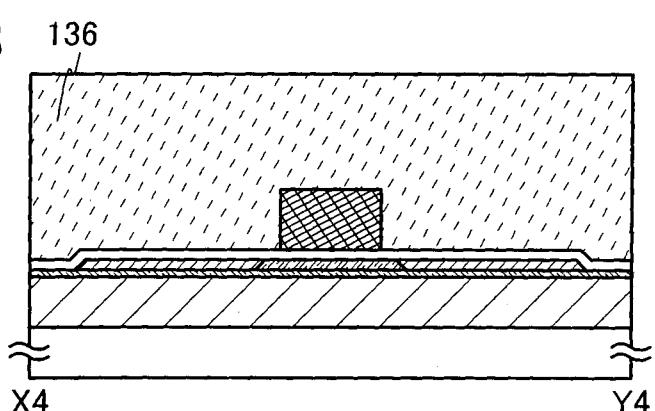


FIG. 15C

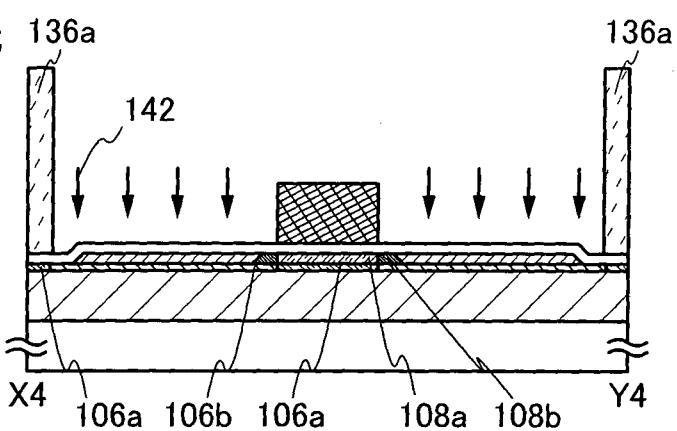
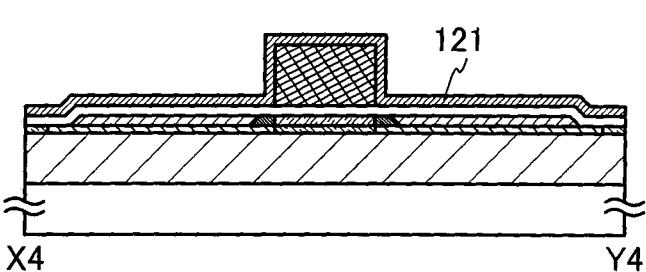


FIG. 15D



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FIG. 16A

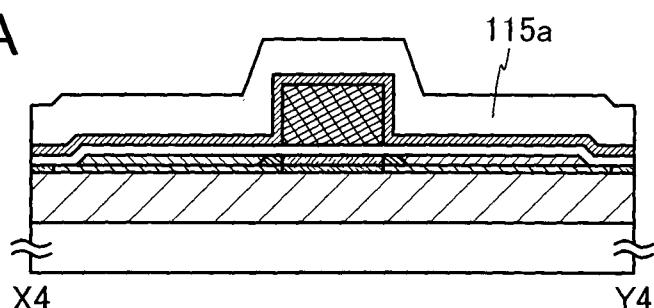


FIG. 16B

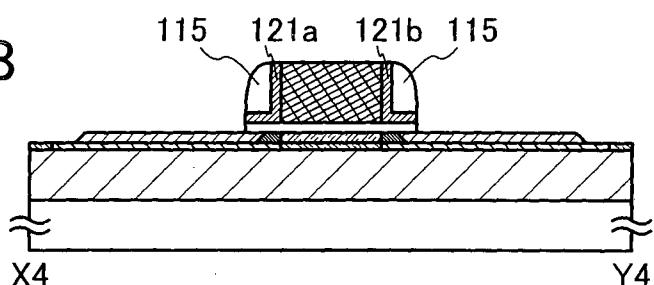


FIG. 16C

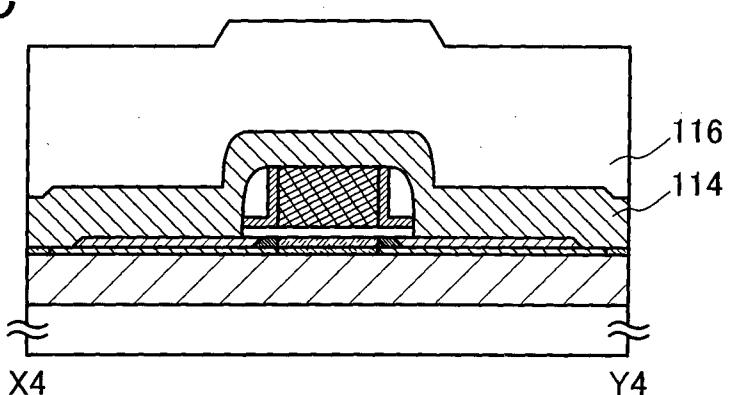
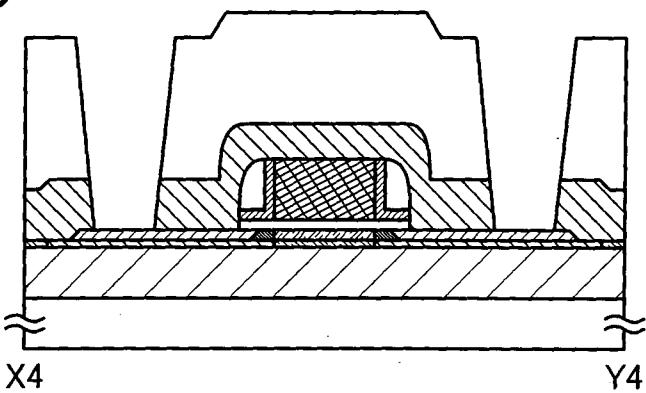


FIG. 16D



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FIG. 17A

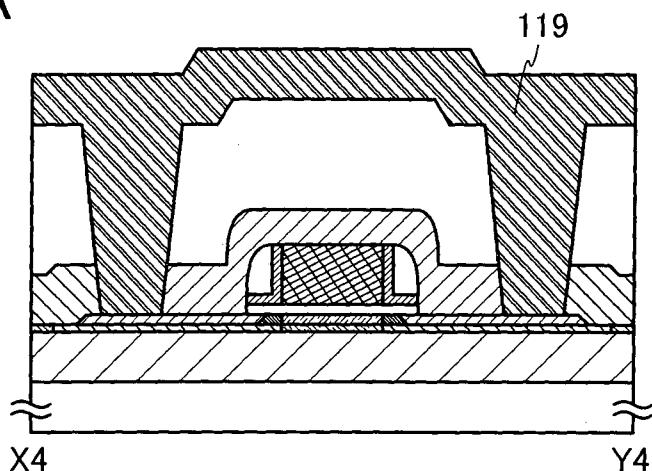
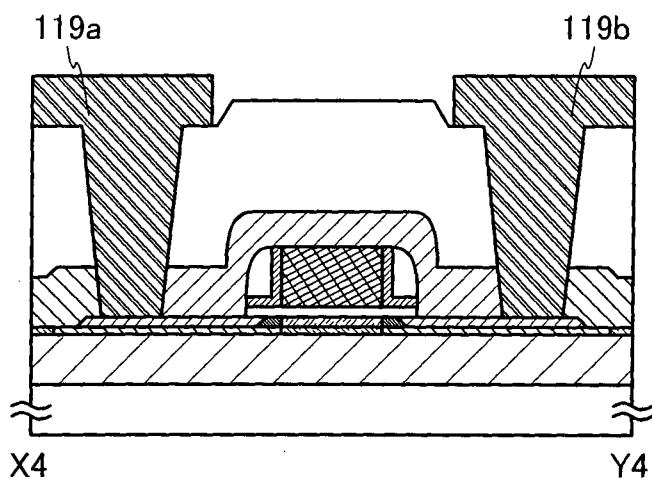


FIG. 17B



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FIG. 18A

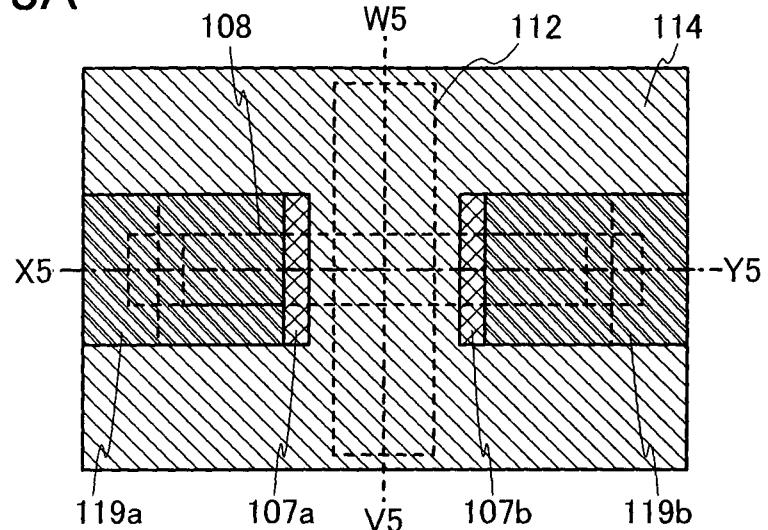


FIG. 18B

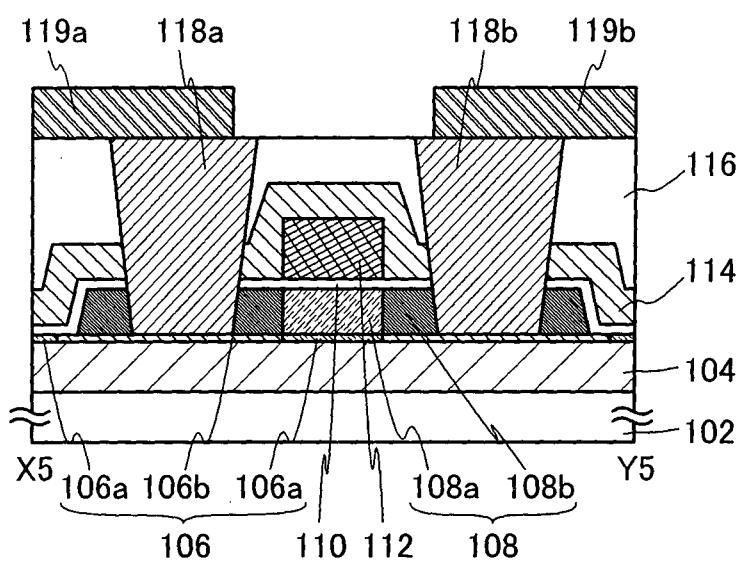
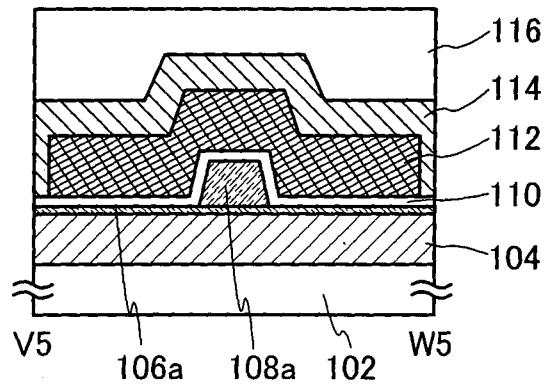


FIG. 18C



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FIG. 19A

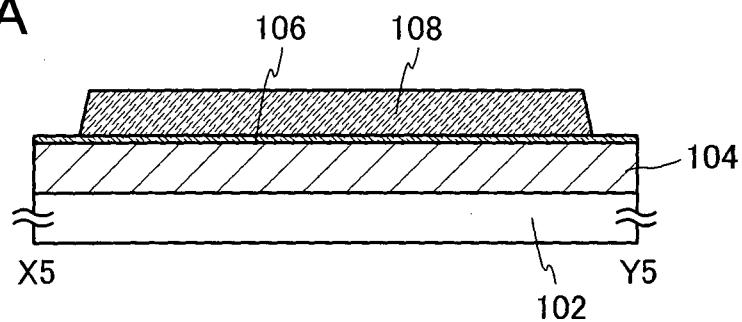


FIG. 19B

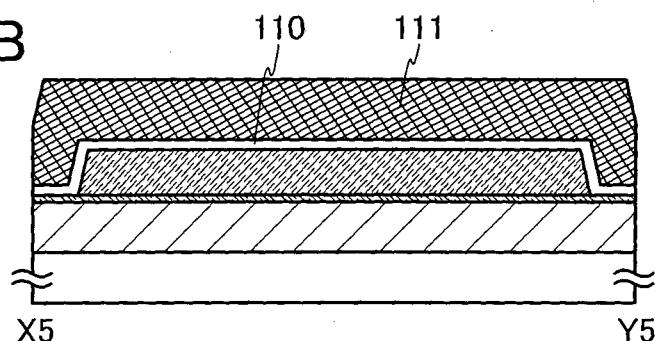


FIG. 19C

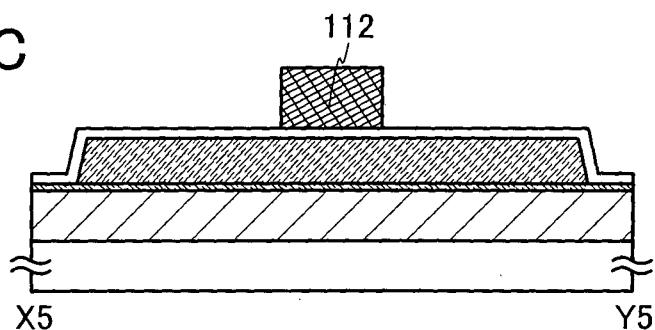
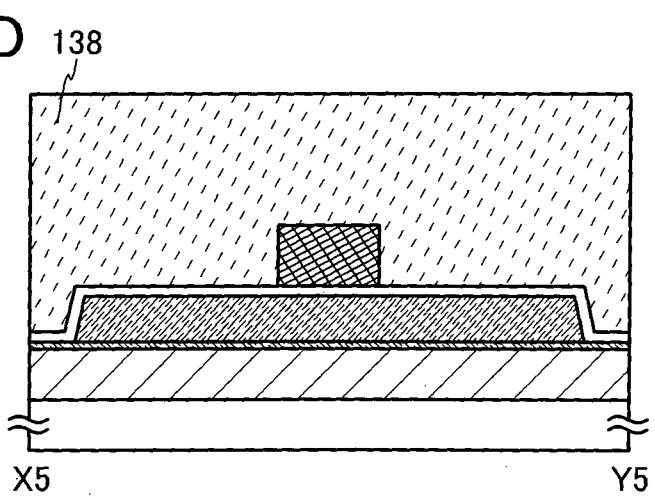
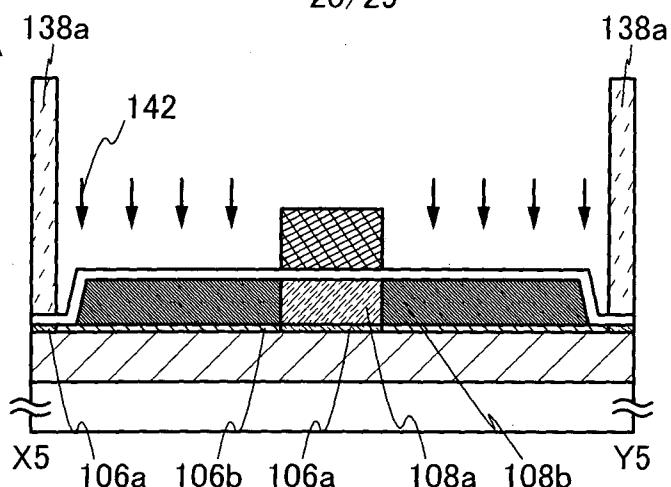
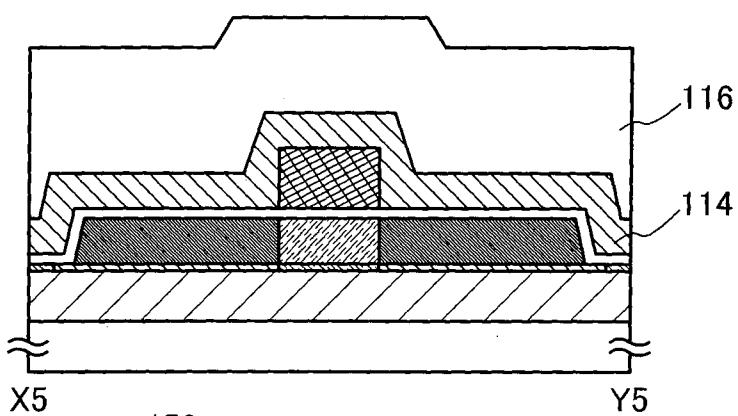
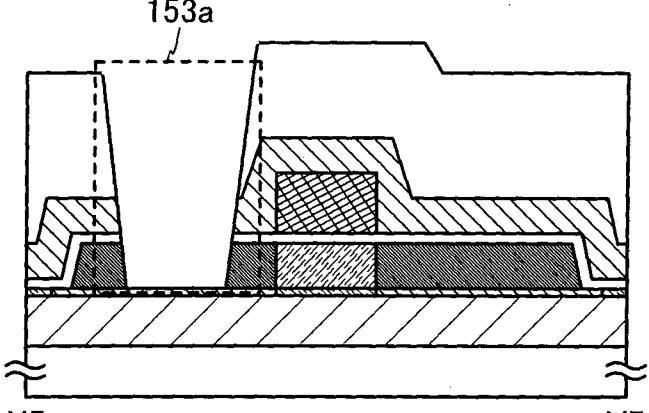
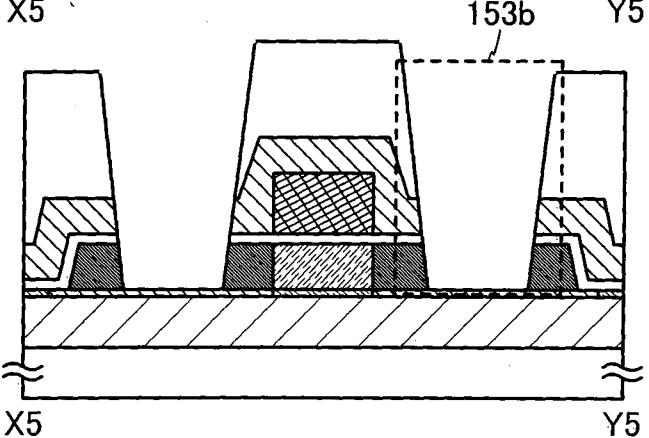


FIG. 19D



**FIG. 20A**

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**FIG. 20B****FIG. 20C****FIG. 20D**

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FIG. 21A

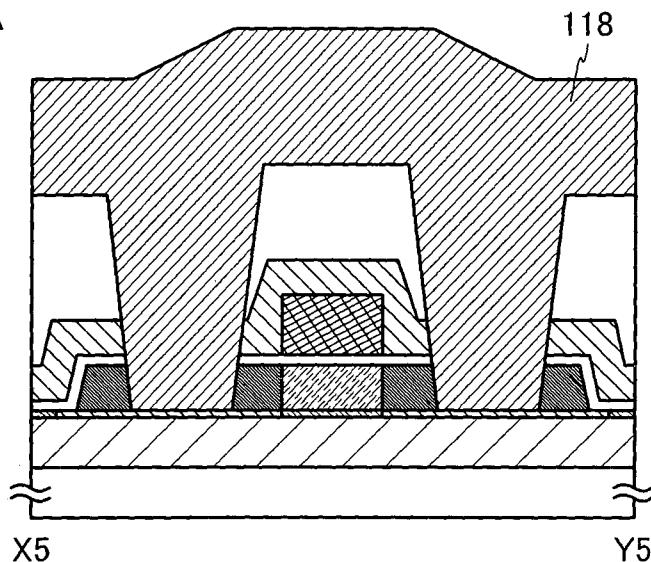


FIG. 21B

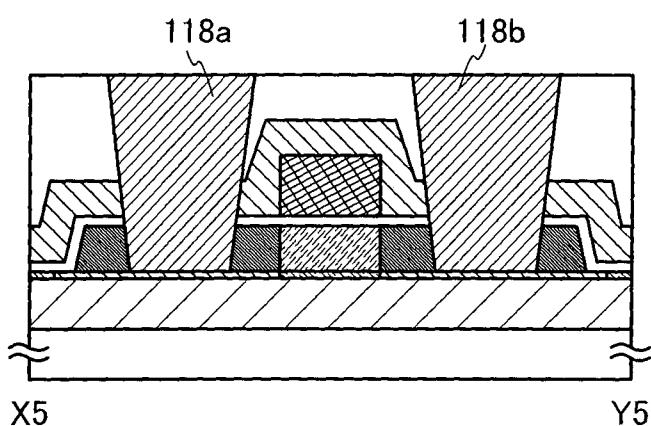


FIG. 21C

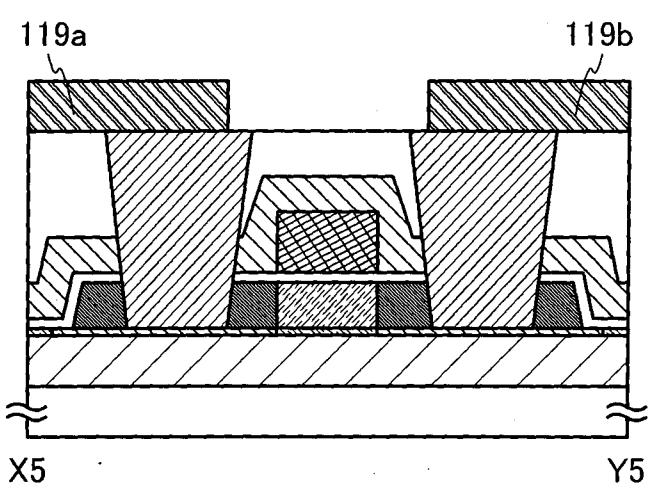


FIG. 22A

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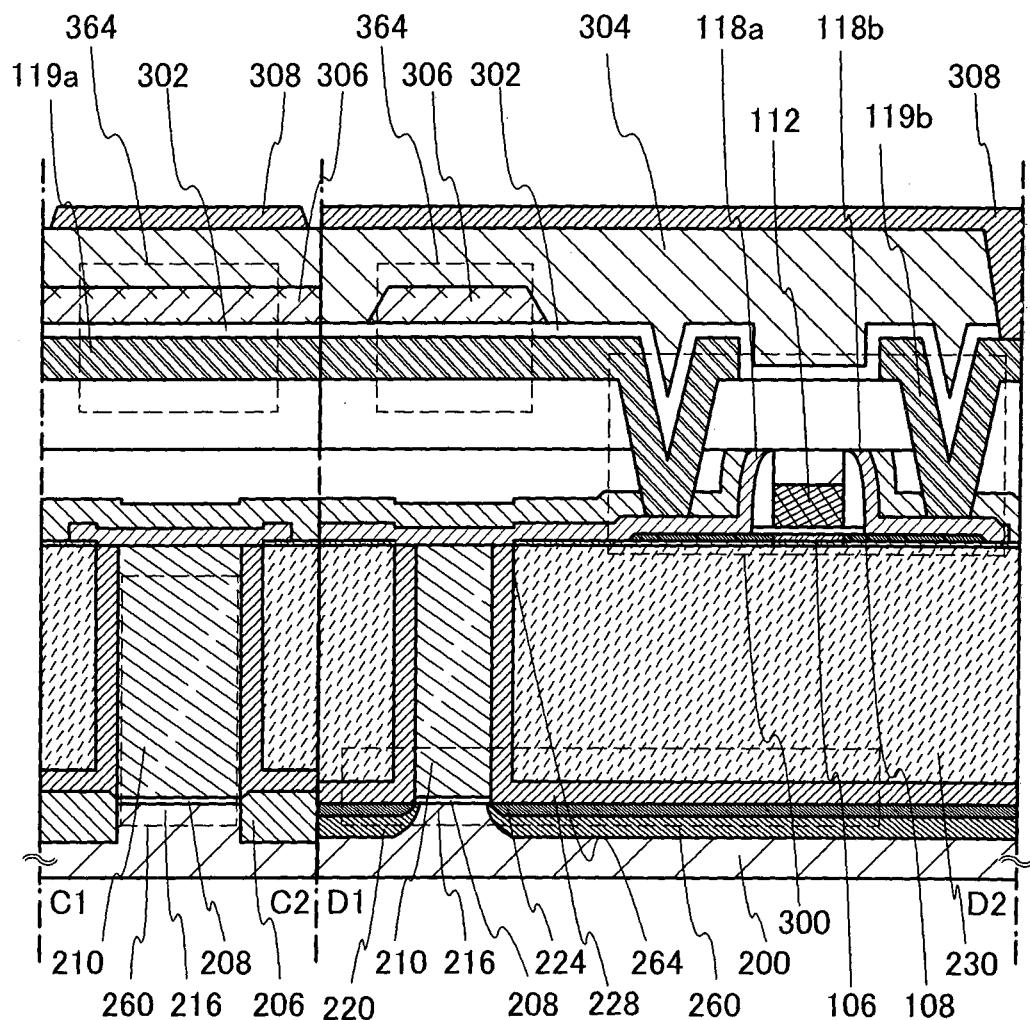


FIG. 22B

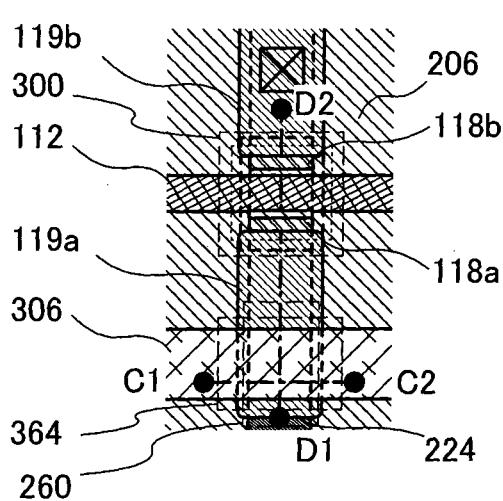
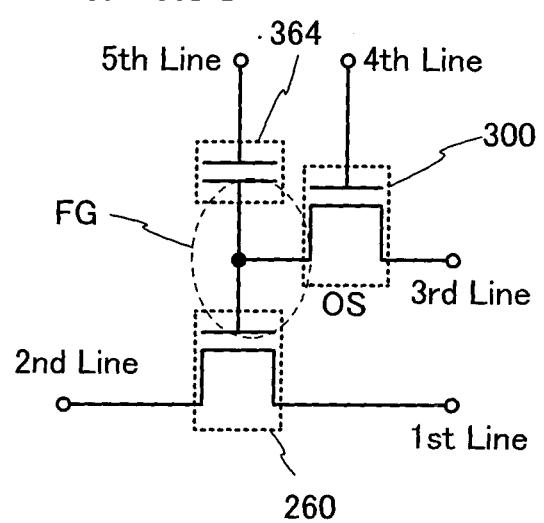


FIG. 22C



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FIG. 23A

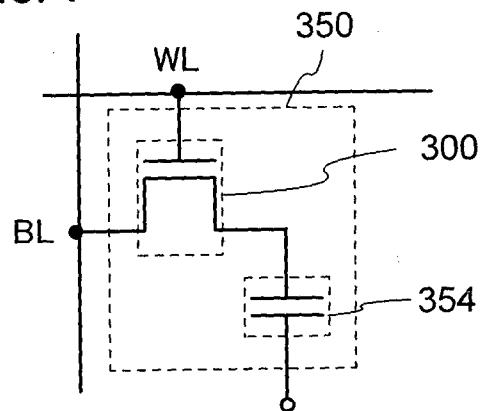


FIG. 23B

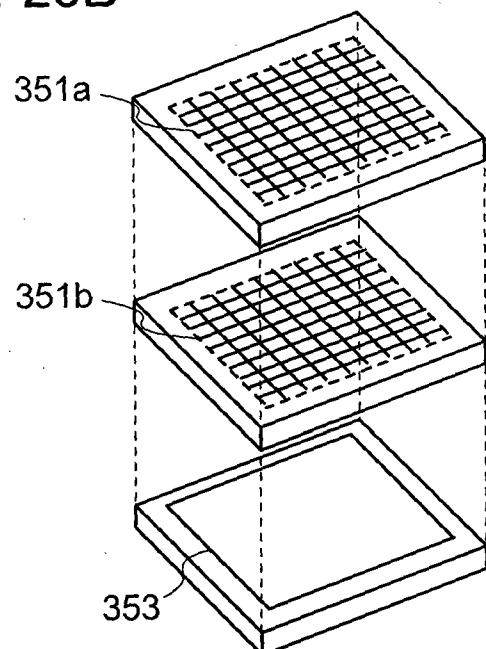


FIG. 24A

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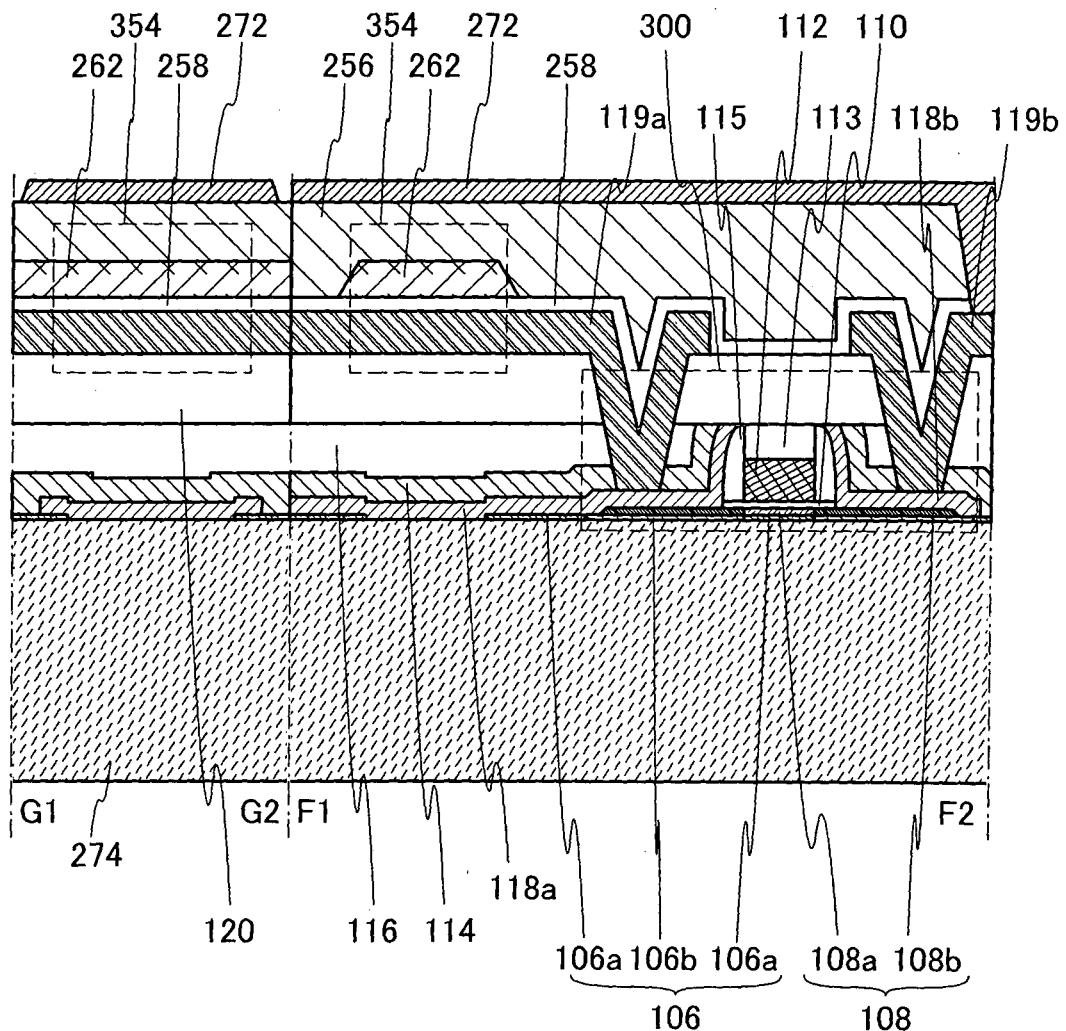
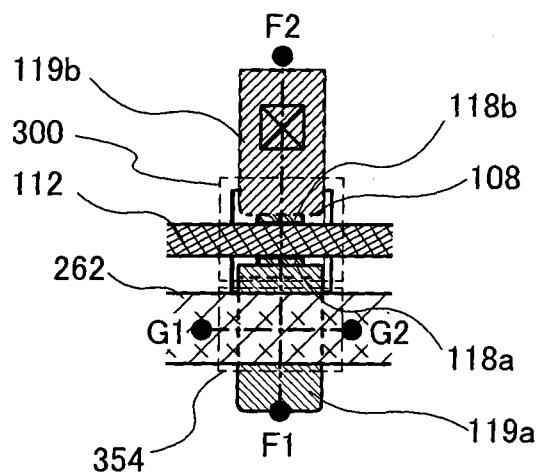


FIG. 24B



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FIG. 25A

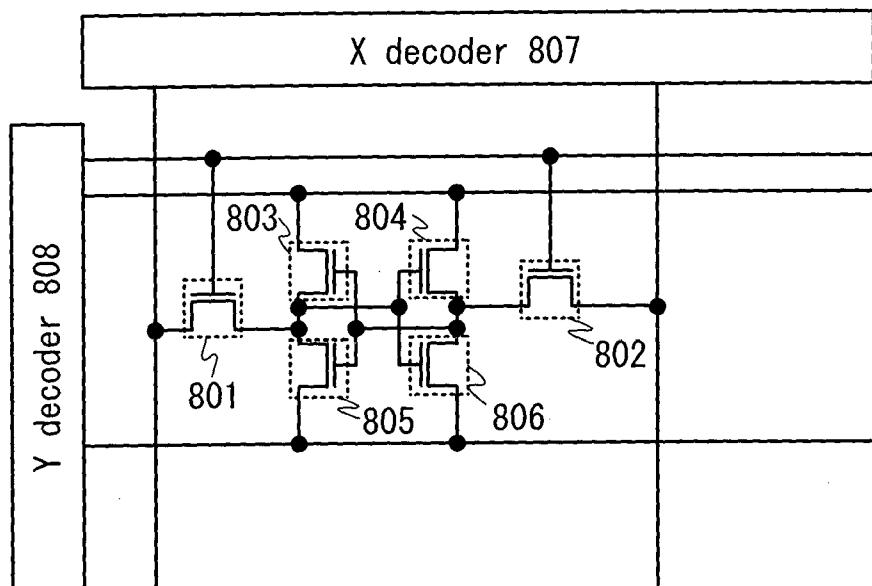
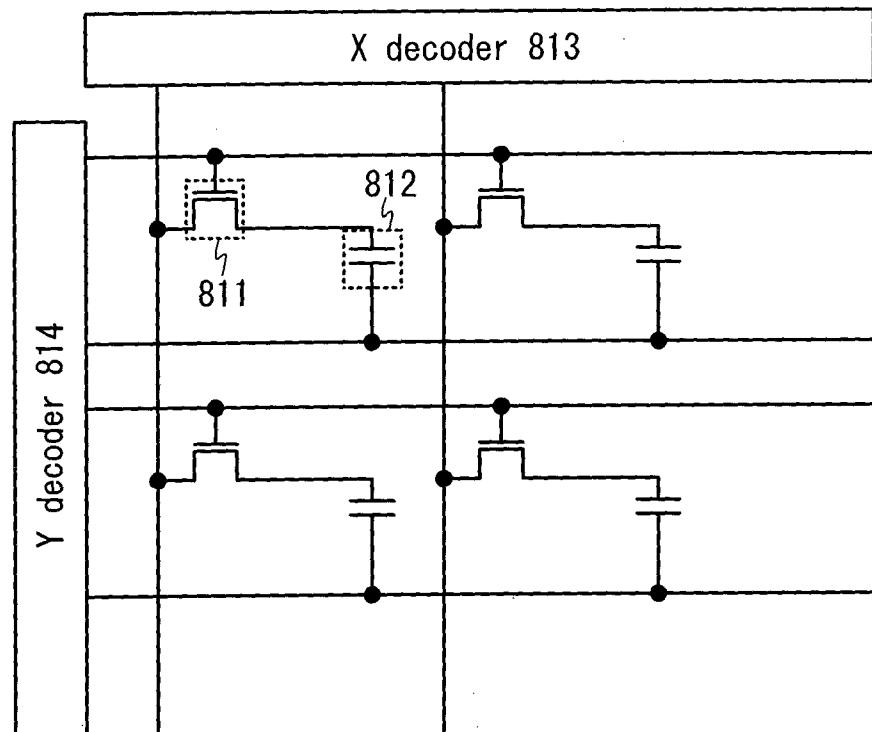


FIG. 25B



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FIG. 26

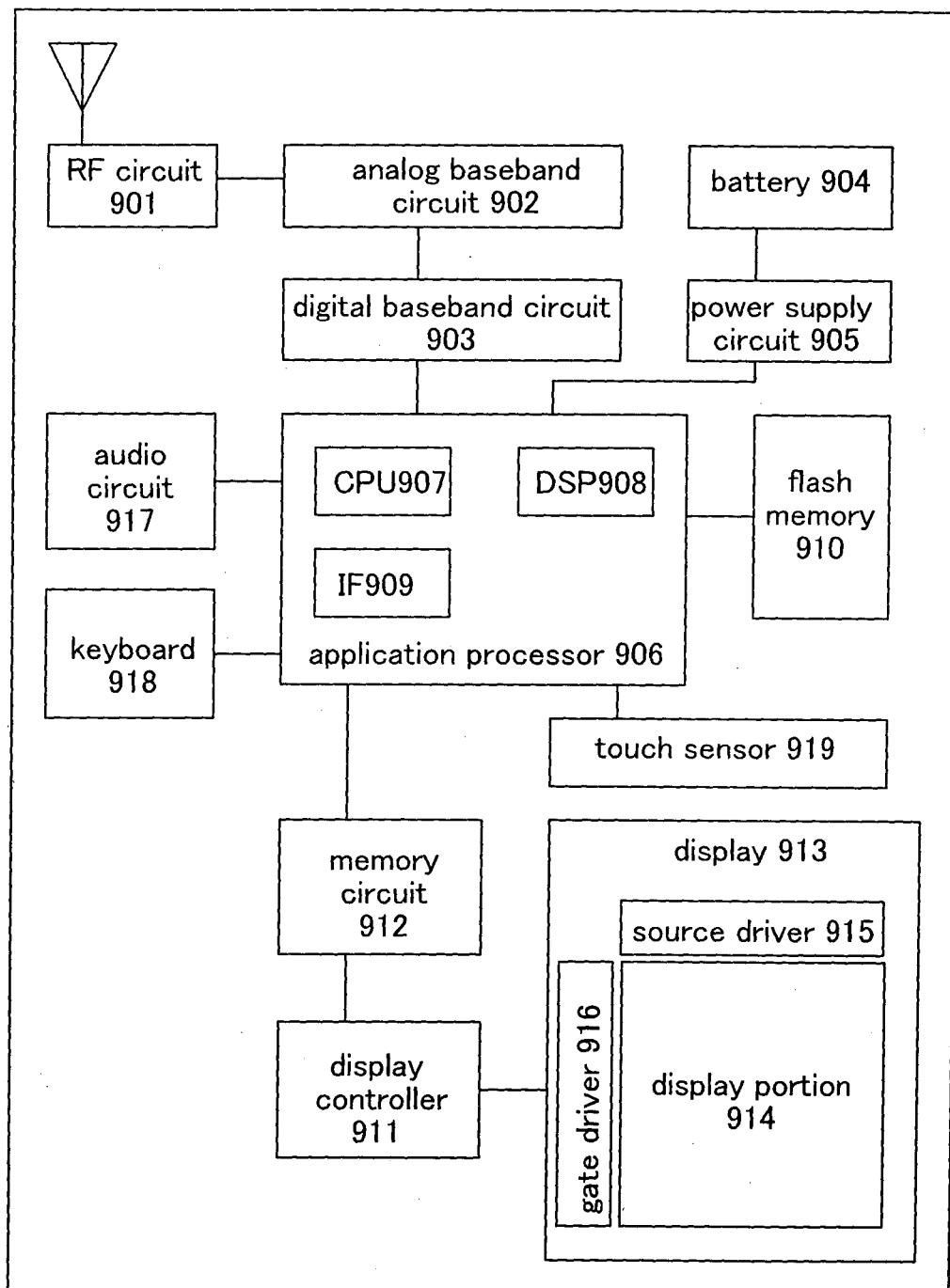
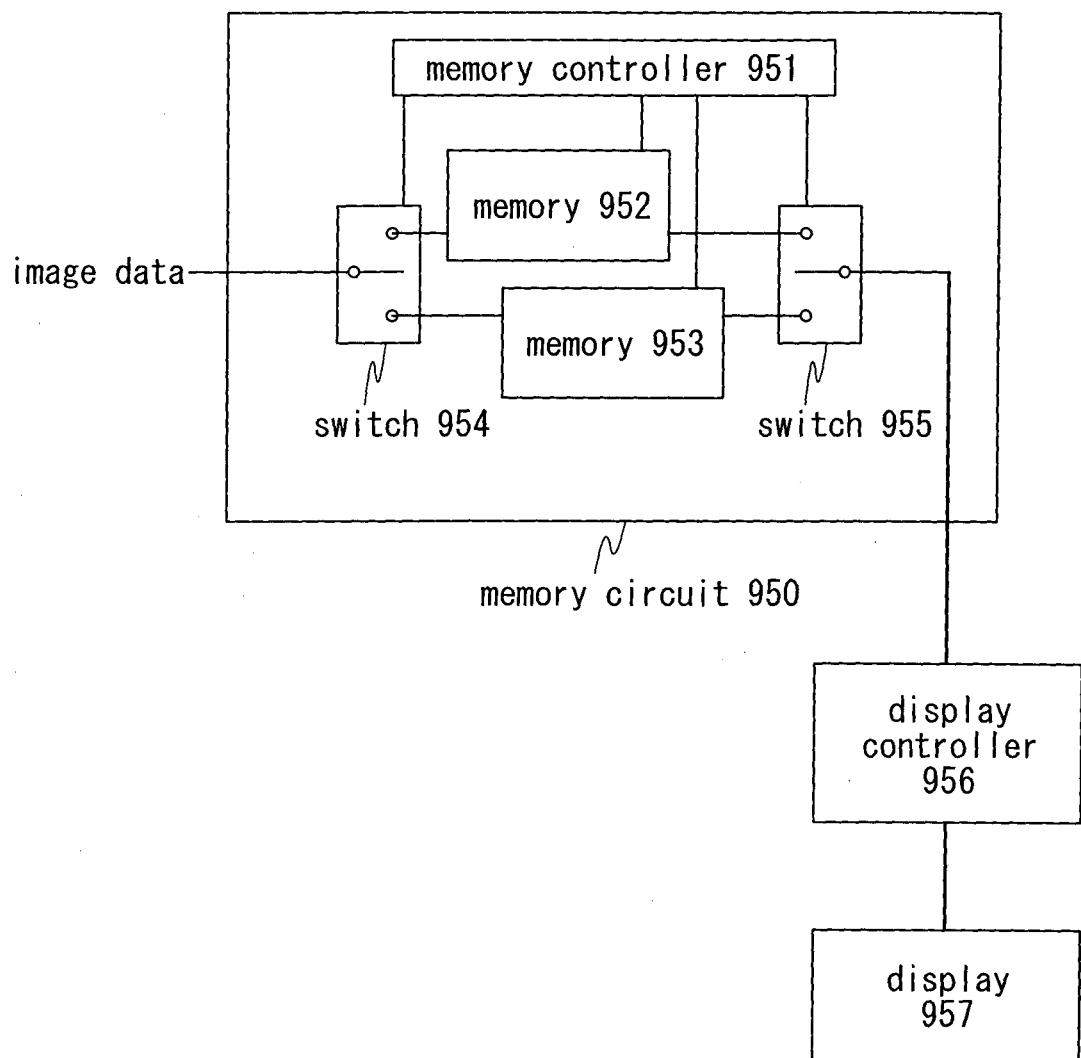


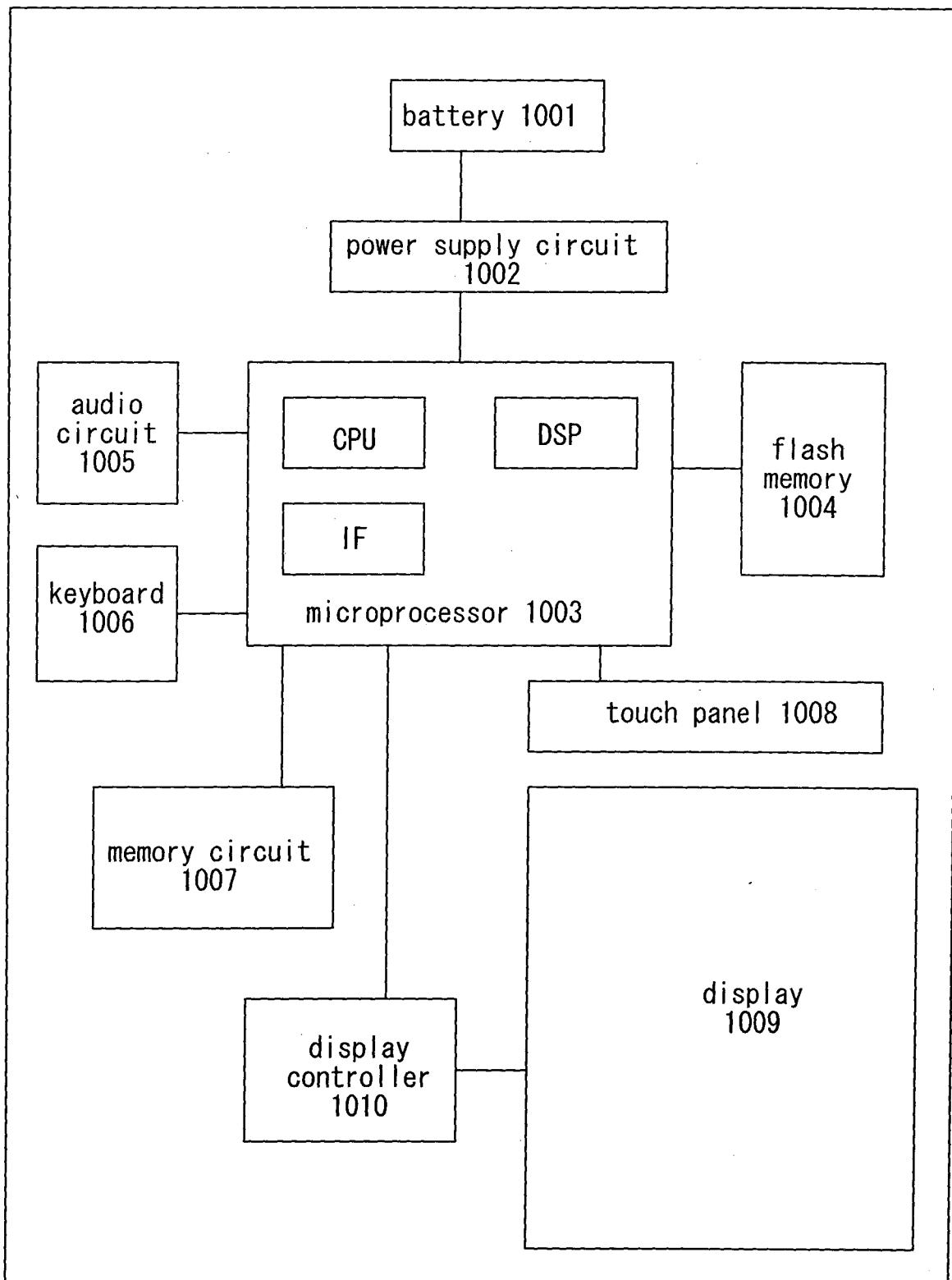
FIG. 27

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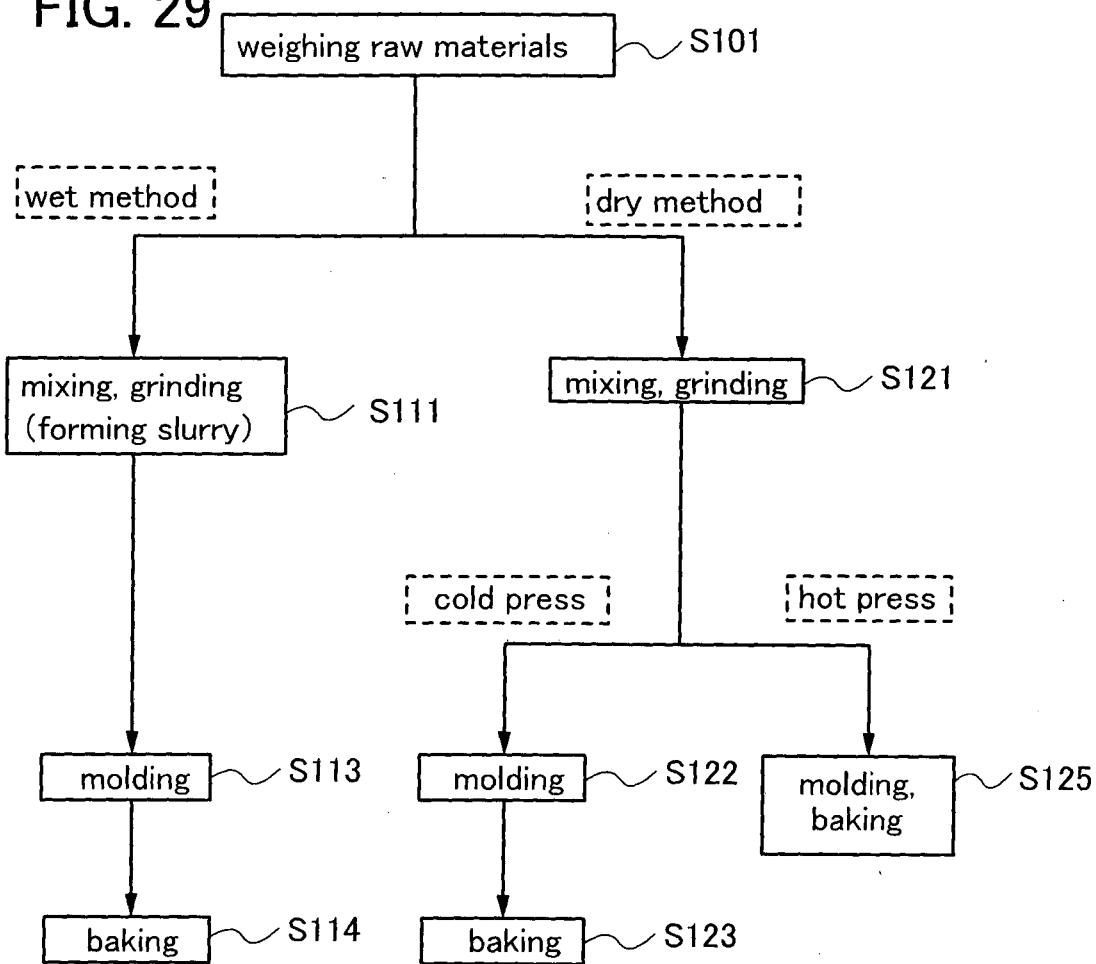
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FIG. 28



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FIG. 29



# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/JP2012/083764

## A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, G02F1/1368, H01L21/336, H01L21/8242, H01L21/8244, H01L27/105, H01L27/108, H01L27/11

## Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996  
Published unexamined utility model applications of Japan 1971-2013  
Registered utility model specifications of Japan 1996-2013  
Published registered utility model applications of Japan 1994-2013

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2010-73881 A (FUJIFILM Corporation) 2010.04.02, paragraphs [0010] - [0045],	1, 5-6
Y	[0110] - [0124] ; fig. 2 (No Family)	2
Y	JP 2008-294136 A (CANON KABUSHIKI KAISHA) 2008.12.04, paragraphs [0013] - [0024] ; fig. 1-3 & US 2008/0291350 A1 & WO 2008/105347 A1 & CN 101617408 A & TW 200901481 A	2

Further documents are listed in the continuation of Box C.

See patent family annex.

\* Special categories of cited documents:

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier application or patent but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed
- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
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Date of the actual completion of the international search

12.03.2013

Date of mailing of the international search report

19.03.2013

Name and mailing address of the ISA/JP

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**INTERNATIONAL SEARCH REPORT**

International application No.

PCT/JP2012/083764

## CLASSIFICATION OF SUBJECT MATTER

H01L29/786 (2006. 01) i, G02F1/1368 (2006. 01) i, H01L21/336 (2006. 01) i,  
H01L21/8242 (2006. 01) i, H01L21/8244 (2006. 01) i, H01L27/105 (2006. 01) i,  
H01L27/108 (2006. 01) i, H01L27/11 (2006. 01) i

**INTERNATIONAL SEARCH REPORT**

International application No.  
PCT/JP2 012 / 083764

**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1.  Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
  
2.  Claims Nos.:  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
  
3.  Claims Nos.:  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

See extra sheet .

1.  As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2.  As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3.  As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
  
4.  No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:  
Claims 1 - 2 , 5 - 6

**Remark on Protest**

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

Document 1 describes an invention relating to a transistor comprising: a resistance layer; and an active layer over the resistance layer, wherein the resistance layer and the active layer each comprises indium, gallium, and zinc, and wherein the resistance layer has a lower content percentage of indium and a higher content percentage of gallium than the active layer. Consequently, the invention set forth in claim 1 cannot be considered to be novel over the invention described in document 1 and hence has no special technical feature.

The claims 1-28 are hence examined as to whether the claims had a special technical feature at the time when the international search report was made. As a result, the application is considered to involve five inventions (invention groups). The special technical features of these inventions (invention groups) are as follows.

Incidentally, the invention set forth in claim 1, which has no special technical feature, is classified in invention 1.

(Invention 1) The inventions set forth in claims 1 and 2 A semiconductor device comprising: "a first oxide semiconductor film; and a second oxide semiconductor film over the first oxide semiconductor film, wherein the first oxide semiconductor film and the second oxide semiconductor film each comprises indium, gallium, and zinc, and wherein the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film" ,and "wherein the first oxide semiconductor film comprises a low-resistance region and a high-resistance region, the high-resistance region being located outside the second oxide semiconductor film".

Incidentally, the invention set forth in claims 5-6 is classified in invention 1 because a search therefore had been substantially finished at the time of the order for payment of additional fees.

(Invention 2) The inventions set forth in claim 3 A semiconductor device comprising: "a first oxide semiconductor film; and a second oxide semiconductor film over the first oxide semiconductor film, wherein the first oxide semiconductor film and the second oxide semiconductor film each comprises indium, gallium, and zinc, and wherein the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film" ,and "wherein the second oxide semiconductor film comprises a channel region and a pair of low-resistance regions in contact with the channel region".

(Invention 3) The inventions set forth in claim 4 A semiconductor device comprising: "a first oxide semiconductor film; and a second oxide semiconductor film over the first oxide semiconductor film, wherein the first oxide semiconductor film and the second oxide semiconductor film each comprises indium, gallium, and zinc, and wherein the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film" ,and "wherein either end of the second oxide semiconductor film in a channel width direction comprises a high-resistance region".

(Invention 4) The inventions set forth in claim 7

A semiconductor device comprising: "a first oxide semiconductor film; and a second oxide semiconductor film over the first oxide semiconductor film; wherein the first oxide semiconductor film and the second oxide semiconductor film each comprises indium, gallium, and zinc, and wherein the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film" ,and "wherein the second oxide semiconductor film comprises a crystal portion having a c-axis aligned in a direction parallel to a normal vector of a surface where the second oxide semiconductor film is formed".

(Invention 5) The inventions set forth in claims 8-28

A semiconductor device comprising: "a first oxide semiconductor film over an oxide film; a second oxide semiconductor film over the first oxide semiconductor film; a gate insulating film over the second oxide semiconductor film; and a gate electrode over the second oxide semiconductor film with the gate insulating film interposed therebetween, wherein the first oxide semiconductor film and the second oxide semiconductor film each comprises indium, gallium, and zinc, and wherein the first oxide semiconductor film has a lower content percentage of indium and a higher content percentage of gallium than the second oxide semiconductor film".