

March 26, 1940.

J. R. GELZER

2,194,499

NOISE REDUCTION SYSTEM

Filed July 25, 1936

2 Sheets-Sheet 1

FIG. 1.

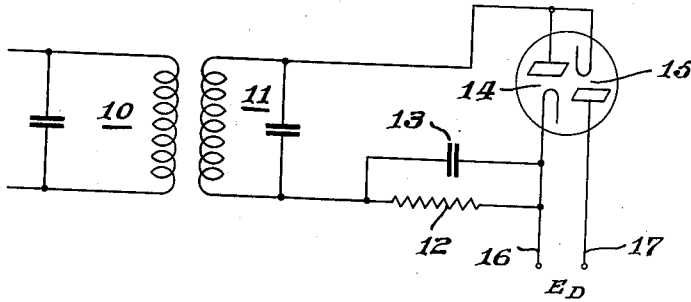


FIG. 2.

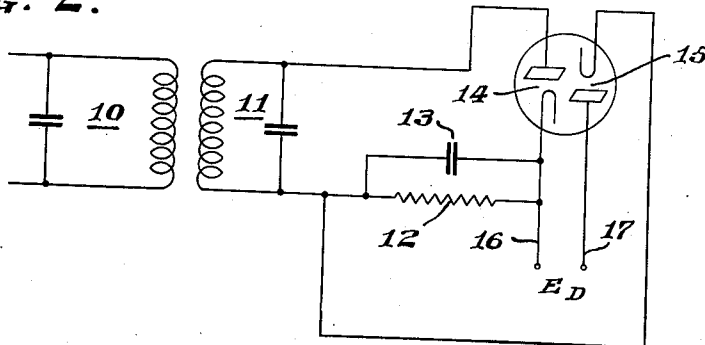


FIG. 3.

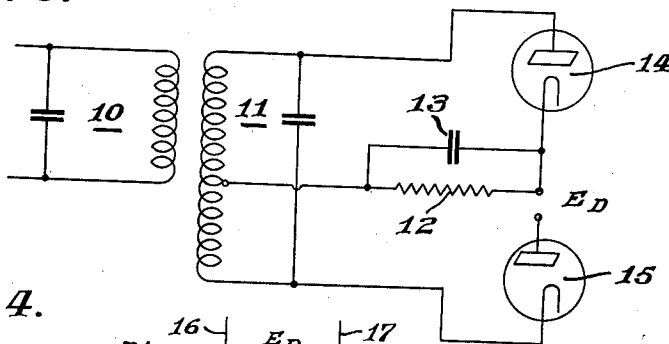
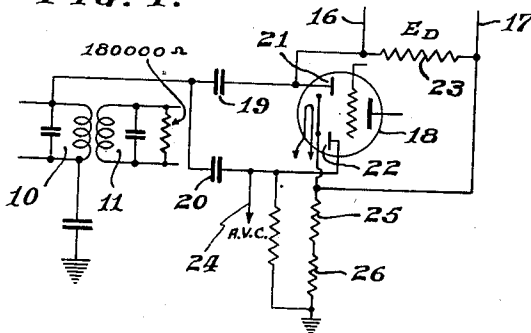


FIG. 4.



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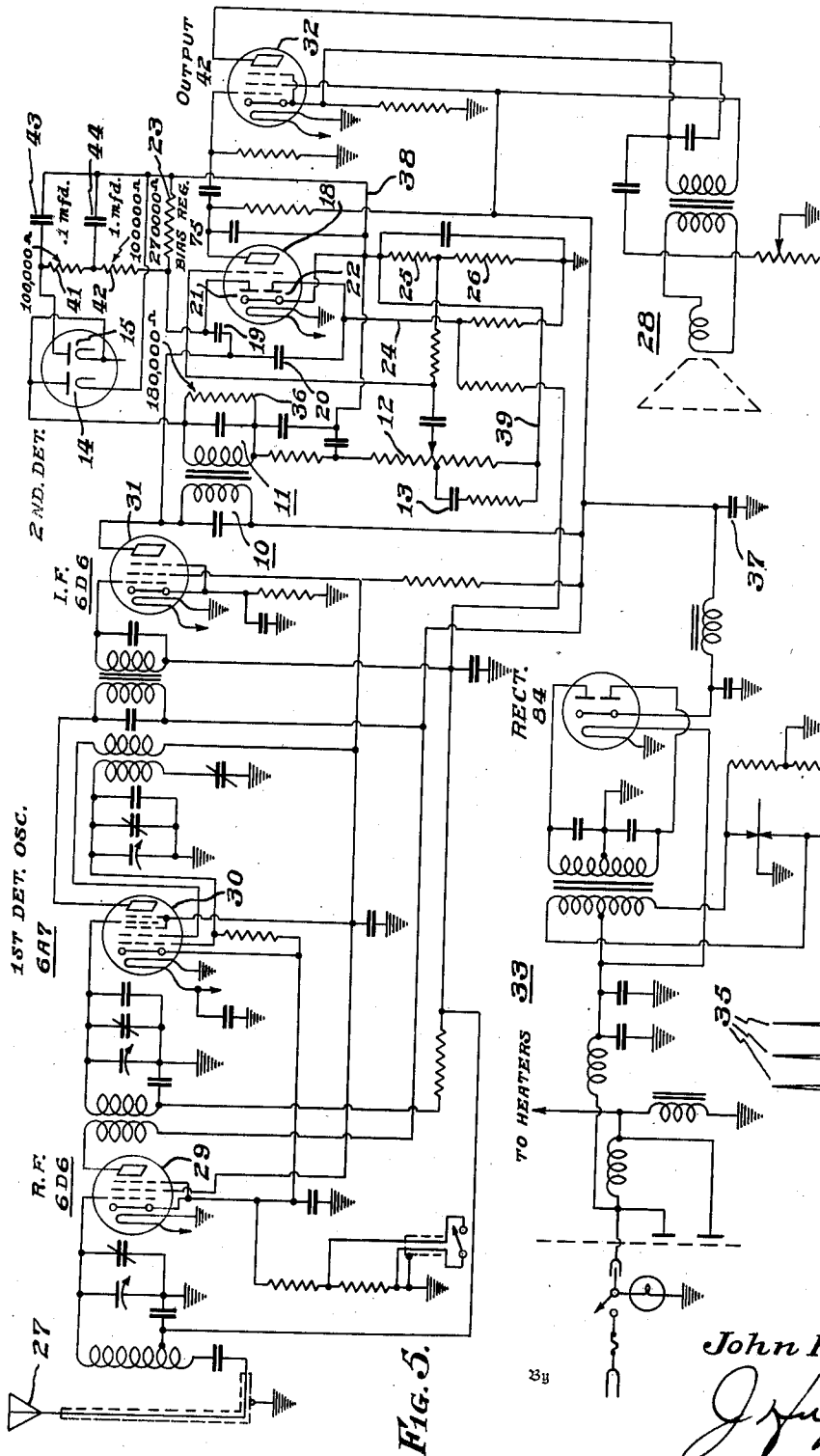


Fig. 5.

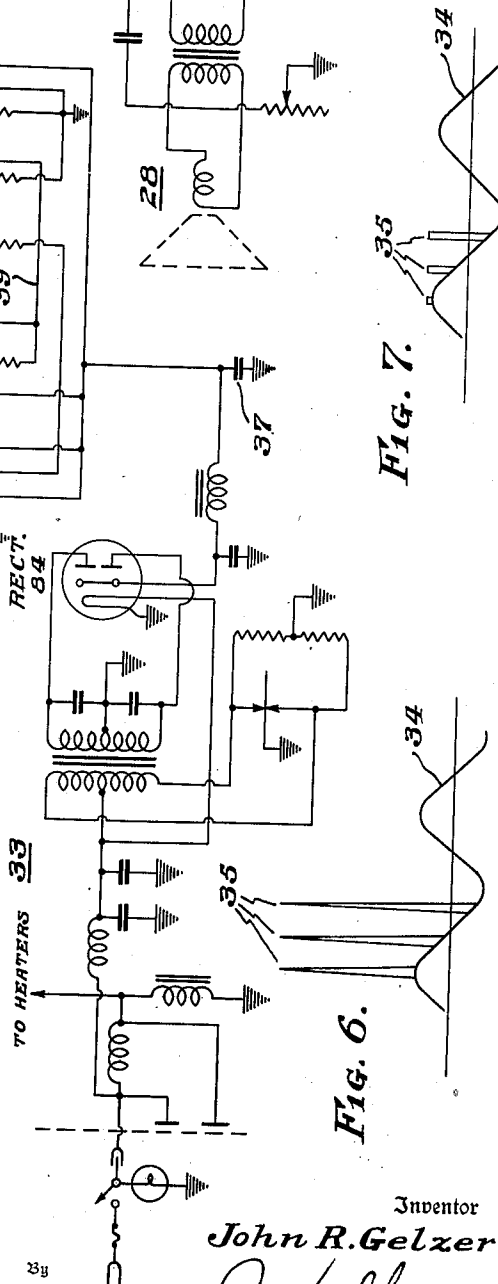


Fig. 6.

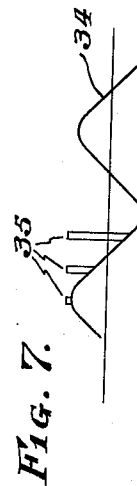


Fig. 7.

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2,194,499

NOISE REDUCTION SYSTEM

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10 Claims. (Cl. 250—20)

This invention relates to the reduction of the noise likely to be produced in radio receivers and similar apparatus by electrical impulses extraneous to the signal, and has for its principal object the provision of an improved apparatus and method of operation whereby the signal channel transmitting efficiency is controlled in a manner to limit or preclude the passage of impulses likely to produce undesired noise.

10 The present invention is similar in some respects to that disclosed by a British Patent No. 185,133 of Scott-Taggart but differs therefrom in that it makes available an improved means for balancing out or limiting received impulses of relatively high amplitude. Stated more specifically, the signal channel is provided with a pair of reversely connected diode detectors one of which is subjected to a delay or bias potential which varies in accordance with the signal level. Under these conditions, one of the diodes functions in a normal manner to detect signal impulses of normal amplitude and the other reversely connected diode functions in response to relatively high level impulses to produce a balancing potential whereby the transmission of such impulses through the channel is limited or prevented. As hereinafter explained, the connections between the signal channel and the reversely connected diode may assume various forms.

The invention will be better understood from the following description when considered in connection with the accompanying drawings and its scope is indicated by the appended claims.

35 Referring to the drawings:

Figs. 1 to 3 are wiring diagrams illustrating different connections of the reversely connected diode detectors.

40 Fig. 4 is a wiring diagram of the circuit through which the delay voltage of the limiter detector is produced.

Fig. 5 illustrates the application of the limiter circuit of Fig. 1 to a radio receiver, and

45 Figs. 6 and 7 are explanatory diagrams relating to the operation of the radio receiver illustrated by Fig. 5.

The limiter circuit of Fig. 1 includes an intermediate frequency transformer provided with a tuned primary circuit 10 and with a tuned secondary circuit 11 in which are connected a resistor 12 and a pair of reversely connected diodes 14 and 15. Hereinafter the diode 14 will be designated as the detector diode and the diode 15 as the limiter diode. These diodes are pro-

vided with terminals 16 and 17 between which a bias or delay voltage E_a may be applied.

As will be readily understood, the current flowing through the resistor 12 is dependent both on the amplitude of the secondary voltage and on the potential E_a . Thus if E_a is zero and the terminals 16 and 17 are short circuited, alternate half cycles of the signal wave are transmitted through the resistor 12 in opposite directions and their resultant is zero. If the voltage E_a is made equal to twice the carrier amplitude, however, no current is transmitted by the limiter diode 15 so long as 100% modulation is not exceeded and the detector diode 14 performs the usual functions of a detector. Greater amplitudes cause the limiter diode 15 to supply to the resistor 12 a balancing current which limits the potential drop of the resistor 12 to a value predetermined by the delay voltage E_a . It will, of course, be understood that establishment of the proper relation between E_a and the carrier amplitude will produce the same action at any selected or desired percent modulation.

The circuit of Fig. 2 is similar to that of Fig. 1 in some respects but differs therefrom in that the limiter diode 15 and the delay potential E_a are connected in shunt to the resistor 12. With these connections, the diode 15 functions to limit the potential drop of the resistor 12 to a value determined by the magnitude of E_a .

In the arrangement of Fig. 3, the two diodes 14 and 15 are fed 180° out of phase. The operation of this arrangement is similar to that of the arrangement of Fig. 1 and will, therefore, be readily understood.

The circuit of Fig. 4 may be utilized to produce the delay voltage E_a of the diode 15. This circuit includes the tuned primary winding 10 and a detector or rectifier amplifier 18 which may be a Type 75 RCA Radiotron tube. It will be observed that the high potential side of the primary circuit 10 is connected through capacitors 19 and 20 respectively to the diodes 21 and 22, that a resistor 23 is connected in shunt to the diode 21, that an automatic volume control terminal 24 is connected to the diode 22 and that bias resistors 25 and 26 are connected in the cathode lead of the detector amplifier 18. With these connections, the voltage E_a appearing between the terminals 16 and 17 is dependent on or directly proportional to the amplitude of the signal, and, as hereinafter explained, may be used to prevent the flow of current through the limiter diode 15 (Figs. 1 to 3) until impulses

of a relatively high level are supplied to the channel.

The radio receiver circuit of Fig. 5 is shown only in order to facilitate an understanding of the present invention and will therefore not be described in great detail. It includes an antenna 27 from which signal impulses are supplied to a receiver, such as a loud speaker 28, through a channel including a radio amplifier 29, a first detector and oscillator 30, an intermediate frequency amplifier 31, the second detector 14, the amplifier electrodes of the electron discharge device 18 and an audio frequency amplifier 32. Power for operating the channel derived through a rectifying and filtering unit designated generally by the reference numeral 33.

The character of the impulses received at the antenna 27 may be as indicated by Fig. 6 in which the desired signal modulation impulses are indicated by the wave 34 and the undesired or noise modulation impulses are indicated at 35. These impulses are amplified and detected in the usual manner until they reach the intermediate frequency coupling transformer 10-11. Since the secondary of this transformer is loaded by a resistor 36 so that a primary to secondary voltage ratio of two to one is realized and the diodes 21 and 22 are fed from the primary side of the transformer, the bias diode 21 and the automatic volume diode 22 are subjected to a voltage greater than that applied to the reversely connected detector diode 14 and the limiter diode 15.

The circuits of the diodes 21 and 22 may be traced from the high voltage side of the primary 10 through the diodes and the bias resistors 25 and 26 to ground and from ground through a capacitor 37 to the low voltage side of the primary 10. The circuit of the diode 14 may be traced from the high voltage side of the secondary 11 through the diode, conductors 38 and 39, and the volume control resistor 12 to the low voltage side of the secondary winding. Connected in circuit with the limiter diode 15 are resistors 41 and 42 and capacitors 43 and 44 which function to filter the limiter bias potential E_a appearing at the terminals of the resistor 23 as a result of its connection in shunt to the diode 21. The circuit of the limiter diode 15 may be traced from the high voltage side of the secondary 11 through the diode, the resistors 41, 42 and 23, the conductors 38 and 39 and the volume control resistor 12 to the low side of the secondary 11. Since the reversely connected diodes 14 and 15 supply current to the same resistor 12 in opposite directions, it is apparent that impulses of an amplitude exceeding a value dependent on the voltage drop of E_a of the resistor 23 are balanced or limited as indicated by the curves 34 and 35 of Fig. 7.

I claim as my invention:

1. A signal channel including a transformer provided with primary and secondary circuits, an amplifier provided with input and output circuits, a rectifier output impedance device connected in said input circuit, a second rectifier output impedance device, a pair of signal detectors reversely connected to said secondary circuit in parallel through said first named impedance device, said second rectifier output impedance being included serially in circuit with only one of said detectors, and means connected to said primary circuit for producing a delay potential in said second rectifier output impedance device in response to received signals.

2. A signal channel including a transformer provided with primary and secondary circuits, an amplifier provided with input and output circuits, a rectifier output impedance device connected in said input circuit, a second rectifier output impedance device, a pair of signal detectors reversely connected to said secondary circuit in parallel through said first named impedance device, said second rectifier output impedance being included serially in circuit with only one of said detectors, and means including a rectifier interposed between said primary circuit and said second rectifier output impedance device for deriving a potential for delaying the action of said one of said detectors in response to received signals.

3. A signal channel including a transformer provided with primary and secondary circuits, an amplifier provided with input and output circuits, a rectifier output impedance device connected in said input circuit, a second rectifier output impedance device, a pair of signal detectors reversely connected to said secondary circuit in parallel through said first named impedance device, said second rectifier output impedance being included serially in circuit with only one of said detectors, and means connected to said primary circuit for producing a delay potential in said second rectifier output impedance device, and a loading resistor connected in shunt to said secondary circuit.

4. In a modulated signal amplifying system, the combination of means for rectifying an amplified signal including a rectifier device having an output resistor, a pair of diode rectifiers, a signal amplifier coupling transformer provided in connection with said rectifier device and diode rectifiers having a primary for supplying signals to said rectifier device and a secondary for supplying signals to said diode rectifiers, means providing a resistance load across the secondary of the transformer, means providing a common output resistor for said diode rectifiers, means including a signal input circuit for applying signals to said rectifiers through said last named resistor in opposing parallel relation to each other, means for deriving a biasing potential from the first named resistor, and means for applying said potential serially in circuit with only one of said diode rectifiers to provide a delayed rectifier action, whereby a signal output voltage is provided across said common output resistor in response to signals below a predetermined amplitude.

5. In a modulated signal amplifying system, the combination of a pair of diode rectifier devices, each having a cathode and an anode electrode, means for applying modulated signals to said rectifiers in parallel opposing relation to each other, the cathode of one rectifier being connected to the anode of the other, means providing a rectified signal voltage between the cathode of one rectifier and the anode of the other, means providing a common output resistor circuit for said rectifiers, means for deriving at least a portion of the modulation component of an amplified signal from said circuit, said first named means including a tunable secondary circuit for a signal coupling transformer, and said second named means including a primary circuit for said transformer, a rectifier connected therewith, and an output resistor for said rectifier providing a rectified signal voltage source.

6. In a modulated signal amplifying system,

the combination of means for rectifying an amplified signal including a rectifier device having a signal input circuit and an output resistor, a pair of diode rectifiers, means providing a common output resistor therefor, means including a second signal input circuit for applying signals to said rectifiers through said last named resistor in opposing parallel relation to each other, means for applying a signal to said input circuits in a predetermined voltage ratio, means for deriving a biasing potential from the first named resistor, and means for applying said potential serially in circuit with only one of said diode rectifiers to provide a delayed rectifier action, whereby a signal output voltage is provided across said common output resistor in response to signals below a predetermined amplitude.

7. In a modulated signal amplifying system, the combination of means for rectifying an amplified signal including a rectifier device having a signal input circuit and an output resistor, a pair of diode rectifiers, means providing a common output resistor therefor, means including a second signal input circuit for applying signals to said rectifiers through said last named resistor in opposing parallel relation to each other, the signal voltage applied to the first named input circuit being higher than that applied to the second named input circuit, means for deriving a biasing potential from the first named resistor, and means for applying said potential serially in circuit with only one of said diode rectifiers to provide a delayed rectifier action, whereby a signal output voltage is provided across said common output resistor in response to signals below a predetermined amplitude.

8. In a modulated signal amplifying system, the combination of means for rectifying an amplified signal including a rectifier device having a signal input circuit and an output resistor, a pair of diode rectifiers, means providing a common output resistor therefor, means including a second signal input circuit for applying signals to said rectifiers through said last named re-

sistor in opposing parallel relation to each other, mean for applying a signal to said input circuits in a predetermined voltage ratio, a second rectifier device connected with the first named input circuit, and an automatic volume control circuit connected with said last named rectifier device to receive controlling potentials therefrom, means for deriving a biasing potential from the first named resistor, and means for applying said potential serially in circuit with only one of said diode rectifiers to provide a delayed rectifier action, whereby a signal output voltage is provided across said common output resistor in response to signals below a predetermined amplitude.

9. A signal channel including an amplifier provided with input and output circuits, an impedance device connected in said input circuit, a second input circuit, a pair of detectors for rectifying signals from said channel in opposition, reversely connected to said channel through said second input circuit and said impedance device, and means including a rectifier energized from said channel for subjecting only one of said detectors to a delay potential having a value dependent upon the carrier wave strength, and means for determining the ratio of the carrier wave level at said detectors with respect to that at said last named rectifier.

10. A signal channel including an amplifier provided with input and output circuits, an impedance device connected in said input circuit, a second input circuit, a pair of detectors for rectifying signals from said channel in opposition, reversely connected to said channel through said second input circuit and said impedance device, and means including a rectifier energized from said channel for subjecting only one of said detectors to a delay potential having a value dependent upon the carrier wave strength, and means for maintaining the ratio of the carrier wave level at said detectors with respect to that at said last named rectifier in a 1:2 ratio.

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