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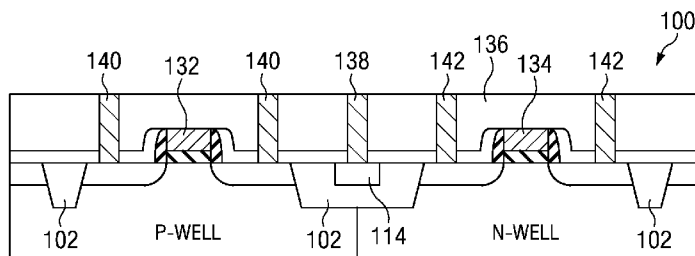


FIG. 11

(57) Abstract: A method of fabricating an integrated circuit is disclosed. The method comprises providing a substrate (100) having an isolation region (102) and etching a trench in the isolation region. A first conductive layer (114) is formed within the trench. A first transistor having a first conductivity type (n-channel) is formed at a face of the substrate. The first transistor has a gate formed of the first conductive layer. A second transistor having a second conductivity type (p-channel) is formed at the face of the substrate. The second transistor has a gate formed of the first conductive layer. The method further comprises replacing the first conductive layer of the first transistor with a first metal gate (132) and replacing the first conductive layer of the second transistor with a second metal gate (134).

POLYCRYSTALLINE SILICON E-FUSE AND RESISTOR FABRICATION IN A METAL REPLACEMENT GATE PROCESS

BACKGROUND

[0001] Embodiments relate to fabrication of a polycrystalline silicon e-fuse in a complementary metal oxide semiconductor (CMOS) metal replacement gate process.

[0002] Shrinking semiconductor integrated circuit feature sizes have placed increasing challenges on semiconductor integrated circuit processing. In particular, a balance between high packing density and yield requires a finely tuned manufacturing process. Recent process advances include various stress memorization techniques (SMT) in both p-channel and n-channel complementary metal oxide semiconductor (CMOS) circuits, metal gate replacement, and composite gate dielectric materials such as silicon oxynitride (SiON). Such advanced processes, however, may present compatibility issues with other integrated circuit features. e-fuses, for example, are used in many integrated circuits for row and column redundancy selection, integrated circuit identification, programmable logic functions, and other functions. With metal gate replacement, however, polycrystalline silicon is no longer readily available for e-fuses. Therefore, some integrated circuit manufacturers have converted to copper e-fuses formed in the back end of line (BEOL) process after first interlevel oxide (ILD1) deposition. Copper e-fuses, however, have a relatively low resistance and require high current to program or blow them. Moreover, they present some programming reliability issues regarding incomplete programming and copper leakage contamination. Therefore, there is a need for a polycrystalline silicon e-fuse/resistor that is reliable, compatible with metal gate replacement processes, and programmable at a relatively low voltage and a current density of less than $8 \text{ A}/\mu\text{m}^2$ without a high cost associated with excessive process complexity.

BRIEF SUMMARY

In an example embodiment, a method of fabricating an integrated circuit is disclosed. The method comprises providing a substrate having an isolation region. A

trench is etched in the isolation region, and a first conductive layer is formed within the trench. A first transistor having a first conductivity type is formed at a face of the substrate. The first transistor has a gate formed of the first conductive layer. A second transistor having a second conductivity type is formed at the face of the substrate. The second transistor has a gate formed of the first conductive layer. The method further comprises replacing the first conductive layer of the first transistor with a first metal gate and replacing the first conductive layer of the second transistor with a second metal gate.

[0003] BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIGS. 1A - 1I are diagrams of a simplified process flow according to a first embodiment;

[0005] FIGS. 2A - 2F and 1G - 1I are diagrams of a simplified process flow according to a second embodiment; and

[0006] FIGS. 3A - 3H are diagrams of a simplified process flow according to a third embodiment.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0007] The example embodiments provide significant advantages in e-fuse/resistor fabrication for a metal replacement gate process over e-fuse/resistor technology of the prior art.

[0008] Referring now to FIGS. 1A through 1I there are diagrams of a simplified process flow according to a first embodiment of the invention. FIG. 1A illustrates a semiconductor substrate 100 having shallow trench isolation (STI) regions 102 as is well known in the art. The left half of the substrate is designated p-well as a bulk terminal for n-channel metal oxide semiconductor (NMOS) transistors. The right half of the substrate is designated n-well as a bulk terminal for p-channel metal oxide semiconductor (PMOS) transistors. Here, and in the following discussion, drawing figures illustrate a simplified fabrication process flow rather than a particular circuit. The drawing figures are not to scale, and the same reference numerals are used to identify similar features.

[0009] At FIG. 1B, a hard mask 106 is formed over the substrate 100 of FIG. 1A. The hard mask is generally an inorganic anti-reflective coating (IARC) and may be silicon nitride

(SiN), silicon carbide (SiC), or other suitable material that does not react with underlying layers during processing. A photoresist layer 104 is formed over the hard mask 106 layer and opening 108 is patterned in the photoresist layer.

[0010] At FIG. 1C, the hard mask 106 and part of the STI 102 are etched according to photoresist pattern 108 to produce a trench 110 in the STI dielectric. Photoresist layer 104 is subsequently removed by a standard ash and clean process.

[0011] At FIG. 1D, conductive layer 112 is formed over the substrate 100 and in the trench 110 of FIG. 1C. The conductive layer 112 is preferably polycrystalline silicon and may be n-type, p-type, or undoped.

[0012] At FIG. 1E, the surface of substrate 100 is planarized by standard chemical mechanical polishing (CMP) to remove a portion of conductive layer 112 and hard mask layer 106. Alternatively, the portion of conductive layer 112 and hard mask layer 106 may be removed by a standard plasma etch process. Thus, a portion 114 of conductive layer 112 remains in the STI trench and will to serve as the e-fuse material or resistor as will be explained in detail.

[0013] At FIG. 1F, an NMOS transistor is formed at a face of substrate 100 within the p-well region. The NMOS transistor includes a sacrificial gate layer 116, sidewall spacers 118, and N⁺ source/drain regions 120. A PMOS transistor is also formed at the face of substrate 100 within the n-well region. The PMOS transistor includes the sacrificial gate layer 124, sidewall spacers 126, and P⁺ source/drain regions 122. A metal silicide layer such as titanium silicide, tantalum silicide, or platinum silicide may optionally be formed over source/drain regions 120, 122 and e-fuse/resistor layer 114.

[0014] At FIG. 1G, preplanarization layers 128 and 130 are preferably formed over substrate 100 of FIG. 1F by chemical vapor deposition (CVD), low pressure CVD (LPCVD), or plasma enhanced CVD (PECVD), for example. Layer 128 may be, for example, SiN, SiON, or SiC. Layer 130 is preferably deposited silicon dioxide.

[0015] At FIG. 1H, the substrate 100 is preferably planarized by CMP. Sacrificial gate layers 116 and 124 (FIG. 1F) are preferably removed by a wet etch or other suitable method that preserves the underlying gate dielectric. Here and in the following discussion it should

be understood that the NMOS and PMOS replacement gates may be processed simultaneously or separately to provide different metal replacement gates with different work functions. The NMOS transistor gate is formed by a first metal layer 132. Similarly, the PMOS transistor gate is formed by a second metal layer 134. As previously mentioned, layers 132 and 134 may be formed from the same or different metal layers and may comprise, for example, hafnium, zirconium, tungsten, titanium, tantalum, titanium nitride, titanium aluminum nitride, aluminum, platinum, or other suitable metal or metal alloy having a suitable work function.

[0016] Finally, at FIG. 1I, a first interlevel dielectric 136 is deposited over substrate 100. Vias 140 are formed for NMOS source/drain regions, vias 142 are formed for PMOS source/drain regions, and via 138 is formed for e-fuse/resistor region 114.

[0017] Referring now to FIGS. 2A through 2F there are diagrams of a simplified process flow according to a second embodiment of the invention. FIG. 2A illustrates a semiconductor substrate 200 having shallow trench isolation (STI) regions 202 as is well known in the art. The left half of the substrate is designated p-well as a bulk terminal for NMOS transistors. The right half of the substrate is designated n-well as a bulk terminal for PMOS transistors.

[0018] At FIG. 2B, a dielectric layer 207 is formed over substrate 200. The dielectric layer may be thermally grown silicon dioxide or a deposited high-k dielectric such as SiON or SiN. Here, high-k refers to a dielectric generally having a relative permittivity greater than 10. A hard mask 206 is formed over the dielectric layer 207 of FIG. 2A. The hard mask is generally an IARC layer as previously described. A photoresist layer 204 is formed over the hard mask 206 layer and opening 208 is patterned in the photoresist layer.

[0019] At FIG. 2C, the hard mask 206, dielectric layer 207, and part of the STI 202 are etched according to photoresist pattern 208 to produce a trench 210 in the STI dielectric. Photoresist layer 204 is subsequently removed by a standard ash and clean process.

[0020] At FIG. 2D, conductive layer 212 is formed over the dielectric layer 206 and in the trench 210 of FIG. 2C. The conductive layer 212 is preferably polycrystalline silicon and

may be n-type, p-type, or undoped. A photoresist layer is subsequently deposited and patterned to produce mask regions 211.

[0021] At FIG. 2E, substrate 200 is etched according to the mask pattern 211 to produce gate stack regions 216 and 224 and to produce e-fuse/resistor region 214 within trench 210. Photoresist layer 211 is subsequently removed by a standard ash and clean process.

[0022] At FIG. 2F, an NMOS transistor is formed at a face of substrate 200 within the p-well region. The NMOS transistor includes a conductive layer 216, sidewall spacers 218, and N⁺ source/drain regions 220. A PMOS transistor is also formed at the face of substrate 200 within the n-well region. The PMOS transistor includes the conductive layer 224, sidewall spacers 226, and P⁺ source/drain regions 222. A metal silicide layer such as titanium silicide, tantalum silicide, or platinum silicide may optionally be formed over source/drain regions 220, 222 and e-fuse/resistor layer 214.

[0023] After processing at FIG. 2F, substrate 200 is processed as previously described at FIGS. 1G through 1I. The previously described embodiments of the invention are highly advantageous over methods of the prior art for several reasons. First, no additional masks are required for either embodiment. A mask to form the e-fuse/resistor layer is added and a mask to form a copper or other e-fuse is removed from the process. Second, the e-fuse layer of the invention is much more flexible than copper e-fuses, since it may be formed of doped or undoped polycrystalline silicon and may be include a metal silicide layer, be fully silicided (FUSI) or be unsilicided. Third, the resistance and eutectic temperature may be adjusted to provide reliable programming at process compatible levels of voltage and current. Finally, the e-fuse/resistor layer may be formed partially or entirely over STI to avoid damage or shorting to nearby structures during programming.

[0024] Referring now to FIGS. 3A through 3H there are diagrams of a simplified process flow according to a third embodiment of the invention. FIG. 3A illustrates a semiconductor substrate 300 having shallow trench isolation (STI) regions 302 as is well known in the art. The left half of the substrate is designated p-well as a bulk terminal for n-channel metal oxide semiconductor (NMOS) transistors. The right half of the substrate is

designated n-well as a bulk terminal for p-channel metal oxide semiconductor (PMOS) transistors.

[0025] At FIG. 3B, a dielectric layer 307 is formed over substrate 300. The dielectric layer may be thermally grown silicon dioxide or a deposited high-k dielectric such as SiON or SiN. Here, high-k refers to a dielectric generally having a relative permittivity greater than 10. A conductive layer 312 is formed over the dielectric layer 307. The conductive layer 112 is preferably polycrystalline silicon and may be n-type, p-type, or undoped. A photoresist layer is formed and patterned over the conductive layer 312 layer to produce mask regions 304.

[0026] At FIG. 3C, substrate 300 is etched according to the mask pattern 304 to produce gate stack regions 316 and 324 and to produce e-fuse/resistor region 314. Photoresist regions 304 are subsequently removed by a standard ash and clean process.

[0027] At FIG. 3D, an NMOS transistor is formed at a face of substrate 300 within the p-well region. The NMOS transistor includes a conductive layer 316, sidewall spacers 318, and N⁺ source/drain regions 320. A PMOS transistor is also formed at the face of substrate 200 within the n-well region. The PMOS transistor includes the conductive layer 324, sidewall spacers 326, and P⁺ source/drain regions 322. Sidewall spacers are also formed adjacent e-fuse/resistor region 314. A metal silicide layer such as titanium silicide, tantalum silicide, or platinum silicide may optionally be formed over source/drain regions 320 and 322.

[0028] At FIG. 3E, preplanarization layers 328 and 330 are preferably formed over substrate 300 of FIG. 3D by chemical vapor deposition (CVD), low pressure CVD (LPCVD), or plasma enhanced CVD (PECVD), for example. Layer 328 may be, for example, SiN, SiON, or SiC. Layer 330 is preferably deposited silicon dioxide.

[0029] At FIG. 3F, the substrate 300 is preferably planarized by CMP. In this embodiment, where NMOS and PMOS gates are separately replaced, a photoresist layer is deposited and patterned to produce mask layer 340. Here and in the following discussion it should be understood that the order of separate gate replacement is optional. Mask layer 340 covers the NMOS transistor and the e-fuse/resistor layer 314. Conductive gate layer 324

(FIG. 3D) is preferably removed by a wet etch or other suitable method that preserves the underlying gate dielectric. The PMOS transistor gate is then formed by a metal layer that is etched back to produce metal gate 334.

[0030] At FIG. 3G, a photoresist layer is deposited and patterned to produce mask layer 342. Mask layer 342 covers the PMOS transistor and the e-fuse/resistor layer 314. Conductive gate layer 316 (FIG. 3D) is preferably removed by a wet etch or other suitable method that preserves the underlying gate dielectric. The NMOS transistor gate is then formed by a metal layer that is etched back to produce metal gate 332. Here, metal gate layers 332 and 334 may comprise, for example, hafnium, zirconium, tungsten, titanium, tantalum, titanium nitride, titanium aluminum nitride, aluminum, platinum, or other suitable metal or metal alloy having a suitable work function.

[0031] Finally, at FIG. 3H, photoresist layer 304 is subsequently removed by a standard ash and clean process. A metal silicide may optionally be formed over region 314 by metal deposition and anneal as is well known in the art. No additional mask is required, since the metal will not react with dielectric layers 328 and 330 or with metal gates 332 and 334. A first interlevel dielectric 336 is deposited over substrate 300. Vias 340 are formed for NMOS source/drain regions, vias 342 are formed for PMOS source/drain regions, and via 338 is formed for e-fuse/resistor region 314. In addition to the previously mentioned advantages of the invention, this embodiment advantageously eliminates a mask to form a copper or other e-fuse from the process. No additional masks are required.

[0032] Those skilled in the art will appreciate that modifications may be made to the described examples, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. A method of fabricating an integrated circuit, comprising:
providing a substrate having an isolation region;
etching a trench in the isolation region;
forming a first conductive layer within the trench;
forming a first transistor having a first conductivity type at a face of the substrate, the first transistor having a gate formed of a sacrificial gate layer;
forming a second transistor having a second conductivity type at the face of the substrate, the second transistor having a gate formed of the sacrificial gate layer;
replacing the sacrificial gate layer of the first transistor with a first metal gate; and
replacing the sacrificial gate layer of the second transistor with a second metal gate.
2. A method as in claim 1, comprising forming a metal silicide layer on the first conductive layer.
3. A method as in claim 1, comprising:
forming a first source/drain region of the first transistor;
forming a metal silicide layer on the first source/drain region;
forming a second source/drain region of the second transistor; and
forming a metal silicide layer on the second source/drain region.
4. A method as in claim 1, wherein the first metal gate comprises a different material than the second metal gate.
5. A method as in claim 1, wherein the first transistor is an n-channel metal oxide semiconductor (NMOS) transistor, and wherein the first metal gate comprises TiAlN.

6. A method as in claim 1, wherein the second transistor is a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the second metal gate comprises TiN.
7. A method as in claim 1, wherein the first conductive layer within the trench comprises an e-fuse.
8. A method as in claim 1, wherein the first conductive layer within the trench comprises a resistor.
9. A method of fabricating an integrated circuit, comprising:
 - providing a substrate having an isolation region;
 - etching a trench in the isolation region;
 - forming a first conductive layer within the trench;
 - forming a first transistor having a first conductivity type at a face of the substrate, the first transistor having a gate formed of the first conductive layer;
 - forming a second transistor having a second conductivity type at the face of the substrate, the second transistor having a gate formed of the first conductive layer;
 - replacing the first conductive layer of the first transistor with a first metal gate; and
 - replacing the first conductive layer of the second transistor with a second metal gate.
10. A method as in claim 9, comprising forming a metal silicide layer on the first conductive layer within the trench.
11. A method as in claim 9, comprising:
 - forming a first source/drain region of the first transistor;
 - forming a metal silicide layer on the first source/drain region;
 - forming a second source/drain region of the second transistor; and
 - forming a metal silicide layer on the second source/drain region.

12. A method as in claim 9, wherein the first metal gate comprises a different material than the second metal gate.
13. A method as in claim 9, wherein the first transistor is an n-channel metal oxide semiconductor (NMOS) transistor, and wherein the first metal gate comprises TiAlN.
14. A method as in claim 9, wherein the second transistor is a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the second metal gate comprises TiN.
15. A method as in claim 9, wherein the first conductive layer within the trench comprises an e-fuse.
16. A method as in claim 9, wherein the first conductive layer within the trench comprises a resistor.
17. A method of fabricating an integrated circuit, comprising:
providing a substrate having an isolation region;
forming a dielectric layer at a face of the substrate;
forming a first conductive layer over the dielectric layer;
forming a first transistor having a first conductivity type at a face of the substrate, the first transistor having a gate formed of the first conductive layer;
forming a patterned layer from the first conductive layer over the isolation region;
forming a second transistor having a second conductivity type at the face of the substrate, the second transistor having a gate formed of the first conductive layer;
forming a first masking layer over the first transistor and the patterned layer;
replacing the first conductive layer of the second transistor with a second metal gate;
forming a second masking layer over the second transistor and the patterned layer;
and
replacing the first conductive layer of the first transistor with a first metal gate.

18. A method as in claim 17, wherein the first transistor is an n-channel metal oxide semiconductor (NMOS) transistor, and wherein the first metal gate comprises TiAlN.
19. A method as in claim 17, wherein the second transistor is a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the second metal gate comprises TiN.
20. A method as in claim 17, wherein the patterned layer comprises one of an e-fuse and a resistor.

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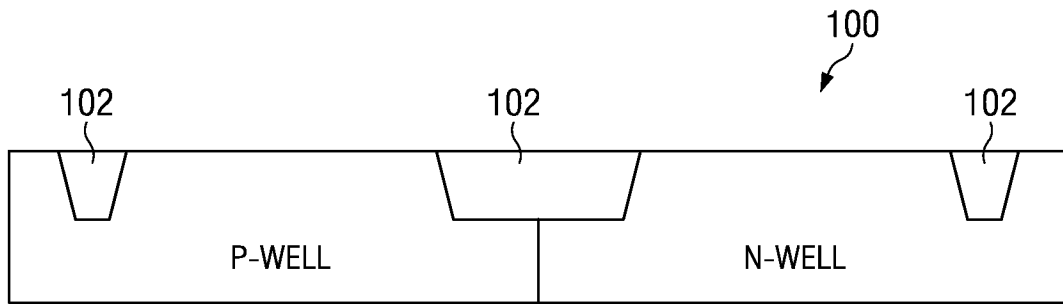


FIG. 1A

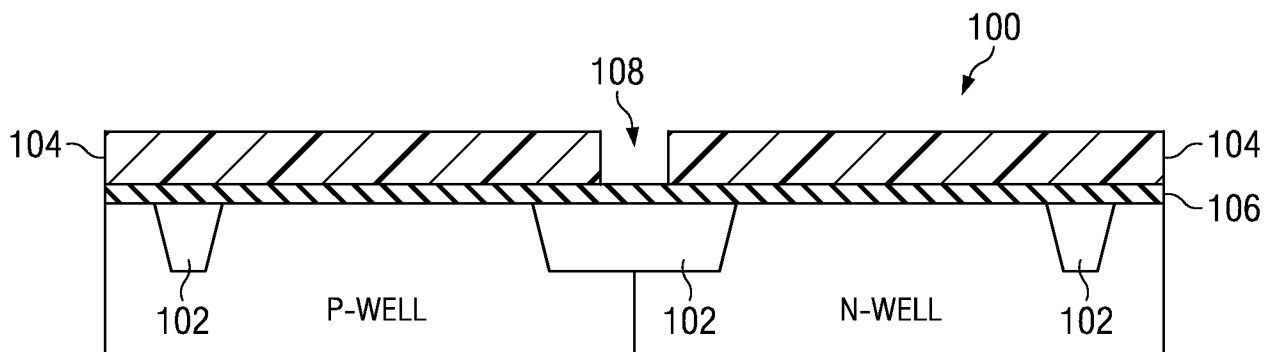


FIG. 1B

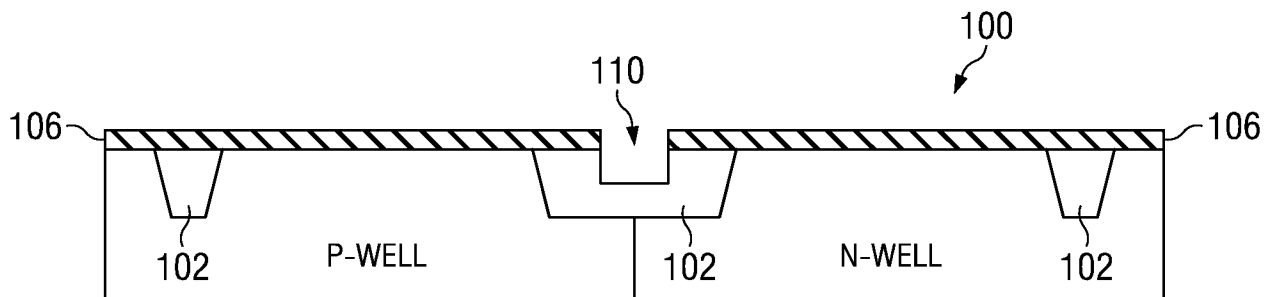


FIG. 1C

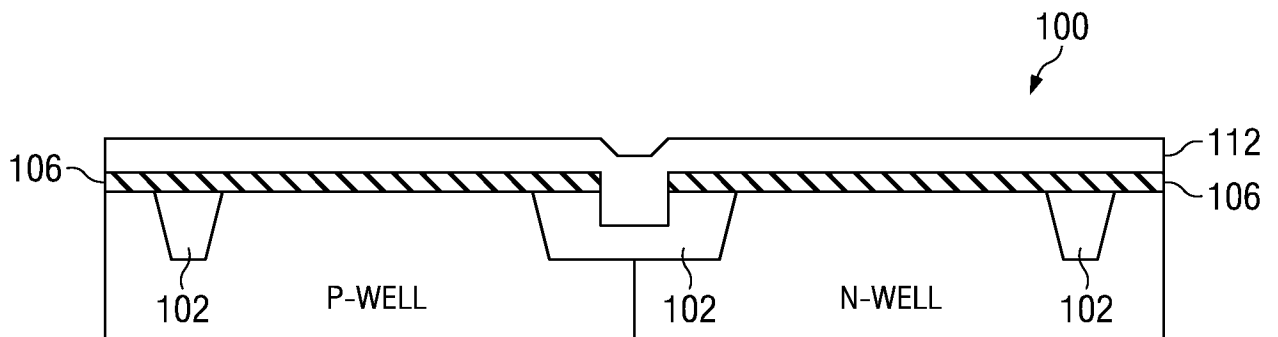


FIG. 1D

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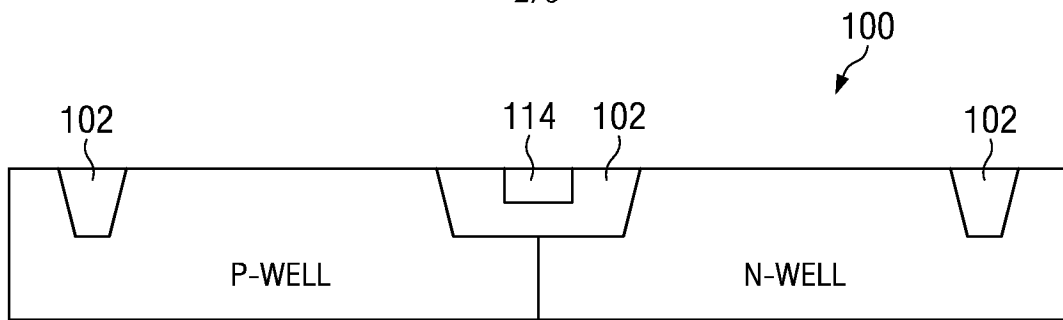


FIG. 1E

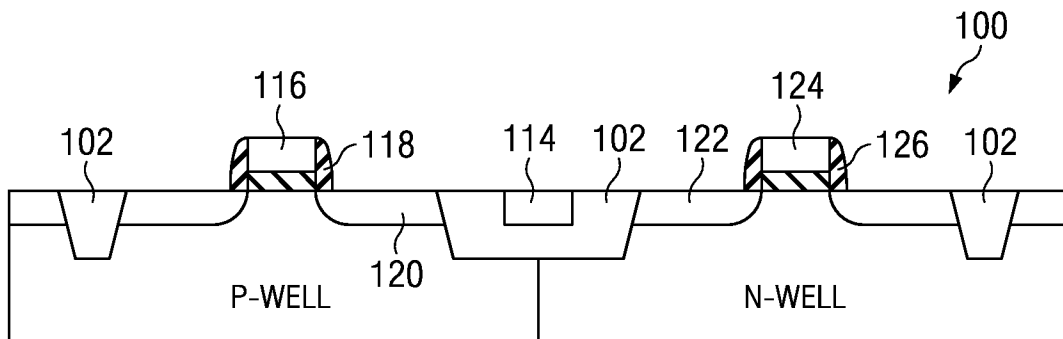


FIG. 1F

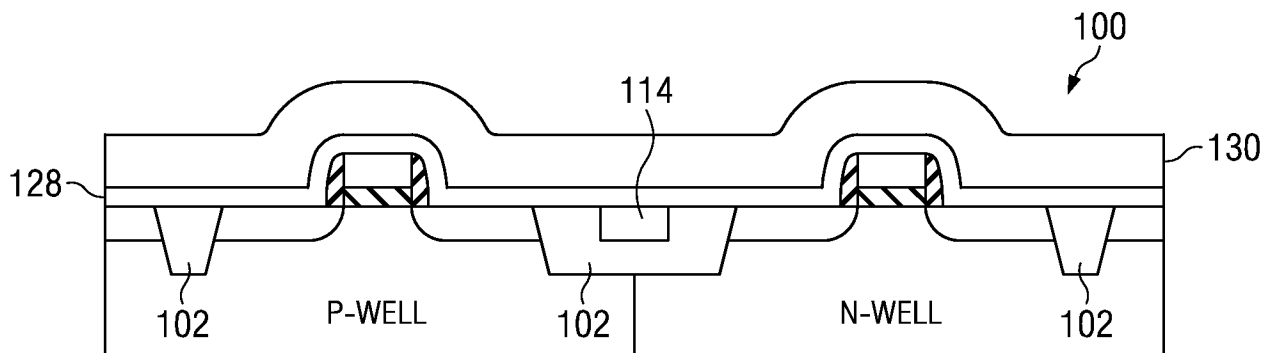


FIG. 1G

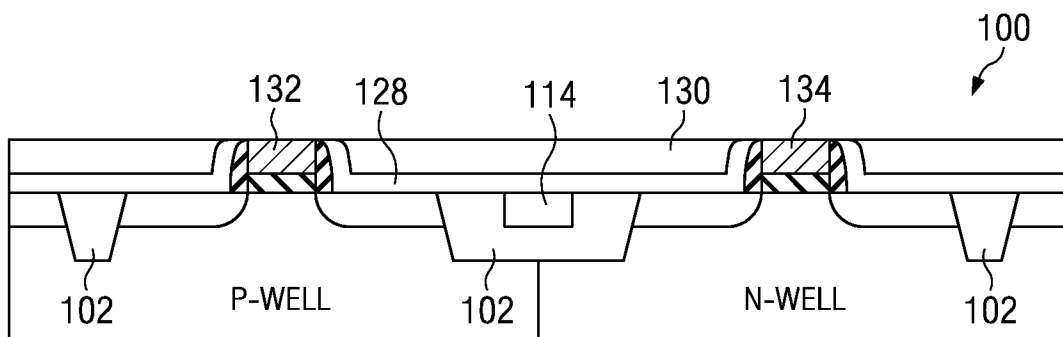


FIG. 1H

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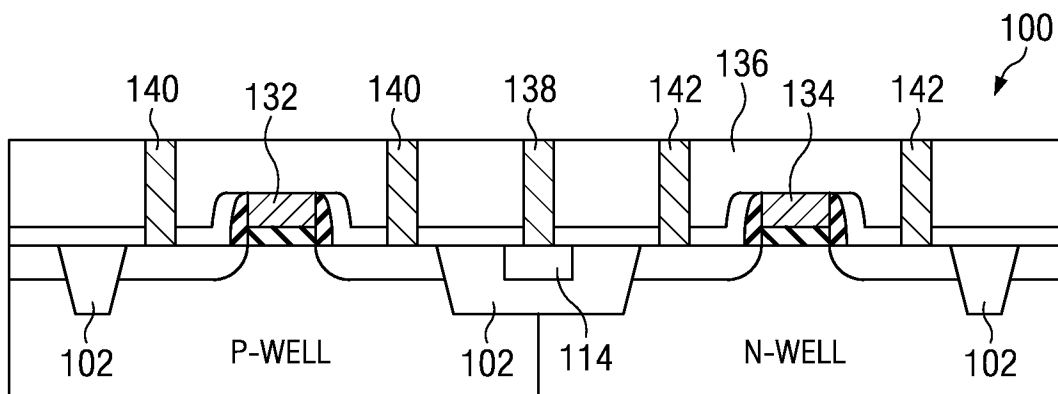


FIG. 1I

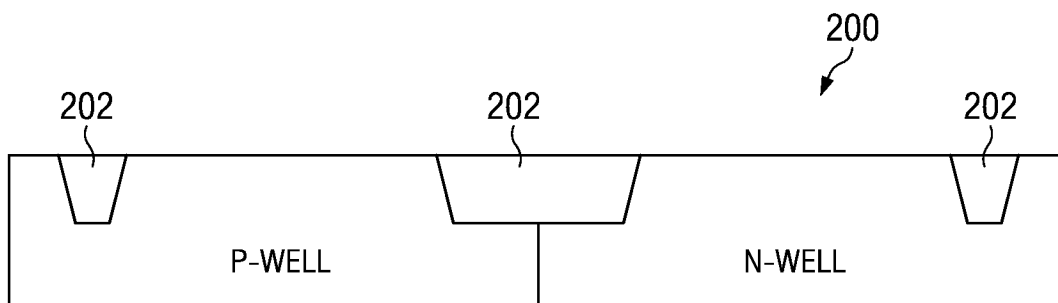


FIG. 2A

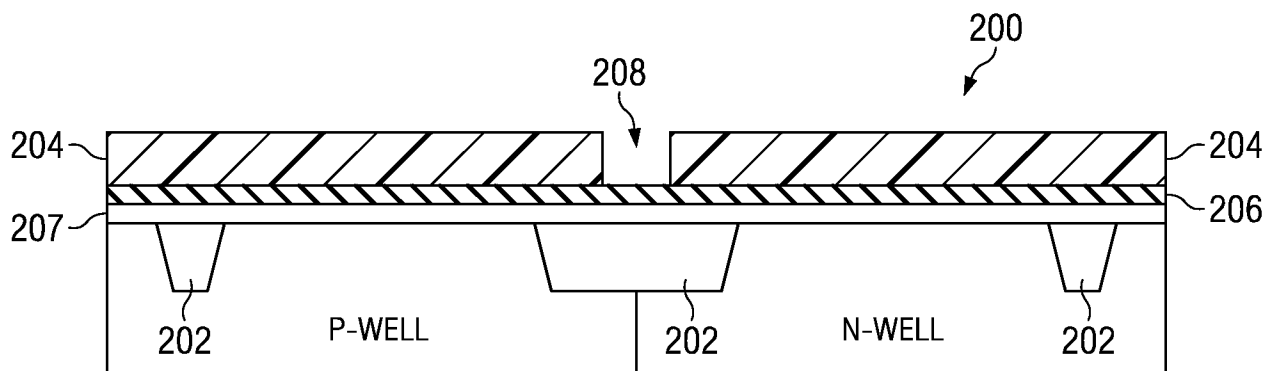


FIG. 2B

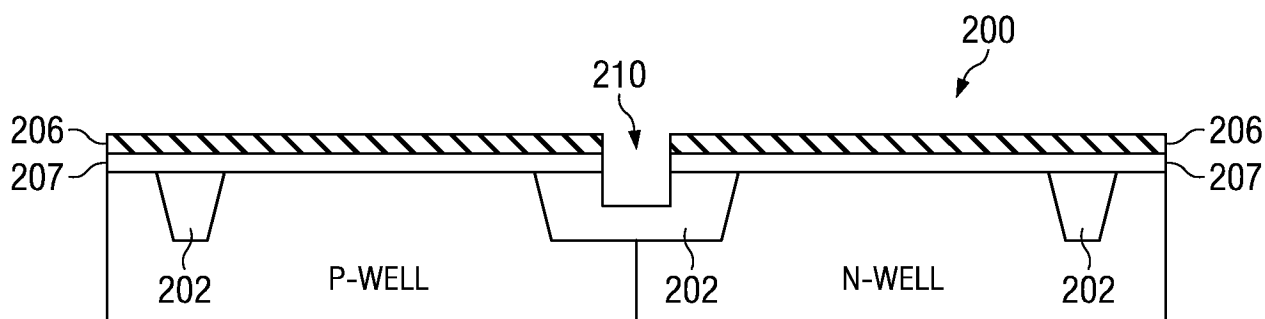


FIG. 2C

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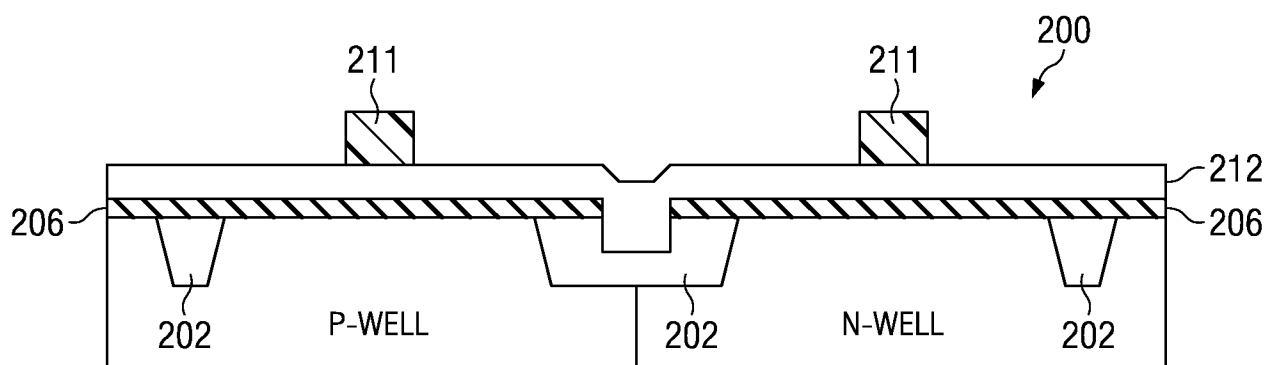


FIG. 2D

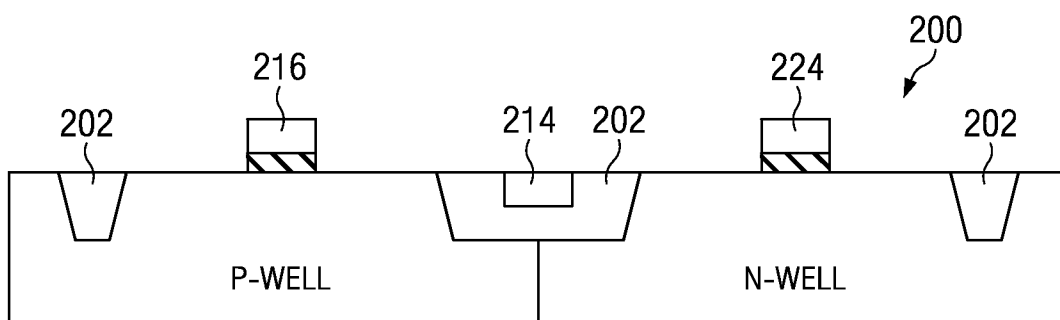


FIG. 2E

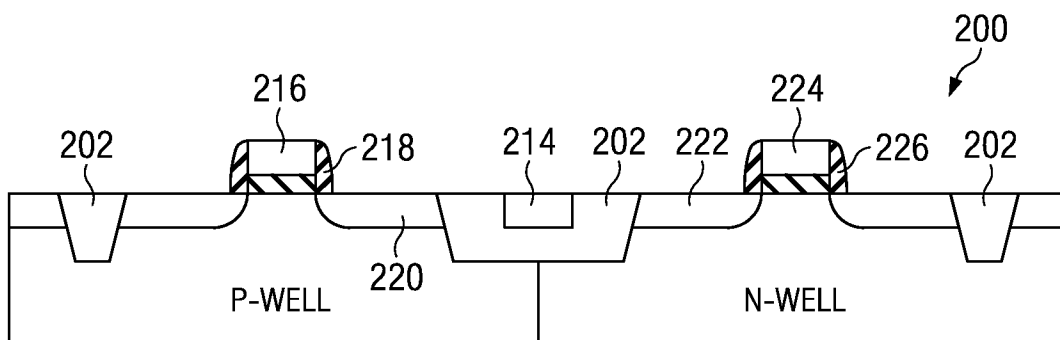


FIG. 2F

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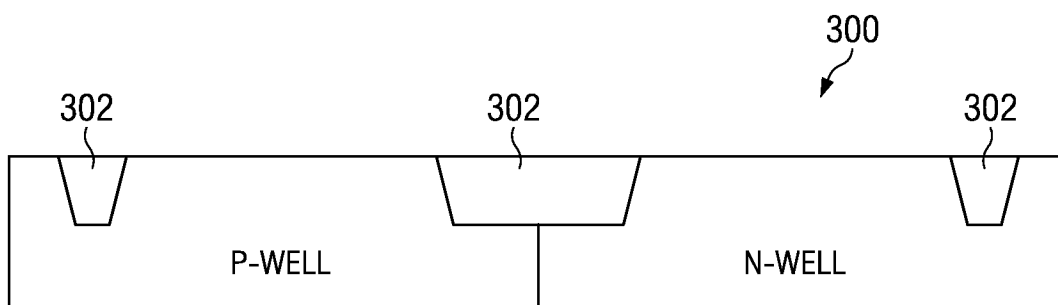


FIG. 3A

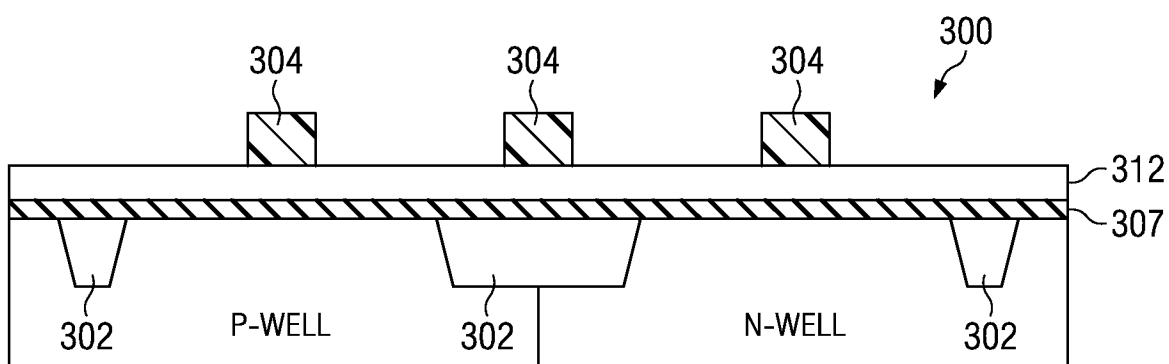


FIG. 3B

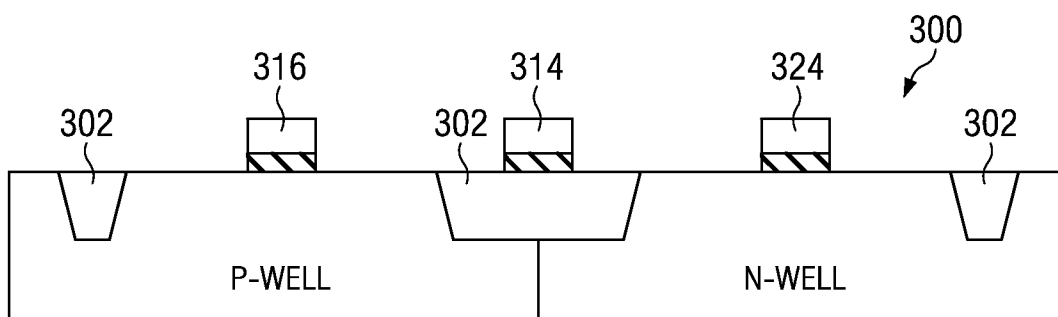


FIG. 3C

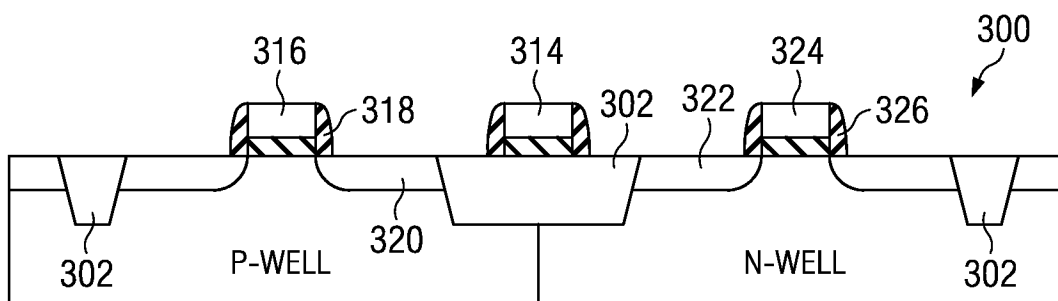


FIG. 3D

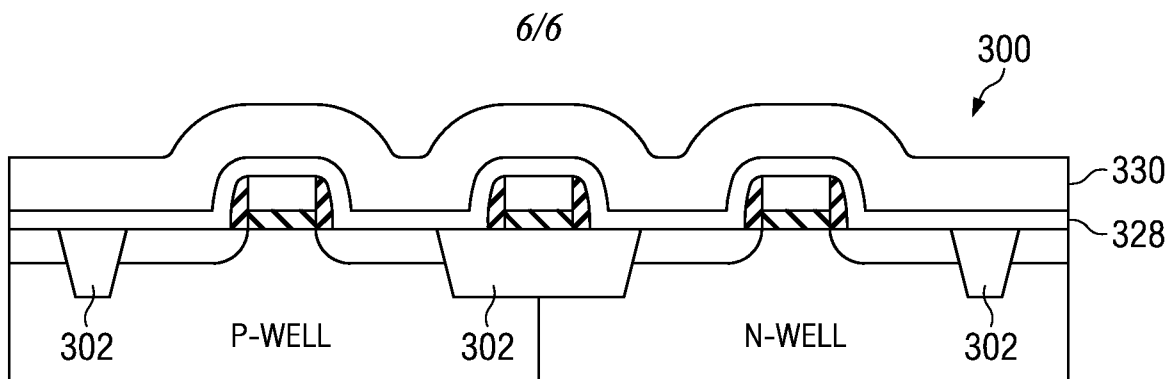


FIG. 3E

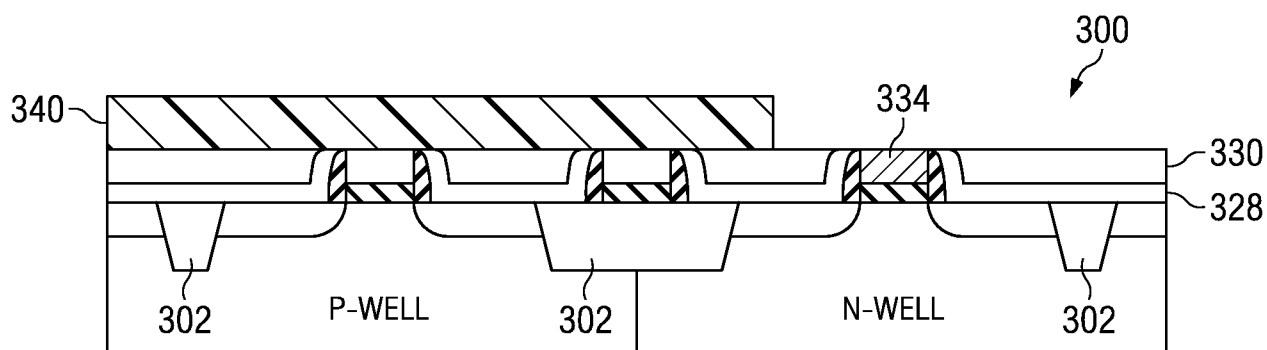


FIG. 3F

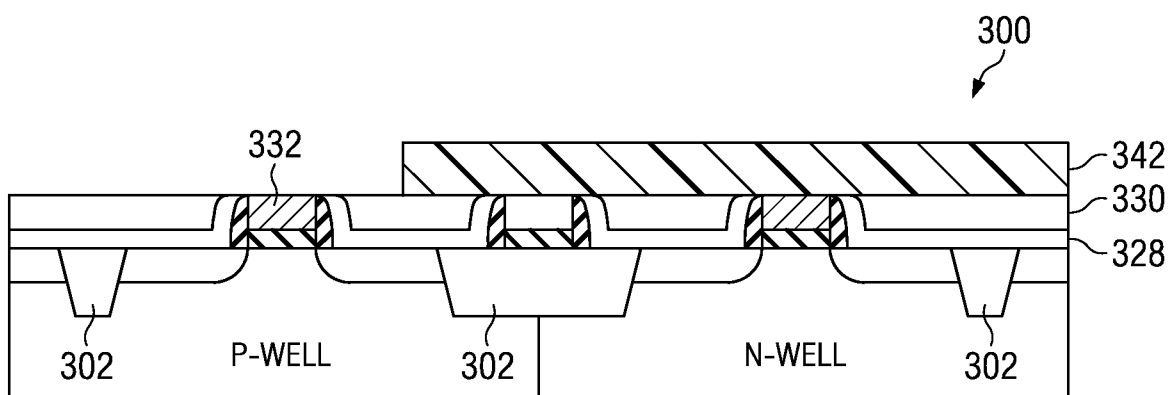


FIG. 3G

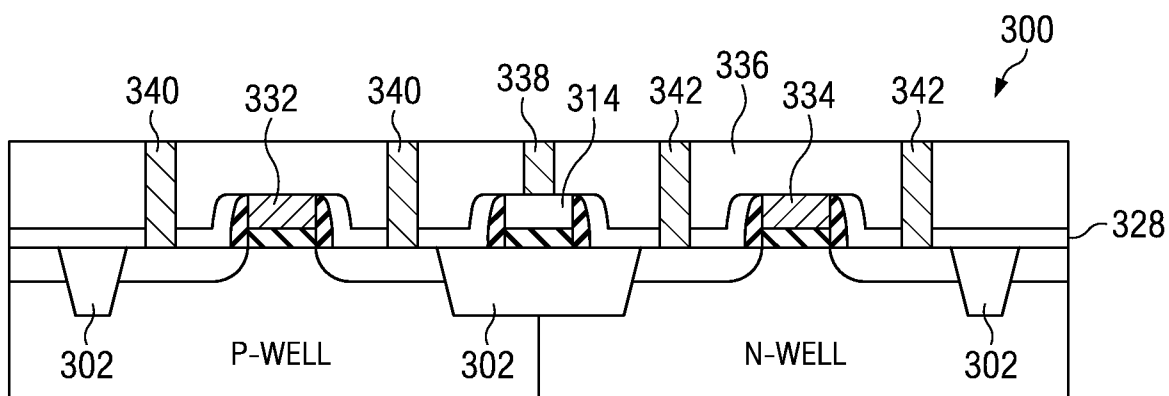


FIG. 3H

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/049736**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/82(2006.01)i, H01L 21/336(2006.01)i, H01L 29/78(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/82; H01L 29/00; H01L 27/06; H01L 29/78; H01L 21/02; H01L 21/8238; H01L 27/10; H01L 23/525; H01L 21/336

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:Fuse, STI, silicide, resist, sacrifice, dummy

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010-0059823 A1 (SHENG-CHEN CHUNG et al.) 11 March 2010 See abstract, paragraphs [0015]-[0018], [0037] and figures 2A-2F.	1,4-8
Y		3
A		2,9-20
Y	US 2007-0145519 A1 (YUAN-CHING PENG et al.) 28 June 2007 See abstract, paragraph [0023] and figure 6.	3
A	US 2010-0019344 A1 (HARRY CHUANG et al.) 28 January 2010 See abstract, paragraph [0032] and figure 6B.	1-20
A	US 6727133 B1 (GREG C. BALDWIN) 27 April 2004 See abstract, claim 1 and figures 1a-1e.	1-20
A	KR 10-2001-0038445 A (ANAM SEMICONDUCTOR., LTD.) 15 May 2001 See abstract, claim 1 and figures 1-2c.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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Date of the actual completion of the international search

21 October 2013 (21.10.2013)

Date of mailing of the international search report

22 October 2013 (22.10.2013)

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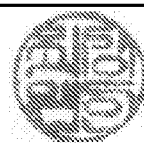
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/049736

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