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(54) **SEMICONDUCTOR PACKAGE AND METHOD FOR MANUFACTURING THE SAME**

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(52) **U.S. Cl.** **257/693; 257/E23**

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(57) **ABSTRACT**

A semiconductor package comprises a chip, a plurality of pad extension traces, a plurality of via holes, a lid and a plurality of metal traces, wherein the chip has an active surface, a back surface opposite to the active surface, an optical component disposed on the active surface, and a plurality of pads disposed on the active surface and electrically connected to the optical component; the pad extension traces are electrically connected to the pads; the via holes are formed through the chip and electrically connected to the pad extension traces; the lid is attached on the active surface of the chip; and the plurality of metal traces are disposed on the back surface of the chip, electrically connected to the plurality of via holes, and defines a plurality of solder pads thereon.

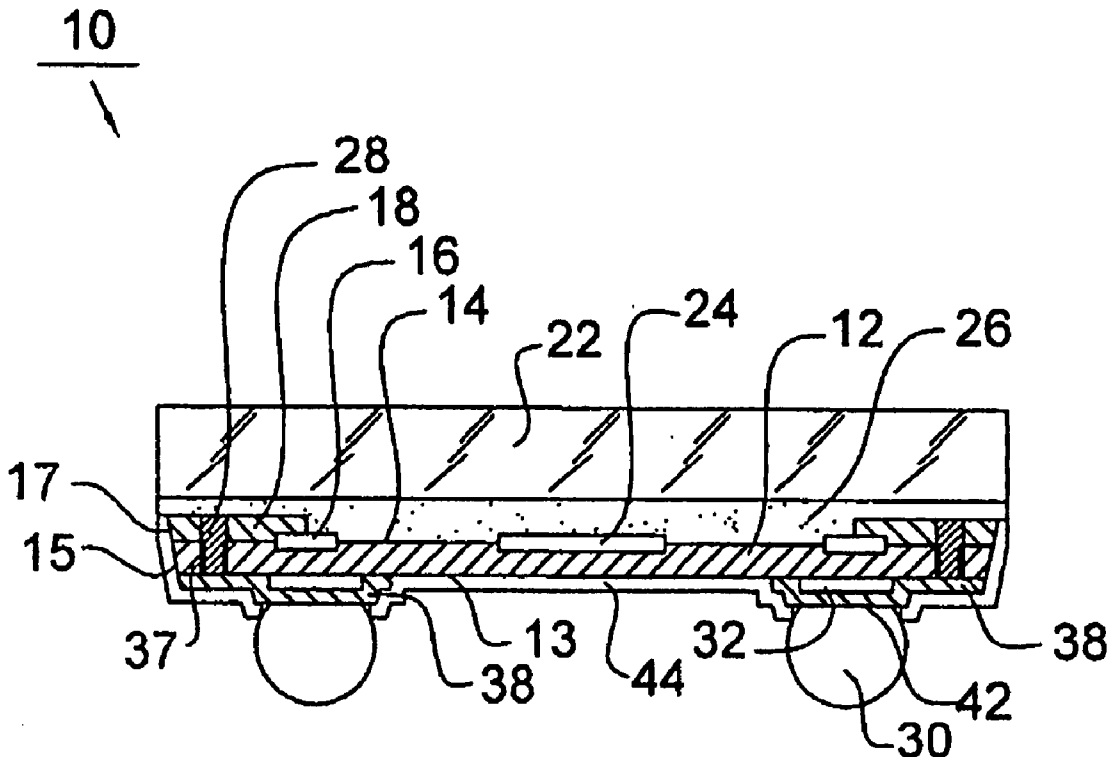
(73) Assignee: **Advanced Semiconductor Engineering, Inc.**

(21) Appl. No.: **11/898,744**

(22) Filed: **Sep. 14, 2007**

Related U.S. Application Data

(62) Division of application No. 11/074,796, filed on Mar. 9, 2005, now Pat. No. 7,285,434.



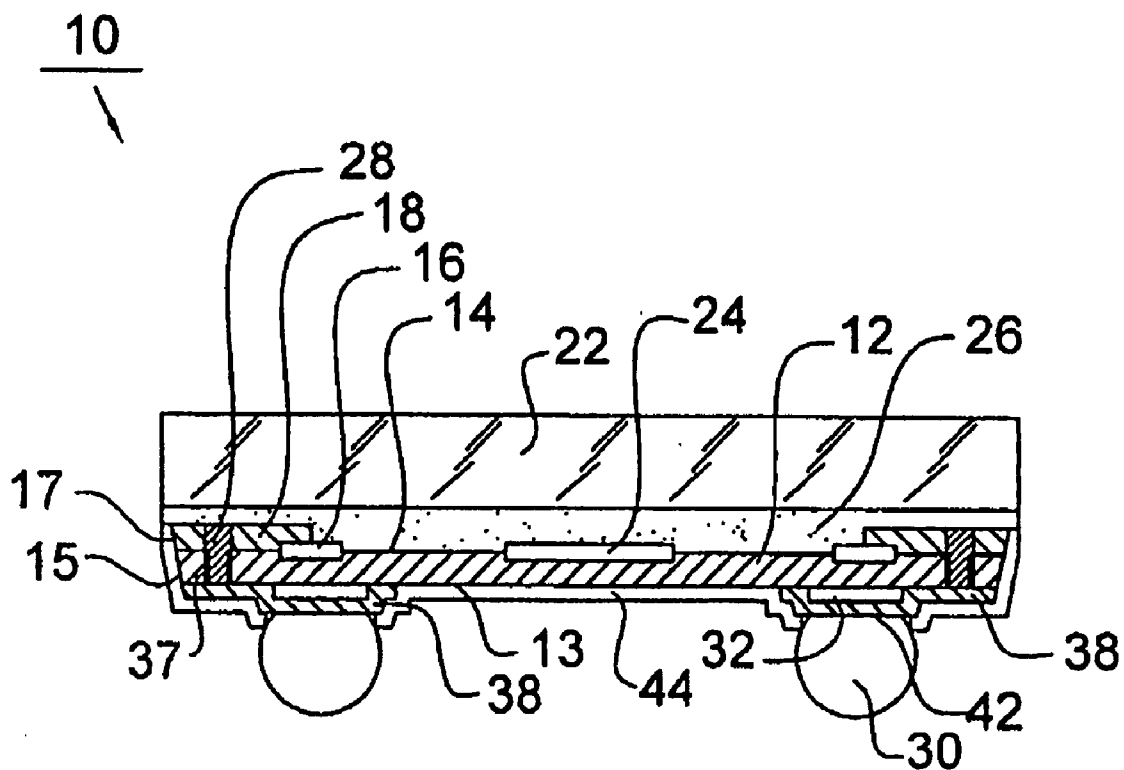


FIG. 1

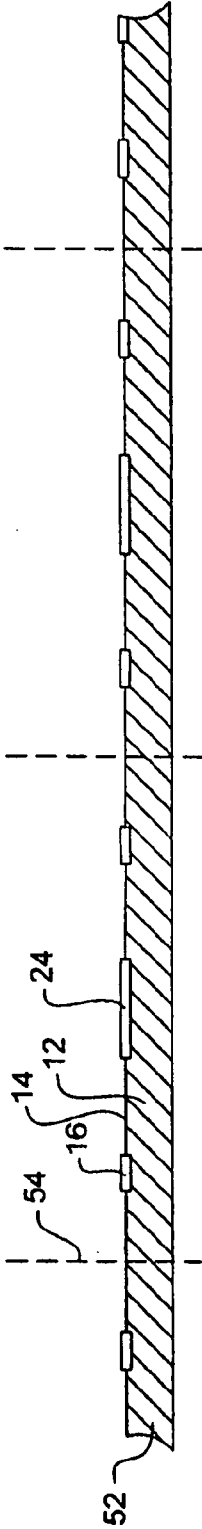


FIG. 2

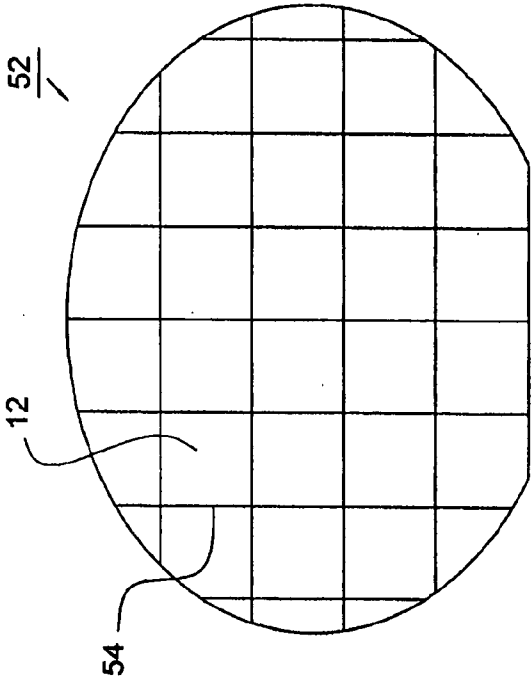


FIG. 3

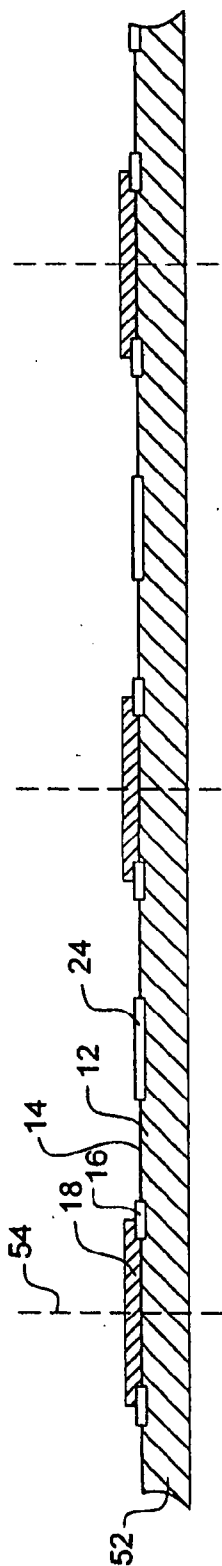


FIG. 4

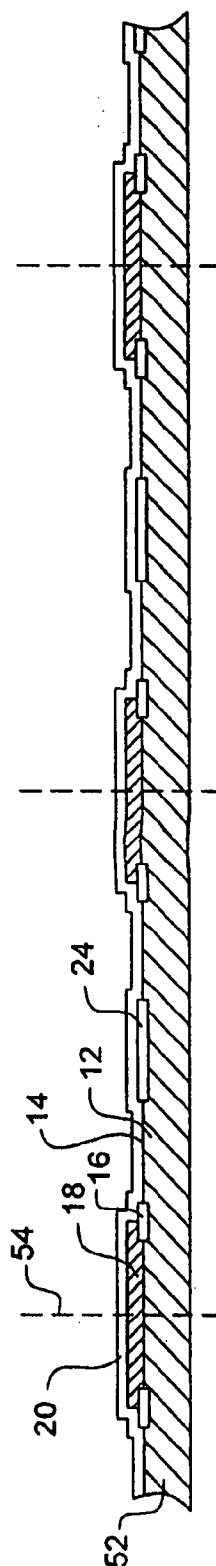


FIG. 5

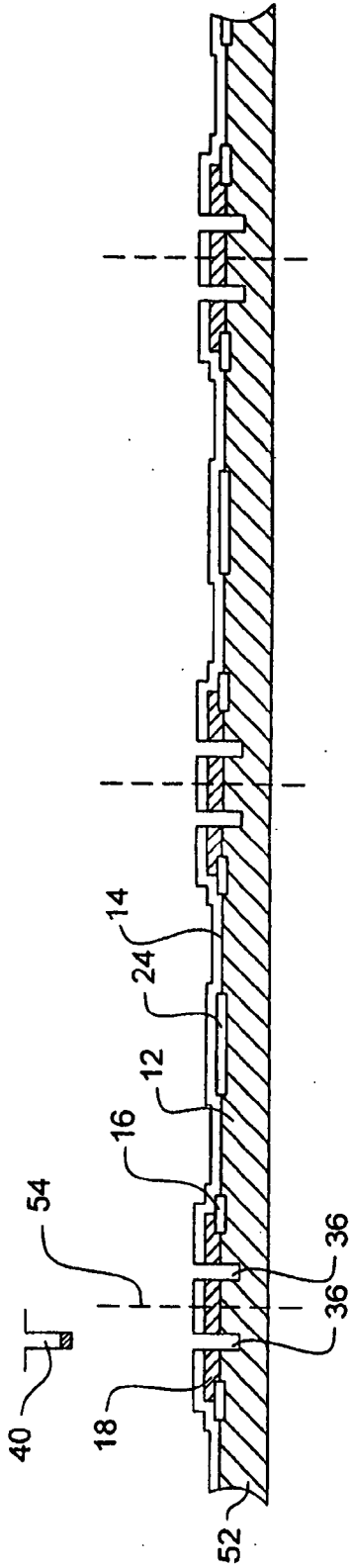


FIG. 6

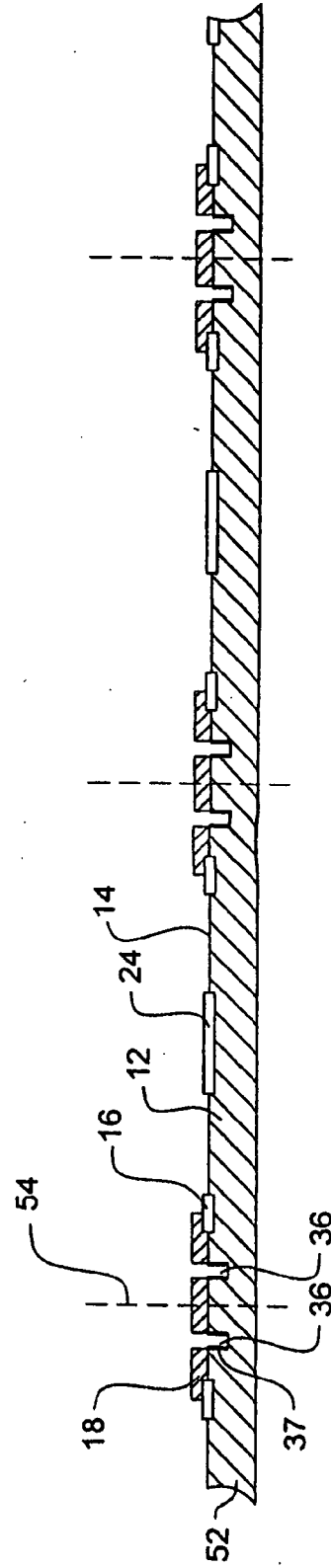


FIG. 7

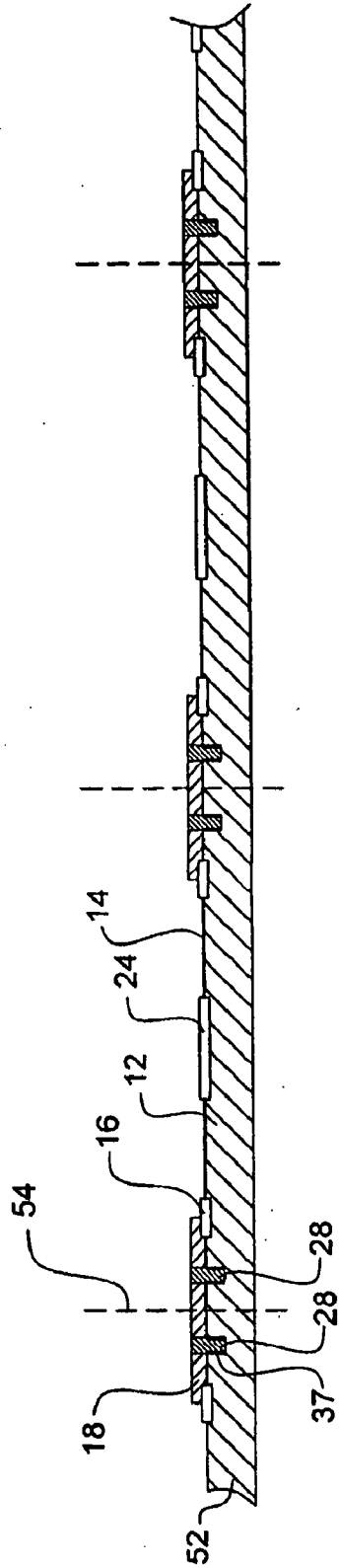


FIG. 8

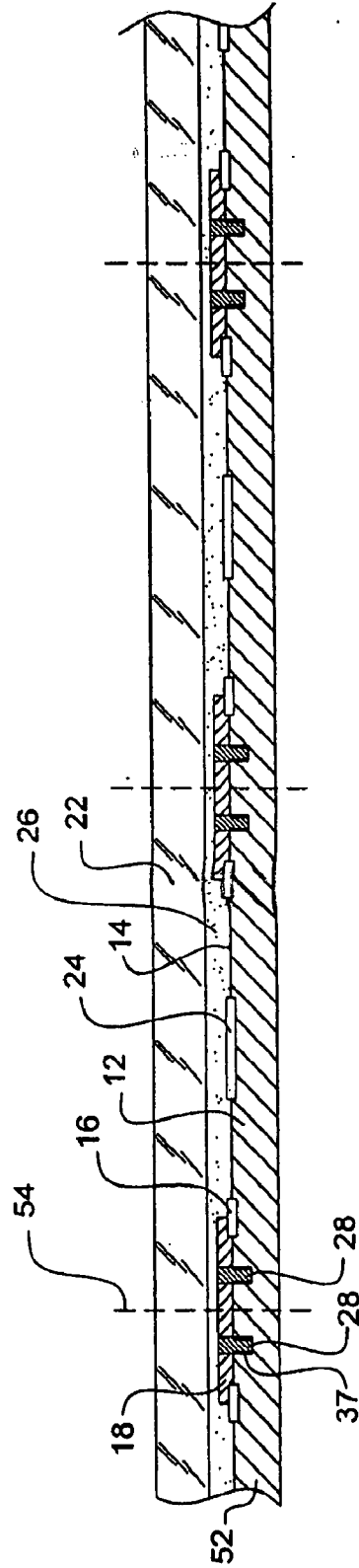


FIG. 9

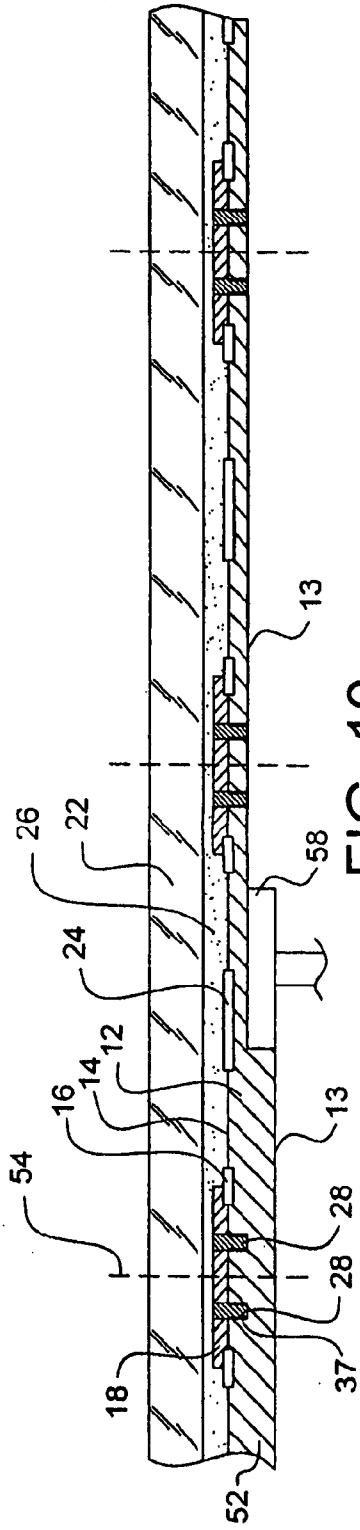


FIG. 10

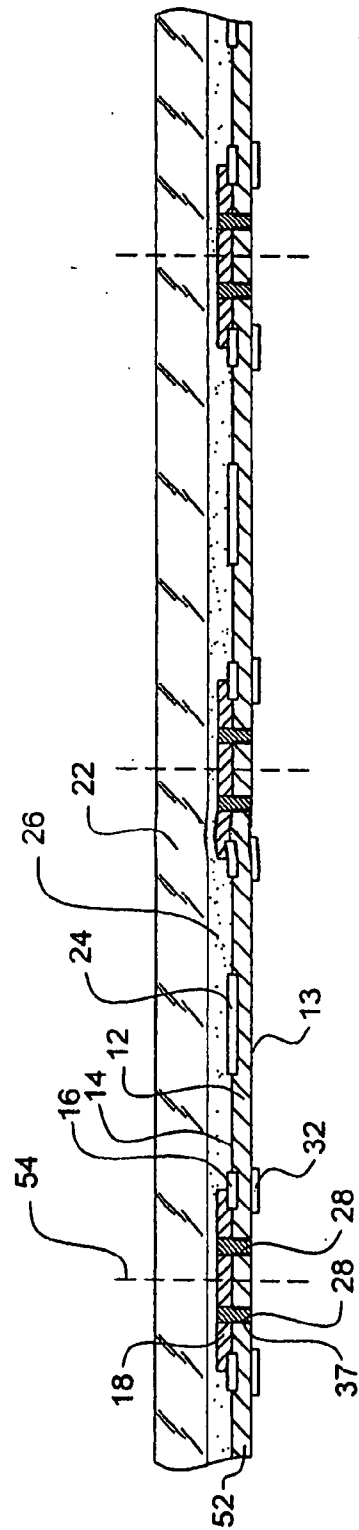


FIG. 11

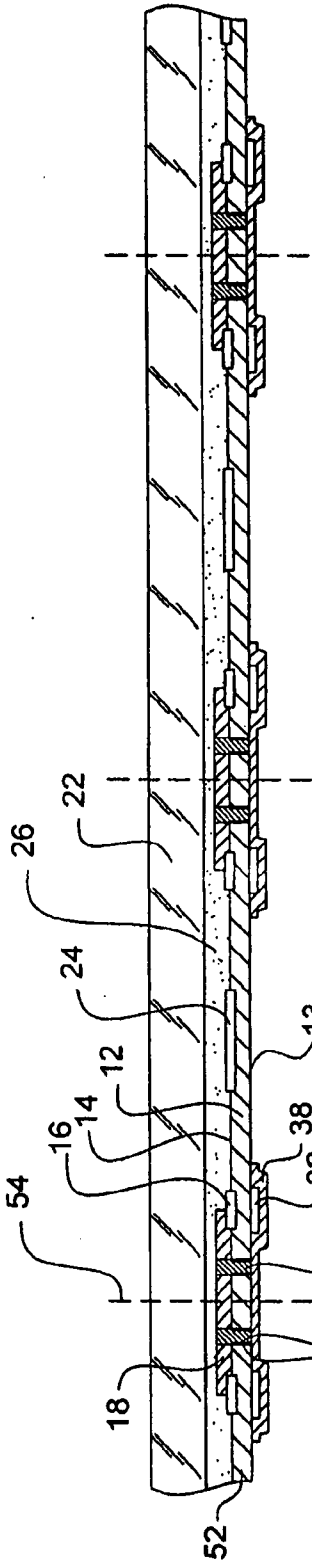


FIG. 12

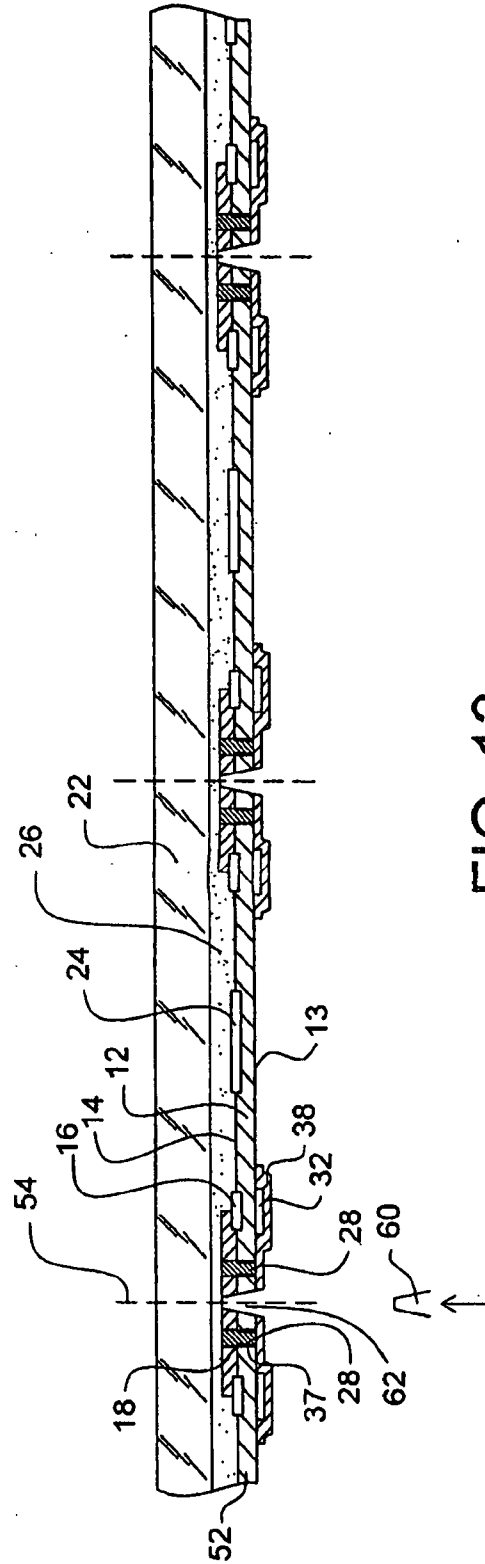


FIG. 13

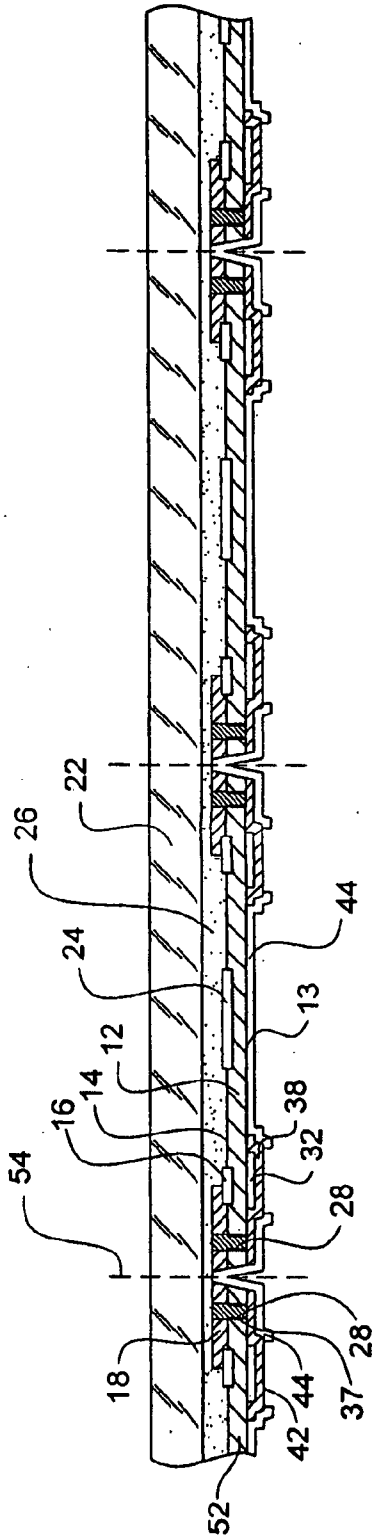


FIG. 14

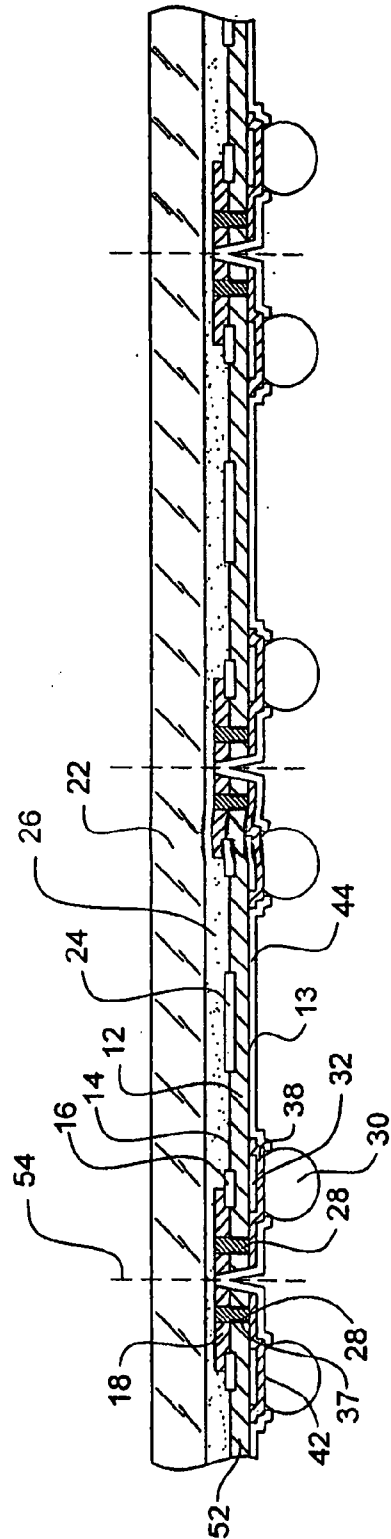


FIG. 15

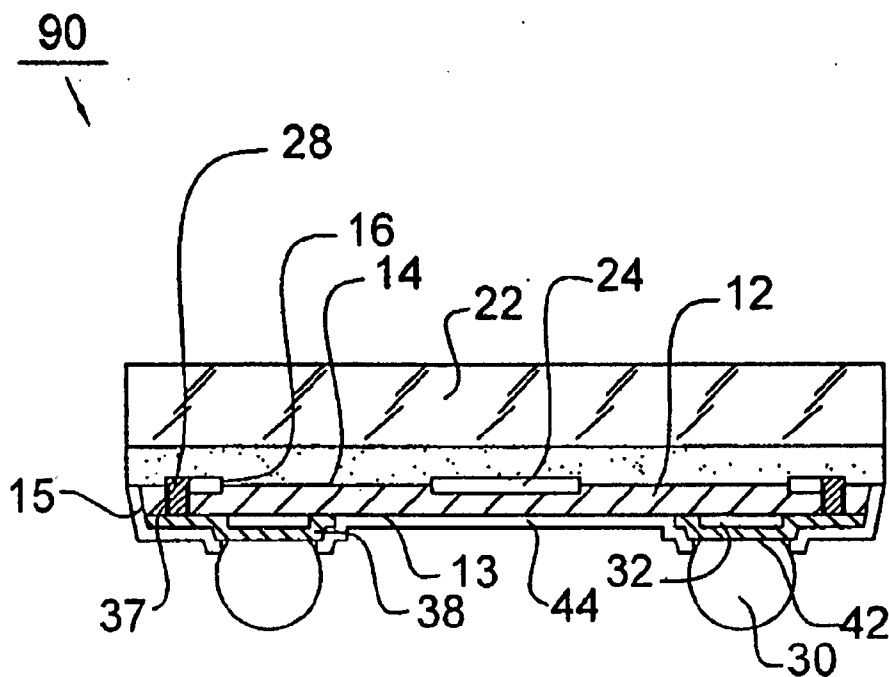


FIG. 16

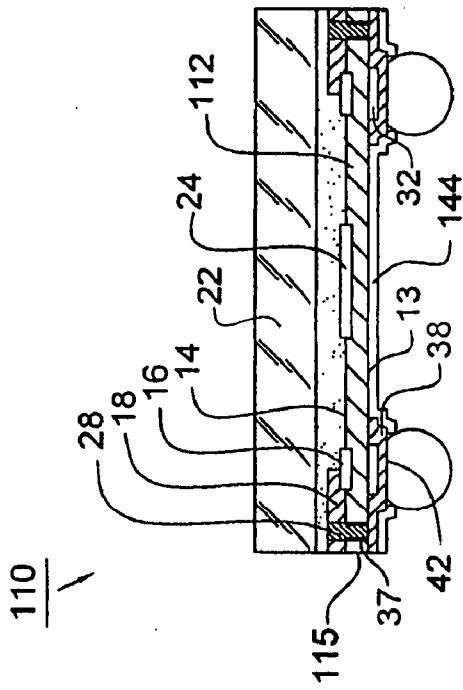


FIG. 17

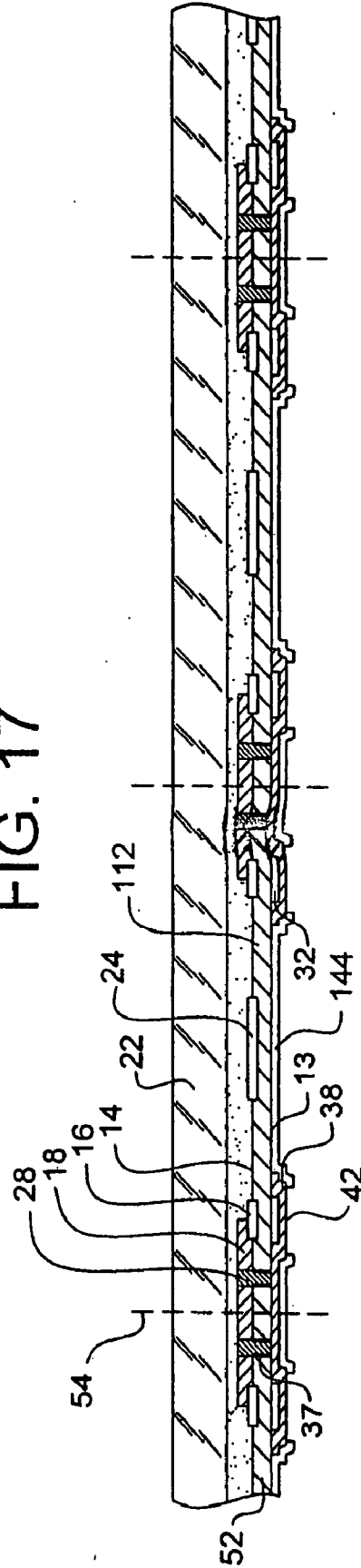


FIG. 18

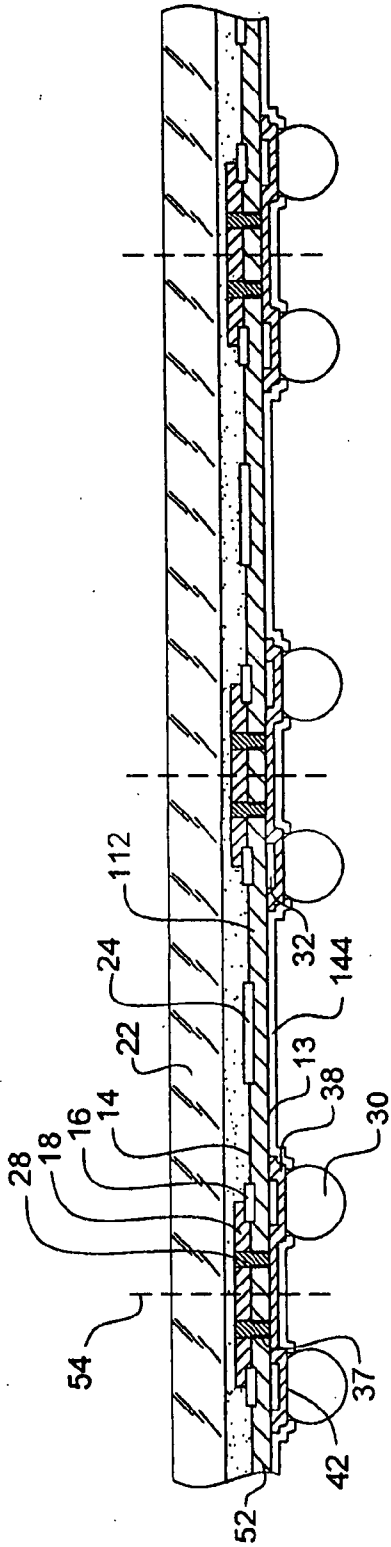


FIG. 19

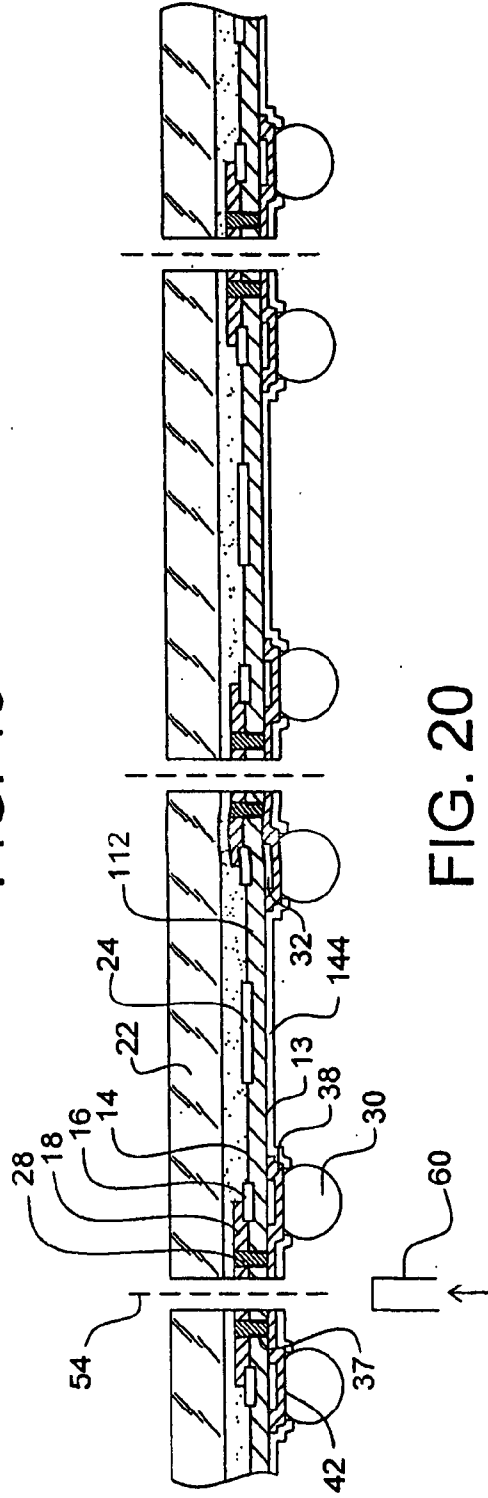


FIG. 20

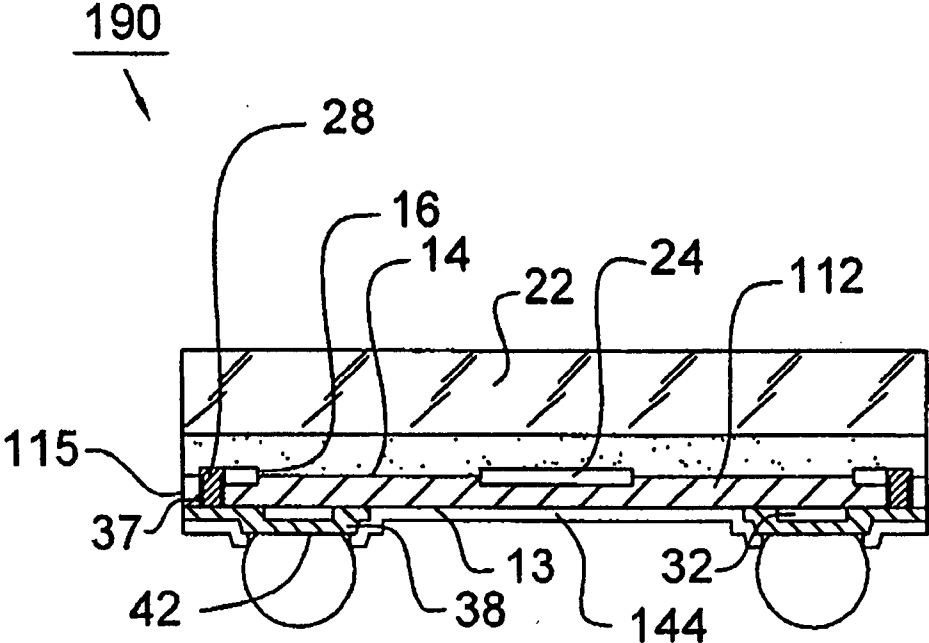


FIG. 21

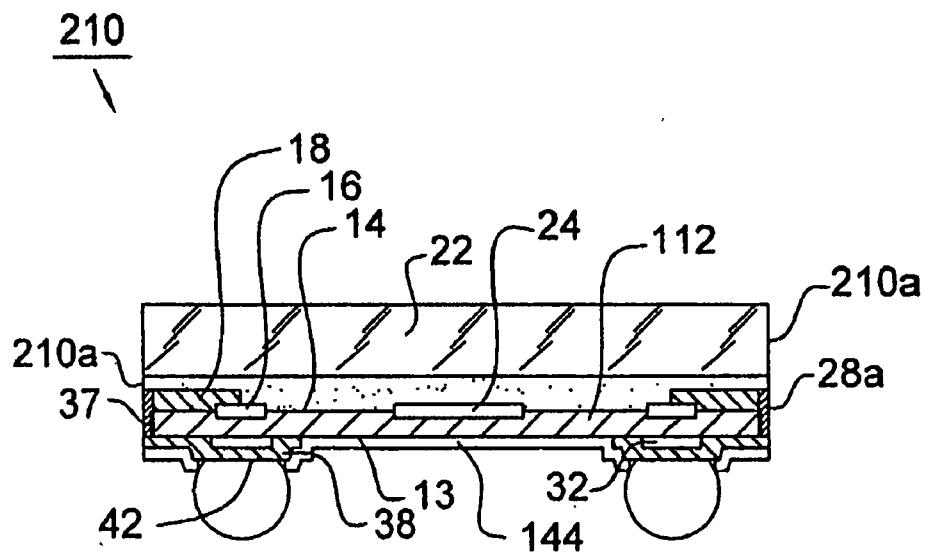


FIG. 22

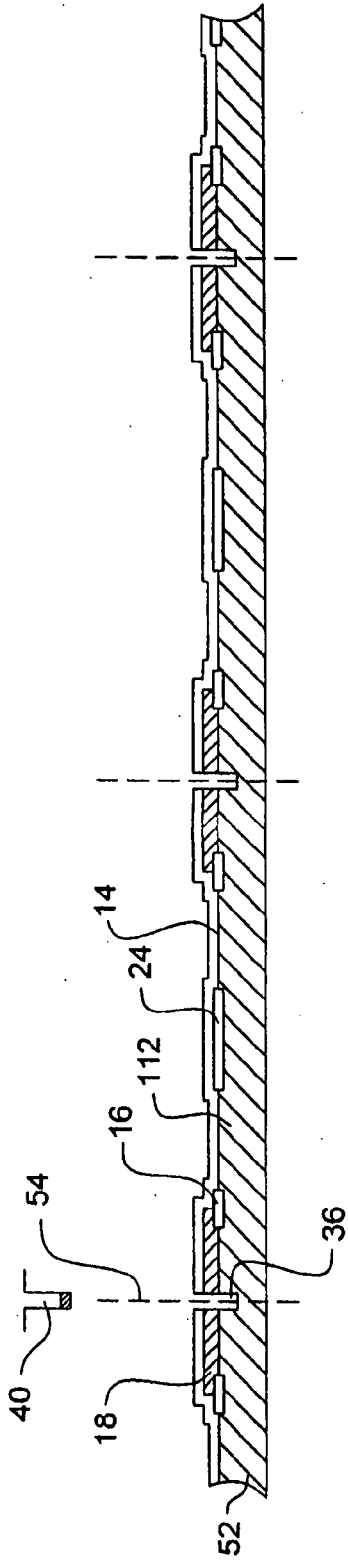


FIG. 23

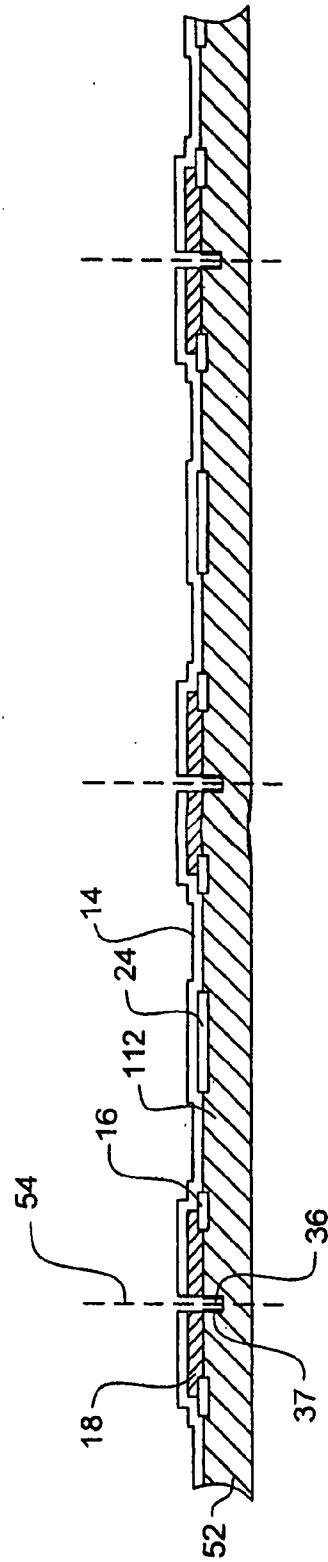


FIG. 24

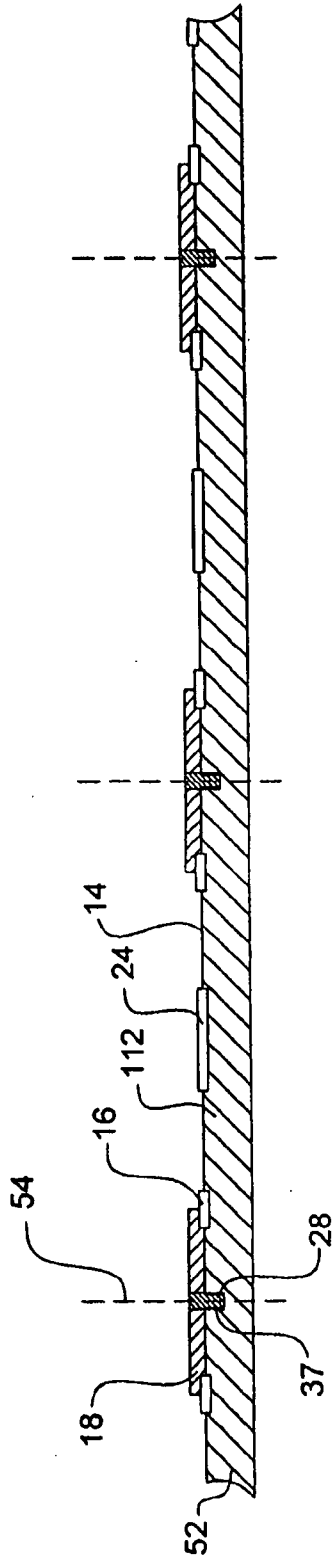


FIG. 25

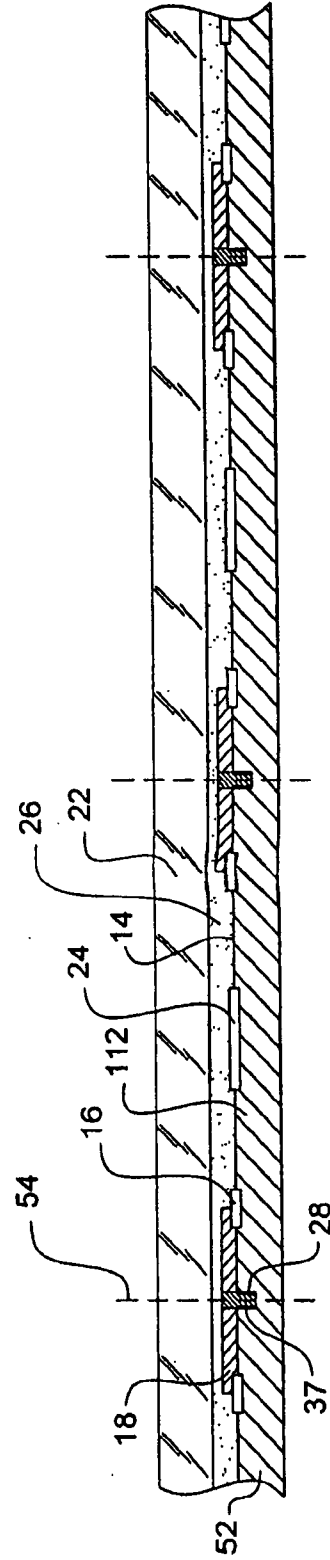


FIG. 26

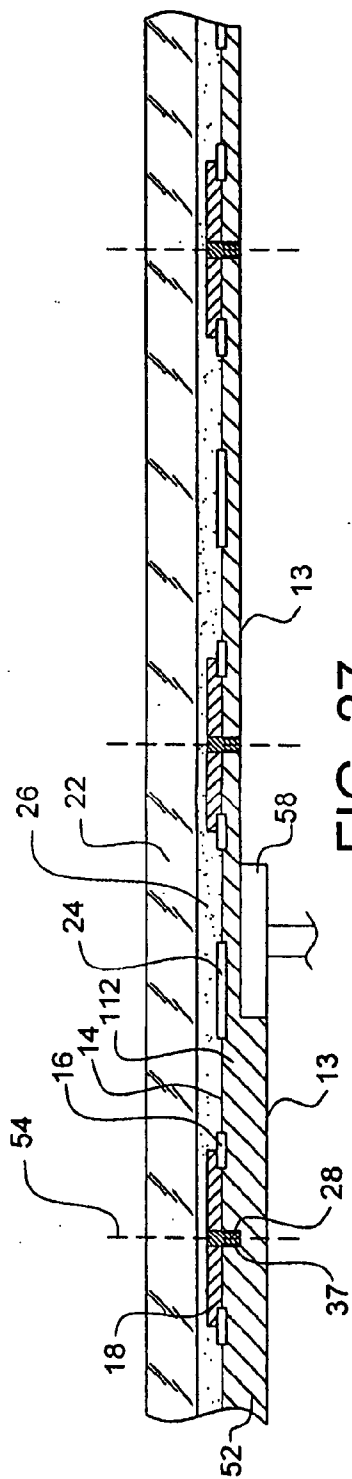


FIG. 27

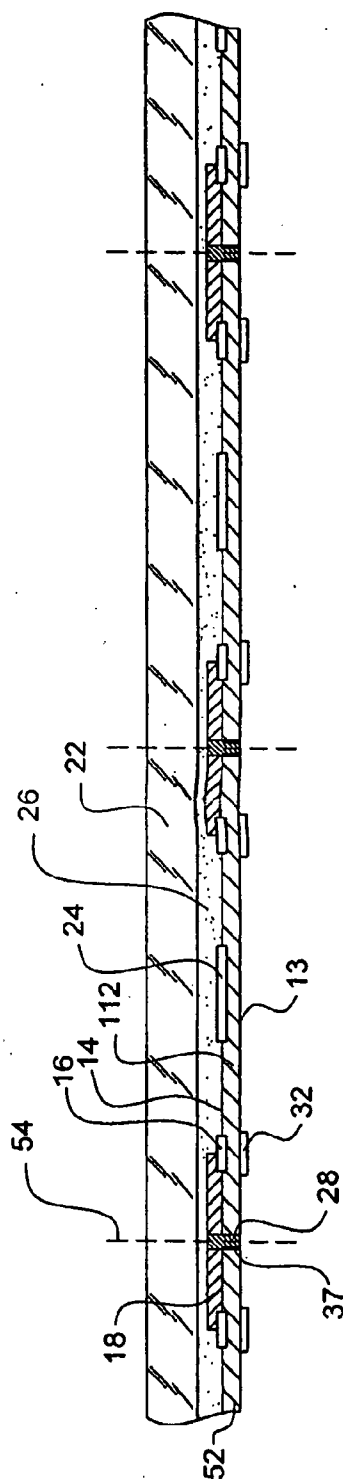


FIG. 28

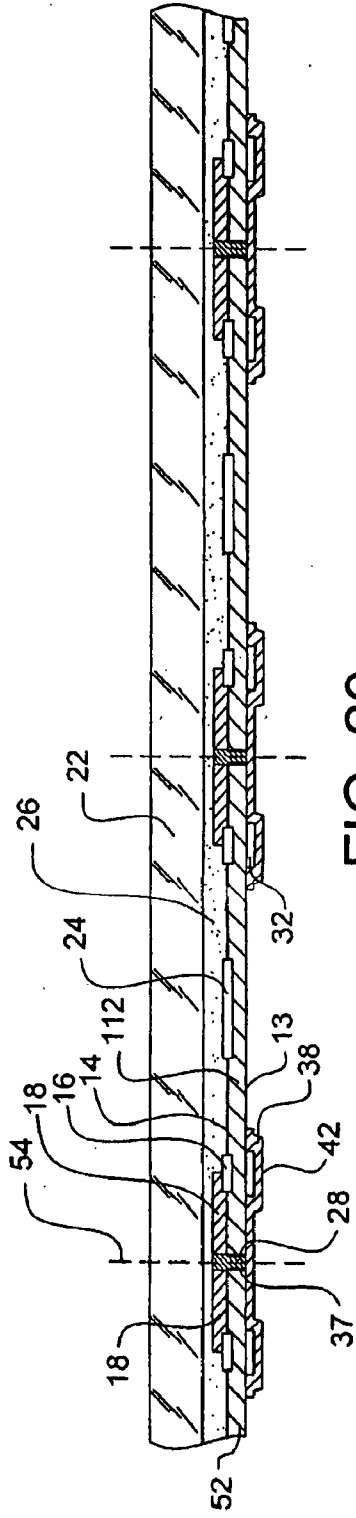


FIG. 29

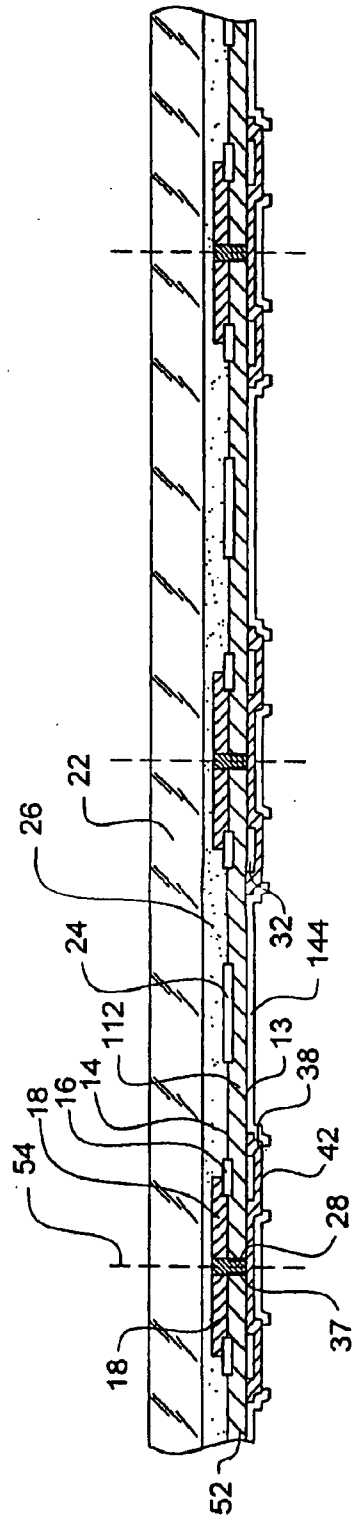


FIG. 30

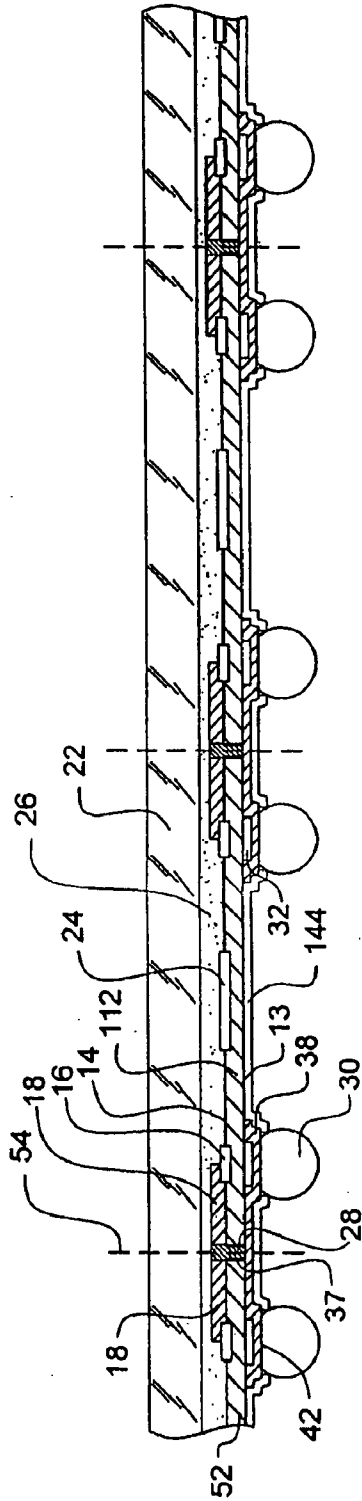


FIG. 31

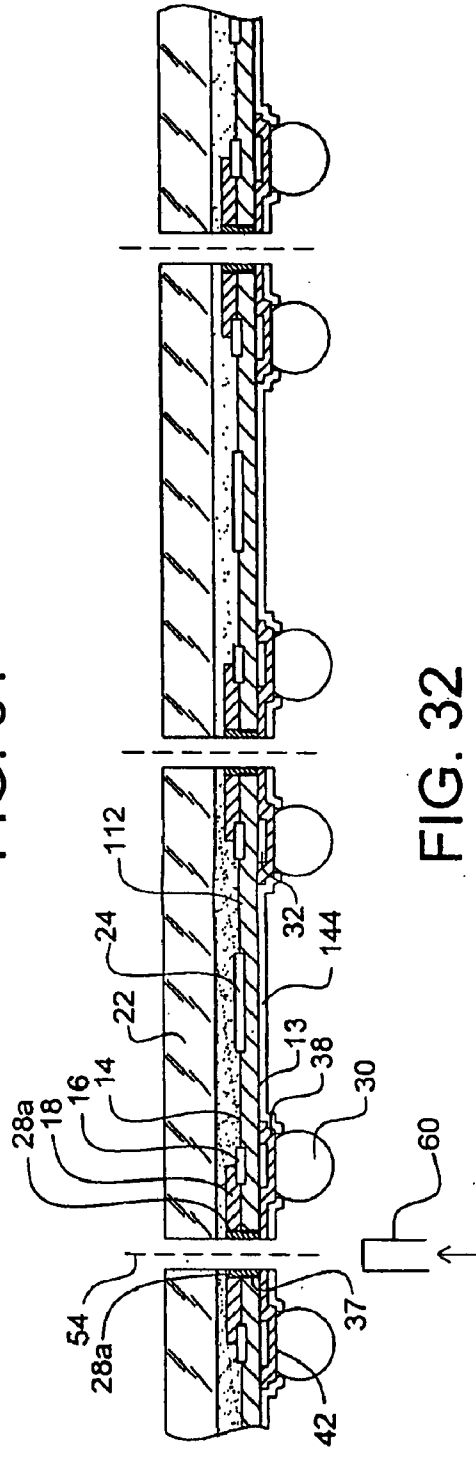


FIG. 32

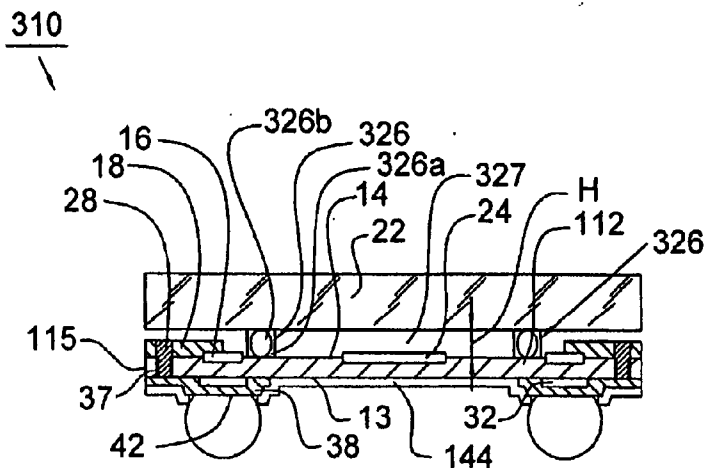


FIG. 33

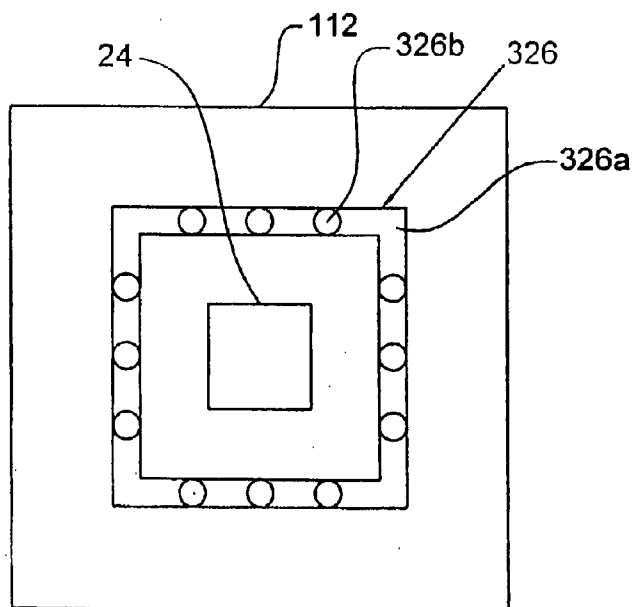


FIG. 34

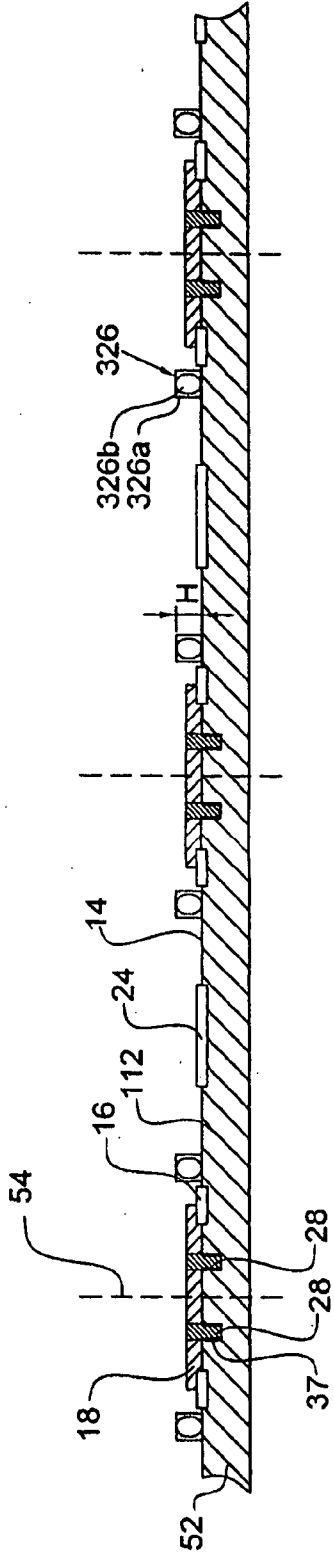


FIG. 35

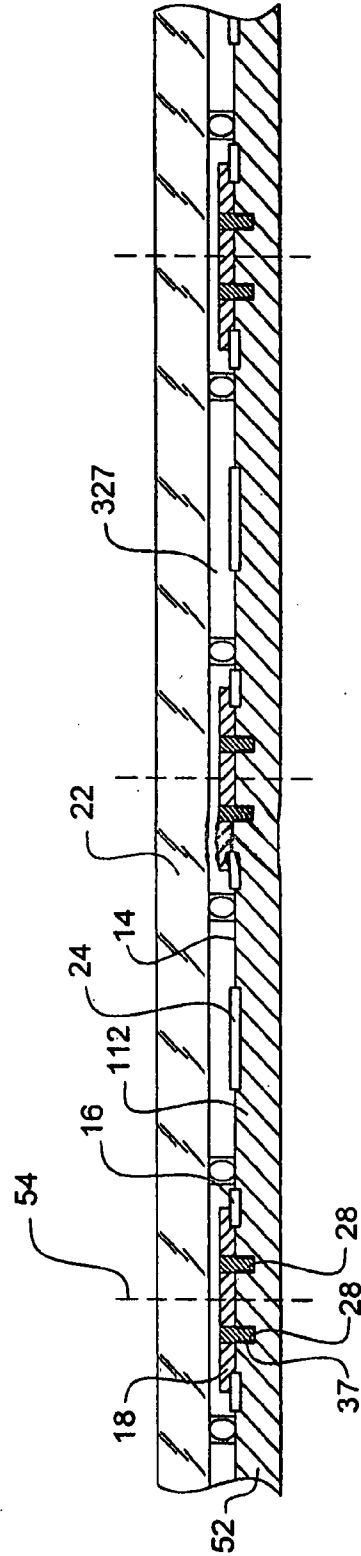


FIG. 36

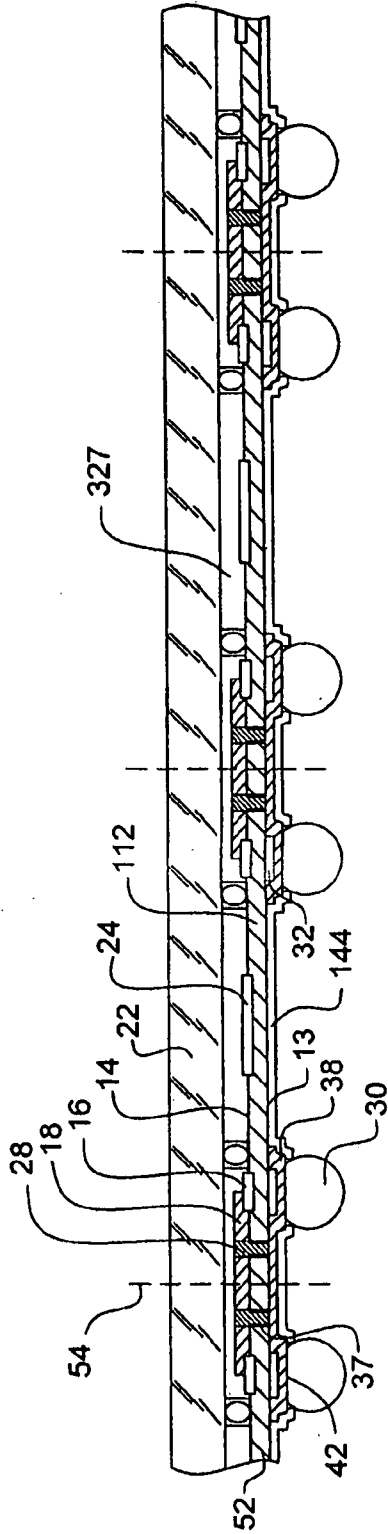


FIG. 37

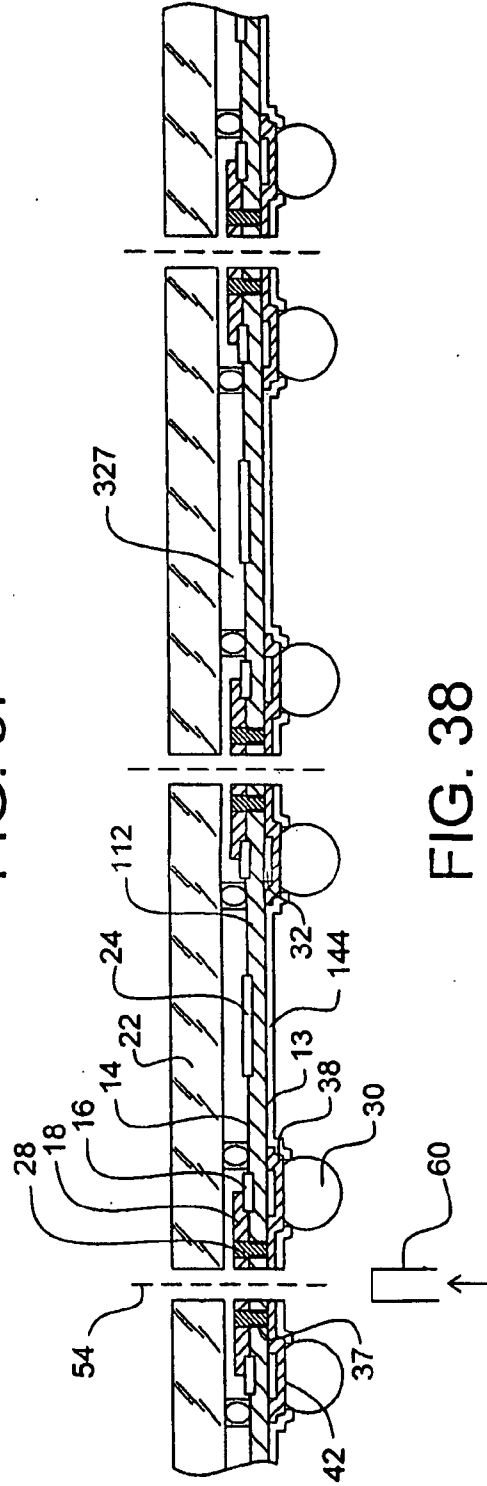


FIG. 38

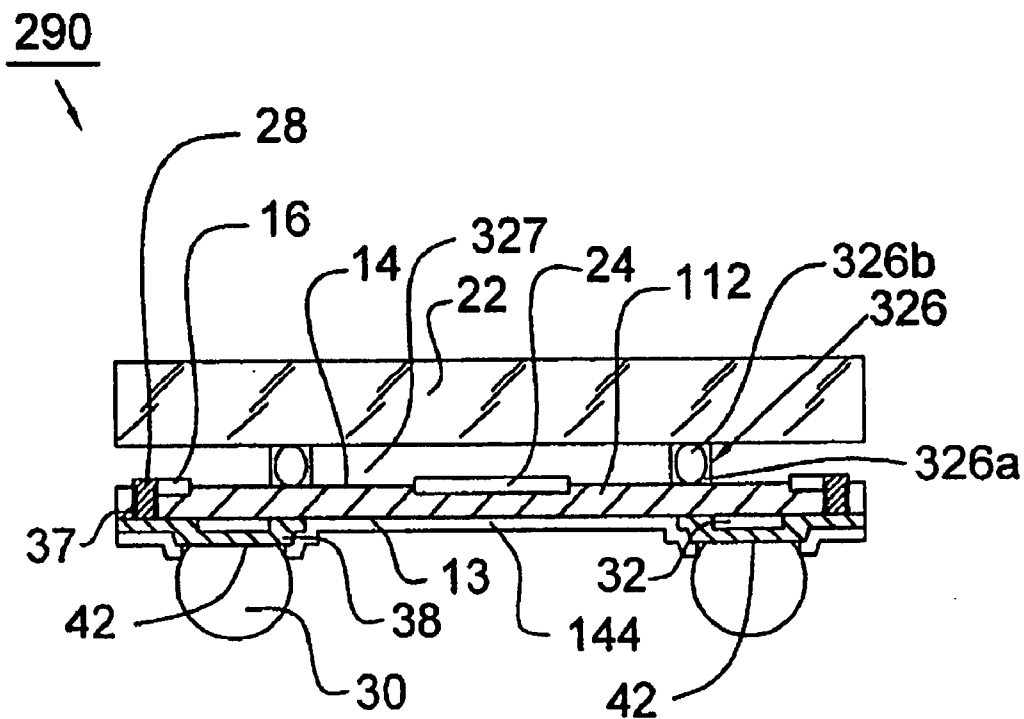


FIG. 39

SEMICONDUCTOR PACKAGE AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Divisional of U.S. Ser. No. 11/074,796 filed Mar. 9, 2005. Priority is claimed based on U.S. Ser. No. 11/074,796 filed Mar. 9, 2005, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention generally relates to a semiconductor package and a method for manufacturing the same, and more particularly to a wafer level semiconductor package and a method for manufacturing the same.

[0004] 2. Description of the Related Art

[0005] The semiconductor package provides four functions, i.e. signal distribution, power distribution, heat dissipation and element protection. In general, a semiconductor chip is packaged into an enclosure (e.g. a single-chip module), and then disposed on a printed circuit board, together with other components, such as capacitors, resistors, inductors, filters, switches, and optical and RF components.

[0006] The complementary metal oxide semiconductor (CMOS) technology for making optical components is similar to that for making semiconductor chips. CMOS is typically formed by silicon (Si) and germanium (Ge) and generally includes NMOS (negative polarity) and PMOS (positive polarity) transistors. For optical components, NMOS and PMOS can generate currents after sensing light, and the currents are then recorded and read as image.

[0007] Further, as the demands for lighter and more complex electronic devices gradually increase, the operating speed and the complexity of IC chips have become higher and higher. Accordingly, a higher packaging efficiency is required. In the prior art, various semiconductor packages and manufacturing methods have been provided for improving the packaging efficiency and reliability. For example, U.S. Pat. No. 6,040,235 entitled "Methods And Apparatus For Producing Integrated Circuit Devices" issued to Badehi on May 21, 2000, and U.S. Pat. No. 6,117,707 entitled "Methods Of Producing Integrated Circuit Devices" issued to Badehi on Sep. 12, 2000 disclose methods for manufacturing the semiconductor packages. However, these semiconductor packages and the manufacturing methods in the prior art still have many limitations and drawbacks, and therefore can not completely meet the requirements for semiconductor packages.

[0008] Accordingly, there exists a need for providing a wafer level semiconductor package to further meet the requirement for semiconductor packages.

SUMMARY OF THE INVENTION

[0009] It is an object of the present invention to provide a semiconductor package and a method for manufacturing the same, which can offer higher packaging efficiency and eliminate the limitations and drawbacks in the prior art.

[0010] In order to achieve the object, the present invention provides a semiconductor package comprising a chip, a plurality of pad extension traces, a plurality of via holes, a lid and a plurality of metal traces. The chip has an active surface, a back surface opposite to the active surface, an optical component disposed on the active surface, and a plurality of bonding pads disposed on the active surface and electrically connected to the optical component. The pad extension traces are electrically connected to the bonding pads. The via holes are formed through the chip and electrically connected to the pad extension traces. The lid is attached on the active surface of the chip. The plurality of metal traces are disposed on the back surface of the chip, electrically connected to the plurality of via holes, and defines a plurality of solder pads thereon.

[0011] The semiconductor package according to the present invention can be massively produced at wafer level, thereby reducing the packaging cost and improving packaging reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Other objects, advantages, and novel features of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

[0013] FIG. 1 shows a sectional view of a semiconductor package according to first embodiment of the present invention.

[0014] FIG. 2 shows a semi-finished wafer structure according to first embodiment of the present invention.

[0015] FIG. 3 shows a top view of the semi-finished wafer structure of FIG. 2.

[0016] FIGS. 4 to 15 illustrate a method for manufacturing the semiconductor package according to first embodiment of the present invention.

[0017] FIG. 16 shows a sectional view of a semiconductor package according to one alternative embodiment of the present invention.

[0018] FIG. 17 shows a sectional view of a semiconductor package according to second embodiment of the present invention.

[0019] FIGS. 18 to 20 illustrate a method for manufacturing the semiconductor package according to second embodiment of the present invention.

[0020] FIG. 21 shows a sectional view of a semiconductor package according to the other alternative embodiment of the present invention.

[0021] FIG. 22 shows a sectional view of a semiconductor package according to third embodiment of the present invention.

[0022] FIGS. 23 to 32 illustrate a method for manufacturing the semiconductor package according to third embodiment of the present invention.

[0023] FIG. 33 shows a sectional view of a semiconductor package according to fourth embodiment of the present invention.

[0024] FIG. 34 shows a schematic top view of the adhesive ring disposed on the chip.

[0025] FIGS. 35 to 38 illustrate a method for manufacturing the semiconductor package according to fourth embodiment of the present invention.

[0026] FIG. 39 shows a sectional view of a semiconductor package according to the other alternative embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0027] Now referring to FIG. 1, it shows a sectional view of a semiconductor package 10 according to first embodiment of the present invention. The semiconductor package 10 comprises a chip 12 having an active surface 14, a back surface 13 opposite to the active surface, an optical component 24 (e.g. sensor and photo coupler) disposed on the active surface 14, and a plurality of bonding pads 16 disposed on the active surface 14. The optical component 24 can be formed by complementary metal oxide semiconductor (CMOS).

[0028] The chip 12 further has a plurality of via holes 28 formed through the chip 12 and a plurality of pad extension traces 18 for electrically connecting the bonding pads 16 to the via holes 28. The semiconductor package 10 further comprises a lid 22 being attached on the active surface 14 of the chip 12 through an adhesive layer 26, and covering the active surface 14 and the plurality of pad extension traces 18.

[0029] The semiconductor package 10 further comprises a plurality of compliant pads 32, a plurality of metal traces 38, a solder mask 44 and a plurality of solder balls 30. The compliant pads 32 are formed on the back surface 13 of the chip 12. The metal traces 38 are formed on the back surface 13 of the chip 12 and the compliant pads 32. The solder mask 44 is coated on the back surface 13 of the chip 12 with parts of the metal traces 38 exposed therefrom, wherein the parts are defined as a plurality of solder pads 42. The solder balls are disposed on the solder pads 42 for being connected to an external circuit, e.g. a printed circuit board. The compliant pads 32 can be formed by photosensitive benzocyclobutene polymer so as to reduce the internal stress or thermal stress inside the semiconductor package 10. Further, the chip 12 and the pad extension traces 18 respectively have inclined side surfaces 15, 17, and the solder mask 44 can optionally cover the inclined side surfaces 15 of the chip 12 and the inclined side surfaces 17 of the pad extension traces 18. The solder mask 44 can be formed by photosensitive benzocyclobutene polymer. The via holes 28 are respectively and electrically connected to the pad extension traces 18 and the metal traces 38.

[0030] FIGS. 2 to 12 illustrate a method for manufacturing the semiconductor package 10 according to present invention.

[0031] As shown in FIGS. 2 and 3, a wafer 52 includes a plurality of chips 12 separated from one another by scribe lines 54. A plurality of bonding pads 16 are formed on the wafer 52.

[0032] Referring to FIG. 4, a plurality of pad extension traces 18 are formed on the wafer 52 through a RDL

(redistribution layer) photolithography process and electrically connected to the bonding pads 16. An optical component 24 is disposed on the active surface 14 of the chip 12, and interacts with incident light or emits light.

[0033] Referring to FIG. 5, a photoresist 20 can be coated on the active surface 14 of the chip 12 so as to prevent contamination caused by next drilling process. It should be understood by the skill in the art that the step of coating the photoresist 20 on the active surface 14 is optional and not absolutely necessary.

[0034] Referring to FIG. 6, a plurality of holes 36 are formed through the pad extension traces 18 on the wafer 52 by using a laser drill 40 and each hole 36 has a predetermined depth.

[0035] Referring to FIG. 7, the photoresist 20 is striped off and an insulating layer 37 is formed on the inner surface of each hole 36 with at least one part of the pad extension trace 18 exposed therefrom.

[0036] Referring to FIG. 8, a conductive material such as copper (Cu) is deposited into the plurality of holes 36 by photomasking and sputtering processes so as to form a plurality of via holes 28. The via holes 28 are electrically connected to the pad extension traces 18. Alternatively, the conductive material can also be plated just on the inner surface of each hole 36 so as to form the via holes 28 electrically connected to the pad extension traces 18.

[0037] Referring to FIG. 9, a lid 22 is attached to the wafer 52 through an adhesive layer 26 and covers the active surface 14 of the chip 12 and the plurality of pad extension traces 18. The lid 22 may be made of transparent material, such as glass, acrylic resin or sapphire, so that light can be transmitted through the lid 22 and interact with the optical component 24 of the semiconductor chip 12.

[0038] Referring to FIG. 10, the back surface 13 of the wafer 52 is ground by a mechanical grinding wheel or chemical grinding process so as to reduce the thickness of the wafer 52 to a predetermined thickness and make the via holes 28 exposed out of the back surface 13 of the chip 12.

[0039] According to one embodiment of the present invention, the plurality of holes 36 can be directly formed through the chip 12 such that the formed via holes 28 can be directly exposed out of the back surface 13. It could be understood by the skill in the art that the wafer 52 can be made to have a predetermined thickness in advance so as to eliminate the above grinding step, or be ground to a predetermined thickness right after forming the via holes 28.

[0040] Referring to FIG. 11, a plurality of compliant pads 32 are formed on the back surface 13 of the chip 12 by a thin-film deposition process and a photolithography and etching process. The compliant pads 32 can be made of photosensitive benzocyclobutene (BCB) resin.

[0041] Referring to FIG. 12, a plurality of metal traces 38 are formed on the back surface 13 of the chip 12 and the plurality of compliant pads 32 by a thin-film deposition process and a photolithography and etching process, and respectively connected to the via holes 28.

[0042] Referring to FIG. 13, a cutting blade 60 cuts the back surface 13 of the wafer 52 along predetermined paths for forming wedged notches 62, thereby forming the

inclined side surfaces **15** of the chip **12**. The predetermined paths can be correspondent to the scribe lines **54** of the wafer **52**.

[0043] Referring to FIG. **14**, the solder mask **44** is coated on the back surface **13** of the chip **12** and covers the metal traces **38**, the side surfaces **15** of the chip **12** and the side surfaces **17** of the pad extension traces **18** with parts of the metal traces **38** exposed therefrom, such that the parts can be defined as a plurality of solder pads **42** and corresponding to the compliant pads **32**. The solder mask **44** can be formed by photosensitive benzocyclobutene polymer.

[0044] Referring to FIG. **15**, a plurality of solder balls **30** are respectively disposed on the solder pads **42** then, the wafer **52** is singulated along the predetermined paths to form the semiconductor package **10** as shown in FIG. **1**.

[0045] Referring to FIG. **16**, it shows a sectional view of a semiconductor package **90** according to one alternative embodiment of the present invention. The semiconductor package **90** is substantially identical to the semiconductor package **10**, and its similar elements will be indicated by the same numerals. In the semiconductor package **90**, the via holes **28** are formed on and electrically connected to the bonding pads **16**.

[0046] Therefore, according to the method of the present invention, the semiconductor packages **10**, **90** can be massively produced at wafer level thereby reducing the manufacturing cost and improving packaging reliability. Further, the semiconductor packages **10**, **90** according to the present invention can be applied to packages for optical components.

[0047] Now referring to FIG. **17**, it shows a sectional view of a semiconductor package **110** according to second embodiment of the present invention. The semiconductor package **110** is substantially identical to the semiconductor package **10**, and its similar elements will be indicated by the same numerals. The solder mask **144** of the semiconductor package **110** is only coated on the back surface **13** of the chip **112** and not coated on the side surfaces **115** of the same. Further, the chip **112** has vertical side surfaces **115** instead of the inclined side surfaces.

[0048] Now referring to FIGS. **2** to **12** and FIGS. **18** to **20**, they illustrate a method for manufacturing the semiconductor package **110** according to present invention.

[0049] Referring to FIG. **18**, a solder mask **144** is coated on the back surface **13** of the wafer **52** with parts of the metal traces **38** exposed therefrom, such that the parts can be defined as a plurality of solder pads **42**.

[0050] Referring to FIG. **19**, a plurality of solder balls **30** are respectively disposed on the solder pads **42**.

[0051] Referring to FIG. **20**, a cutting blade **60** cuts the back surface **13** of the wafer **52** along predetermined paths, i.e. along the scribe lines **54** of the wafer **52**, thereby forming the individual semiconductor package **110** as shown in FIG. **17**.

[0052] Now referring to FIG. **21**, it shows a sectional view of a semiconductor package **190** according to the other alternative embodiment of the present invention. The semiconductor package **190** is substantially identical to the semiconductor package **110**, and its similar elements will be

indicated by the same numerals. In the semiconductor package **190**, the via holes **28** are formed on and electrically connected to the bonding pads **16**.

[0053] Now referring to FIG. **22**, it shows a sectional view of a semiconductor package **210** according to third embodiment of the present invention. The semiconductor package **210** is substantially identical to the semiconductor package **110**, and its similar elements will be indicated by the same numerals. In this embodiment, the via holes **28a** are exposed out of the side surfaces **210a** of the semiconductor package **210**.

[0054] Now referring to FIGS. **2** to **5** and FIGS. **23** to **32**, they illustrate a method for manufacturing the semiconductor package **210** according to present invention.

[0055] Referring to FIG. **23**, a plurality of holes **36** are formed through the pad extension traces **18** on the scribe lines **54** by using a laser drill **40** and each hole **36** has a predetermined depth.

[0056] Referring to FIG. **24**, the photoresist **20** is striped off and an insulating layer **37** is formed on the inner surface of each hole **36** according to the same manner illustrated in FIG. **7**.

[0057] Referring to FIG. **25**, a plurality of via holes **28** are formed and electrically connected to the pad extension traces **18** according to the same manner illustrated in FIG. **8**.

[0058] Referring to FIG. **26**, a lid **22** is attached to the wafer **52** through an adhesive layer **26** according to the same manner illustrated in FIG. **9**.

[0059] Referring to FIG. **27**, the back surface **13** of the wafer **52** is ground according to the same manner illustrated in FIG. **10** such that the via holes **28** exposed out of the back surface **13** of the chip **12**.

[0060] Referring to FIG. **28**, a plurality of compliant pads **32** are formed on the back surface **13** of the chip **12** according to the same manner illustrated in FIG. **11**.

[0061] Referring to FIG. **29**, a plurality of metal traces **38** are formed on the back surface **13** of the chip **12** and the plurality of compliant pads **32** according to the same manner illustrated in FIG. **12**.

[0062] Referring to FIG. **30**, a solder mask **144** is coated on the back surface **13** of the wafer **52** according to the same manner illustrated in FIG. **18** such that a plurality of solder pads **42** are defined.

[0063] Referring to FIG. **31**, a plurality of solder balls **30** are respectively disposed on the solder pads **42**.

[0064] Referring to FIG. **32**, a cutting blade **60** cuts the back surface **13** of the wafer **52** along the scribe lines **54** of the wafer **52** thereby forming the individual semiconductor package **210** as shown in FIG. **22**. In this step, each via hole **28** is cut into two parts **28a**.

[0065] Now referring to FIG. **33**, it shows a sectional view of a semiconductor package **310** according to fourth embodiment of the present invention. The semiconductor package **310** is substantially identical to the semiconductor package **110**, and its similar elements will be indicated by the same numerals. In this embodiment, the lid **22** is attached on the active surface **14** of the chip **112** through an adhesive ring **326** such that light can be transmitted to the optical

component 24 or emitted from the optical component 24 without passing the adhesive layer 26 of FIG. 17, thereby improving the light transmitting property within the semiconductor package 310.

[0066] Referring to FIG. 34, it shows a schematic top view of the adhesive ring 326 disposed on the chip 112. The adhesive ring 326 is made of an adhesive material 326a having a plurality of spacers 326b mixed thereinto, and disposed around the optical component 24 for attaching the lid 22 on the active surface 14 of the chip 112. The spacers 326b have substantially the same height H to support the lid 22 above the active surface 14 of the chip 112 such that the lid 22 and the chip 112 have a gap formed therebetween. In addition, the lid 22, the chip 112 and the adhesive ring 326 further define a hermetical cavity 327 within which the optical component 24 is disposed.

[0067] Now referring to FIGS. 2 to 8 and FIGS. 35 to 38, they illustrate a method for manufacturing the semiconductor package 310 according to present invention.

[0068] Referring to FIG. 35, a plurality of adhesive rings 326 are respectively formed on the active surface 14 of each chip 112. The adhesive ring 326 is made of an adhesive material 326a having a plurality of spacers 326b mixed thereinto, and disposed around the optical component 24 on the active surface 14 of the chip 112 as shown in FIG. 34. Preferably, the spacers 326b have substantially the same size or same height H.

[0069] Referring to FIG. 36, a lid 22 is attached to the wafer 52 through the plurality of adhesive rings 326 and covers the active surface 14 of the chip 12 and the plurality of pad extension traces 18. Since the spacers 326b of the adhesive rings 326 have the same height H, the lid 22 can be supported above the active surface 14 of the chip 12. Further, the lid 22, the chip 112 and the adhesive ring 326 define a hermetical cavity 327 within which the optical component 24 is disposed.

[0070] According to another embodiment of the present invention, the plurality of adhesive rings 326 can be formed on the lid 22 and then attached to the active surface 14 of each chip 112 so as to form the same structure as shown in FIG. 36.

[0071] In next steps, the back surface 13 of the wafer 52 is ground, followed by the formations of a plurality of compliant pads 32, a plurality of metal traces 38, a solder mask 144 and a plurality of solder balls 30, according to the same manners illustrated in FIGS. 10-12 and FIGS. 18-19 so as to form a structure as shown in FIG. 37.

[0072] Referring to FIG. 38, a cutting blade 60 cuts the back surface 13 of the wafer 52 along the scribe lines 54, thereby forming the individual semiconductor package 310 as shown in FIG. 33.

[0073] Now referring to FIG. 39, it shows a sectional view of a semiconductor package 290 according to the other alternative embodiment of the present invention. The semiconductor package 290 is substantially identical to the semiconductor package 190 as shown in FIG. 21, and its similar elements will be indicated by the same numerals. In the semiconductor package 290, the lid 22 is attached to the active surface 14 of the chip 112 by an adhesive ring 326 according to the same manner as illustrated in FIGS. 33 and 34.

[0074] Although the invention has been explained in relation to its preferred embodiment, it is not used to limit the invention. It is to be understood that many other possible modifications and variations can be made by those skilled in the art without departing from the spirit and scope of the invention as hereinafter claimed.

What is claimed is:

1. A semiconductor package comprising:
 - a chip having an active surface, a back surface opposite to the active surface, an optical component disposed on the active surface, and a plurality of bonding pads disposed on the active surface and electrically connected to the optical component;
 - a plurality of via holes formed through the chip and electrically connected to the plurality of bonding pads;
 - a lid attached on the active surface of the chip; and
 - a plurality of metal traces being disposed on the back surface of the chip, electrically connected to the plurality of via holes, and defining a plurality of solder pads thereon.
2. The semiconductor package as claimed in claim 1, further comprising an adhesive ring disposed around the optical component for attaching the lid on the active surface of the chip.
3. The semiconductor package as claimed in claim 2, wherein the adhesive ring is made of an adhesive material having a plurality of spacers mixed thereinto.
4. The semiconductor package as claimed in claim 1, having at least one side surface wherein the plurality of via holes are exposed out of the side surface.
5. The semiconductor package as claimed in claim 1, further comprising a plurality of pad extension traces for electrically connecting the via holes with the bonding pads.
6. The semiconductor package as claimed in claim 1, further comprising a plurality of compliant pads formed between the back surface of the chip and the metal traces and corresponding to the solder pads.
7. The semiconductor package as claimed in claim 1, further comprising a solder mask, which covers the back surface of the chip and the metal traces with the solder pads exposed therefrom.
8. The semiconductor package as claimed in claim 7, wherein the solder mask further covers at least one side surface of the chip.
9. The semiconductor package as claimed in claim 1, further comprising a plurality of solder balls respectively disposed on the solder pads.
10. The semiconductor package as claimed in claim 1, wherein the lid is made of transparent material.
11. The semiconductor package as claimed in claim 10, wherein the transparent material is selected from a group consisting of glass, acrylic resin and sapphire.
12. The semiconductor package as claimed in claim 1, wherein the optical component is formed by complementary metal oxide semiconductor (CMOS).
13. The semiconductor package as claimed in claim 6, wherein the compliant pads are made of photosensitive benzocyclobutene polymer.
14. The semiconductor package as claimed in claim 7, the solder mask is made of photosensitive benzocyclobutene polymer.