April 18, 1967 R. E. BENN ETAL 3,315,248

DISPLAY TUBE HAVING AN ENCAPSULATED DIODE SWITCHING MATRIX

Filed Dec. 9, 1963 6 Sheets-Sheet 1

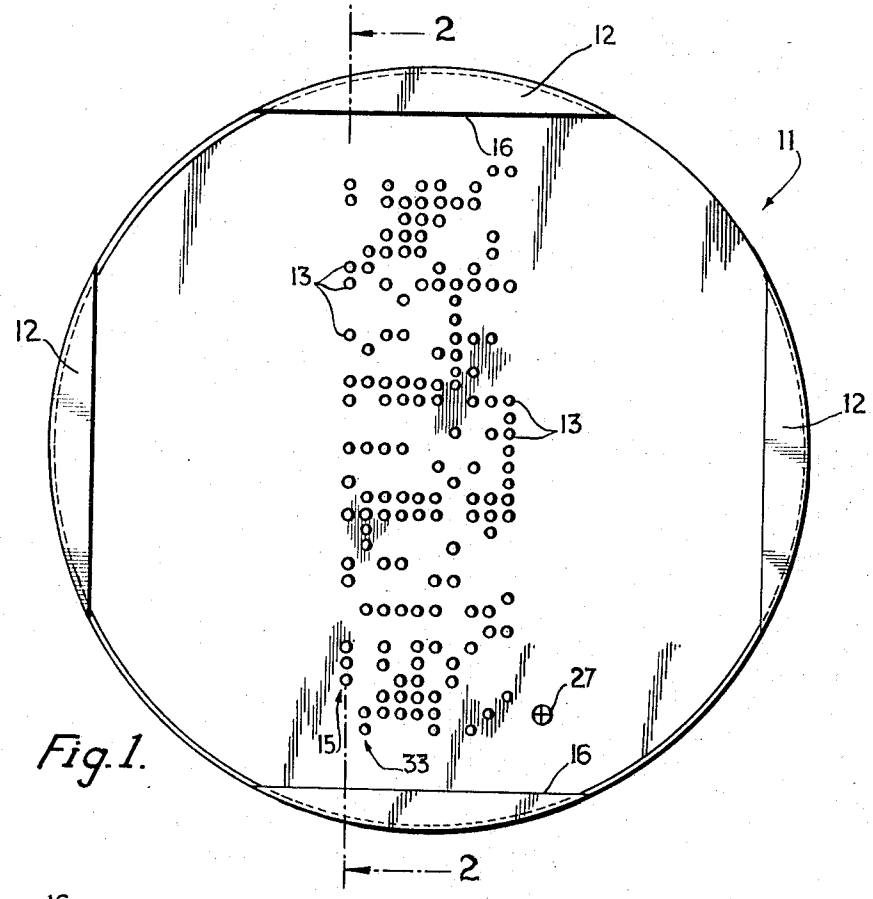

Fig. 1.

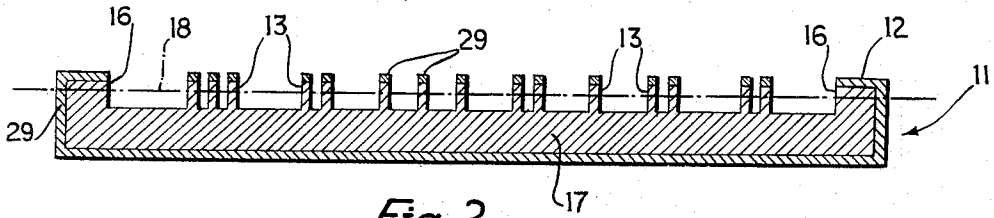

Fig. 2.

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DISPLAY TUBE HAVING AN ENCAPSULATED DIODE SWITCHING MATRIX

Filed Dec. 9, 1963 6 Sheets-Sheet 2

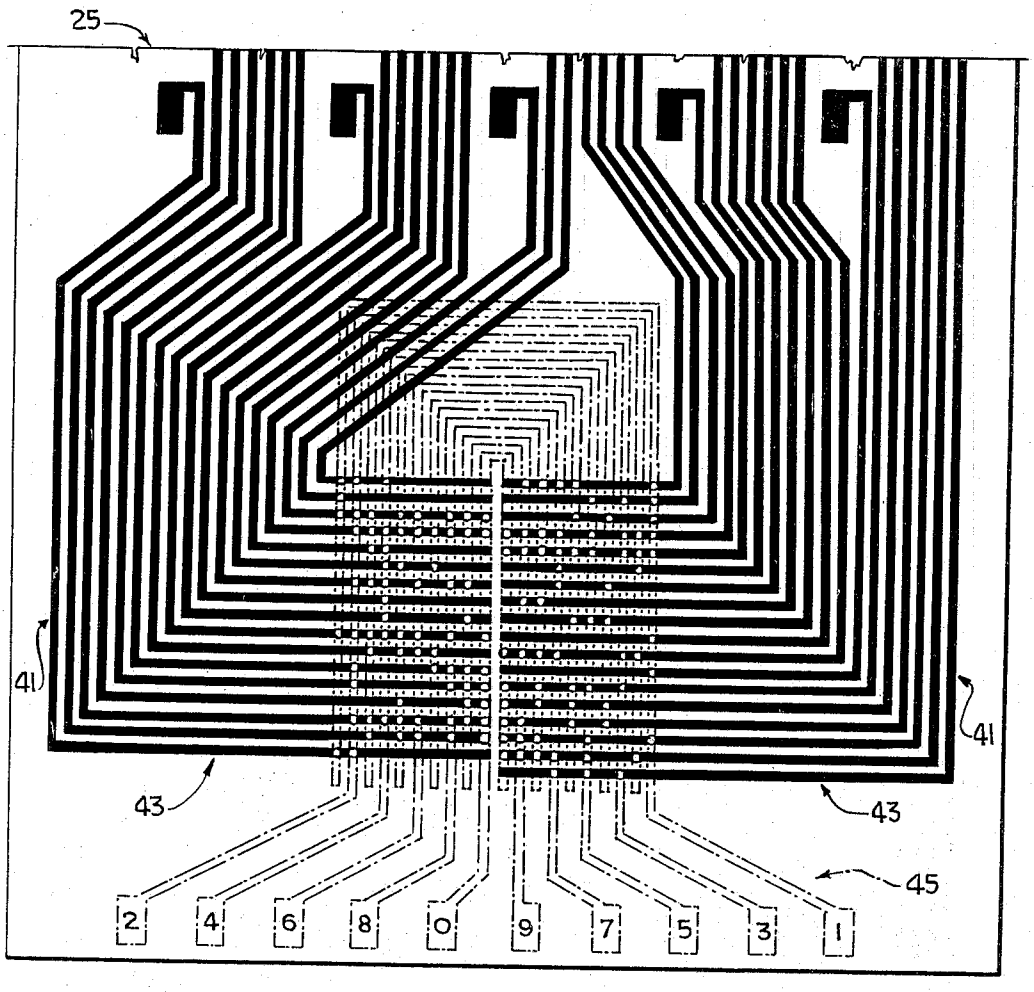

Fig. 6.

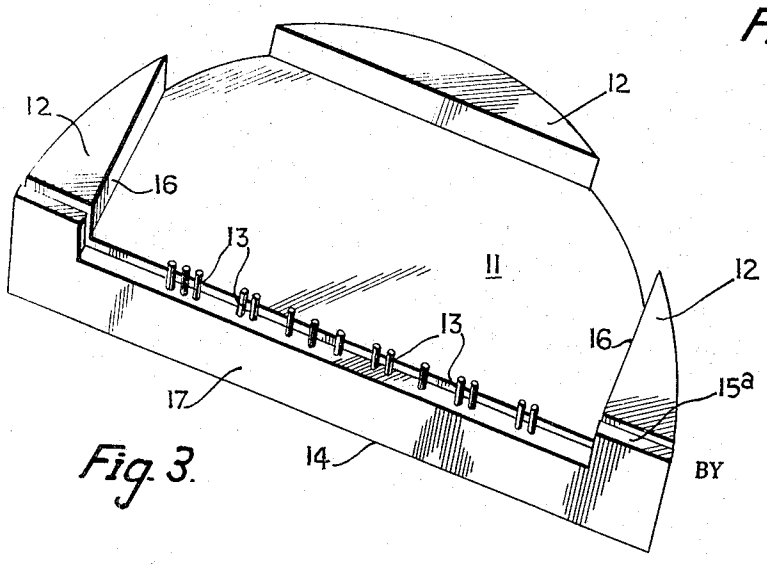

Fig. 3.

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DISPLAY TUBE HAVING AN ENCAPSULATED DIODE SWITCHING MATRIX

Filed Dec. 9, 1963 6 Sheets-Sheet 3

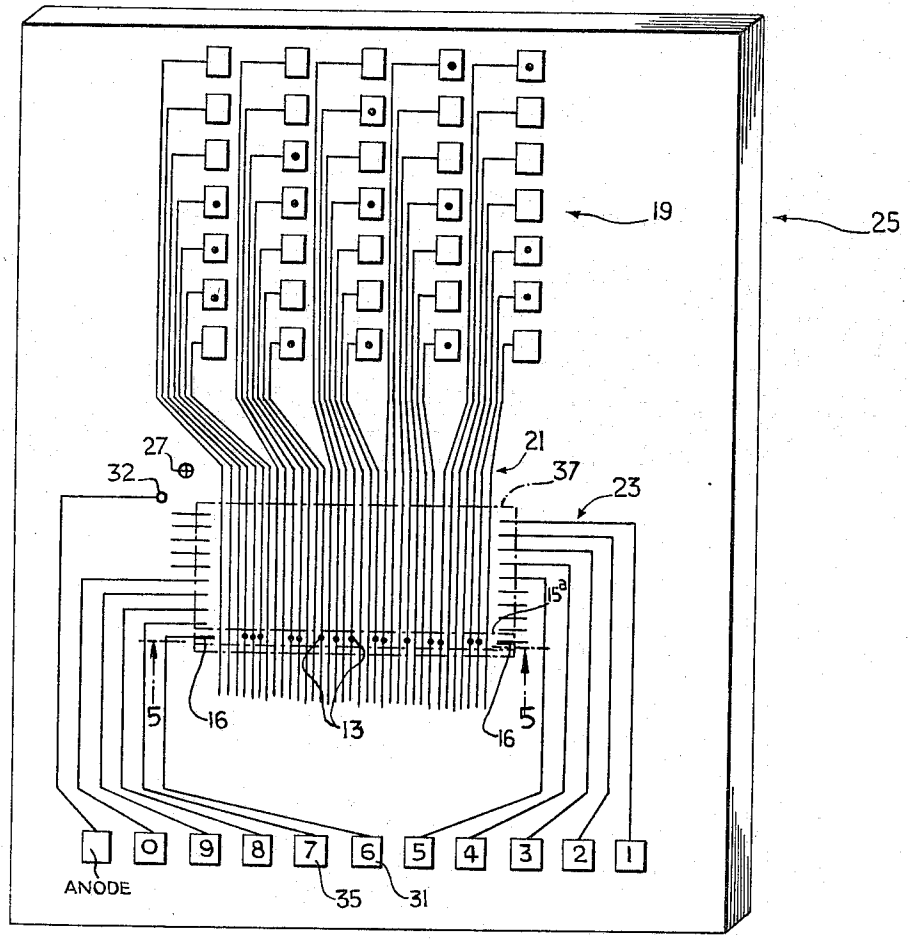

Fig. 4.

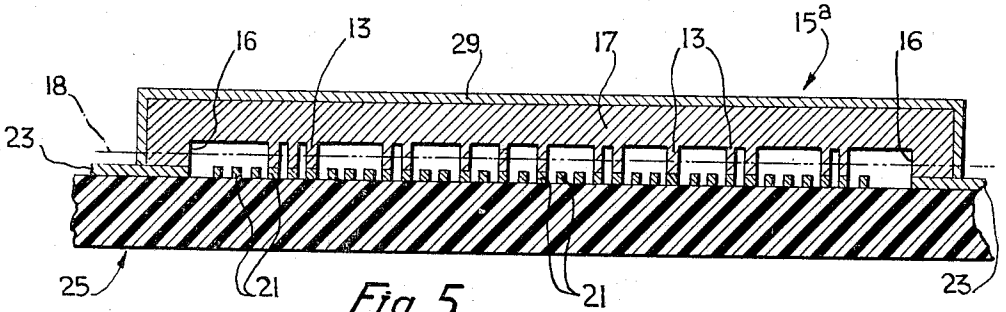

Fig. 5.

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DISPLAY TUBE HAVING AN ENCAPSULATED DIODE SWITCHING MATRIX

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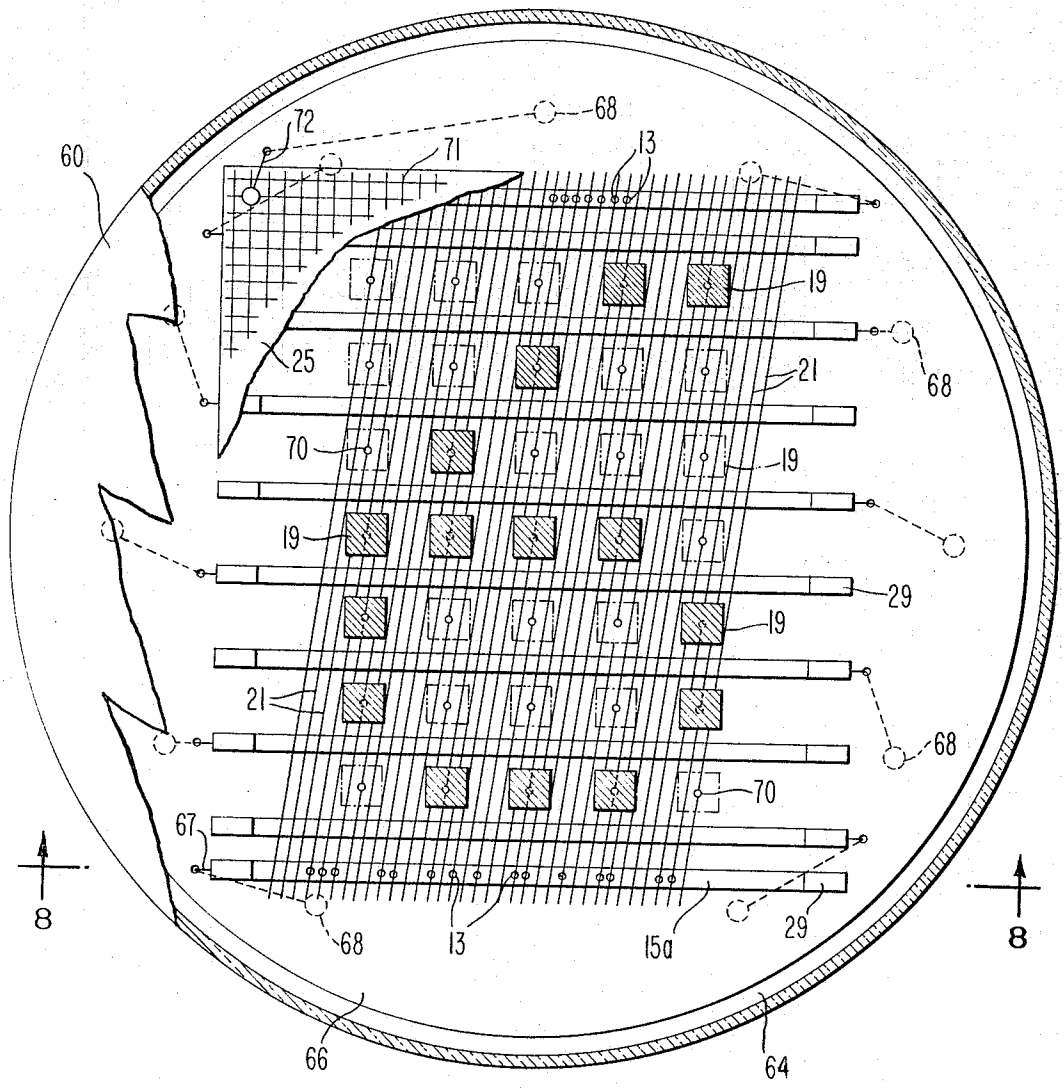

Fig. 7

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DISPLAY TUBE HAVING AN ENCAPSULATED DIODE SWITCHING MATRIX

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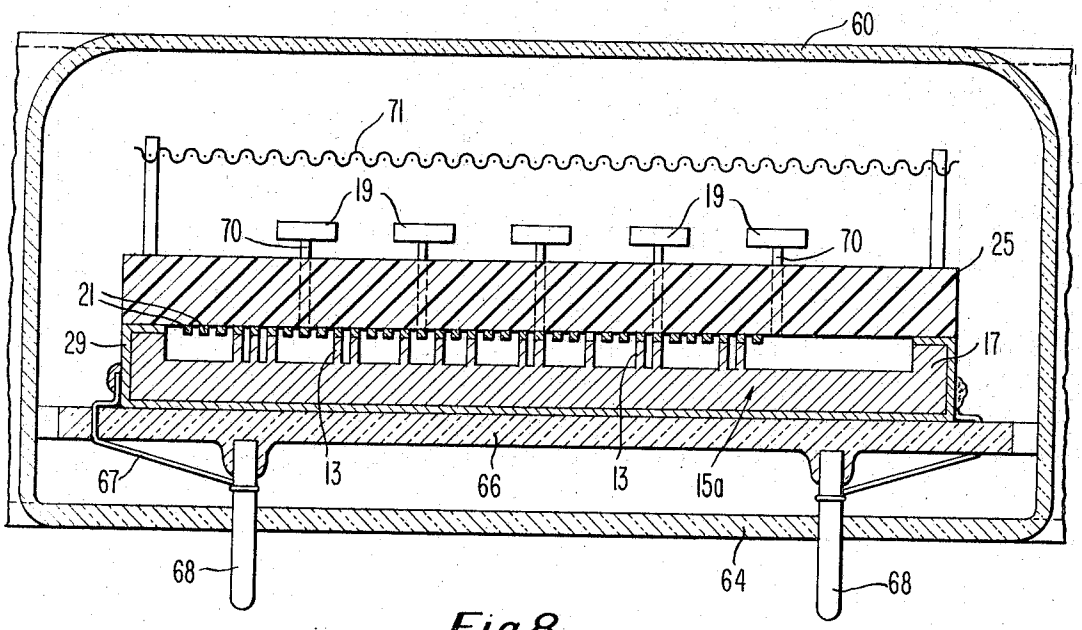

Fig.8

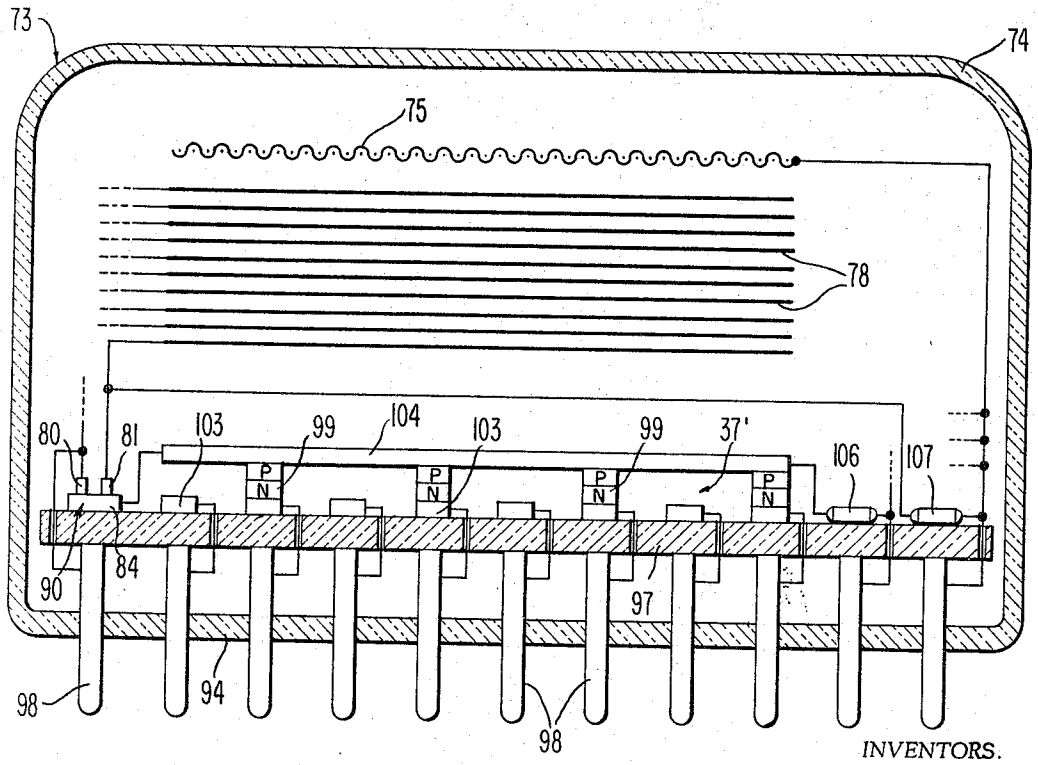

Fig.10

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DISPLAY TUBE HAVING AN ENCAPSULATED DIODE SWITCHING MATRIX

Filed Dec. 9, 1963 6 Sheets-Sheet 6

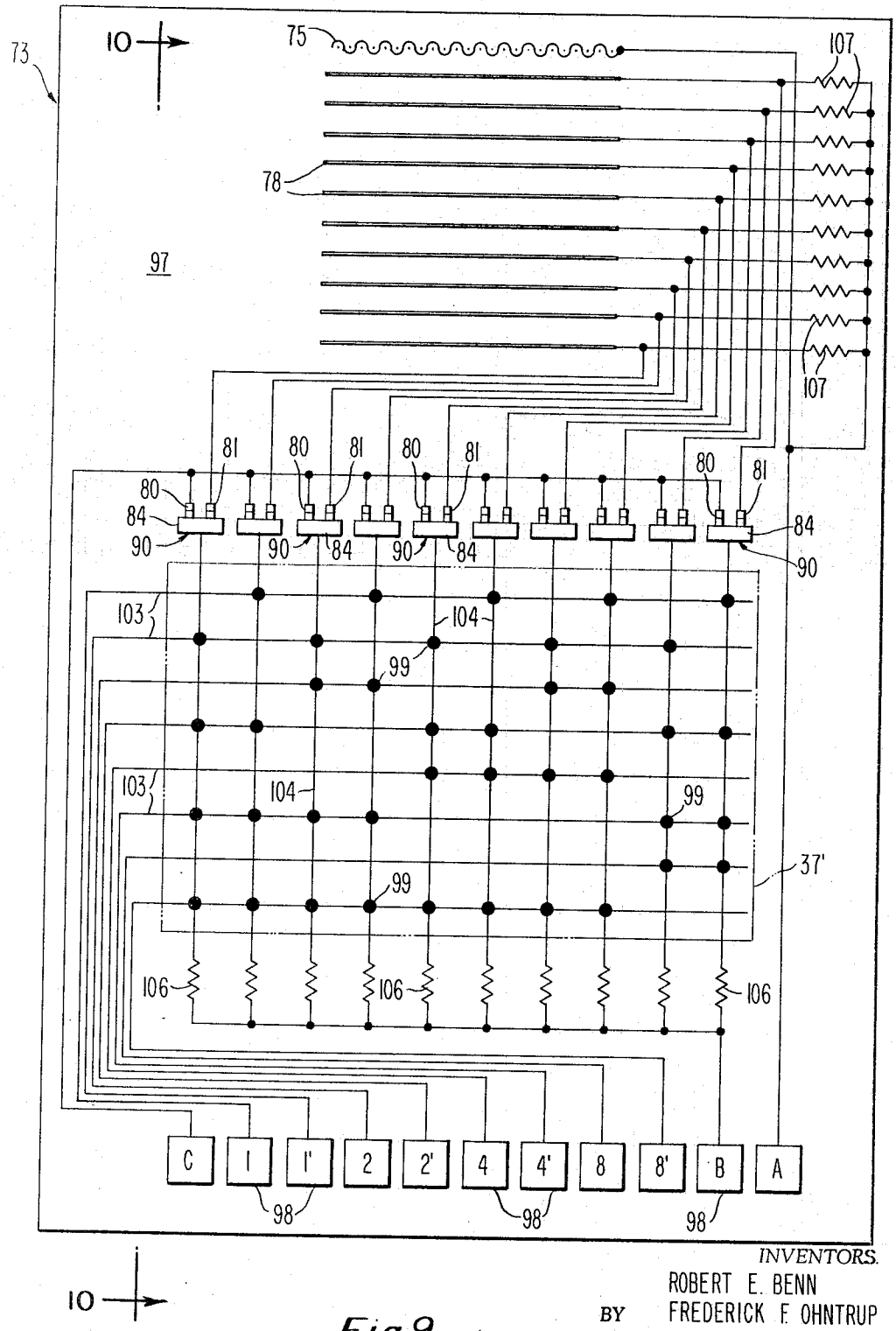

Fig. 9

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Patented Apr. 18, 1967

3,315,248

DISPLAY TUBE HAVING AN ENCAPSULATED DIODE SWITCHING MATRIX

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Filed Dec. 9, 1963, Ser. No. 329,198
14 Claims. (Cl. 340—324)

This invention relates to switching circuits and more particularly to miniaturized switching circuits.

This is a continuation-in-part of application Ser. No. 10,940, now Patent No. 3,122,680 filed Feb. 25, 1960.

Miniaturized electronic elements, units and assemblies have found widespread application in electronic equipment, especially where such equipment has had to meet stringent design tolerances aimed at an economy of space and weight. For instance, in the design of electronic equipment to be used in aircraft, it is usually requisite that great consideration be given to minimizing the space and weight for such equipment.

One electronic innovation, which has greatly aided the efforts to save space and weight, has been the introduction of diode matrices to replace banks of relays or other signal switching arrangements. In the art at present a diode matrix customarily comprises a base member with rows of pairs of electrical terminals thereon, and further includes diodes selectively connected between associated pairs of these terminals. Each electrical terminal of a pair is respectively common connected with other like electrical terminals to provide the normal row and column conductors needed for input and output signal connections. By way of example, a typical diode matrix of the type just described, designed to handle sixteen input signals and provide thirty-two output signals, is mounted on a base member measuring 6 x 9½ inches, and the entire assembly weighs approximately 150 grams. When compared with the banks of relays which would be needed to perform the same signal switching operation which such a diode matrix can accomplish, this matrix represents a substantial saving in space and weight.

The present invention provides an even greater reduction of space and weight for switching circuits, and more particularly for a diode matrix.

It is an object of the present invention to provide an improved miniaturized signal switching circuit.

It is another object of the invention to provide an improved miniaturized signal switching circuit and display means therefor.

It is a further object of the present invention to provide a diode matrix switching circuit whose weight is less than 1/10th of the weight of a prior art diode matrix and whose size when compared to the prior art represents a reduction by more than 400 times.

It is a further object of the present invention to provide a novel method for building a miniaturized diode matrix of the type described in the preceding object.

In accordance with a feature of the present invention there is provided a first unit to be assembled which has input and output circuits printed thereon. This first unit (hereinafter sometimes called "Unit I") provides the vertical electrical conducting paths and provides input signal connections for horizontal electrical conducting paths.

In accordance with another feature of the present invention there is provided a second unit to be assembled (hereinafter sometimes called "Unit II") which includes a plurality of strips of semiconducting material, a first portion of which is donor-type (or N-type) semiconducting material and the remainder of which is acceptor-type (or P-type) semiconducting material. Each of these strips is formed such that mesas, or flat-topped mounds

of semiconducting material having individual P-N (or N-P) junctions are available. If the mesas are formed with the acceptor-type material at the flat-topped end, then the donor-type material forms a bar which is common connected to each of the mesas, and when the mesas are formed with the donor-type material at the flat-topped end, the arrangement is vice-versa. These strips are positioned horizontally in registration with respect to the vertical electrical conducting paths of Unit I, such that each junction mesa on a strip engages a different one of the vertical electrical conducting paths and the ends of the strips respectively engage an assigned input signal connection for the horizontal conducting paths described above. When thus positioned together, these strips form a second unit to be assembled and provide horizontal electrical conducting paths as well as diode elements connected to the vertical conducting paths.

In accordance with another feature of the present invention, the novel steps for building the miniaturized diode matrix comprise (1) fabricating a wafer of semiconducting material into a large area PN junction device; (2) (preferably) coating the wafer surface with relatively highly conductive material, thereby providing a bonding medium to subsequently effect a bond; (3) cutting away portions of the P-type material and the joined N-type material to a depth below the P-N junction, as well as the immediately adjacent conductive coating, leaving flat-topped mounds or junction mesas, each junction mesa having an individual P-N junction and a conductive coating on its end and further leaving wafer end portions of the P-type material; (4) printing vertical conducting paths and connecting means for horizontal conducting paths on a suitable base of Unit I; (5) overlaying the wafer so that the junction mesas engage the vertical printed conducting paths and the wafer end portions engage the connecting means for the horizontal conducting paths; (6) bonding said wafer to said printed circuits; (7) slicing the wafer horizontally to provide horizontal strips, each of which has one or more junction mesas with their respective individual P-N junctions and a common bar of N-type material to complete Unit II; and (8) encapsulating both units to reduce atmospheric effect thereon. The term "printed" circuit as used in the art includes etched, milled or routed, and similar conductor patterns.

A visual display device is also coupled to Units I and II to provide a visual representation of the operation thereof.

The foregoing and other objects and features of this invention will be best understood by reference to the following description of an embodiment of the invention taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a top plan view of a semiconductor wafer with mesas formed therefrom;

FIG. 2 is a cross-sectional view of the wafer shown in FIG. 1;

FIG. 3 is a cut-away pictorial representation of the wafer shown in FIGS. 1 and 2;

FIG. 4 is a schematic of the printed circuit of Unit I with one strip of Unit II shown in phantom overlaying the circuits of FIG. 1;

FIG. 5 is a partial sectional view of FIG. 4;

FIG. 6 represents a second embodiment of complete diode matrix;

FIG. 7 is a plan view with portions cut away of a modification of the device of FIG. 4;

FIG. 8 is a section taken along lines 8—8 of the FIG. 7 embodiment;

FIG. 9 is a schematic presentation of an indicator suitable for converting binary input codes to a decimal presentation; and

FIG. 10 shows a modified tube construction viewed as a section along lines **10—10** of FIG. 9 and illustrating pins in line for ease of understanding.

In general, the present invention provides a diode matrix which is principally formed by two units assembled together. The first unit has individual printed circuits which serve as the vertical conductors normally found in a diode matrix. The second unit has a plurality of P-N junction semiconductor strips which have had portions of the P-type material and adjacent N-type material cut away to a depth below the P–N junction, leaving flat-topped mounds, descriptively referred to through the specification and the claims as junction mesas. Although the mesas could be cut entirely (or only) from P-type material, it has been found that, if the P-N junctions are formed in each individual mesa, there results: a reduction in cross talk; an elimination in spurious transistor action between P-type elements; etc. Each junction mesa provides a P-N junction diode so that each strip further provides a number of diodes having individual P portions and a common N portion. These strips are mounted horizontally across the printed circuits, with each mesa of a strip bonded to, or engaged with, a different vertical printed circuit. The strips serve as the horizontal conductors normally found in such a matrix. Accordingly, there is provided a miniaturized diode matrix which, for instance, in an embodiment to be described below, provided 148 selectively positioned diodes in a space $1\frac{1}{16} \times \frac{3}{16}$ inches, and weighing less than 15 grams.

Consider FIGS. 1 and 2, of which the former is a top plan view of a wafer **11** of semiconducting material. The wafer **11** shown in FIG. 1 has been machined to form junction mesas **13**, each having an individual P-N junction. In a preferred embodiment, the wafer **11** was formed by initially having N-type silicon material whose upper half (i.e., the half lying toward the upper surface **12**) has diffused therein P-type impurities and whose lower half (lying toward the lower surface **14**) has diffused therein N-type impurities. In this preferred embodiment, the diffusion of the impurities is accomplished by first depositing P-type impurities such as boron on the upper surface of the wafer and/or depositing N-type impurities such as phosphorus pentoxide on the lower surface of the wafer. It should be understood that many other suitable P-type and N-type impurities are known in the art and may be used. The impurities are deposited on these surfaces by a gaseous deposition technique. Thereafter, the wafer **11**, with the P-type impurities deposited on its upper surface and/or the N-type impurities deposited on its lower surface, is subjected to heat at approximately 1300 degrees centigrade to diffuse the impurities into the wafer and form N-P junction material. The depth of the junction is dependent upon the amount of heat to which the wafer is subjected. In effect, then, there results a wafer-sized device with a P-N junction of relatively large area. While in a preferred embodiment, the material is initially N-type silicon, it is to be understood that any semiconducting material such as germanium could be used and, further, that the initial state of the material might be P-type semiconducting material.

After the wafer-sized P-N junction semiconductor has been produced, the wafer **11** is coated with a silver conducting paint **29** (FIG. 2) as will be more fully described hereinafter. It is to be understood that the inventive circuit is operative without the addition of the silver paint (which merely serves as a convenient bonding medium) and would be operative with another type of conductive coating to serve as a bonding medium. The wafer **11** is then machined ultrasonically to selectively remove portions of the P-type material and the integral or adjacent N-type material to a depth below the P-N junction depicted as dashed line **18**. The ultrasonic machining operation can be accomplished by means of a Sheffield Ultrasonic Cavitron, manufactured by The Sheffield Corp., Dayton, Ohio, or some other suitable ultrasonic machine tool device. After cutting away certain portions of the P-type and N-type materials there remains standing flat-topped mounds, or junction mesas **13**, each of which has an end coating of silver paint **29**. In addition to the junction mesas which remain, the wafer end portions **16** are likewise left standing. As will become apparent hereinafter, the end portions **16** serve as input signal connecting means.

FIG. 2 is a cross-sectional view cut along the line **2—2** of FIG. 1 showing the junction mesa protrusions **13** which form the bottom row **15** (FIG. 1). Although the lines of mesas in FIG. 1 lie along column positions, they will be referred to as rows since they assume row positions in most of the figures. It can be clearly seen from FIG. 2 how the junction mesas **13** (having individual P-N junctions at level **18**) provide a plurality of P-N junction diodes having individual P portions and a common N-type material portion, or bar **17**. The junction mesas **13** along row **15** are selectively disposed so that when the mesas engage the printed circuits of Unit I, to be described hereinafter, the diodes can be operated to energize a display means to effect a visual representation such as the numeral SIX.

Consider now FIG. 4 which represents Unit I. Printed circuit means are shown which are arranged to be used with the display means **19**. The vertical conducting paths **21** and the connectors **23** for the horizontal paths are printed with preparations which, by suitable treatment such as heating, produce continuous deposits of conducting material, such as silver, palladium, etc. on some suitable base **25** such as porcelain. A screen printing technique is employed according to a preferred method, but other well-known methods of printing circuits may be used. After the printed circuits have been placed on the base **25**, the assembly is "fired" or cured to bond the printed circuits to the base **25**.

The wafer **11**, whose fabrication has been described above, is then mounted over the vertical conducting paths **21** of Unit I. The rows of junction mesas **13** on the wafer **11**, such as row **15**, are positioned to run horizontally across the vertical conducting paths **21**. A marker **27** which is a circle with an X therein is shown in both FIGS. 1 and 4. If the wafer **11** of FIG. 1 is positioned with the junction mesas **13** coming in contact with the vertical conducting paths **21** so that the markers **27** of FIGS. 1 and 4 engage each other, then the row **15** of FIG. 1 will lie in the position shown in phantom between the dotted lines **15*a*** in FIG. 4. The mesas **13** in FIG. 4 are shown lying in registration and selective positions with respect to certain of the vertical conducting paths **21**.

After the wafer **11** is positioned in registration with the vertical conducting paths **21** of Unit I, the assembly is "fired" or cured to bond the junction mesas **13** and the end portions **16** of wafer **11** respectively to the vertical conducting paths **21** and the horizontal connectors **23**. In other words, the silver coating **29** described earlier and depicted in FIG. 2, is fused with the conducting material of which the printed circuits **21** and **23** are composed. The junction mesas **13** are each bonded to an associated vertical conducting path **21**. A single strip, such as strip **15*a***, will have each mesa bonded to a different vertical path although there may be many mesas from different strips bonded to the same vertical path. Mesas which are bonded to the same vertical path will have their common portions electrically isolated from each other when the wafer is sliced, which operation will be described presently.

With the wafer **11** bonded to the printed circuits, such that the surface **14** of FIG. 2 faces outwardly, the assembly is then again subjected to an ultrasonic machining operation. As was previously suggested, the ultrasonic machining operation can be accomplished with a Sheffiield Ultrasonic Cavitron, or some other suitable device. In this second machining operation, the wafer **11** is sliced between the rows of junction mesas **13**, as shown in FIG. 3, to form strips of semiconducting ma-

terial such as strip **15***a*. These strips are electrically isolated from each other and serve to provide the horizontal electrical conducting paths for the matrix, as well as for a plurality of P-N junction diodes. A strip **15***a* is shown positioned in FIG. 4. The strip **15***a*, which bears the mesas of row **15** (FIG. 1), is positioned to engage the vertical conducting paths **21** (FIG. 4) of Unit I so that an input signal to terminal **31** representing the numeral SIX will in fact energize the proper display elements **19** to represent the numeral SIX.

FIG. 5 is a partial sectional view of FIG. 4 cut along the line **5—5** thereof showing the strip **15***a* overlaying the base **25** and engaging certain of the printed circuits **21** and **23**. The junction mesas **13**, which have the individual P-N junctions are shown having an integral common N-type portion **17**. Each of the diodes is selectively engaged with a different one of the printed circuits **23**, as is evident in FIG. 5. This selective engagement enables a signal applied to the terminal **31** of FIG. 4 to provide a visual display of the numeral SIX, as discussed earlier. The strip **15***a* is bonded to the printed circuits **21** and **23** by means of the bonding medium **29**. The dashed line **18** indicates the relative position of the P-N junction level. It should be understood that the height of the mesas and the position of the P-N junction level are not drawn to scale but merely as illustrative.

If the vertical conducting paths **21** which are engaged by the diodes of strip **15***a* (FIG. 4) are traced to their respective terminating points, in the display device **19**, it will be found that the elements of the display device **19** which have the black circular dots therein will be the respective terminating points of the paths traced. The black circular dots present a visual representation of the numeral SIX. The black circles can be cathode elements of a device which has a common anode connected to point **32** and which is enclosed in neon gas, thereby providing an illuminated vertical display of the numeral SIX.

If the second row **33** of junction mesas **13** (FIG. 1) were engaged with the vertical conducting paths **21** (FIG. 4), there would be a further connection to the input terminal **35** representing the numeral SEVEN. If these last-mentioned paths were traced as described above, the numeral SEVEN would be visually represented at the terminating elements of the display means **19**.

The present inventive diode matrix has been described in connection with a visual display device for purposes of illustration. This inventive diode matrix has great utility with signal switching arrangements, for instance, code converters and the like. The diode matrix itself requires only the space enclosed by the dot-dash line **37** of FIG. 4 which, as stated earlier, in a preferred embodiment, is a space of $\frac{11}{16}$ x $\frac{3}{16}$ inches. The miniaturization of this diode matrix is made possible principally by fabricating a pulrality of strips of P-N material in the novel manner described and further, forming a plurality of diodes having individual P-type material portions and a common N-type material portion in the novel manner described earlier.

In a preferred embodiment, the entire assembly (the printed circuits with the strips bonded thereto) is potted or encapsulated in suitable material such as glass, epoxy resin, etc., to protect the elements from atmospheric effects. The molten encapsulating compound during the encapsulation finds its way between the layers and strips to fill the voids, for instance, between the mesas.

FIG. 6 is another embodiment of the present invention. The display means, such as means **19** of FIG. 4, are not shown in FIG. 6 but may be identical to means **19**, and would be connected to the upper ends of the vertical printed circuit paths **41**. In the embodiment shown in FIG. 6, the printed circuits on the base unit are shaped to provide horizontal circuit paths **43**. The circuit paths **41** and **43** are printed initially on some suitable base. Thereafter strips of semiconducting material with junction mesas formed therefrom (thereby providing a plurality of diodes), as described above, are positioned in vertical columns across the horizontal circuits **43**, as shown by the white circular dots **13***a*. The junction mesas are bonded to the horizontal printed circuits **43** as described earlier, in connection with FIGS. 4 and 5. Second printed circuit means providing vertical circuits **45** with input signal means included are then individually positioned over the semiconducting strips and bonded thereto to provide the vertical conductors and input signal means necessary to complete the diode matrix. If the input terminals of FIG. 6 are traced out and a display means similar to display means **19** (but inverted) is considered connected to paths **41**, it will be found that the proper output lines **41** are responsive to represent the numerals shown at the input signal terminals. Obviously, there are other ways of fabricating the unit with different combinations of printed circuits and diode overlays, which fabrication and resultant diode matrices are within the scope of the invention herein described

It will be clear to those skilled in the art that the devices shown in FIGS. 4 and 6 might be enclosed in a common glass envelope. In such a construction, the terminals **31**, **35**, etc. might be conductive pins extending through the envelope where they would be accessible to suitable signal sources. In addition, where the display elements **19** are cathode glow elements, the envelope would be filled with an ionizable gas such as neon or the like. Since neon is an inert gas, it would provide a favorable atmosphere for the diode matrix, or, if desired, the diode matrix could be encased in a protective medium such as glass or the like (not shown).

One suitable arrangement for enclosing the device of FIG. 4 in a glass envelope is shown in FIG. 7. The portion of the device shown in FIG. 5 is employed for this purpose. The construction of FIG. 7 includes a glass envelope **60** having a stem **64** which carries a plurality of conductive pins **68** which are accessible both outside and inside the envelope. The diode strips of the matrix, such as strip **15***a*, are supported on an insulating plate **66** which in turn may be firmly held in place by pins **68**. Each diode strip is electrically connected through its conductive silver paint **29** and a lead **67** to a respective tube pin **68**. Each conductive strip **21** on insulating circuit board **25** is connected to a pin, rivet, or plated-through element or the like **70** which extends through the board and makes contact with one of the display elements or cathodes **19**. Each strip, such as **15***a*, is connected through its own group of conductors **21** and pins **70** to a particular group of display elements **19**, such as the group forming the outline of the symbol SIX shown in FIG. 7.

As is well known in this type of gaseous indicator tube, an anode, which may include a screen **71** positioned between the display elements **19** and the viewing window of the envelope **60**, is likewise connected electrically through a lead **72** to an anode tube pin **68**. The sectional elevational view of FIG. 8 clearly illustrates the manner of connecting the strip of FIG. 5 into the tube envelope. It is also clear that the operation of the device of FIGS. 7 and 8 is identical to that described above with respect to FIG. 4.

The invention may also be modified in the manner shown in FIG. 10 to utilize a visual display device such as a Type 6844A indicator gas tube. This type of tube **73** comprises a gas-filled envelope **74** which includes an anode cut (not shown) connected to an anode screen **75** and a stack of glow cathodes **78** in the shape of characters mounted in the cup. Each cathode may be in the shape of a number, a letter, a symbol, or the like. With such a display device, it is customary to include NPN transistors between the diode matrix and the cathode characters. Any known technique for constructing transistors to provide emitter, base and collector electrodes may be utilized. Emitter and collector terminals **80**, **81**, respec-

tively, and a P type base **84** comprise a transistor **90**, and one such transistor is provided for each cathode character in the tube. All of the transistors may be mounted on a common insulating board **97**. The diode matrix and the strip of transistors may be constructed in forms such as taught in an application of Frederick F. Ohntrup, Serial No. 189,752, filed April 24, 1962, and assigned to a common assignee. In this particular construction, the individual diode elements appear in a conductor grid matrix at the appropriate code converting locations. This alternative diode matrix construction may likewise be included in the tube structure of FIG. 7 in place of the diode strips. The transistor strip made in this fashion may be encapsulated if desired.

In one arrangement as shown in FIG. 10, only a portion of a typical device using a Type 6844A tube is shown. The tube includes a stem **94** and pins **98**, and the diode matrix **37'** as viewed from the left of the first column of diodes **99** of the schematic presentation of FIG. 9. An insulating support plate **97** is mounted in the tube on the tube pins **98**. Plate **97** in turn supports row conductors **103** which are electrically connected to individual tube pins **98**. Column conductors **104** of the diode matrix are connected to individual base electrodes **84** of a strip of transistors **90** and also through individual bias resistors **106** to a base voltage supply pin **98**. The strip of transistors have their emitter electrodes **80** connected in common and to a common pin **98**. The collector electrodes **81** of the NPN transistors each are connected to individual cathode characters **78** and through stabilizing resistors **107**, if desired, to the positive voltage supply externally connectible to anode pin **98** of the tube.

As shown in the FIG. 9 schematic presentation of the tube of FIG. 10, the base of each transistor is connected to a column conductor **104** and receives through resistors **106** the bias voltage resulting from the positive base voltage supply connected to pin **98** designated B. The row wires **103** are connected to the binary coded input voltages applied to input and complement pins **98**. The diode positioning within the grid matrix is such as to enable the base electrode of one transistor only to receive an appropriate gated positive voltage with respect to the emitter reference potential applied to pin **98** designated C. With this construction, the binary coded signals and complements when applied permit the transistor connected to the single decimal equivalent cathode character **78** to give a visual decimal representation of the binary input.

It is clear that the elements of FIGS. 7–10 are shown in somewhat schematic form and not necessarily to scale in order to emphasize a ready understanding of the invention. The invention is not limited to the particular code conversion scheme described and other diode decode arrangements would, of course, be provided when converting from modified binary to decimal or binary to biquinary, for example.

While we have described above the principles of our invention in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation to the scope of our invention as set forth in the objects thereof and in the accompanying claims.

What is claimed is:

1. A character display tube comprising in combination: an envelope containing an ionizable gas capable of sustaining cathode glow; a plurality of tube pins sealed in said envelope and accessible both inside and outside said envelope; first means having a plurality of separate input signal and separate output signal electrical conducting paths, each of said conducting paths electrically isolated from each other; second means having a plurality of strips of semiconducting material each of which strips has a first portion of first type semiconducting material and a second portion of second type semiconducting material, said first type semiconducting material co-acting with said second type semiconducting material across the junction thereof to provide unidirectional current conducting means; each of said strips being formed so that its said first portion provides a bar of first type semiconducting material and its second portion provides one or more junction mesas primarily of second type semiconducting material, said mesas being common connected to said bar and selectively disposed relative to said bar, each bar having a unique arrangement of its mesas; said second means engaging in registration said first means such that both (1) each junction mesa of a strip is electrically connected to a different associated one of said output signal electrical conducting paths to form a matrix of unidirectional current conducting devices and (2) each of said bars is electrically connected to a different associated input signal electrical conducting path, each input signal path being connected to a separate one of said tube pins; an anode electrode mounted within said envelope; and a plurality of glow cathode display elements disposed in a selected arrangement in operative relation with said anode, each of said display elements capable of exhibiting cathode glow and being made visible and each connected to a different one of said output signal electrical conducting paths thereby enabling certain of said elements, forming an information pattern, to be rendered visible in response to an information signal being applied to any one of said input signal electrical conducting paths.

2. A character display tube comprising in combination: an envelope containing an ionizable gas capable of sustaining cathode glow; a plurality of tube pins sealed in said envelope and accessible both inside and outside said envelope; first means having a plurality of separate input signal and separate output signal electrical conducting paths, each of said conducting paths electrically isolated from each other; second means having a plurality of strips of semiconducting material each of which strips has a first portion of first type semiconducting material and a second portion of second type semiconducting material, said first type semiconducting material co-acting with said second type semiconducting material to provide diode means; each of said strips being formed so that there is provided one or more diodes, each diode having an individual first type semiconducting material portion while having with respect to evary other diode on its strip an integral common second type semiconducting material portion, said diodes being selectively disposed relative to said common portion, each strip having a unique arrangement of its diodes; said second means engaging in registration said first means, such that both (1) each diode of a strip is electrically connected to a different associated one of said output signal electrical conducting paths to form a diode matrix and (2) each of said common connected portions is electrically connected to a different associated input signal conducting path, each input signal path being connected to a separate one of said tube pins; an anode electrode mounted within said envelope; and a plurality of glow cathode display elements disposed in a selected arrangement in operative relation with said anode, each of said display elements capable of exhibiting cathode glow and being made visible and each connected to a different one of said output signal electrical conducting paths thereby enabling certain of said display elements to be rendered visible, forming an information pattern, in response to an information signal being applied to any one of said tube pins and its input signal electrical conducting path.

3. An information presentation tube comprising, in combination, an envelope containing an ionizable gas capable of sustaining cathode glow, a plurality of tube pins sealed in said envelope and accessible both inside and outside said envelope, a base member of electrically insulating material having on a surface thereof a plurality of generally parallelly extending electrically conducting paths, each of said conducting paths being electrically in-

sulated from one another, a wafer-like member composed of a plurality of strips of semiconducting material compactly assembled in parallel but electrically insulated relationship to one another, said strips having one or more protrusions of semiconducting material projecting from the same side thereof and forming separate unidirectional current conducting diodes, each strip having its diodes uniquely arranged, said diodes being integrally connected to their respective strips and disposed thereon in differently spaced relationship, said wafer-like member overlying a portion of the base member with the strips of semiconducting material extending crosswise to the conducting paths such that each diode of a strip is electrically connected to a different associated one of the conducting paths, input means connected to a separate one of said tube pins, individual to each strip and responsive to signal received thereby for delivering current to its strip for flow through the diodes thereof to their associated conducting paths, an anode electrode mounted within said envelope, and information presentation means comprising glow cathodes mounted in operative relation with said anode mounted on another portion of the base member and electrically connected to said conducting paths for exhibiting cathode glow and providing a readable presentation of the information represented by the signals received by said input means.

4. An information presentation tube comprising, in combination, an envelope containing an ionizable gas capable of sustaining cathode glow, a plurality of tube pins sealed in said envelope and accessible both inside and outside said envelope, a base member of insulating material mounted inside said envelope and having on a surface thereof a plurality of conductive paths, a wafer-like member mounted inside said envelope and composed of a plurality of strips of semiconducting material compactly assembled in parallel but electrically insulated relationship to one another, said strips having one or more protrusions of semiconducting material projecting from the same side thereof and forming separate unidirectional current conducting diodes, each strip having its diodes uniquely arranged, said wafer-like member overlying a portion of the base member and having each diode of a strip electrically connected to a different one of the conducting paths, input means individual to each strip and responsive to signals received thereby for delivering current to its strip for flow through the diodes thereof to their associated conducting paths, each input means being connected to a separate one of said tube pins, an anode electrode mounted within said envelope, and information presentation means comprising glow cathodes supported on a portion of the base member in operative relation with said anode and electrically connected to said conducting paths for exhibiting cathode glow and providing a readable presentation of the information represented by the signals received by said input means.

5. An information presentation tube comprising, in combination, an envelope containing an ionizable gas capable of sustaining cathode glow, a plurality of tube pins sealed in said envelope and accessible both inside and outside said envelope, a base member of electrically insulating material inside said envelope and having on a surface thereof a plurality of conducting paths, a plurality of strips of semiconducting diodes arrayed across said paths and in electrical contact with a group of said conducting paths, each group of diodes being uniquely spaced and electrically connected to a different group of conductive paths, separate input means coupled to each strip and responsive to signals received thereby for delivering current to its strip for flow through the diodes thereof to their associated conducting paths, each input means being connected to a separate one of said tube pins, an anode electrode mounted within said envelope, and information presentation means comprising glow cathodes mounted in operative relation with said anode and electrically connected to said conducting paths for exhibiting cathode glow and providing a readable presentation of the information represented by the signals received by said input means.

6. An information presentation tube comprising, in combination, an envelope containing an ionizable gas capable of sustaining cathode glow, a plurality of tube pins sealed in said envelope and accessible both inside and outside said envelope, a base member of electrically insulating material mounted inside said envelope and having on a surface thereof a plurality of electrically conducting output paths, each of said output paths being electrically insulated from one another, one or more bodies of semiconducting material, each of said bodies having one or more protrusions of semiconducting material projecting therefrom and forming separate unidirectional current conducting diodes, said diodes being integrally connected to their respective bodies and selectively disposed thereon, each body having its diodes uniquely disposed, means mounting said one or more bodies in overlying relation to a portion of the base member and over the output paths such that each diode of a body is electrically connected to a different associated one of the output paths, an electrical input path individual to each of said one or more bodies and connected to a separate one of said tube pins and operable upon receipt of a signal to deliver current to its respective body for flow through the diodes thereof to their associated output paths, an anode electrode mounted within said envelope, and information presentation means comprising glow cathodes mounted on another portion of the base member in operative relation with said anode and electrically connected to said output paths, said presentation means responding to current flow in the output paths for exhibiting cathode glow and providing a detectable presentation of information represented by the signals received by said input paths.

7. An information presentation device comprising, in combination,

a base member of electrically insulating material having on a surface thereof a plurality of electrically conducting paths,

said conducting paths being electrically insulated from one another,

a plurality of rows of diodes, each row having a common conductor, the rows being arrayed across said conducting paths,

the diodes of each row being electrically connected to different ones of said conducting paths, with each conducting path comprising the output for the diodes to which it is connected,

signal input means conductively connected to each row of diodes,

the positioning of the diodes with respect to said conducting paths being such that, when a group of signals is applied by said signal input means to said rows of diodes, only one conducting path receives a signal useful for purposes of information presentation,

transistors having input and output means,

each conducting path being connected to the input of an individual transistor,

a plurality of information presentation means supported by the base member and electrically connected to the outputs of said transistors,

and an envelope enclosing said base member, said rows of diodes, said transistors and said information presentation means,

said envelope including conductive pins coupled to said signal input means for applying input signals selectively to said rows of diodes to thereby cause a visible energization of one of said plurality of information presentation means.

8. An information presentation device comprising, in combination,

a base member of electrically insulating material having mounted thereon a plurality of row conductors,

individual diode elements arranged on said row conductors and uniquely spaced to form a rectangular matrix of diodes,

a plurality of column conductors making electrical contact with the diodes along the individual columns,

separate input means connected to each row conductor of the matrix,

a plurality of semiconductor switches, each having input and output electrodes, the input electrode of each switch being connected to a different column conductor so that it can be switched by a signal appearing thereon,

information presentation elements electrically coupled each to the output electrode of one of said semiconductor switches, each presentation element being adapted to be energized by its switch for providing a readable presentation of the information represented by signals received by said separate input means,

an envelope enclosing said base member, said rectangular matrix of diode elements and said information presentation elements,

said envelope including a plurality of conductive pins, one each being connected to the separate input means of the matrix,

and an anode means for said information presentation elements connected to another conductive pin.

9. An information presentation device as defined in claim **8**, wherein said information presentation elements includes a plurality of symbol shaped cathode glow electrodes arranged to glow singly when a plurality of row conductors are simultaneously energized in accordance with a coded input of voltages applied to respective groups of said conductive pins.

10. An information presentation device as defined in claim **9**, wherein said semiconductor switches comprise individual transistors which are mounted within said envelope and have their base electrodes connected to said column conductors and their collector electrodes to individual ones of said cathode glow electrodes so that only one transistor becomes biased into conduction at a time in response to said coded input of voltages.

11. An information presentation device as defined in claim **10**, wherein bias resistors are supported by said base member and have one end connected in common to another of said conductive pins and have their other ends connected individually to said column conductors.

12. An information display tube comprising, in combination,

an envelope having an ionizable gas capable of sustaining cathode glow,

a plurality of tube pins sealed in said envelope and accessible both inside and outside thereof,

a base member of electrically insulating material having mounted thereon a plurality of rows of diodes each having an input electrode and an output electrode,

each row of diodes having a unique physical spacing of its diodes along the row so that when the rows are compared, each has a different spacing of its diodes along the row,

each row of diodes having its input electrodes connected together to a common row conductor,

each row conductor being connected to a tube pin for the application of input signals thereto,

a plurality of output conductors mounted in operative relation with all of said rows of diodes but each electrically connected to a different group of diodes, each diode in a group being in a different one of said rows, and

information presentation means mounted in operative relation with said anode and electrically connected to said output paths for exhibiting cathode glow and providing a visual representation of the input signals applied to said row conductors.

13. An information presentation device as defined in claim **12**, wherein said information presentation elements are arranged in a rectangular matrix array of cathode glow electrodes arranged to glow in various groups representing visible symbol input information when a plurality of column conductors are simultaneously energized as a result of the selected application of voltage to a single one of said row conductors.

14. The tube defined in claim **12** and including semiconductor switches in circuit between each output conductor and an information presentation element.

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