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(71) **Applicant** *(for all designated States except US)*: **ADVANCED POWER CONVERSION PLC** [GB/GB]; Unit B5, Armstrong Mall, Southwood Summit Centre, Farnborough, Hants GU14 0NR (GB).

(72) **Inventor; and**
(75) **Inventor/Applicant** *(for US only)*: **STEPHENS, John** [GB/GB]; 59 Fennel Close, Basingstoke RG24 8XF (GB).

(74) **Agent: HILLGATE PATENT SERVICES**; 6 Aztec Row, Berners Road, Islington, London N1 0PW (GB).

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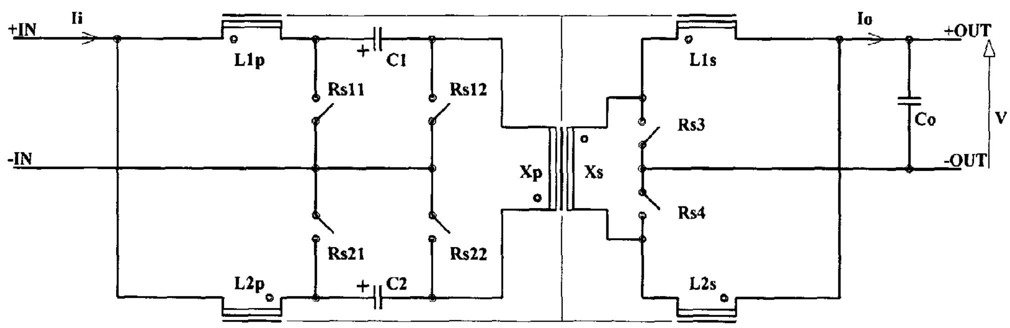
(54) **Title:** A CONVERTER



(57) **Abstract:** A DC-DC converter comprises a primary circuit fed by a DC power source. The primary circuit comprises a transformer primary winding having a first end coupled to one side of the DC power source through a capacitor and inductor, the capacitor being coupled to the second side of the DC power source through a switching means comprising a pair of switches connected to the inductor side and transformer primary winding side of the capacitor; a transformer coupling the primary and secondary circuits together; a secondary circuit including a transformer secondary winding and rectifying means for producing a DC output; and control circuitry operating the switches of the switching means to connect the second side of the DC power source to the inductor side and transformer primary winding side of the capacitor alternately, such that the capacitor discharges through the primary winding alternately. The control circuitry for the switching means causes a transient delay in the closing of one switch relative to the opening of the other switch of the switching means.

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A Converter

The present invention relates to a converter, typically for a power supply for supplying a continuous output current, from a continuous input current, with particular applications, amongst others, as power supplies for examples in automotive or telecoms applications.

Transformers used in electrical and electronic applications for 'transforming' an input voltage to a higher or lower voltage (and often referred to as "Buck" and "Boost" converters respectively) are well known to persons skilled in the art. A problem with known transformers is to provide assemblies which operate with both continuous input and output currents. This is possible with a series of boost and buck converters, but a simple cascade of these two has an increased component count and is additionally complex to drive the devices.

A known DC – DC converter is described in US 5 886 882 (Rodolpho), which features primary and secondary transformer windings, together with two pairs of primary and secondary choke windings, wound upon a three limbed core. A switching circuit is coupled between the first primary choke and the primary transformer winding, and a similar switching circuit is coupled between the first secondary choke and the primary transformer winding. Each switching circuit comprises a capacitor, diode and a MOSFET. The switching circuits are switched on and off in a cyclic manner (the MOSFETs being driven by two interleaved square pulse trains) to provide a continuous output current from a continuous input current in a push-pull manner.

It is an object of the present invention to provide a DC to DC converter and method of driving it to efficiently produce a continuous output current for a continuous input current.

According to the present invention there is provided a DC-DC converter comprising:

a primary circuit fed by a DC power source;

the primary circuit comprising a transformer primary winding having a first end coupled to one side of the DC power source through a capacitor and inductor, the capacitor being coupled to the second side of the DC power source through a switching means comprising a pair of switches connected to the inductor side and transformer primary winding side of the capacitor;

a transformer coupling the primary and secondary circuits together;

a secondary circuit including a transformer secondary winding and rectifying means for producing a DC output; and

control circuitry operating the switches of the switching means to connect the second side of the DC power source to the inductor side and transformer primary winding side of the capacitor alternately, such that the capacitor discharges through the primary winding alternately;

characterised in that the control circuitry for the switching means causes a transient delay in the closing of one switch relative to the opening of the other switch of the switching means.

Preferably, the second end of the transformer primary winding is connected to the DC power source through a second capacitor and second inductor, the second capacitor being coupled to the second side of the DC power source through a second switching means comprising a second pair of switches connected to the inductor side and transformer primary winding side of the capacitor;

Preferably, there is provided a delay between one capacitor discharging through the primary coil, and the other capacitor discharging through the primary coil.

According to another aspect of the invention, there is provided a DC-DC converter comprising:

a primary circuit fed by a DC power source;

the primary circuit comprising a transformer primary winding having each end coupled to the same side of the DC power source through a respective capacitor and inductor, each capacitor being coupled to the second side of the DC power source through respective switching means comprising a pair of switches connected to the inductor side and transformer primary winding side of the capacitor;

a transformer coupling the primary and secondary circuits together;

a secondary circuit including a transformer secondary winding and rectifying means for producing a DC output; and control circuitry operating the switches of each switching means to connect the second side of the DC power source to the inductor side and transformer primary winding side of each capacitor alternately, such that each capacitor discharges through the primary winding alternately;

characterised in that the control circuitry operates the at least one of the switches when there is substantially no voltage across it.

According to another aspect of the invention, there is provided a DC-DC converter comprising:

a primary circuit fed by a DC power source;

the primary circuit comprising a transformer primary winding having each end coupled to the same side of the DC power source through a respective capacitor and inductor, each capacitor being coupled to the second side of the DC power source through respective switching means comprising a pair of switches connected to the inductor side and transformer primary winding side of the capacitor;

a transformer coupling the primary and secondary circuits together;

a secondary circuit including a transformer secondary winding and rectifying means for producing a DC output; and

control circuitry operating the switches of each switching means to connect the second side of the DC power source to the inductor side and transformer primary winding side of each capacitor alternately, such that each capacitor discharges through the primary winding alternately;

characterised in that for one or both switch means, the switch connected to the transformer primary winding side of the capacitor is kept open for approximately twice the period over a complete switching cycle that the switch connected to the inductor side of the capacitor is kept open for.

A converter according to the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows a circuit diagram of a converter;

Figure 2 shows the current flow during the basic phases of a cycle in the converter;

Figure 3 shows the voltages and currents across particular components due to the basic phases;

Figure 4 shows the switching timings of the converter;

Figures 5 to 9 shows other embodiments of the converter;

Figure 10 shows alternative switching timings of the converter; and

Figure 11 shows a further embodiment of the converter;

Referring to Figure 1, the converter comprises an input, an output, and a transformer assembly having a ferrite core. The core is formed from two 'E' shaped core pieces, each core piece having three limbs. The core pieces are placed together to form three limbs. Primary and secondary transformer windings x_p and x_s are provided on the centre limb of the ferrite core. Windings L_{1p} and L_{1s} are provided on an outer limb to form primary and secondary chokes, and windings L_{2p} and L_{2s} on the other outer limb form a second pair or primary and secondary chokes. Other core shapes, such as ‘I’ shaped pieces, may be used.

A capacitor C_1 is provided between the primary transformer winding x_p and the first primary choke winding L_{1p}. Similarly, a capacitor C_2 is provided between the primary transformer winding x_p and the second primary choke winding L_{2p}. Two switches RS_{11} and RS_{21} are coupled between the capacitor C_1 and the first primary choke winding L_{1p}, and capacitor C_2 and the second primary choke winding L_{2p} respectively. Similarly, two switches RS_{12} and RS_{22} are coupled between the capacitor C_1 and the primary transformer winding x_p, and capacitor C_2 and the primary transformer winding x_p. The switches RS_{11} and RS_{12} and the capacitor C_1 form a first switching circuit for the first primary choke winding L_{1p}, and the switches RS_{21} and RS_{22} and the capacitor C_2 form a second switching circuit for the second primary choke winding L_{2p}

An input voltage is applied to the first primary choke winding L_{1p} and the first switching circuit, and to the second primary choke winding L_{2p} and the second switching circuit.

In the secondary circuit, the secondary transformer winding x_s is connected between the first secondary choke winding L_{1s} and the first secondary choke winding L_{2s}. Two switches RS_3 and RS_4 are coupled to points between the secondary transformer winding x_s and the first secondary choke winding L_{1s}, and between the secondary transformer winding x_s and the second secondary choke winding L_{2s}. A capacitor C_o is coupled across the output for smoothing.

Referring to figure 2, the basic cycle of the circuit has four separate phases. In this figure, the first primary choke is labelled L_{xfmr1}, the second primary choke is labelled L_{xfmr2}, the primary transistor winding is labelled L_{xfmr3}, the secondary transistor winding is labelled L_{xfmr33}, first secondary choke is labelled L_{xfmr11}, the second secondary choke is labelled L_{xfmr22}. It will also be noticed that for the purposes of explaining the basic mode of operation, the pair of switches RS_{11} and RS_{12}, has been illustrated as a single switch having two contact positions RS_{11} and RS_{12}. Switch pair RS_{21} and RS_{22} have been simplified in a corresponding manner. A capacitor C_i is added across the voltage source (here a battery) to smooth the input.

In an initial state (say before t_0), switches RS_{12} and RS_{22} are closed in the primary circuit, while RS_{11} and RS_{21} are open. Capacitor C_1 is charged through the first primary choke winding L_{1p}, and similarly capacitor C_2 is charged through the second primary choke winding L_{2p} at the input voltage. Capacitors C_1 and C_2 are sufficiently large to smooth the ripple voltage caused by switching, and the choke windings L_{1p} and L_{2p} are sufficiently large to smooth the ripple current.

Figure 3 shows the currents and/or voltages across various of the components in the circuit through two switching cycles. Figure 3 shows respectively the current across the switches RS_{11}, RS_{12}, RS_{21}, and RS_{22}, the voltage across the switches RS_{11}, RS_{12}, RS_{21}, and RS_{22}, the current across the first and second primary choke windings L_{1p} and L_{1p}, the current through the capacitors C_1 and C_2, the voltage across the primary transformer winding x_p, the magnetic current across the primary transformer winding x_p, the total current across the primary transformer winding x_p, the voltage across the secondary transformer winding x_s, the current through the diodes D_1 and D_2, (which are substantially equivalent to the switches RS_3 and RS_4 of figure 1) the current across the first and second secondary choke windings L_{1s} and L_{1s}, and the current through the smoothing capacitor C_o.

Referring back to Figure 2, at a time t_0, switch RS_{11} is closed and RS_{12} is opened. The voltage across C_1 is applied upon the primary transformer winding x_p, the secondary voltage at x_s reverse biases D_1 and causes the current to increase through x_s. The current in D_2 increases to the sum of both the currents flowing in L_{xfmr11} and L. The output voltage is dependent upon the turn ratio of the primary and secondary transformer windings x_p and x_s, the secondary choke arrangement halving the output voltage, half the current flowing through each inductor.

At a time t_1, switch RS_{11} is opened and RS_{12} is closed. The primary transformer winding x_p is clamped by RS_{22} and RS_{12} to 0 volts, the stored energy in the primary transformer winding x_p circulating as current. The secondary transformer winding x_s is clamped by the primary transformer winding. Energy stored in the first secondary choke winding circulates as current through D_1. Current through the first primary choke L_{1p} decreases and capacitor C_1 recharges. The current through L_s decreases.

At a time t_2, switch RS_{22} is opened and RS_{21} is closed. The charge on capacitor C_2 discharges through the primary transformer winding x_p, taking the lower connection negative and causing a current to flow through D_1 and x_s. As previously, the output voltage is dependent upon the turn ratio of the transformer windings.

At a time t_3, switch RS_{21} is opened and RS_{22} is closed. The primary transformer winding x_p is clamped by RS_{22} and RS_{12} to 0 volts, the stored energy in the primary transformer winding x_p circulating as current. The secondary transformer winding x_s is clamped by the primary transformer winding. Energy stored in the second secondary choke winding circulates as current through D_2. This phase resets the transformer. At t_4, the circuit switches as described from t_0, and the cycle is repeated indefinitely.

It can be shown that the output voltage, V_o,

$$V_o = N_s/N_p \cdot V_i \cdot D/(1-D)$$

where V_i is the input voltage,. N_s/N_p is the transformer turn ratio, and D is the duty cycle of the switching circuits.

The switches are operated by a control circuit (not here shown). A typical switching cycle would be over a 5μs period, as shown in Figure 4. Initially, only switch RS_{12} is closed, whilst all the other switches are open. After 0.1μs, switch RS_{22} is closed. After 0.7μs from the beginning of the cycle switch RS_{12} is opened. At 0.8μs from the beginning of the cycle, RS_{11} is closed. 2.5μs through the cycle, RS_{11} is opened. At 2.6μs from the beginning of the cycle, switch RS_{12} is closed. At 3.2μs from the beginning of the cycle, switch RS_{22} is opened, and at 3.3μs from the beginning of the cycle, switch RS_{21} is closed. Switch RS_{21} is opened 5μs from the beginning of the cycle, which marks the start of a new cycle.

It will also be seen that during this time, diodes D_1 and D_2 follow the timings of RS_{12} and RS_{22} respectively. Switches, such as MOSFETs could though be used instead or diodes.

When each switching circuit is switched, it will be seen that there is a delay between the first switch opening and the second switch closing, (i.e. between RS_{12} opening and RS_{22} closing, between RS_{22} closing and RS_{12} closing, between RS_{22} opening and RS_{21} closing, and between RS_{21} opening and RS_{22} closing). Under this timing sequence, the delay is 0.1µs, but the optimum delay is dependant upon the components in the circuit, throughput power, supply voltage, operational switching frequency and other effects. Typical delays range from 50ns to 100ns.

The ferrite core indicated in figure 1 as a dotted line, and as previously mentioned, is formed from two 'E' or 'I' shaped core pieces. The ferrite cores need not be in this integral form however. Referring to figure 5, the windings L_{1p}, L_{1s}, L_{2p} and L_{2s} may be provided as discrete magnetic components (Windings x_p and x_s sharing a single magnetic core in this and every other embodiment).

Referring to Figure 6, the first and second primary choke windings L_{1p} and L_{2p} may be magnetically coupled to the transformer windings x_p and x_s. The first and second secondary choke windings L_{1s} and L_{2s} are each magnetically discrete components. Conveniently, the first and second primary choke windings L_{1p} and L_{2p} are wound upon the outer limbs of the core, while the first and second secondary choke windings L_{1s} and L_{2s} are provided as discrete inductors.

Referring to Figure 7, the first and second secondary choke windings L_{1s} and L_{2s} are magnetically coupled to the transformer windings x_p and x_s, the first and second primary choke windings L_{1p} and L_{2p} being magnetically discrete components. In a similar manner to the previous embodiment the first and second secondary choke windings L_{1s} and L_{2s} are conveniently wound upon the outer limbs of the core, while the first and second primary choke windings L_{1p} and L_{2p} are provided as discrete inductors.

In an alternative circuit, shown in figure 8, the first primary choke winding L_{1p} is magnetically coupled to the first secondary choke winding L_{1s} in a discrete magnetic component, and the second primary choke winding L_{2p} is likewise magnetically coupled to the second secondary choke winding L_{2s}.

It will be realised of course that different inductors may be coupled by different degrees. Rather than all the inductors (with the exception of the transformed inductors, which are always substantially tightly coupled) being discrete components with no coupling between them, some inductors may be loosely coupled.

A fully or partially integrated form of circuitry, where the primary and secondary choke windings are coupled, allows the input and output ripple currents to be steered so that the net output is relatively free from ripple.

The switching of a switching circuit associated with a particular winding applies an AC waveform, via the decoupling capacitor, to a any second or further winding which is magnetically coupled to the first. By applying an AC waveform to the second winding matching the switching waveform of the first winding, the current flow into the first winding, caused by the switching action, can be halved. Also, by changing the turns ratio between the first and second windings, it becomes possible to further reduce the ripple current in the first winding, to the extent that the switching frequency ripple current can be reduce close to zero. This technique has the effect of apparently increasing the inductance of the first winding to a value significantly greater than the actual electronic value.

Referring to Figure 9, capacitors C_{rs11} and C_{rs21} may be provided in parallel with switches RS_{11} and RS_{21}. The primary transformer winding is in reality not completely coupled to the secondary winding, but includes a component of pure inductor which is represented here as L_{ZVRT}.

The capacitances C_{rs11} and C_{rs21} are coupled with the primary transformer winding's reactance to establish a resonant circuit such that the switching is effected at zero volts.

When RS_{11} is closed, the charge accumulated on C_{rs11} discharges through RS_{11}, and C_{rs21} similarly discharges on RS_{12}'s closing. In this manner, a waveform is obtained that counteracts the effect of the parasitic inductance L_{ZVRT} and reduces the losses otherwise attributable to it.

Rs21 and Rs22 are, by circuit operation, switched-ON with zero volt across them. On opening, the current flow is through the capacitors due to the capacitors charging-up (CV=IT). The capacitance, rather than being provided as a discrete component, may be an integral parasitic feature of the MOSFET (C_{oss}). If it is external to the MOSFET i.e. additional capacitors as shown, then there are greatly reduced turn-OFF losses in RS_{11} and RS_{21}.

The inductance L_{zvrt} and the capacitors C_{rs11} and C_{rs21} form a resonant tank swinging the voltage across the switch to zero at which point the MOSFET, Rs11 or Rs21 as the case may be, are switched-ON.

By switching the MOSFETs at the correct time and utilising ZVRT (Zero Volt Resonant Transition) switching noise (and the losses it causes) of RS_{11} and RS_{21} can be reduced. It is dependant upon the rate of change of voltage across the MOSFETs, this being controlled by the capacitors Crs11 and Crs21.

Other switching regimes may be followed. Such a further switching regime is shown in Figure 10. As is the previous example, the switching cycle is over a 5μs period. Initially, only switches D_1 and D_1 (referring also to the circuit in Figure 2) are closed, all the other switches being open. After 0.1μs from the beginning of the cycle, switches RS_{22} is closed. After 0.8μs from the beginning of the cycle switch RS_{11} is closed whilst D_1 is opened. At 2.5μs from the beginning of the cycle, switches RS_{11} and RS_{22} are opened whilst D_1 is closed. 2.6μs through the cycle, switch RS_{21} is closed. At 3.3μs from the beginning of the cycle, switch RS_{21} is closed and D_2 is opened. At the end of the cycle, i.e. 5μs from the beginning of the cycle, switches RS_{12} and RS_{21} are opened and D_2 is closed. The cycle then repeats.

In this timing regime, it can be seen that the switches RS_{11} and RS_{22} are kept open for a longer period than in the previous timing regime. The switches therefore are not switched at zero volts, and cannot be switched in a resonant manner to reduce the inductive losses of the transformer winding. When in the open position however, the switches conduct no current and therefore will not dissipate energy, so the circuit is made more efficient.

The primary circuit may drive two or more secondary circuits. Figure 11 shows two secondary circuits (the second secondary circuit having similar components as the secondary circuit already described) magnetically coupled to the primary circuit. The windings and capacitance's may of course be different, so that the two secondary circuits give different output voltages.

The switches described here have been MOSFETs, but other switching devices could substituted. Conveniently, RS_{11}, RS_{12}, D_1 and D_2 could be n-channel MOSFETs, while RS_{21} and RS_{22} are p-channel MOSFETs. Alternatively, a p-channel MOSFET with a Schottky diode coupled across it could be used for the switches RS_{21} and RS_{22}. RS_{21} and RS_{22} could also be n-channel MOSFETs with a Schottky diode coupled across it. Diodes D_1 and D_2 could conveniently be Schottky diodes. Other suitable transistors or other switching devices will be apparent to one skilled in the art.

The principles disclosed herein could equally be applied to other DC-DC converter topographies, such as circuits having only one discharging capacitor in the primary circuit, and a correspondingly simplified secondary circuit.

Claims

1. A DC-DC converter comprising:

a primary circuit fed by a DC power source;

the primary circuit comprising a transformer primary winding having a first end coupled to one side of the DC power source through a capacitor and inductor, the capacitor being coupled to the second side of the DC power source through a switching means comprising a pair of switches connected to the inductor side and transformer primary winding side of the capacitor;

a transformer coupling the primary and secondary circuits together;

a secondary circuit including a transformer secondary winding and rectifying means for producing a DC output; and

control circuitry operating the switches of the switching means to connect the second side of the DC power source to the inductor side and transformer primary winding side of the capacitor alternately, such that the capacitor discharges through the primary winding alternately;

characterised in that the control circuitry for the switching means causes a transient delay in the closing of one switch relative to the opening of the other switch of the switching means.

2. A converter according to claim 1, wherein the second end of the transformer primary winding is connected to the DC power source through a second capacitor and second inductor, the second capacitor being coupled

to the second side of the DC power source through a second switching means comprising a second pair of switches connected to the inductor side and transformer primary winding side of the capacitor;

3. A converter according to previous claim 2 characterised in that there is provided a delay between one capacitor discharging through the primary coil, and the other capacitor discharging through the primary coil.

4. A converter according to claim 3 characterised in that period of the delay is approximately the same as the period over which one of the capacitors is discharged.

5. A converter according to any previous claim characterised in that the control circuitry operates at least one of the switches when there is substantially no voltage across it.

6. A converter according to any previous claim characterised in that for one or both switch means, the switch connected to the transformer primary winding side of the capacitor is kept open for approximately twice the period over a complete switching cycle that the switch connected to the inductor side of the capacitor is kept open for.

7. A converter according to any previous claim characterised in that the control circuitry operates the switches such that the switch coupled when the voltage across it is substantially zero.

8. A converter according to any previous claim characterised in that the transient delay is approximately 1μs.

9. A DC-DC converter comprising:

a primary circuit fed by a DC power source;

the primary circuit comprising a transformer primary winding having a first end coupled to one side of the DC power source through a capacitor and inductor, the capacitor being coupled to the second side of the DC power source through a switching means comprising a pair of switches connected to the inductor side and transformer primary winding side of the capacitor;

a transformer coupling the primary and secondary circuits together;

a secondary circuit including a transformer secondary winding and rectifying means for producing a DC output; and

control circuitry operating the switches of the switching means to connect the second side of the DC power source to the inductor side and transformer primary winding side of the capacitor alternately, such that the capacitor discharges through the primary winding alternately;

characterised in that the control circuitry operates the at least one of the switches when there is substantially no voltage across it.

10. A DC-DC converter comprising:

a primary circuit fed by a DC power source;

the primary circuit comprising a transformer primary winding having a first end coupled to one side of the DC power source through a capacitor and inductor, the capacitor being coupled to the second side of the DC power source through a switching means comprising a pair of switches connected to the inductor side and transformer primary winding side of the capacitor;

a transformer coupling the primary and secondary circuits together;

a secondary circuit including a transformer secondary winding and rectifying means for producing a DC output; and

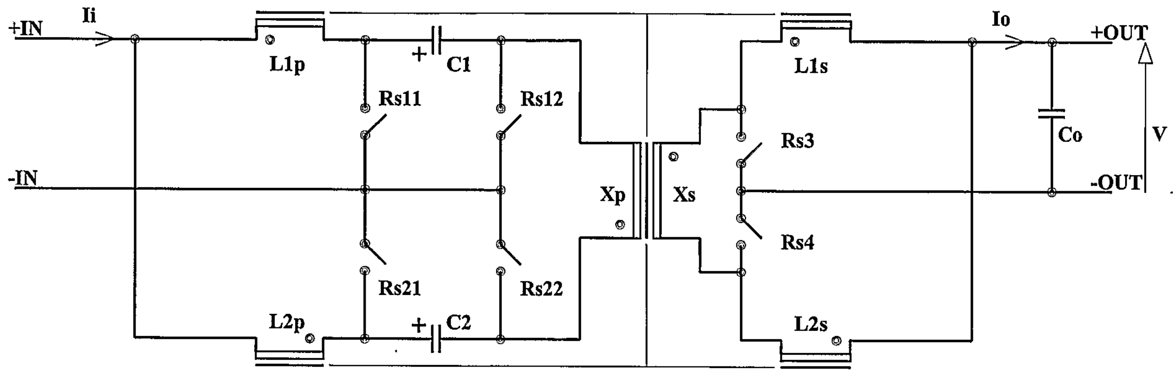
control circuitry operating the switches of the switching means to connect the second side of the DC power source to the inductor side and transformer primary winding side of the capacitor alternately, such that the capacitor discharges through the primary winding alternately;

characterised in that for one or both switch means, the switch connected to the transformer primary winding side of the capacitor is kept open for approximately twice the period over a complete switching cycle that the switch connected to the inductor side of the capacitor is kept open for.

11. A primary circuit according to any previous claim.

12. A converter as herein described and illustrated.

13. Any novel and inventive feature or combination of features specifically disclosed herein within the meaning of Article 4H of the International Convention (Paris Convention).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Ii
L1p
C1
Rs11
Rs12
-IN
Xp
Xs
Rs21
Rs22
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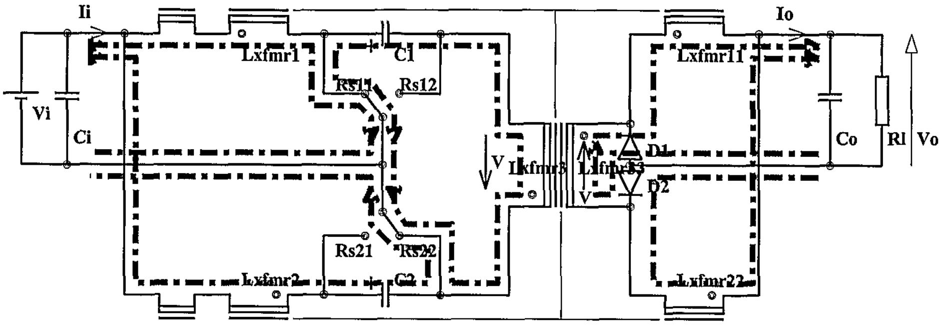
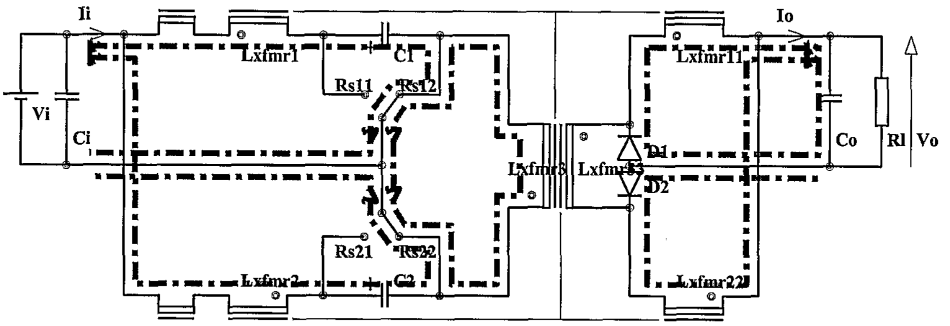
L1s
Rs3
Rs4
L2s
Io
+OUT
Co
V
-OUT

Fig. 1

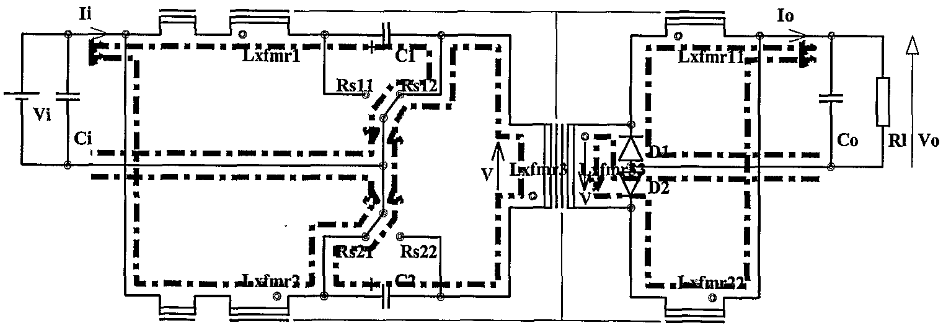
t0 to t1



t1 to t2



t2 to t3



t3 to t4

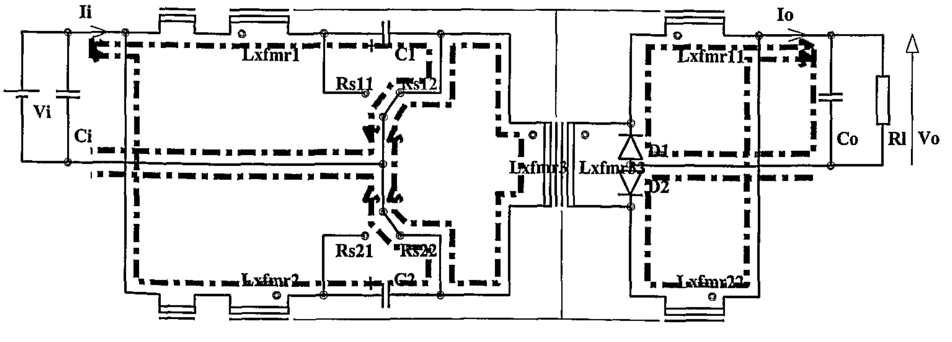
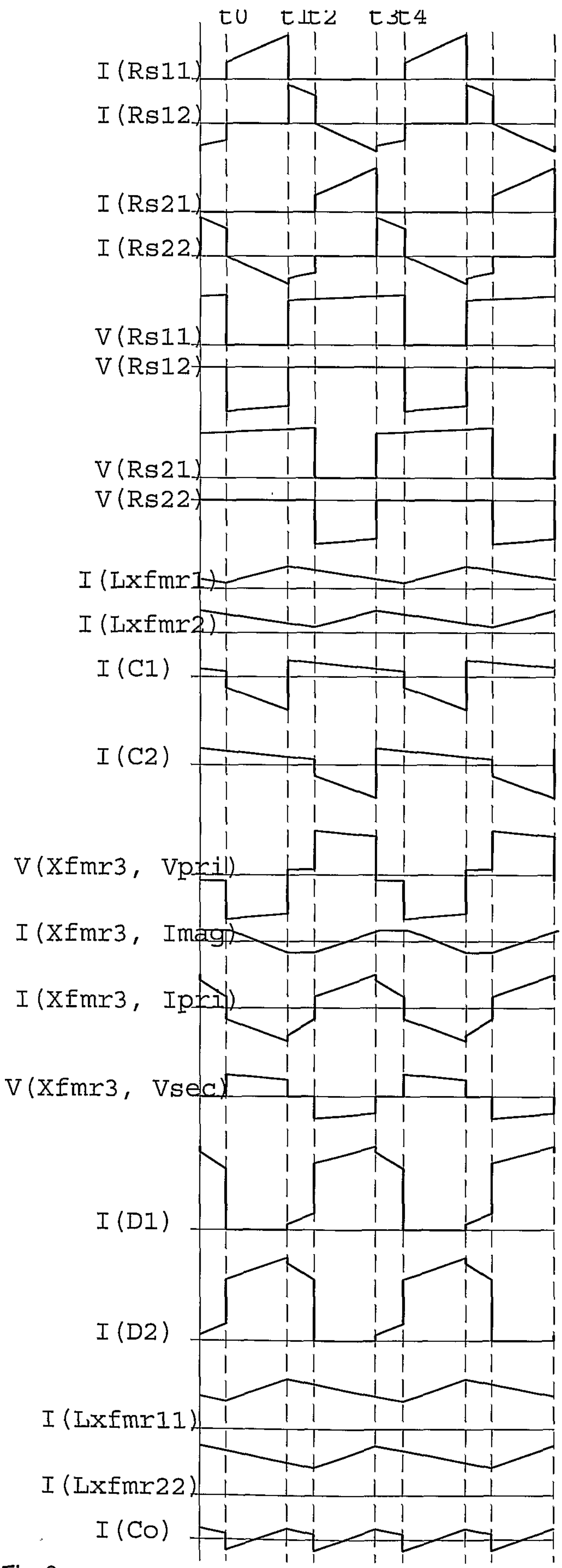


Fig 2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I(Rs12)
I(Rs21)
I(Rs22)
V(Rs11)
V(Rs12)
V(Rs21)
V(Rs22)
I(Lxfmr1)
I(Lxfmr2)
I(C1)
I(C2)
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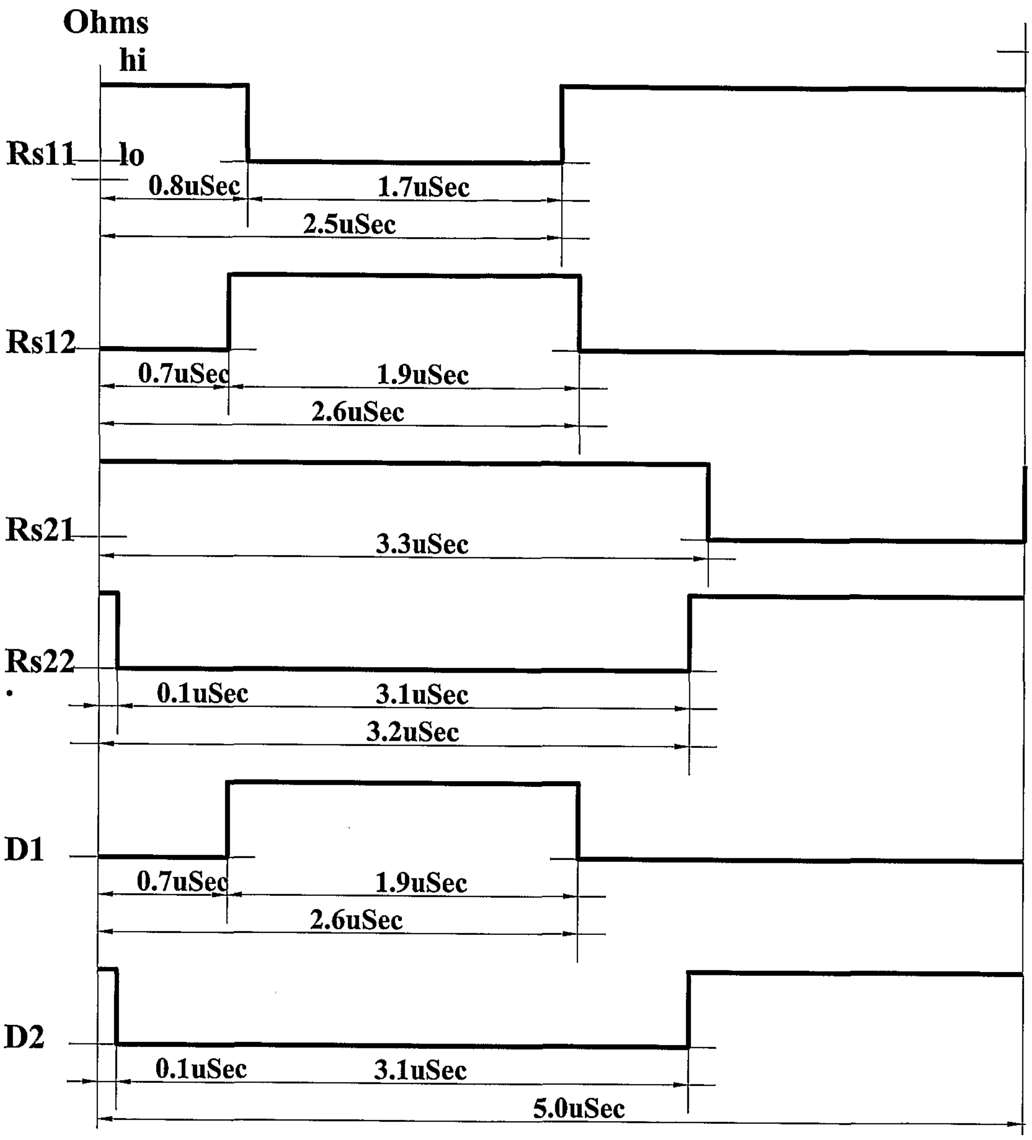
Fig. 3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1.9uSec
2.6uSec
D2
0.1uSec
3.1uSec
5.0uSec

Fig 4

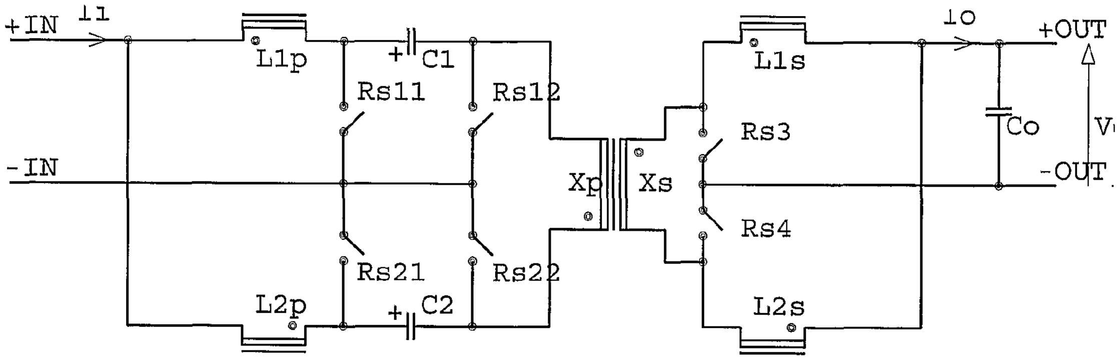


Fig. 5

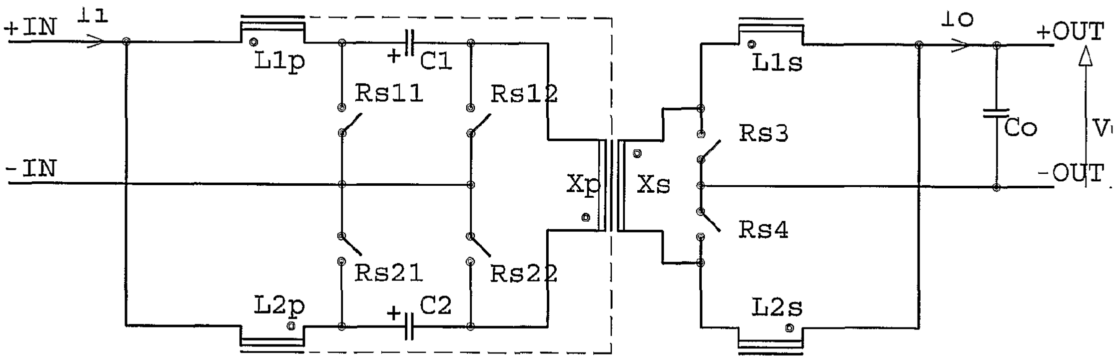


Fig. 6

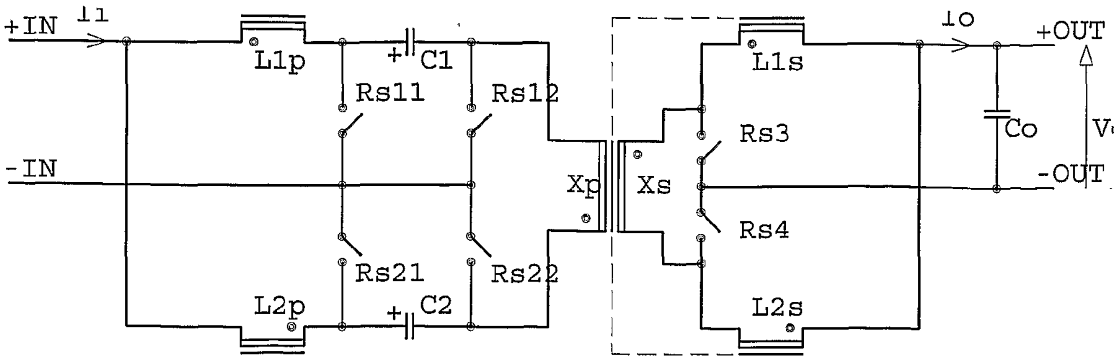
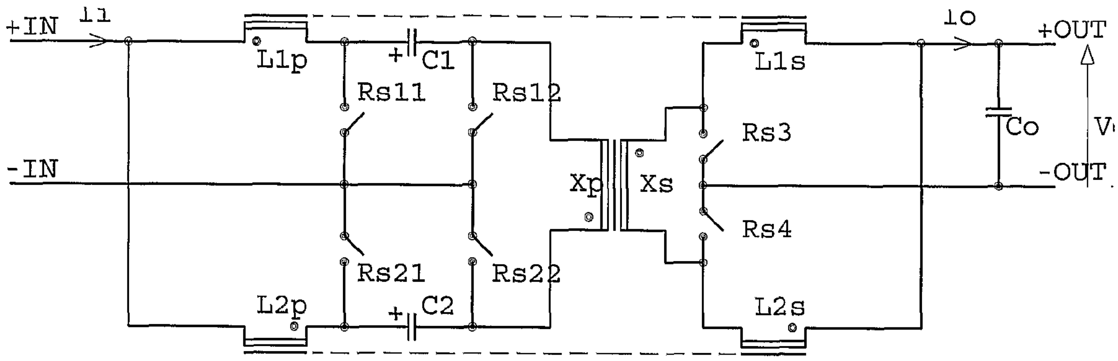


Fig. 7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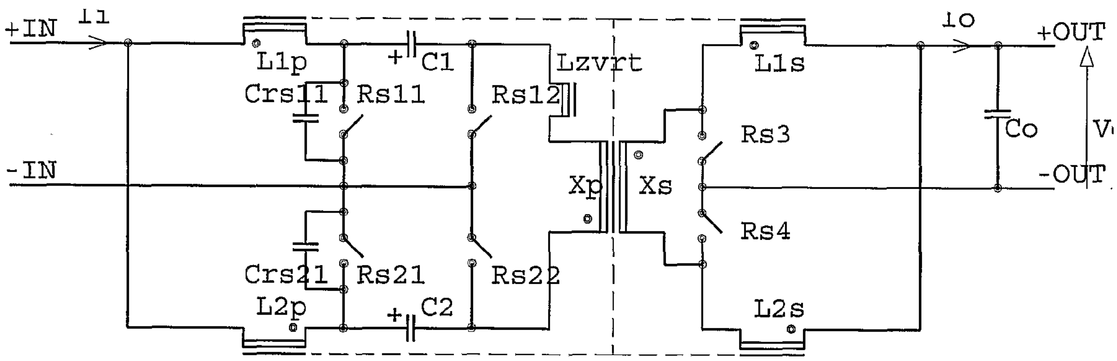
L1p
C1
Rs11
Rs12
-IN
Xp
Xs
Rs21
Rs22
L2p
C2
L1s
Rs3
Rs4
L2s
Io
+OUT
Co
-OUT

Fig. 8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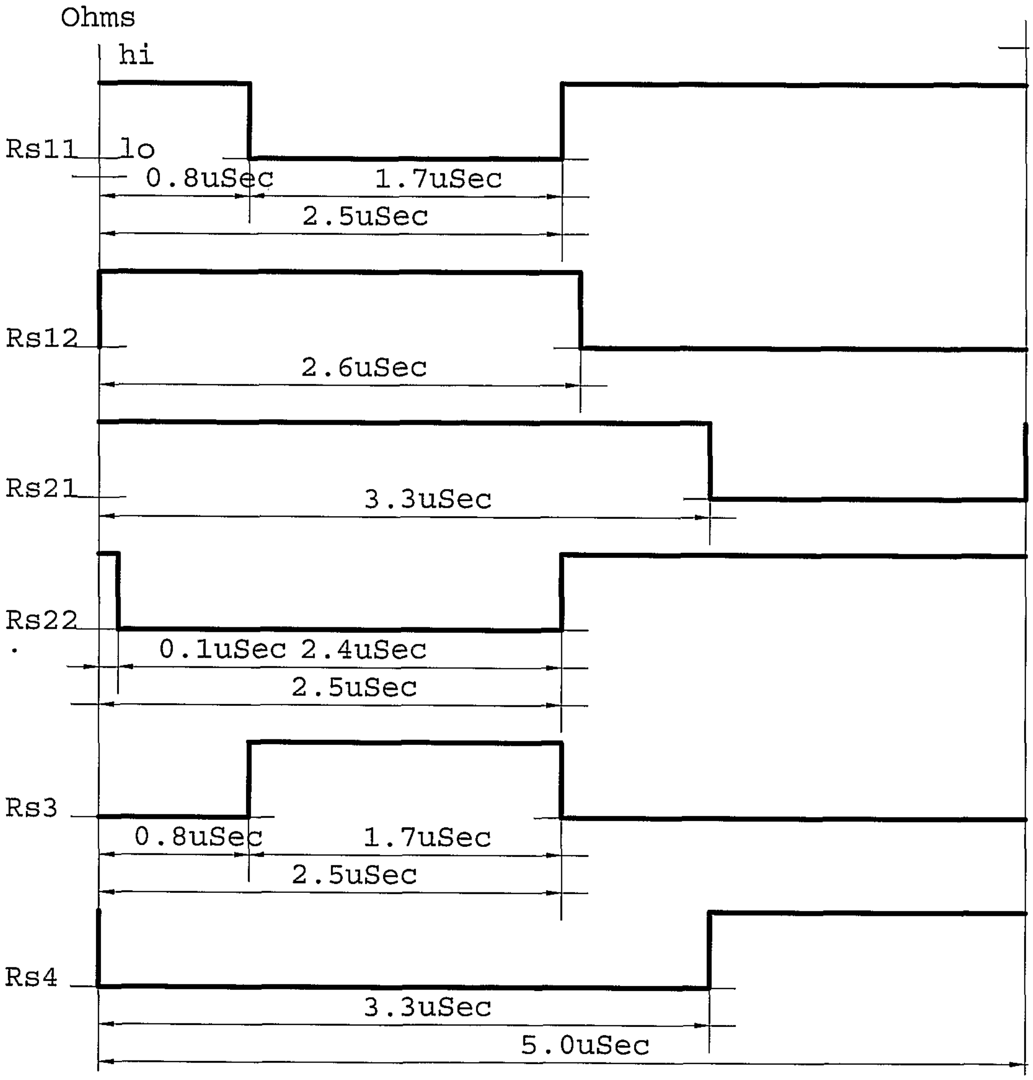
C1
Lzvrt
Crs11
Rs11
Rs12
-IN
Xp
Xs
Crs21
Rs21
Rs22
L2p
C2
L1s
Rs3
Rs4
L2s
Io
+OUT
Co
-OUT

Fig. 9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lo
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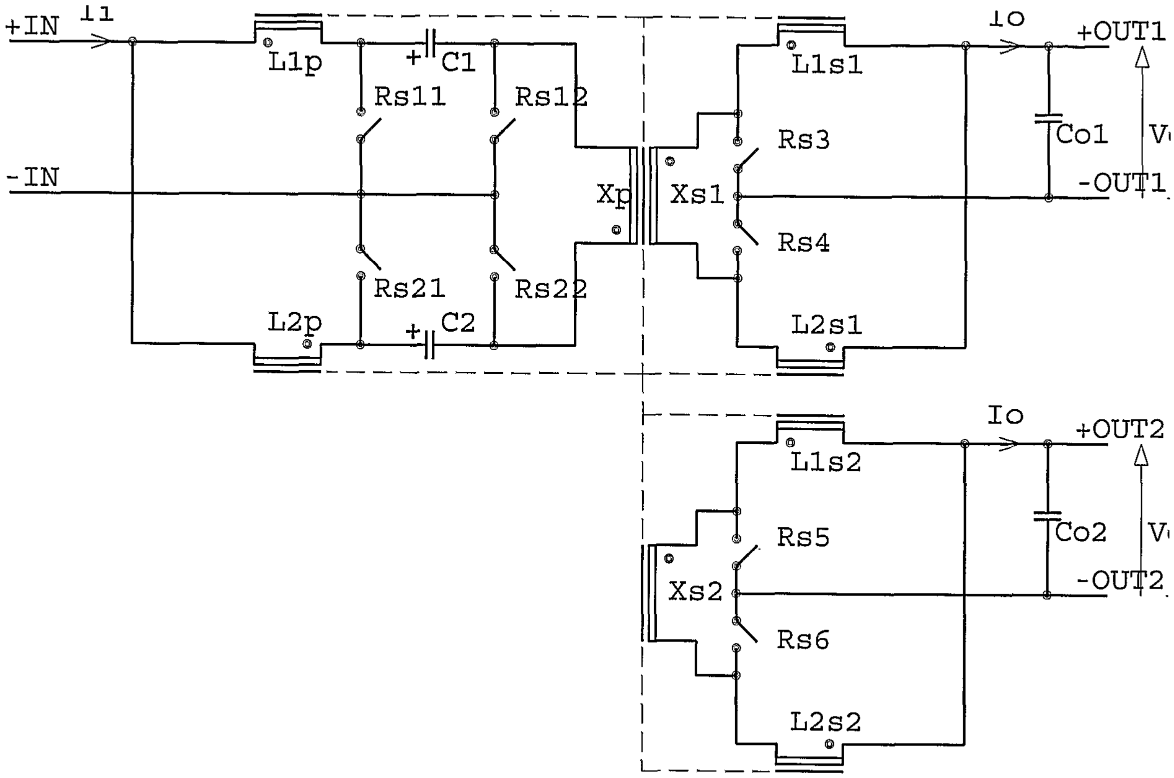
1.7uSec
2.5uSec
Rs12
2.6uSec
Rs21
3.3uSec
Rs22
0.1uSec 2.4uSec
2.5uSec
Rs3
0.8uSec
1.7uSec
2.5uSec
Rs4
3.3uSec
5.0uSec

Fig. 10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Ii
-IN
L1p
C1
Rs11
Rs12
Rs21
Rs22
L2p
C2
Xp
Xs1
Rs3
Rs4
L1s1
L2s1
Io
+OUT1
Co1
-OUT1
L1s2
Rs5
Xs2
Rs6
L2s2
Io
+OUT2
Co2
-OUT2

Fig. 11