(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
9 September 2011 (09.09.2011)

PCT

(10) International Publication Number
WO 2011/109057 A2

(51) International Patent Classification: Not classified

(21) International Application Number:
PCT/US2010/062032

(22) International Filing Date:
23 December 2010 (23.12.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/718,152 5 March 2010 (05.03.2010) US

(71) Applicant *(for all designated States except US)*: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.o. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant *(for JP only)*: **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-shinjuku 6 Chome, Shinjuku-ku, Tokyo, 160-8366 (JP).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **MUJICA, Fernando, A.** [US/US]; 1206 Bel Air Drive, Allen, TX 75013 (US). **GANDHI, Hardik, P.** [US/US]; 600 Rainbow Drive, #188, Mt. View, CA 94041 (US). **SHI, Kun** [US/US]; 540 Buckingham Road, Apt. 1030, Richardson, TX 75081 (US).

(74) Agents: **PATTI, John, J.** et al.; Texas Instruments Incorporated, Deputy General Patent Counsel, P.o. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) **Title**: ROBUST TRANSMIT/FEEDBACK ALIGNMENT

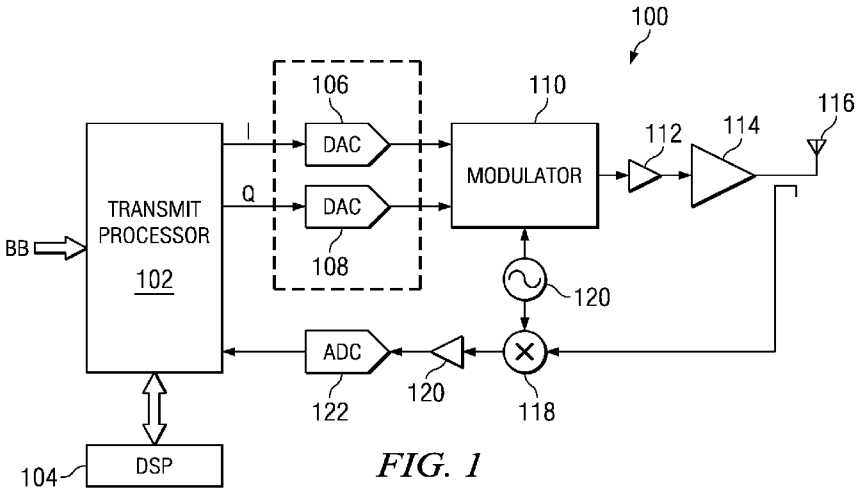


FIG. 1

(57) **Abstract**: A system (100) performs digital predistortion (DPD) for widely spaced narrowband signals, such as used in multi-carrier GSM using a polynomial curve for values of a cross-correlation function (above a predetermined threshold) to determine a delay estimate. A transmit processor (102) and digital signal processor (104) generate in-phase (I) and quadrature (Q) components for a baseband signal (BB). The components (I, Q) are provided to digital-to-analog converters (106, 108) and converted to analog signals. A modulator (110) (which uses a local oscillator 120) converts the analog signal to an RF signal which is amplified by amplifiers (112, 114) and transmitted by an antenna (116). A mixer (118) (which also uses local oscillator 120), a buffer (120) and an analog-to-digital converter (122) provide feedback to the transmit processor (102) to compensate for errors and nonlinearities.

WO 2011/109057 A2

ROBUST TRANSMIT/FEEDBACK ALIGNMENT

[0001] This relates generally to digital predistortion (DPD) and, more particularly, to delay estimation for a DPD system.

BACKGROUND

[0002] Widely spaced narrow band signals are becoming increasingly common in wireless telecommunications systems, such as multi-carrier or MC-GSM. In real world communications, noise in the narrowband signals can cause the peaks to vary in height. As a result, it is not uncommon for peaks around the center peak to be larger than the center peak, which can cause delay misalignment and a non-functioning system. Thus, it is highly desirable to have accurate and robust alignment to achieve high performance in these closed loop systems.

[0003] Some examples of conventional systems are described in: U.S. Patent Pre-Grant Publ. No. 2004/0052314; U.S. Patent Pre-Grant Publ. No. 2006/0209984; U.S. Patent Pre-Grant Publ. No. 2008/0130788; and U.S. Patent Pre-Grant Publ. No. 2008/0130789.

SUMMARY

[0004] A example embodiment comprises a digital predistortion (DPD) circuit that receives an input signal and that generates a predistorted signal from the input signal and predistortion coefficients; a delay element that receives an amplified signal and that provides a delayed output signal; a delay estimator that receives the delayed output signal and the predistorted signal and that generates a delay estimation by determining a peak value from a polynomial curve fit of values from a cross-correlation function of the delayed output signal, wherein the values of the cross-correlation function are greater than a predetermined threshold; and a DPD adapter that receives the delay estimation and that generates the predistortion coefficients.

[0005] In accordance with an example embodiment of the invention, the delay estimator further comprises: a pre-processing circuit that receives the delay output signal and the

predistorted signal; a cross-correlator that receives an output from the pre-processing circuit and that generate the values from the cross-correlation function of the delayed output signal; and a post-processing circuit that the values from the cross-correlation function of the delayed output signal and that generates the delay estimation.

[0006] In accordance with an example embodiment of the invention, the delay, the delay estimator, and the DPD adapter further comprise a processor with a computer program product embodied thereon that includes: computer code for delaying the amplified signal to produce the delayed output signal; computer code for generating a delay estimation by determining the peak value from the polynomial curve fit of values from the cross-correlation function of the delayed output signal; and computer code for generating the predistortion coefficients from the delay estimation.

[0007] In accordance with an example embodiment of the invention, the processor further comprises a digital signals processor (DSP).

[0008] In accordance with an example embodiment of the invention, the input signal is a widely spaced narrowband signal.

[0009] In accordance with an example embodiment of the invention, a system is provided. The system comprises a transmit path having an amplifier; an antenna that is coupled to the transmit path; a feedback path that is coupled to the transmit path; and transmit processing circuitry that is coupled to transmit path and the feedback path, wherein the transmit processing circuitry includes: a DPD circuit that receives a input signal and that generates a predistorted signal from the input signal and predistortion coefficients; a delay element that receives an amplified signal from the feedback path and that provides a delayed output signal; a delay estimator that receives the delayed output signal and the predistorted signal and that generates a delay estimation by determining a peak value from a polynomial curve fit of values from a cross-correlation function of the delayed output signal, wherein the values of the cross-correlation function are greater than a predetermined threshold; and a DPD adapter that receives the delay estimation and that generates the predistortion coefficients.

[0010] In accordance with an example embodiment of the invention, the delay estimator further comprises: a pre-processing circuit that receives the delay output signal and the predistorted signal; a cross-correlator that receives an output from the pre-processing circuit and that generate the values from the cross-correlation function of the delayed output signal; and a

post-processing circuit that the values from the cross-correlation function of the delayed output signal and that generates the delay estimation.

[0011] In accordance with an example embodiment of the invention, the transmit processing circuitry further comprises: a transmit processor that is coupled to the transmit path and the feedback path; and a DSP that is coupled to the transmit processor.

[0012] In accordance with an example embodiment of the invention, the DSP includes a computer program product that comprises: computer code for delaying the amplified signal to produce the delayed output signal; computer code for generating a delay estimation by determining the peak value from the polynomial curve fit of values from the cross-correlation function of the delayed output signal; and computer code for generating the predistortion coefficients from the delay estimation.

[0013] In accordance with an example embodiment of the invention, the transmit path further comprises: a digital-to-analog converter (DAC) that is coupled to the transmit processor; a modulator that is coupled to the DAC; a low power amplifier that is coupled to the modulator; and a high power amplifier that is coupled between the low power amplifier and the antenna.

[0014] In accordance with an example embodiment of the invention, the DAC further comprises: a first DAC that receives an in-phase signal from the transmit processor; and a second DAC that receives a quadrature signal from the transmit processor.

[0015] In accordance with an example embodiment of the invention, the feedback path further comprises: a mixer that is coupled to the high power amplifier; a buffer that is coupled to the mixer; and an analog-to-digital converter that is coupled between the buffer and the transmit processor.

[0016] In accordance with an example embodiment of the invention, an apparatus is provided. The apparatus comprises a transmit processor having a DPD circuit that receives a input signal and that generates a predistorted signal from the input signal and predistortion coefficients; and a DSP that is coupled to the transmit processor having a computer program product embodied thereon, wherein the computer program product includes: computer code for delaying the amplified signal to produce the delayed output signal; computer code for generating a delay estimation by determining the peak value from the polynomial curve fit of values from the cross-correlation function of the delayed output signal; and computer code for generating the predistortion coefficients from the delay estimation.

[0017] In accordance with an example embodiment of the invention, the transmit processor further comprises: a baseband section; and a DPD section that includes the DPD circuit, wherein the DPD circuit is coupled to the baseband section.

[0018] In accordance with an example embodiment of the invention, the DPD section further comprises a feedback pipeline; buffer circuit that is coupled to the feedback pipeline and the baseband section; an equalizer that is coupled to the DPD circuit; a mixer that is coupled to the equalizer; and a DAC interface that is coupled to the mixer;

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] Example embodiments are described with reference to accompanying drawings, wherein:

[0020] FIG. 1 is a block diagram of an example of a system in accordance with an example embodiment of the invention;

[0021] FIG. 2 is a block diagram of an example of the transmit processor of FIG. 1;

[0022] FIG. 3 is a block diagram of an example of the DPD system of FIGS. 1 and 2;

[0023] FIG. 4 is a block diagram of an example of the delay estimator of FIG. 3;

[0024] FIG. 5 is simulation for the system of FIG. 1; and

[0025] FIG. 6 is diagram depicting the operation of the delay estimator of FIG. 4.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0026] In FIG. 1, the reference numeral 200 generally designates a system in accordance with an example embodiment of the invention. System 200 generally comprises a transmit path, a feedback path, an antenna 116, a transmit processor 102 and a digital signals processor (DSP) 104. The transmit path is generally comprised of an IQ digital-to-analog converter (DAC), modulator 110, low power amplifier 112, and high power amplifier. The feedback path is generally comprised of mixer 118, buffer 120, and analog-to-digital converter (ADC) 122.

[0027] In operation, the system 100 converts a baseband signal BB into an radio frequency (RF) signal that is transmitted through antenna 116. Preferably, the transmit processor 102 receives the baseband signal BB, and, in combination with the DSP 104, processes the baseband signal BB for transmission. In particular, the transmit processor 102 and DSP 104 generates in-phase (I) and quadrature (q) components which are provided to DACs 106 and 108 (of the IQ DAC) to be converted to analog signals. Modulator 110 (with the use of local oscillator 120) converts the analog signal to an RF signal which is amplified by amplifiers 112

and 114 and transmitted through antenna 116. To ensure a relatively clean signal, the mixer 118 (which also uses local oscillator 120), buffer 120, and ADC 122 provide a feedbacks signal to the transmit processor 102 so that the transmit processor 102 and DSP 104 can compensate for errors and nonlinearities.

[0028] Turning to FIG. 2, the transmit processor 102 can be seen in greater detail. In particular, the transmit processor 102 can be subdivided into two sections: a baseband section 228 and a digital predistortion (DPD) section 230. Each of these sections 228 and 230 operates on a different time domain (namely, generated by the baseband clock signal BBCLK and phased locked loop or PLL 214 or by the DPD clock signal DPDCLK and PLL 216). The baseband section 228 employs an interface circuit 202, digital upconverters (DUCs) 204 and 206, an adder 208, crest factor reduction (CFR) circuit 210, and output circuit 212 to perform processing on the baseband signal BB, the result of which is provided to buffers 218 in the DPD section 230. The DPD section 230 employs a feedback pipeline 232 (which is coupled to ADC 122), DPD circuit 220, equalizer 222, mixer 224 and DAC interface 226 (which is coupled to DACs 106 and 108) to perform digital predistortion. Additionally, interface 234 allows for communication with DSP 104.

[0029] The DPD system 400 used in system 100 can be seen in greater detail in FIG. 3. This DPD system 400 is generally implemented as a combination of hardware in the transmit processor 102 and software in DSP 104, but may also be fully implemented as hardware in the transmit processor 102. Because the amplifier 402 (which is generally comprised of amplifiers 112 and 114 of FIG. 1) has nonlinear characteristics, the DPD system 400 generally operates to digitally predistort the input signal X to generate a predistorted signal Y, so that the amplifier 402 can output a generally clean signal. Preferably, the DPD circuit 220 is a multi-tap finite impulse response (FIR) filter, with its filter or predistortion coefficients being calculated through feedback. As a result of the construction of the system 100 of FIG. 1, a delay is introduced by the feedback path of system 100 and is represented by delay 404 to generate a delayed signal Z. The delay estimator 406 determines or estimates the delay $\hat{D}$ caused by the feedback path of system 100 by performing a calculation from the predistorted signal Y and the delayed signal Z. With the estimated delay $\hat{D}$ and the input signal X, the DPD adapter 408 can calculate the predistortion coefficients.

[0030] Turning to FIG. 4, the delay estimator 406 can be seen in greater detail. Specifically, it performs the estimation in three stages, which can be implemented through software or hardware. Delay estimator 406 performs preprocessing in stage 502, determines the cross-correlation function values in stage 504, and performs post-processing in stage 506. Additionally, in the delay estimator 406, a simple model between the signals Y and Z, which is as follows, is presumed:

(1) $Z(t) = Y(t - D) - V(t)$,

where D denotes the delay from delay 404 and V(t) denotes noise. The cross-correlation function between Y(t) and Z(t) with a lag time τ is:

(2) $R_{YZ}(\tau) = R_{YY}(\tau - D)$,

where a maximum is obtained at τ = D. Thus, the delay estimation $\hat{D}$ can determined by searching for the peak of values from the cross-correlation function of equation (2); this estimation can be represented as follows:

(3) $\hat{D} = \arg\left(\max_{\tau}\left(R_{YY}(\tau - D)\right)\right)$.

It should also be noted that the cross-correlation function of equation (3) is a complex valued function because of the complex baseband signal representation with the peak searching based on its absolute value.

[0031] Assuming for such systems (i.e., system 100) that the amplifier 402 can be modeled by a Hammerstein-Wiener system (namely, a memoryless nonlinearity sandwiched between two infinite impulse response or IIR filters), the memoryless nonlinearity introduces distortion, while IIR filters introduce fractional delay. To examine these two effects, a simulation can be performed that compares estimated delay (that uses equation (3)) and true delay, where the system has a known delay of 6 samples that is introduced by two interpolation filters (forward path 10 samples, backward path 6 samples).

[0032] Turning first to the memoryless nonlinearity, the delay estimation $\hat{D}$ is performed using equation (3) for two cases: with and without PA nonlinearity. The test signal, here, is 2-carrier GSM signal with frequency locations +/-9.9MHz and with a buffer size set to be 40,000. The delay estimation $\hat{D}$ results are shown in Table 1 below, and it is observed that memoryless nonlinearity does not affect delay estimation $\hat{D}$.

Table 1		
Nonlinearity	$\hat{D}$	D
w/	16	16
w/o	16	16

[0033] Turning now to fractional delay, the delay estimation $\hat{D}$is performed using equation (3) assuming that the amplifier 402 is linear and modeled by IIR filters. Here, as with the memoryless nonlinearity estimation, the test signal is 2-carrier GSM with frequency locations +/-9.9MHz and with a buffer size set to be 40,000. The delay estimation $\hat{D}$ for the fractional delay results are shown in Table 2 below, and it can seen that fractional delay results in the incorrect estimate of delay $\hat{D}$.

Table 2		
	$\hat{D}$	D
IIR PA	22	16

[0034] Based on these results, several observations can be made. First, the sufficiency of the number of samples depends on the carrier spacing, and the further the two carriers are from each other, the greater the number of samples needed for estimation. Second, the carrier spacing plays a significant role in delay estimation $\hat{D}$, and it might be speculated that fractional delay effect is inversely proportional to carrier spacing. Turning to FIG. 5, plots for the cross-correlation function of equation (2) can be seen for 2-carrier GSM system with frequency locations +/-0.9MHz and with a buffer size of 4,000. It is seen that cross-correlation function of equation (2) is comprised of a high frequency component, which is the frequency difference between two carriers (i.e., $f_d = |f_2 - f_1|$). Furthermore, with sampling frequency f_s, the distance between adjacent peaks can be obtained by f_s / f_d . Therefore, with the increase of carrier spacing, the adjacent peak gets closer, which, in turn makes the delay estimation $\hat{D}$ less and less robust.

[0035] As can be observed, it is the closeness of the closeness between different peaks of cross-correlation function of equation (2) and the fractional delay causes the incorrect delay

estimation. However, if it is assumed that equation (2) is the auto-correlation function of the information signal modulating some higher frequency component and if it is assumed that equation (2) is symmetrical, an optimal delay resides in the peak of its envelope. Thus, the "demodulated" information signal can be "reconstructed," and the estimate of the delay $\hat{D}$ can be determined through locating its peak. This process is illustrated in FIG. 6, where a quadratic curve fit is applied to the N-largest values (above a predetermined threshold) of cross-correlation function of equation (2) to obtain a parabola with the delay estimation $\hat{D}$ being at the parabola's apex.

[0036] Embodiments having different combinations of one or more of the features or steps described in the context of example embodiments having all or just some of such features or steps are intended to be covered hereby. Those skilled in the art will appreciate that many other embodiments and variations are also possible within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus comprising:

a digital predistortion (DPD) circuit that receives an input signal and that generates a predistorted signal from the input signal and predistortion coefficients;

a delay element that receives an amplified signal and that provides a delayed output signal;

a delay estimator that receives the delayed output signal and the predistorted signal and that generates a delay estimation by determining a peak value from a polynomial curve fit of values from a cross-correlation function of the delayed output signal, wherein the values of the cross-correlation function are greater than a predetermined threshold; and

a digital predistortion adapter that receives the delay estimation and that generates the predistortion coefficients.

2. The apparatus of Claim 1, wherein the delay estimator further comprises:

a pre-processing circuit that receives the delay output signal and the predistorted signal;

a cross-correlator that receives an output from the pre-processing circuit and that generate the values from the cross-correlation function of the delayed output signal; and

a post-processing circuit that the values from the cross-correlation function of the delayed output signal and that generates the delay estimation.

3. The apparatus of Claim 1, wherein the delay, the delay estimator, and the digital predistortion adapter further comprise a processor with a computer program product embodied thereon that includes:

computer code for delaying the amplified signal to produce the delayed output signal;

computer code for generating a delay estimation by determining the peak value from the polynomial curve fit of values from the cross-correlation function of the delayed output signal; and

computer code for generating the predistortion coefficients from the delay estimation.

4. The apparatus of Claim 3, wherein the processor further comprises a digital signal processor (DSP).

5. The apparatus of Claim 1, wherein the input signal is a widely spaced narrowband signal.

6. A system comprising:

a transmit path having an amplifier;

an antenna that is coupled to the transmit path;

a feedback path that is coupled to the transmit path; and

transmit processing circuitry that is coupled to transmit path and the feedback path, wherein the transmit processing circuitry includes:

a digital predistortion (DPD) circuit that receives a input signal and that generates a predistorted signal from the input signal and predistortion coefficients;

a delay element that receives an amplified signal from the feedback path and that provides a delayed output signal;

a delay estimator that receives the delayed output signal and the predistorted signal and that generates a delay estimation by determining a peak value from a polynomial curve fit of values from a cross-correlation function of the delayed output signal, wherein the values of the cross-correlation function are greater than a predetermined threshold; and

a digital predistortion adapter that receives the delay estimation and that generates the predistortion coefficients.

7. The apparatus of Claim 6, wherein the delay estimator further comprises:

a pre-processing circuit that receives the delay output signal and the predistorted signal;

a cross-correlator that receives an output from the pre-processing circuit and that generate the values from the cross-correlation function of the delayed output signal; and

a post-processing circuit that the values from the cross-correlation function of the delayed output signal and that generates the delay estimation.

8. The system of Claim 6, wherein the transmit processing circuitry further comprises:

a transmit processor that is coupled to the transmit path and the feedback path; and

a digital signal processor (DSP) that is coupled to the transmit processor.

9. The system of claim 8, wherein the digital signal processor includes a computer program product that comprises:

computer code for delaying the amplified signal to produce the delayed output signal;

computer code for generating a delay estimation by determining the peak value from the polynomial curve fit of values from the cross-correlation function of the delayed output signal; and

computer code for generating the predistortion coefficients from the delay estimation.

10. The system of Claim 9, wherein the transmit path further comprises:

a digital-to-analog converter (DAC) that is coupled to the transmit processor;

a modulator that is coupled to the digital-to-analog converter;

a low power amplifier that is coupled to the modulator; and

a high power amplifier that is coupled between the low power amplifier and the antenna.

11. The system of claim 10, wherein the digital-to-analog converter further comprises:

a first digital-to-analog converter that receives an in-phase signal from the transmit processor; and

a second digital-to-analog converter that receives a quadrature signal from the transmit processor.

12. The system of Claim 11, wherein the feedback path further comprises:

a mixer that is coupled to the high power amplifier;

a buffer that is coupled to the mixer; and

an analog-to-digital converter that is coupled between the buffer and the transmit processor.

13. An apparatus comprising:

a transmit processor having a DPD circuit that receives a input signal and that generates a predistorted signal from the input signal and predistortion coefficients; and

a DSP that is coupled to the transmit processor having a computer program product embodied thereon, wherein the computer program product includes:

computer code for delaying the amplified signal to produce the delayed output signal;

computer code for generating a delay estimation by determining the peak value from the polynomial curve fit of values from the cross-correlation function of the delayed output signal; and

computer code for generating the predistortion coefficients from the delay estimation.

14. The apparatus of Claim 13, wherein the transmit processor further comprises:

a baseband section; and

a DPD section that includes the DPD circuit, wherein the DPD circuit is coupled to the baseband section.

15. The apparatus of Claim 14, wherein the DPD section further comprises:

a feedback pipeline;

buffer circuit that is coupled to the feedback pipeline and the baseband section;

an equalizer that is coupled to the DPD circuit;

a mixer that is coupled to the equalizer; and

a DAC interface that is coupled to the mixer.

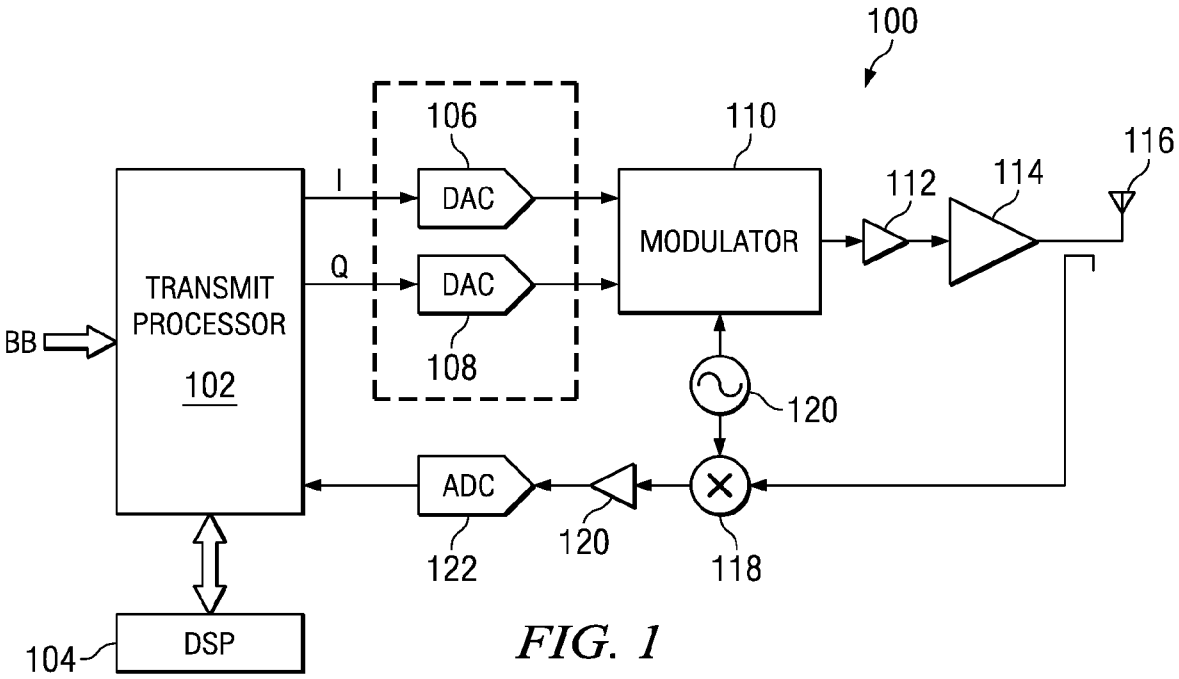


FIG. 1

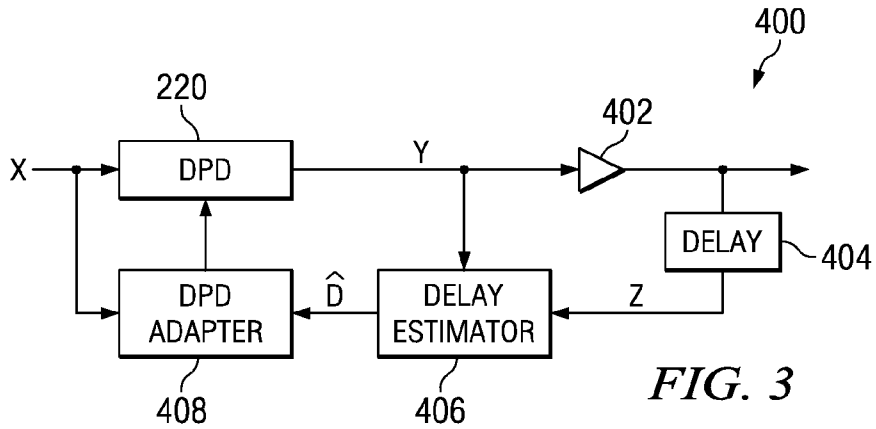


FIG. 3

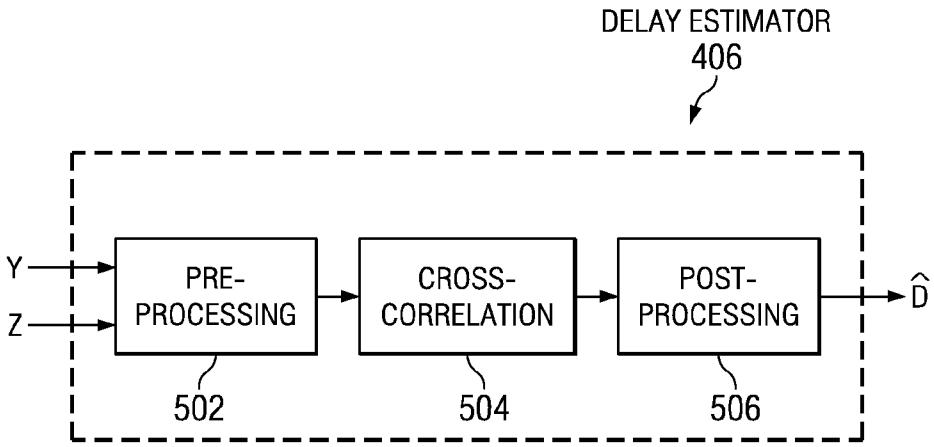


FIG. 4

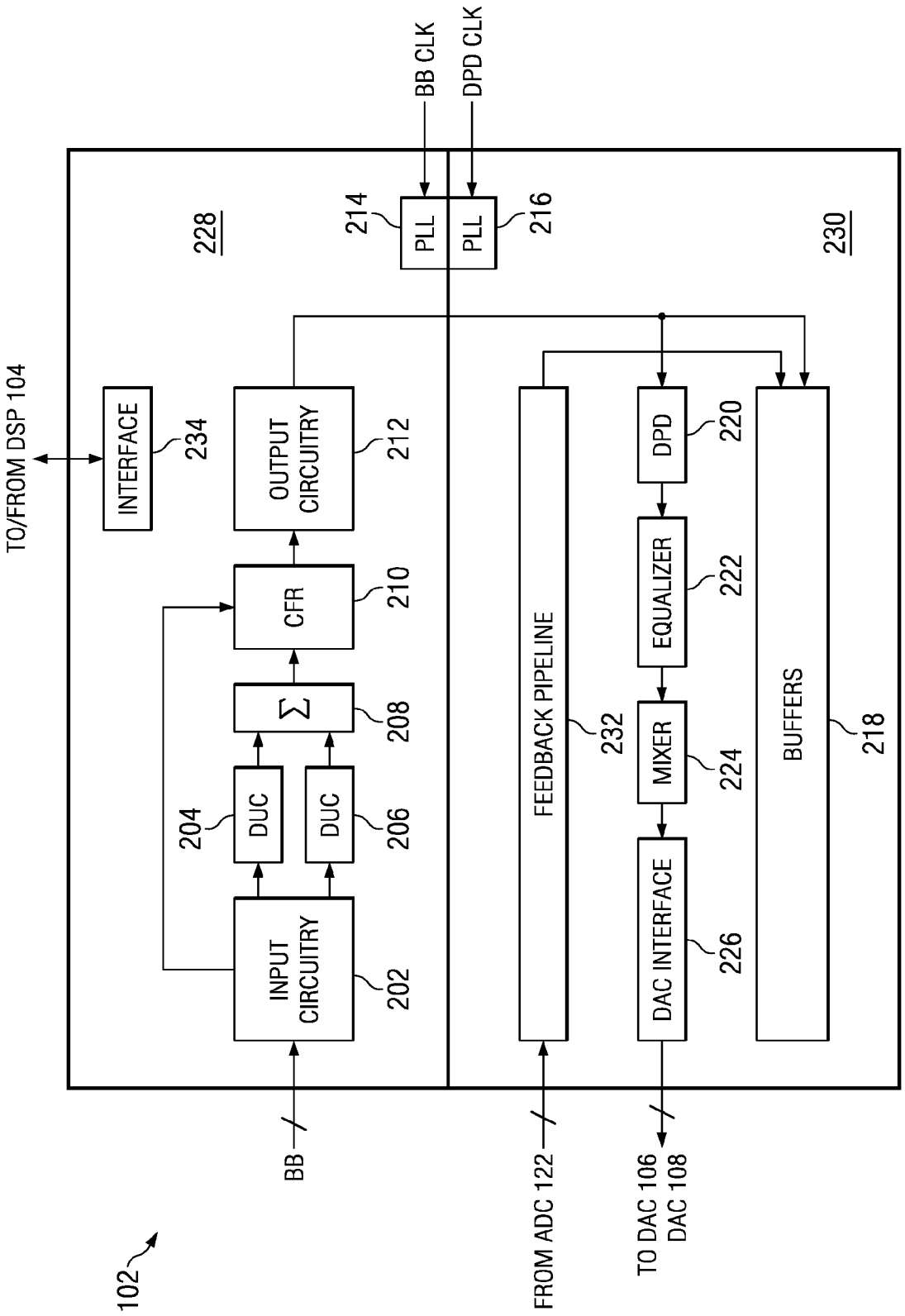

BB CLK
DPD CLK
228
214
PLL
PLL
216
230
TO/FROM DSP 104
INTERFACE
234
OUTPUT CIRCUITRY
212
CFR
210
Σ
208
204
DUC
DUC
206
INPUT CIRCUITRY
202
FEEDBACK PIPELINE
232
DPD
220
EQUALIZER
222
MIXER
224
DAC INTERFACE
226
BUFFERS
218
BB
FROM ADC 122
TO DAC 106
DAC 108
102

FIG. 2

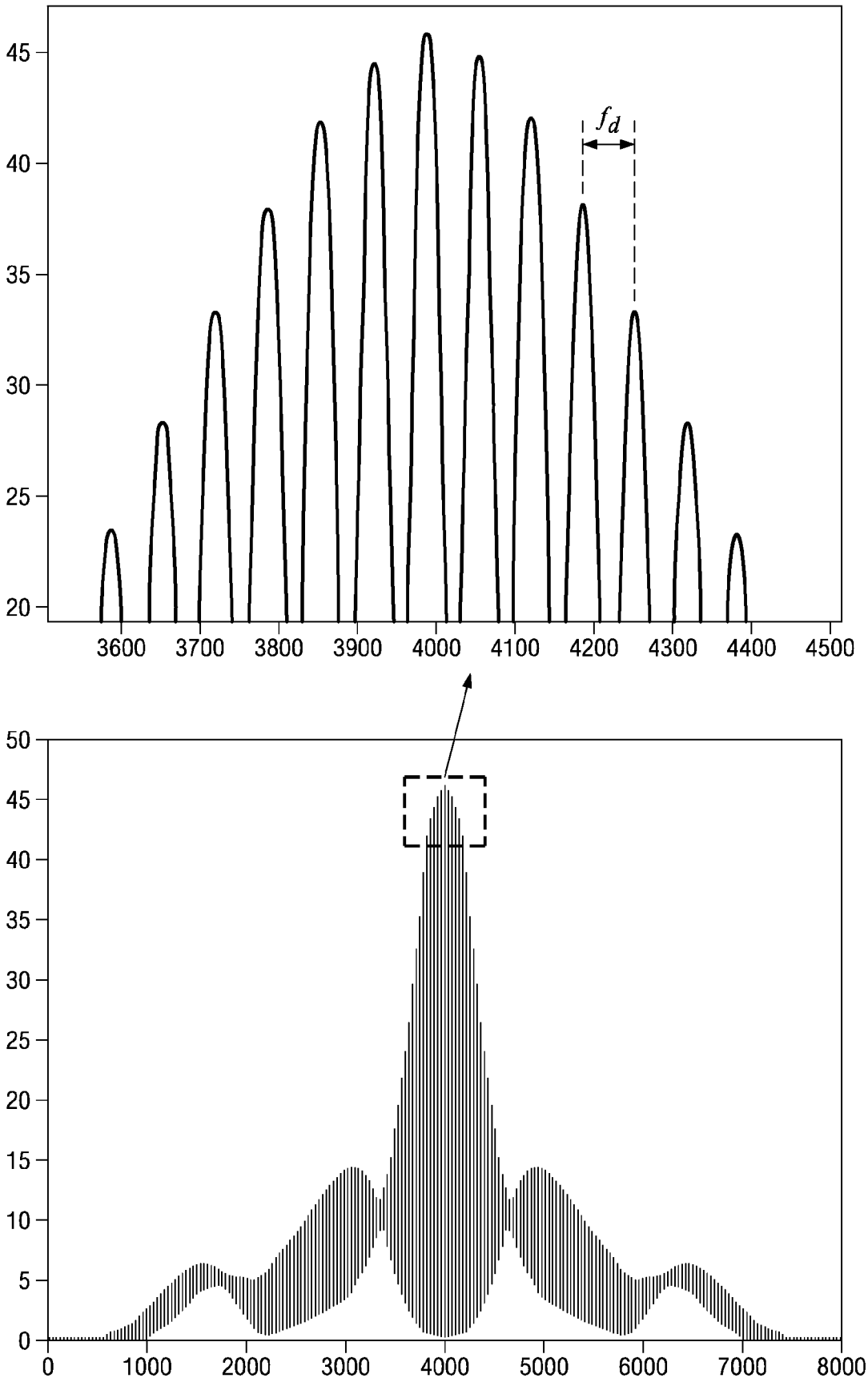

45
40
35
30
25
20
f_d
3600
3700
3800
3900
4000
4100
4200
4300
4400
4500
50
45
40
35
30
25
20
15
10
5
0
0
1000
2000
3000
4000
5000
6000
7000
8000

FIG. 5

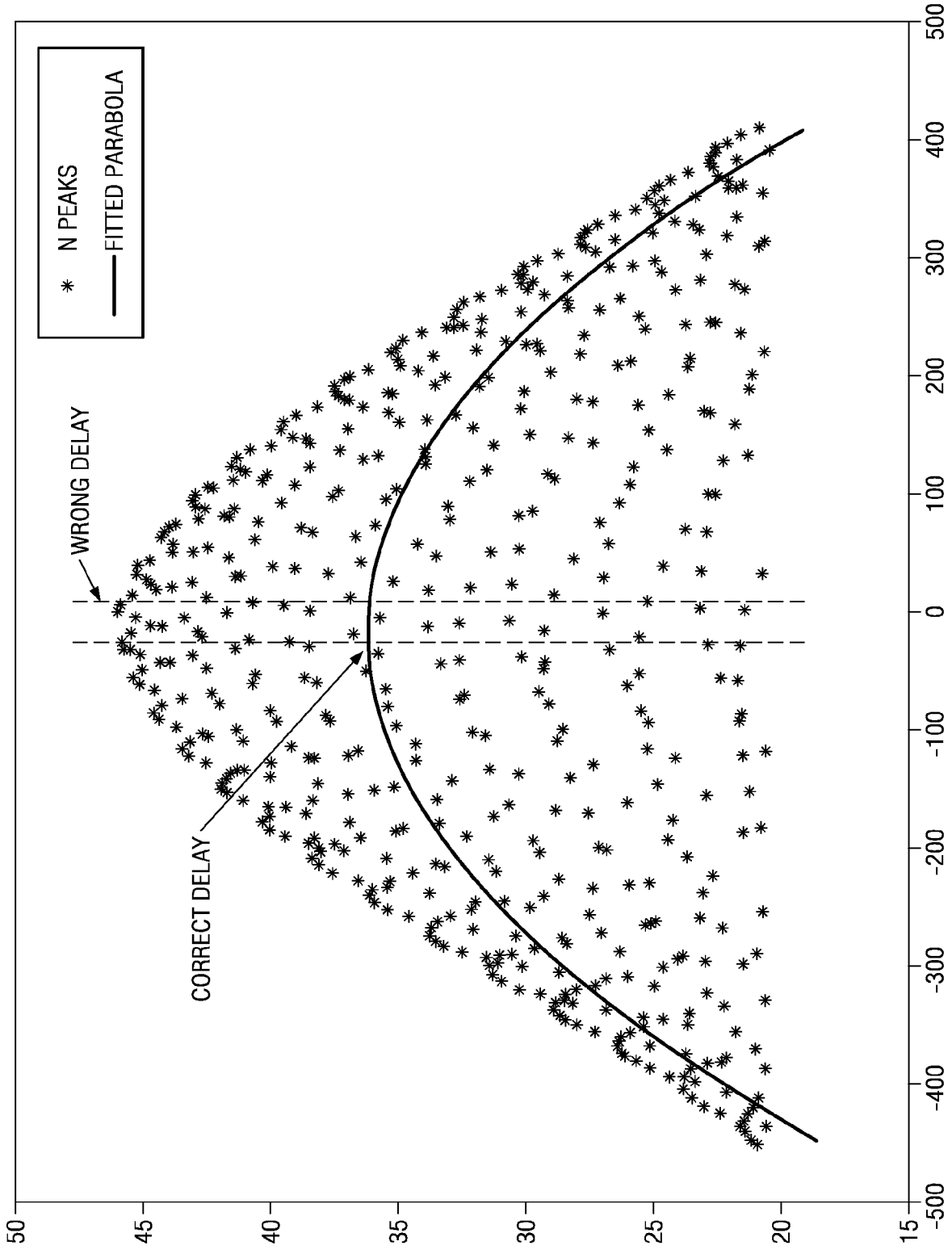

N PEAKS
FITTED PARABOLA
WRONG DELAY
CORRECT DELAY
50
45
40
35
30
25
20
15
-500
-400
-300
-200
-100
0
100
200
300
400
500

FIG. 6