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[Continued on next page]

(54) Title: LOW-STRESS LOW-HYDROGEN LPCVD SILICON NITRIDE

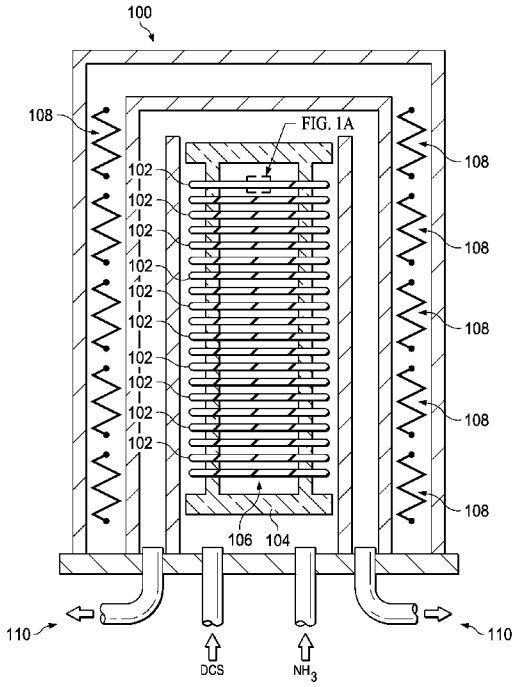

FIG. 1

(57) Abstract: In described examples, a microelectronic device (102) contains a high performance silicon nitride layer, which is stoichiometric within 2 atomic percent, has a low stress of 600 MPa to 1000 MPa, and has a low hydrogen content, less than 5 atomic percent, formed by an LPCVD process. The LPCVD process uses ammonia NH3 and dichlorosilane DCS gases in a ratio of 4 to 6, at a pressure of 150 millitorr to 250 millitorr, and at a temperature of 800°C to 820°C.

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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

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LOW-STRESS LOW-HYDROGEN LPCVD SILICON NITRIDE

[0001] This relates generally to microelectronic devices, and more particularly to silicon nitride layers in microelectronic devices.

BACKGROUND

[0002] In microelectronic devices, stoichiometric silicon nitride layers are desirably formed, which simultaneously have low stress that is less than 1000 megapascals (MPa), and low hydrogen content that is less than 5 atomic percent. Such films would be useful for a variety of microelectronic applications. Silicon nitride films formed by plasma enhanced chemical vapor deposition (PECVD) may have low stress, but have high hydrogen content, above 15 atomic percent, which can cause reliability problems and poor etch resistance. Films formed by low pressure chemical vapor deposition (LPCVD) have low hydrogen content, but high stress, above 1000 MPa, which can cause device performance problems.

SUMMARY

[0003] In described examples, a microelectronic device contains a high performance silicon nitride layer, which is stoichiometric within 2 atomic percent, has a low stress of 600 MPa to 1000 MPa, and has a low hydrogen content, less than 5 atomic percent. The high performance silicon nitride layer is formed by an LPCVD process. The LPCVD process uses ammonia and dichlorosilane gases in a ratio of 4 to 6, at a pressure of 150 millitorr to 250 millitorr, and at a temperature of 800°C to 820°C.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 depicts an LPCVD furnace in an example process of forming a high performance silicon nitride on microelectronic devices and FIG. 1A is an expanded view of the silicon nitride layer formed on the microelectronic devices within the furnace of FIG. 1.

[0005] FIG. 2 is a cross section of an example semiconductor device with a high performance silicon nitride layer.

[0006] FIG. 3A and FIG. 3B are cross sections of the semiconductor device of FIG. 2, depicted in key stages of formation.

[0007] FIG. 4 is a cross section of an example integrated circuit with a high performance

silicon nitride layer.

[0008] FIG. 5A and FIG. 5B are cross sections of the integrated circuit of FIG. 4, depicted in key stages of fabrication.

[0009] FIG. 6A and FIG. 6B are cross sections of an example microelectronic mechanical system (MEMS) device with a high performance silicon nitride layer, depicted in key stages of fabrication.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0010] The figures are not drawn to scale. Some acts may occur in different orders and/or concurrently with other acts or events. Not all illustrated acts or events are required to implement a methodology in accordance with example embodiments.

[0011] A high performance silicon nitride layer, which is stoichiometric within 2 atomic percent, has a low stress of 600 MPa to 1000 MPa, and has a low hydrogen content, less than 5 atomic percent, is formed by an LPCVD process. The LPCVD process uses ammonia and dichlorosilane gases in a ratio of 4 to 6, at a pressure of 150 millitorr to 250 millitorr, and at a temperature of 800°C to 820°C. The combination of stoichiometry, low stress and low hydrogen content were not expected to be provided by the disclosed process conditions, and were discovered during investigations of LPCVD processes. For the purposes of this disclosure, stoichiometric silicon nitride has a silicon:nitrogen atomic ratio of 3:4.

[0012] FIG. 1 depicts an LPCVD furnace in an example process of forming a high performance silicon nitride on microelectronic devices. The LPCVD furnace 100 holds the microelectronic devices 102 on substrates, such as semiconductor wafers, in a boat 104. The boat 104 is held in a reaction chamber 106 of the LPCVD furnace 100. The reaction chamber 106 is heated to a temperature of 800°C to 820°C by heating elements 108 of the LPCVD furnace 100 disposed around the reaction chamber 106. Ammonia (NH_3) and dichlorosilane (DCS) gases are introduced into the reaction chamber 106 at a ratio of 4 to 6. Pressure inside the reaction chamber 106 is maintained at 150 millitorr to 250 millitorr by an exhaust system 110, such as including a combination of an exhaust pump and an adjustable exhaust valve. As shown in the expanded view of FIG. 1A, the high performance silicon nitride layer 112 is formed on the microelectronic devices 102 by reaction of nitrogen in the ammonia and silicon in the dichlorosilane. Formation of the high performance silicon nitride layer 112 is continued until a desired thickness is attained. Subsequently, flows of the ammonia and dichlorosilane are ended

and the microelectronic devices 102 are extracted from the LPCVD furnace 100.

[0013] Formation of the high performance silicon nitride layer 112 by maintaining the temperature at 800°C to 820°C, the ratio of ammonia to dichlorosilane at 4 to 6, and the pressure at 150 millitorr to 250 millitorr advantageously provides a silicon:nitrogen atomic ratio within 2 percent of the ratio 3:4, a low stress of 600 MPa to 1000 MPa, and a low hydrogen content of less than 5 atomic percent. The high performance silicon nitride layer 112 may have an index of refraction of 2.0 to 2.1 as a result of being formed by the process described in reference to FIG. 1. Further, the high performance silicon nitride layer 112 may have a dielectric breakdown strength of greater than 12 megavolts per centimeter (MV/cm), which may advantageously contribute to higher reliability of the microelectronic devices 102. Increasing the ratio of ammonia to dichlorosilane reduces the stoichiometry and the dielectric breakdown strength, which may disadvantageously contribute to lower reliability. Reducing the ratio of ammonia to dichlorosilane disadvantageously increases the stress. Reducing the temperature and increasing the pressure also disadvantageously increases the stress.

[0014] FIG. 2 is a cross section of an example semiconductor device with a high performance silicon nitride layer. The semiconductor device 200 is formed on a semiconductor substrate 202, such as a stack gallium nitride and aluminum gallium nitride epitaxial layers, and possibly other III-V layers. A cap layer 204 of gallium nitride is disposed on the substrate 202. A high performance silicon nitride layer 206 is disposed on the cap layer 204 on two sides of a gate 208 and between a source 210 and drain 212 of a gallium nitride field effect transistor (GaN FET) 214 of the semiconductor device 200. The gate 208 may partially overlap the high performance silicon nitride layer 206. For example, the high performance silicon nitride layer 206 may be 10 nanometers to 20 nanometers thick.

[0015] Contact metal 216 is disposed on the substrate 202 in the source 210 and drain 212. A field plate dielectric layer 218 is disposed over the gate 208 and the high performance silicon nitride layer 206, around the contact metal 216. Source metal 220 makes an electrical connection to the contact metal 216 in the source 210 and overlaps the gate 208 and extends partway to the drain 212 over the field plate dielectric layer 218 to provide a field plate for the GaN FET 214. Drain metal 222 makes electrical connection to the contact metal 216 in the drain 212. Additional dielectric layers and metal layers may be formed to provide low resistance connections to the GaN FET 214.

[0016] The low stress of the high performance silicon nitride layer 206 advantageously improves on-state current in the GaN FET 214 compared to a GaN FET with a silicon nitride layer having high stress. The low hydrogen content of the high performance silicon nitride layer 206 advantageously reduces charge trapping and improves reliability of the GaN FET 214 compared to a GaN FET with a silicon nitride layer having a high hydrogen content.

[0017] FIG. 3A and FIG. 3B are cross sections of the semiconductor device of FIG. 2, depicted in key stages of formation. Referring to FIG. 3A, the cap layer 204 is formed on the substrate 202 by an epitaxial process. A portion of the cap layer 204 and the substrate 202 may be removed to provide a lateral isolation boundary 224 for the GaN FET 214. The high performance silicon nitride layer 206 is formed on the cap layer 204 by an LPCVD process as described in reference to FIG. 1. An etch mask 226 is formed over the high performance silicon nitride layer 206 to cover areas for the high performance silicon nitride layer 206 of the completed GaN FET 214 of FIG. 2. The etch mask 226 may include photoresist formed by a photolithographic process, and may possibly include an anti-reflection layer.

[0018] Referring to FIG. 3B, a reactive ion etch (RIE) process 228 containing fluorine (F) removes the high performance silicon nitride layer 206 where exposed by the etch mask 226. Reactant gas flows and a pressure in the RIE process 228 may be adjusted to provide sloped edges on the high performance silicon nitride layer 206 as depicted in FIG. 3B. Subsequently, the etch mask 226 is removed, such as by an ash process. Fabrication of the semiconductor device 200 is continued to provide the structure of FIG. 2. The method described in reference to FIG. 3A and FIG. 3B advantageously provides the patterned high performance silicon nitride layer 206 with the desired properties of low stress and low hydrogen content.

[0019] FIG. 4 is a cross section of an example integrated circuit with a high performance silicon nitride layer. The integrated circuit 400 is formed on a semiconductor substrate 402 such as a silicon wafer. The integrated circuit 400 includes a p-channel metal oxide semiconductor (PMOS) transistor 404 and/or an n-channel metal oxide semiconductor (NMOS) transistor 406. Field oxide 408 is disposed in the substrate 402 to laterally isolate the PMOS transistor 404 and the NMOS transistor 406.

[0020] The PMOS transistor 404 is disposed in an n-type well 410 extending below the field oxide 408. The PMOS transistor 404 includes a gate dielectric layer 412 on the n-type well 410 and a gate 414 on the gate dielectric layer 412. Offset spacers 416 are disposed on lateral

surfaces of the gate 414. P-type source and drain regions 418 are disposed in the n-type well 410 on two sides of the gate 414. The source and drain regions 418 include source/drain extensions 420 extending under the gate 414 and deep source/drain regions 422 adjacent to the gate 414.

[0021] Gate sidewall spacers 424 are disposed adjacent to the gate 414, on the offset spacers 416. The gate sidewall spacers 424 include one or more layers of high performance silicon nitride, with low stress and low hydrogen content. Metal silicide 426 is disposed on the source and drain regions 418 adjacent to the gate sidewall spacers 424, and possibly on the gate 414. The gate sidewall spacers 424 provide lateral separation between a channel layer immediately below the gate dielectric layer 412 and the deep source/drain regions 422, and between the channel layer and the metal silicide 426 on the source and drain regions 418. The high performance silicon nitride in the gate sidewall spacers 424 may be within 10 nanometers of the semiconductor substrate 402. The low stress of the gate sidewall spacers 424 may advantageously reduce stress in the channel layer, and so improve an on-state current and/or an off-state current of the PMOS transistor 404. The low hydrogen content of the gate sidewall spacers 424 may advantageously improve reliability of the PMOS transistor 404.

[0022] Similarly, the NMOS transistor 406 is disposed in a p-type well 428 extending below the field oxide 408. The NMOS transistor 406 includes a gate dielectric layer 430 on the p-type well 428 and a gate 432 on the gate dielectric layer 430. Offset spacers 434 are disposed on lateral surfaces of the gate 432. N-type source and drain regions 436 are disposed in the p-type well 428 on two sides of the gate 432. The source and drain regions 436 include source/drain extensions 438 extending under the gate 432 and deep source/drain regions 440 adjacent to the gate 432. Gate sidewall spacers 442 including one or more high performance silicon nitride layers are disposed adjacent to the gate 432. The gate sidewall spacers 424 of the PMOS transistor 404 and the gate sidewall spacers 424 of the NMOS transistor 406 may possibly have a same layer structure as a result of being formed concurrently. Metal silicide 444 is disposed on the source and drain regions 436 adjacent to the gate sidewall spacers 442, and possibly on the gate 432. The NMOS transistor may accrue advantages from the low stress and low hydrogen content of the gate sidewall spacers 442 similar to those described in reference to the PMOS transistor 404.

[0023] FIG. 5A and FIG. 5B are cross sections of the integrated circuit of FIG. 4, depicted in key stages of fabrication. Referring to FIG. 5A, the p-type source/drain extensions 420 are

formed by implanting p-type dopants into the n-type well 410 using the gate 414 and offset spacers 416 of the PMOS transistor 404 as an implant mask, so that the source/drain extensions 420 do not extend completely under the gate 414. Similarly, the n-type source/drain extensions 438 are formed by implanting n-type dopants into the p-type well 428 using the gate 432 and offset spacers 434 of the NMOS transistor 406 as an implant mask, so that the source/drain extensions 438 do not extend completely under the gate 432. The substrate 402 is subsequently annealed to activate the implanted dopants.

[0024] A high performance silicon nitride layer 450 is formed over the gate 414, the offset spacers 416 and the source/drain extensions 420 of the PMOS transistor 404 and over the gate 432, the offset spacers 434 and the source/drain extensions 438 of the NMOS transistor 406. The high performance silicon nitride layer 450 is formed by an LPCVD process as described in reference to FIG. 1, which provides at least a partially conformal layer as depicted in FIG. 5A, so that a thickness of the high performance silicon nitride layer 450 on vertical surfaces of the offset spacers 416 and 434 is sufficient to form the gate sidewall spacers 424 and 442 of FIG. 4, respectively.

[0025] Referring to FIG. 5B, an anisotropic RIE process 452 containing fluorine (F) removes the high performance silicon nitride layer 450 of FIG. 5A over horizontal surfaces of the gate 414 and the source/drain extensions 420 of the PMOS transistor 404 and over the gate 432 and the source/drain extensions 438 of the NMOS transistor 406, leaving the high performance silicon nitride layer 450 to form the gate sidewall spacers 424 on the vertical surfaces of the offset spacers 416 of the PMOS transistor 404, and to form the gate sidewall spacers 442 on the vertical surfaces of the offset spacers 434 of the NMOS transistor 406. The conformal aspect of the LPCVD process to form the high performance silicon nitride layer 450 enables the gate sidewall spacers 424 and 442 to be formed without a photolithographic operation, advantageously reducing fabrication cost and complexity of the integrated circuit 400.

[0026] FIG. 6A and FIG. 6B are cross sections of an example microelectronic mechanical system (MEMS) device with a high performance silicon nitride layer, depicted in key stages of fabrication. Referring to FIG. 6A, the MEMS device 600 is formed in a silicon substrate 602, such as a single crystalline silicon wafer. A cavity 604 is formed in the substrate 602 leaving material of the substrate 602 above the cavity 604 in the form of a cantilevered element 606 such as a perforated membrane 606. The perforated membrane 606 may be part of a sensor, such as a

thermal sensor or a microphone, or may be part of an actuator such as a speaker. It may be desirable to partially isolate the perforated membrane 606 from adjacent regions 608 of the substrate 602. A layer of high performance silicon nitride 610 is formed on the perforated membrane 606 and interior surfaces of the cavity 604 and adjacent regions 608 of the substrate 602. The high performance silicon nitride layer 610 is formed by an LPCVD process as described in reference to FIG. 1 to have low stress and a low hydrogen content, which provides at least a partially conformal layer, so that the high performance silicon nitride layer 610 covers all exposed surfaces of the perforated membrane 606 as depicted in FIG. 6A. Due to restricted access to the cavity 604 through the perforated membrane 606, the high performance silicon nitride layer 610 is thicker on a top surface of the perforated membrane 606 outside of the cavity 604 than on a bottom surface of the perforated membrane 606 facing the cavity 604. The low stress of the high performance silicon nitride layer 610 advantageously reduces deformation of the perforated membrane 606 due to the unequal thickness on the top and bottom surfaces of the perforated membrane 606.

[0027] Referring to FIG. 6B, the high performance silicon nitride layer 610 is removed from a portion of the substrate 602 in the regions 608 adjacent to the perforated membrane 606. The MEMS device 600 is immersed in a crystallographic wet etch solution 612, such as a potassium hydroxide solution, which removes silicon from the substrate 602 in the areas exposed by the high performance silicon nitride layer 610 along crystal planes of the substrate 602 to form isolation cavities 614 adjacent to the perforated membrane 606. The low hydrogen content of the high performance silicon nitride layer 610 advantageously provides etch resistance to the crystallographic wet etch solution 612 at a desired thickness. The MEMS device 600 is subsequently rinsed and dried. The high performance silicon nitride layer 610 may be left in place in the completed MEMS device 600 or may be removed during subsequent fabrication processes.

[0028] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A microelectronic device, comprising:

a substrate; and

a silicon nitride layer disposed over the substrate, the silicon nitride layer having the following properties: a silicon:nitrogen atomic ratio within 2 percent of the ratio 3:4; a stress of 600 megapascals (MPa) to 1000 MPa; and a hydrogen content of less than 5 atomic percent.

2. The microelectronic device of claim 1, wherein the silicon nitride layer is less than 25 nanometers thick:

3. The microelectronic device of claim 1, wherein the silicon nitride layer has an index of refraction of 2.0 to 2.1:

4. The microelectronic device of claim 1, wherein the silicon nitride layer has a dielectric breakdown strength of greater than 12 megavolts per centimeter (MV/cm).

5. The microelectronic device of claim 1, wherein the microelectronic device includes semiconductor material, and the silicon nitride layer is within 10 nanometers of the semiconductor material.

6. The microelectronic device of claim 1, wherein the semiconductor material includes III-V semiconductor material.

7. The microelectronic device of claim 1, wherein the microelectronic device includes a gallium nitride field effect transistor (GaN FET).

8. The microelectronic device of claim 7, wherein the silicon nitride layer contacts III-V semiconductor material and contacts a gate of the GaN FET.

9. The microelectronic device of claim 1, wherein the microelectronic device includes an n-channel metal oxide semiconductor (NMOS) transistor with first gate sidewall spacers adjacent to a first gate of the NMOS transistor, and the first gate sidewall spacers include the silicon nitride layer.

10. The microelectronic device of claim 9, wherein the microelectronic device includes a p-channel metal oxide semiconductor (PMOS) transistor with second gate sidewall spacers adjacent to a second gate of the PMOS transistor, and the second gate sidewall spacers include the silicon nitride layer.

11. The microelectronic device of claim 1, wherein the microelectronic device is a

microelectronic mechanical system (MEMS) device containing a cantilevered element, and the silicon nitride layer is disposed on a top surface of the cantilevered element and on a bottom surface of the cantilevered element.

12. A method of forming a microelectronic device, comprising:

providing a substrate;

placing the substrate in a low pressure chemical vapor deposition (LPCVD) furnace;

heating the substrate to a temperature of 800°C to 820°C in the LPCVD furnace;

providing ammonia gas and dichlorosilane gas to the reaction chamber at a ratio of 4 to 6, and at a pressure of 150 millitorr to 250 millitorr to form a silicon nitride layer over the substrate; and

removing the substrate from the LPCVD furnace.

13. The method of claim 12, comprising:

forming an etch mask over the silicon nitride layer;

removing the silicon nitride layer exposed by the etch mask by a reactive ion etch (RIE) process with fluorine radicals; and

subsequently removing the etch mask.

14. The method of claim 13, comprising forming an electrically conductive element at least partially overlapping the silicon nitride layer.

15. The method of claim 14, wherein electrically conductive element is a gate of a GaN FET, and the silicon nitride layer is disposed on a cap layer on the substrate.

16. The method of claim 12, wherein the silicon nitride layer is formed as a conformal layer, and comprising removing the silicon nitride layer from horizontal surfaces of the substrate by an anisotropic RIE process with fluorine radicals, leaving the silicon nitride layer on vertical surfaces of the substrate.

17. The method of claim 16, wherein the microelectronic device is an integrated circuit containing an NMOS transistor, and the silicon nitride layer is formed over a gate of the NMOS transistor, and wherein the silicon nitride layer remaining after the anisotropic RIE process provides gate sidewall spacers adjacent to the gate of the NMOS transistor.

18. The method of claim 12, wherein the microelectronic device is a MEMS device containing a cantilevered element, and the silicon nitride layer is formed as a conformal layer to form on a top surface of the cantilevered element and on a bottom surface of the cantilevered

element.

19. The method of claim 12, wherein the silicon nitride layer protects the substrate during a wet etch process in which material is removed from the substrate in an area exposed by the silicon nitride layer.

20. A method of forming a microelectronic device, comprising:

providing a substrate including gallium nitride;

forming a cap layer of gallium nitride on the substrate;

placing the substrate in an LPCVD furnace;

heating the substrate to a temperature of 800°C to 820°C in the LPCVD furnace;

providing ammonia gas and dichlorosilane gas to the reaction chamber at a ratio of 4 to 6, and at a pressure of 150 millitorr to 250 millitorr to form a silicon nitride layer on the cap layer, the silicon nitride layer having the following properties: a silicon:nitrogen atomic ratio within 2 percent of the ratio 3:4; a stress of 600 megapascals (MPa) to 1000 MPa; and a hydrogen content of less than 5 atomic percent;

removing the substrate from the LPCVD furnace;

forming an etch mask over the silicon nitride layer;

removing the silicon nitride layer exposed by the etch mask by an RIE process with fluorine radicals;

subsequently removing the etch mask; and

forming a gate of a GaN FET over the cap layer between, and partially overlapping, portions of the silicon nitride layer.

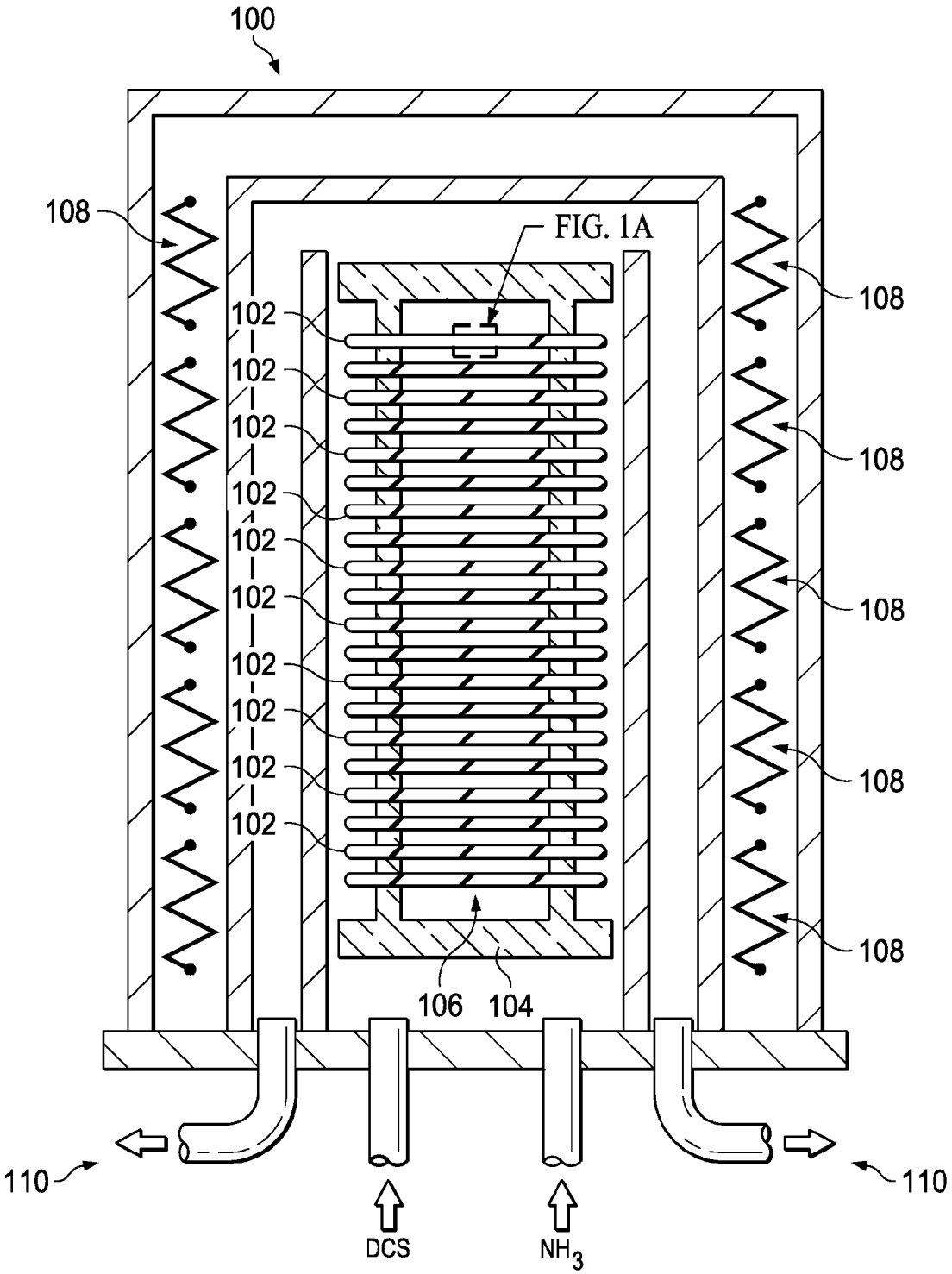
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FIG. 1A
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FIG. 1

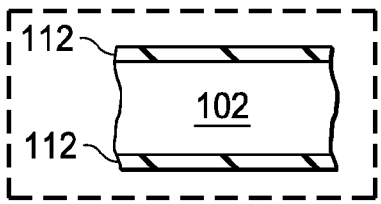
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FIG. 1A

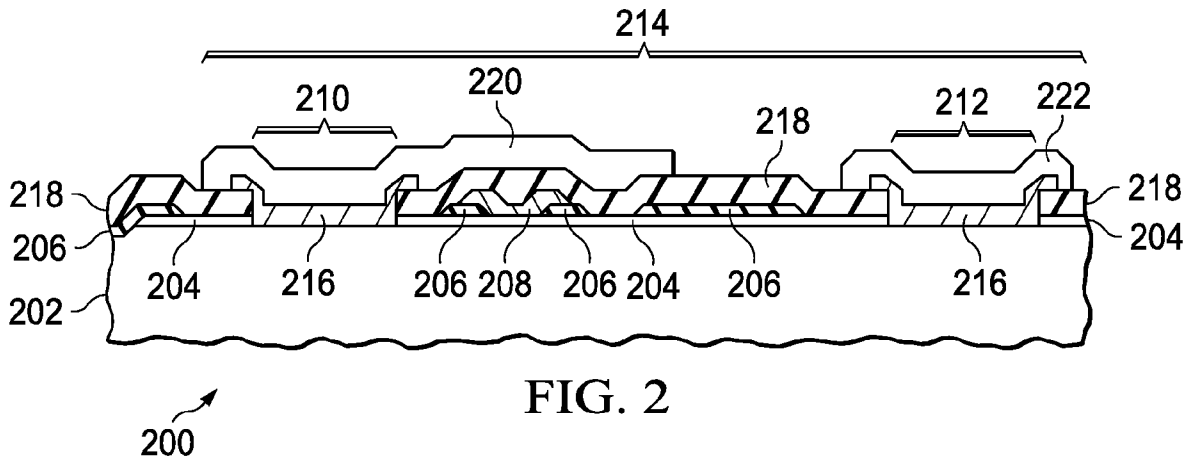

FIG. 2

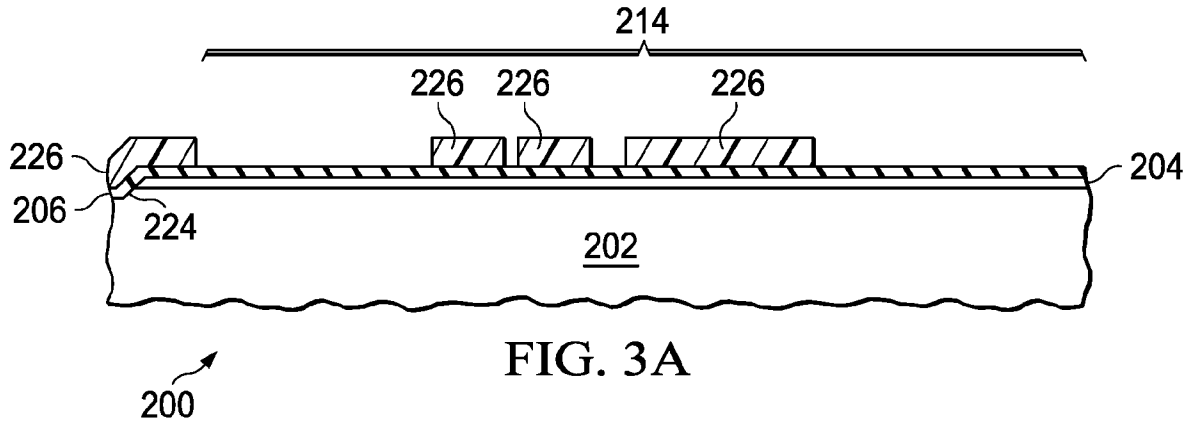

FIG. 3A

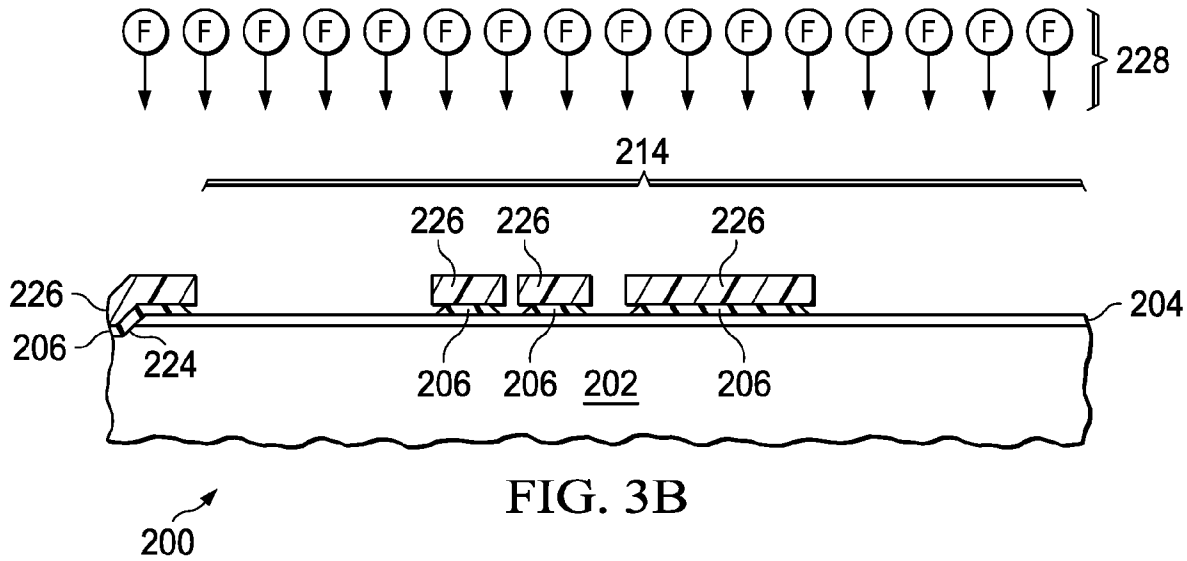

FIG. 3B

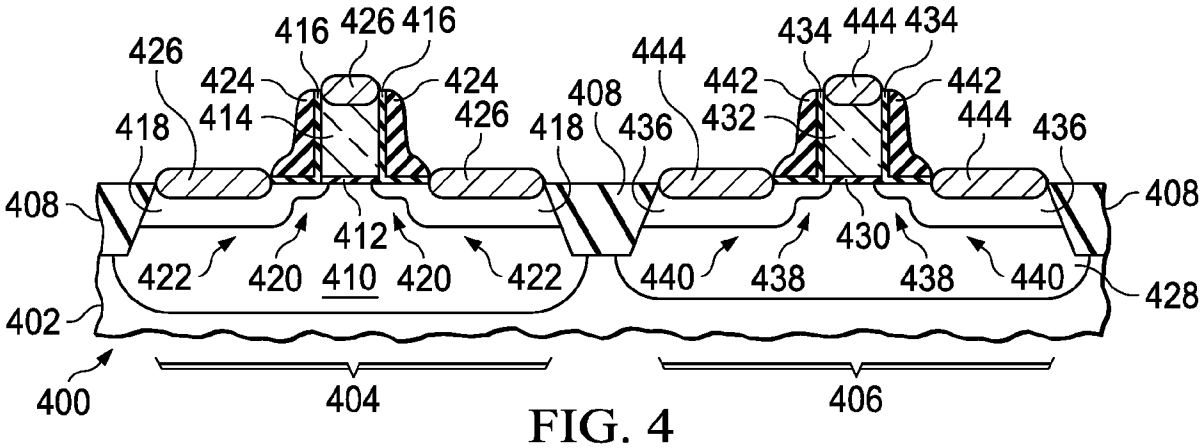

FIG. 4

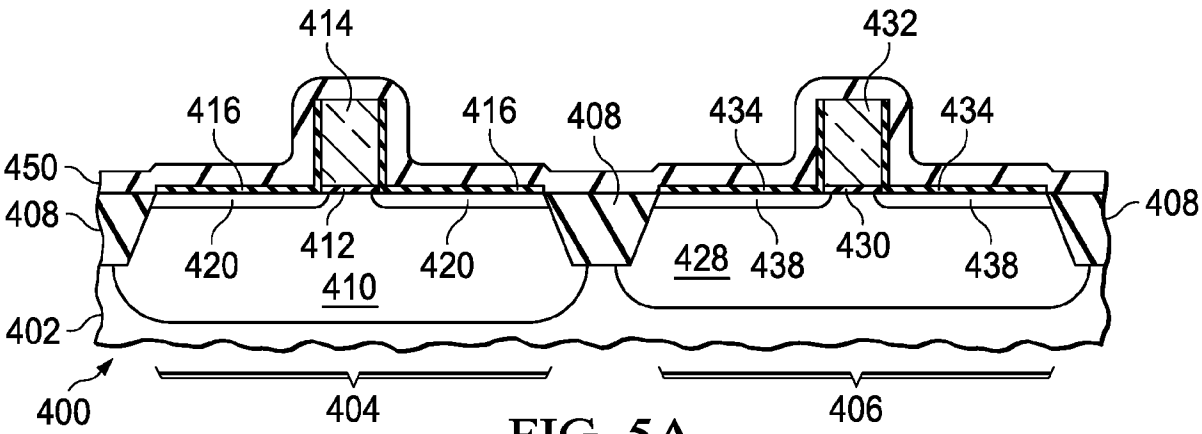

FIG. 5A

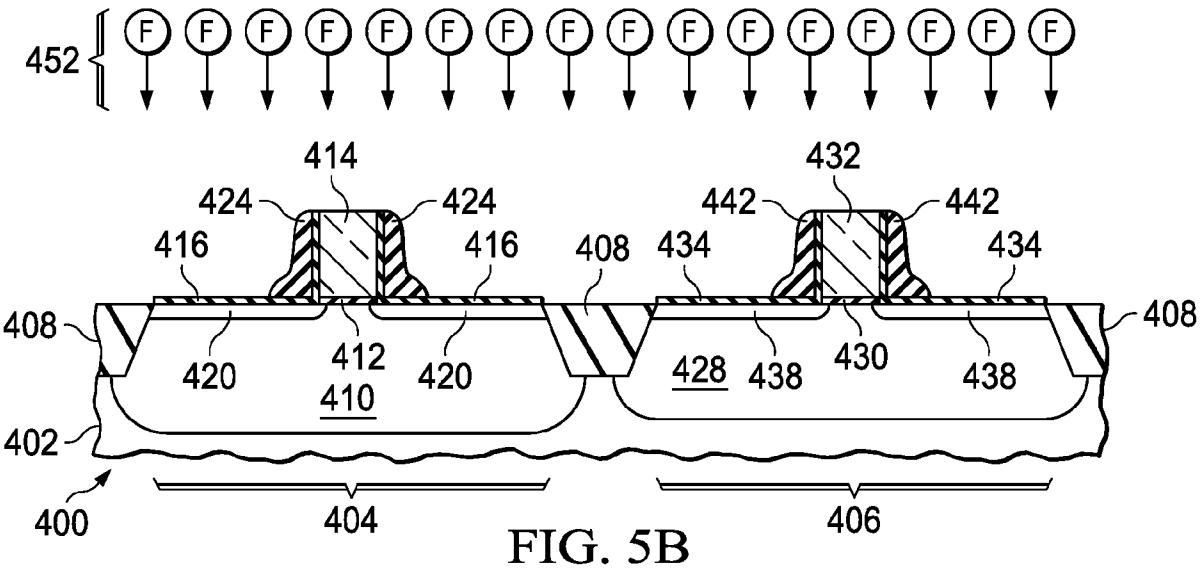

FIG. 5B

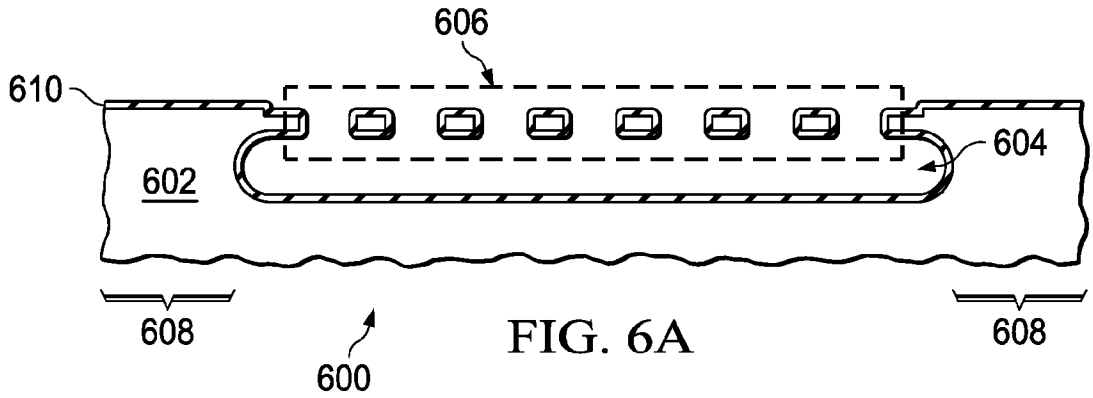
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FIG. 6A

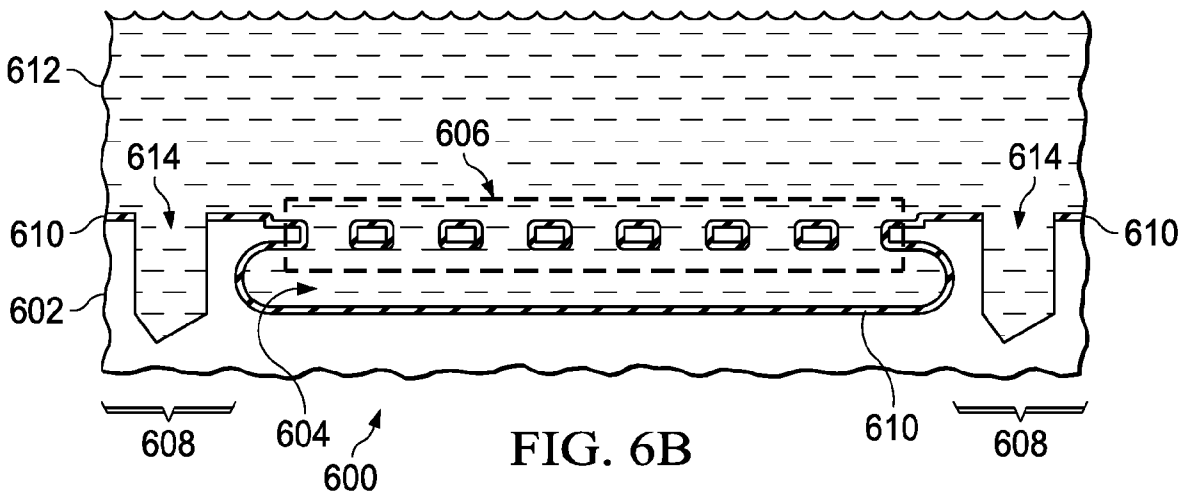
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FIG. 6B

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/031509

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/318 *(2006.01)*
C23C 16/34 *(2006.01)*
H05K 3/02 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/00, 21/02, 21/04, 21/18, 21/30, 21/31, 21/318, 21/336, 21/822, 21/8238, 21/8242, 29/00, 29/40, 29/43, 29/49, 29/51, 29/778, 29/84, H05K 3/00-3/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	TONNBERG Sofia. Optimisation and characterisation of LPCVD silicon nitride thin film growth. Chalmers University of Technology, Goteborg, Sweden, 2006, p. 22, 23, fig. 5.3	12
Y		13-17, 19-20
A		18
Y	GARDENIERS J. G. E. et al. LPCVD silicon-rich silicon nitride films for applications in micromechanics, studied with statistical experimental design. J. Vac. Sci. Technol. A 14(5), Sep/Oct 1996, p. 2879-2892, p. 2879, 2884	1, 3, 6-10, 20
A		2, 4-5, 11

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 July 2016 (20.07.2016)	18 August 2016 (18.08.2016)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer M. Adireeva Telephone No. 499-240-25-91

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2016/031509

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WEBER Hao Jin K. J. et al. Characterization of Low Pressure Chemical Vapour Deposited Si3N4 films. Deniation Renewables-ANZSES 2006, p. 1	1, 3, 6-10, 20
Y	US 2003/0178633 A1 (JEFFREY S. FLYNN et al.) 25.09.2003, [0005], [0021], [0025], [0026]	6, 7
Y	US 2005/0112817 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 26.05.2005, [0002], [0043], fig. 1	14-15, 20
Y	US 2012/0104505 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 03.05.2012, [0028]	9-10, 13, 16-17, 20
Y	US 2011/0297961 A1 (VISIC TECHNOLOGIES LTD.) 08.12.2011, fig. 1a	8
Y	JOSHI B C et al. LPCVD and PECVD silicon nitride for microelectronics technology. Indian Journal of Engineering & Materials Sciences, Vol. 7, October-December 2000, pp. 303-309	19