Title: ASSEMBLIES HAVING SHIELD LINES OF AN UPPER WIRING LEVEL ELECTRICALLY COUPLED WITH SHIELD LINES OF A LOWER WIRING LEVEL

Abstract: Some embodiments include an assembly having a first wiring level with a plurality of first shield lines and first signal lines. The first shield lines and first signal lines have first segments extending along a first direction and second segments extending along the first direction and laterally offset from the first segments. The assembly includes a second wiring level below the first wiring level and having a plurality of second shield lines and second signal lines. The second shield lines and second signal lines have third segments extending along the first direction and fourth segments extending along the first direction and laterally offset from the third segments. The fourth segments of the second shield lines extend to under the first segments of the first shield lines and are electrically coupled to the first segments of the first shield lines through vertical interconnects.
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DESCRIPTION

ASSEMBLIES HAVING SHIELD LINES OF AN UPPER WIRING LEVEL ELECTRICALLY COUPLED WITH SHIELD LINES OF A LOWER WIRING LEVEL

TECHNICAL FIELD

Assemblies having shield lines of an upper wiring level electrically coupled with shield lines of a lower wiring level.

BACKGROUND

Integrated circuitry may comprise multiple levels of stacked wiring. The levels may include signal lines alternately arranged with shield lines. The shield lines may be utilized to alleviate cross-talk between adjacent signal lines. An example configuration comprising three stacked wiring levels is shown in FIG. 1. Specifically, the configuration shows a first level of wiring M1, a second level of wiring M2, and a third level of wiring M3; with M3 being over M2 which in turn is over M1. Although three wiring levels are shown, it is to be understood that there may be other wiring levels below the illustrated levels and/or above the illustrated levels. Also, although the illustrated wiring levels are labeled M1-M3, if other wiring levels are present the shown levels may in fact be M2-M4; M3-M6; etc., depending on the number of wiring levels present beneath the illustrated wiring levels.

Each of the illustrated levels comprises signal lines alternately arranged with shield lines. It may be desired for the shield lines within one level to be electrically connected with shield lines at other levels above and below said one level. For instance, it may be desired for the shield lines within level M2 to be electrically connected with shield lines within level M1 and shield lines within level M3, as such may alleviate coupling noises between the vertically-stacked levels.

Connection of shield lines from level M2 with those of level M1 is relatively straightforward since the lines within level M1 run perpendicular to the lines within level M2. However, the connection of shield lines from level M2 with those of level M3 is problematic since the wiring within level M2 runs parallel to that within level M3, and the shield lines are staggered in level M2 relative to level M3. Thus there is no vertical overlap between the shield lines of level M2 with those of level M3.
It would be desirable to develop architectures which enable coupling between shield lines of stacked levels of the type illustrated as levels M2 and M3 in FIG. 1.

**BRIEF DESCRIPTION OF THE DRAWINGS**

FIG. 1 is a diagrammatic three-dimensional view of a prior art arrangement of wiring levels.

FIGS. 2-2C are diagrammatic views of an example embodiment arrangement of wiring levels. FIG. 2 is a top view. FIGS. 2A-2C are diagrammatic cross-sectional views along the lines 2A-2A, 2B-2B and 2C-2C of FIG. 2, respectively.

FIG. 3 is an enlarged view of a region "3" of FIG. 2.

FIGS. 4 and 4A are diagrammatic views of an example embodiment arrangement of wiring levels. FIG. 4 is a top view. FIG. 4A is a diagrammatic cross-sectional view along the line 4A-4A of FIG. 4.

FIG. 5 is an exploded view of an example embodiment assembly of wiring levels.

Three levels are stacked in the view of FIG. 5.

FIGS. 6-8 are diagrammatic top views of the individual levels of FIG. 5.

FIG. 9 is a diagrammatic top view showing an example mesh containing interconnected shield lines of the three levels of FIG. 5.

FIG. 10 is an exploded view of another example embodiment assembly of wiring levels. Three levels are stacked in the view of FIG. 10.

FIGS. 11-13 are diagrammatic top views of the individual levels of FIG. 10.

FIG. 14 is a diagrammatic top view showing an example mesh containing interconnected shield lines of the three levels of FIG. 10.

FIG. 15A is a diagrammatic top view of an assembly of wiring layers across a substrate, and FIG. 15B is a view of an expanded region of FIG. 15A to illustrate alternating signal lines and shield lines. The three wiring layers of FIG. 5 are stacked in the top view of FIG. 15A, with the portion shown in FIG. 5 being within a region "FIG. 5" of FIG. 15A.

FIG. 16A is a diagrammatic top view of an example arrangement of circuitry across a substrate. FIG. 16B is a view of an expanded region of FIG. 16A to illustrate alternating signal lines and shield lines, and to show a redundant (or dummy) structure.

FIG. 17 is a diagrammatic top view of an example arrangement of circuitry from two stacked wiring layers.
FIG. 18 is a view of an expanded region of FIG. 17 to illustrate alternating signal and shield wiring lines within the stacked wiring layers, and to show redundant (or dummy) structures.

FIG. 19 shows diagrammatic top views comparing example circuit arrangements.

FIG. 20 shows diagrammatic top views comparing a pair of example circuit arrangements.

FIG. 21 is an exploded view of an assembly of example wiring layers that may be utilized in one of the circuit arrangements of FIG. 20. Three wiring layers are stacked in the view of FIG. 21.

FIGS. 22-24 are diagrammatic top views of the individual wiring layers of FIG. 21.

FIG. 25 is a diagrammatic cross-sectional side view along a line 25-25 shown in FIGS. 23 and 24, and through the wiring layers M2 and M3 of FIGS. 23 and 24.

FIG. 26 is a view of an expanded region of FIGS. 23 and 24, and shows the wiring layer of FIG. 24 stacked over that of FIG. 23. The region of FIG. 26 is indicated by a dashed line "FIG. 26" in FIGS. 23 and 24.

FIGS. 27A-27C are expanded diagrammatic top views of a region of the M2 wiring layer of FIG. 23 showing example alternative configurations.

FIG. 28 is an exploded view of an assembly of example wiring layers that may be utilized in one of the circuit arrangements of FIG. 20. Three layers are stacked in the view of FIG. 28.

FIGS. 29-31 are diagrammatic top views of the individual layers of FIG. 28.

FIGS. 32A-C are diagrammatic cross-sectional side views along lines 32A-32A, 32B-32B and 32C-32C of FIGS. 30 and 31, and are through the wiring layers M2 and M3 of FIGS. 30 and 31.

FIGS. 33 and 34 are expanded diagrammatic top views of regions of the wiring layer M3 of FIG. 31 showing example alternative configurations.

FIGS. 35 and 36 are expanded diagrammatic top views of regions of the wiring layer M2 of FIG. 30 showing example alternative configurations.

**DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS**

Some embodiments include architectures in which the signal lines and shield lines within wiring layers are configured to have offset regions. Such offset regions may enable a vertical overlap to occur between shield lines of an upper wiring layer and
shield lines of a lower wiring layer, even though the shield lines within both wiring layers run substantially parallel with one another, and even though the shield lines within the lower wiring layer are staggered relative to the shield lines within the upper wiring layer in a configuration analogous to that of FIG. 1.

Example embodiments are described with reference to FIGS. 2-36.

Referring to FIGS. 2-2C, a region of an integrated assembly 510 is illustrated. The assembly 510 includes a pair of vertically-stacked wiring levels M2 and M3. The level M2 is shown in dashed-line in the top-down view of FIG. 2 to indicate that such level is beneath the level M3.

Level M3 comprises a shield line 512 and a signal line 514 immediately adjacent the shield line. The lines 512 and 514 may be representative of a large plurality of shield lines and signal lines formed in alternating relationship within the wiring level M3.

Level M2 comprises a shield line 516 and a signal line 518 immediately adjacent the shield line. The lines 516 and 518 may be representative of a large plurality of shield lines and signal lines formed in alternating relationship within the wiring level M2.

In some embodiments the wiring level M3 may be referred to as a first wiring level, and the wiring level M2 may be referred to as a second wiring level beneath the first wiring level. The shield line 512 and signal line 514 within the first wiring level may be referred to as a first shield line and a first signal line, and such may be representative of a plurality of first shield lines and first signal lines formed in alternating arrangement across the first wiring level. Similarly, the shield line 516 and signal line 518 of the second wiring level be referred to as a second shield line and second signal line, and such may be representative of a plurality of second shield lines and second signal lines formed in alternating arrangement across the second wiring level.

The first shield line 512 has a first segment 520 and a second segment 522 laterally offset from the first segment. The first and second segments 520 and 522 are connected to one another through a linking segment 524. The linking segment 524 may be arranged to connect an end of the first segment 520 and an end of the second segment 522. The first segment 520 may be elongated from one end of the linking segment 524.

The second segment 522 may be elongated oppositely against the first segment 520 from another end of the linking segment 524. Similarly, the first signal line 514 has a first segment 526, a second segment 528 laterally offset from the first segment, and a linking segment 530 which interconnects the first and second segments 526 and 528 to one another. The linking segment 530 may be arranged to connect an end of the first segment
526 and an end of the second segment 528. The first segment 526 may be elongated from one end of the linking segment 530. The second segment 528 may be elongated oppositely against the first segment 526 from another end of the linking segment 530.

The second shield line and second signal line within the second wiring level M2 have segments similar to those of the first wiring level M3. However, in order to simplify the explanation, the segments of the second shield line and second signal line will be referred to as third and fourth segments to distinguish them from the first and second segments of the first shield line 512 and first signal line 514. Accordingly, the second shield line 516 has a third segment 532 and a fourth segment 534 laterally offset from the third segment. The third and fourth segments 532 and 534 are connected to one another through a linking segment 536. The linking segment 536 may be arranged to connect an end of the third segment 532 and an end of the fourth segment 534. The third segment 532 may be elongated from one end of the linking segment 536. The fourth segment 534 may be elongated oppositely against the third segment 532 from another end of the linking segment 536. Similarly, the second signal line 518 has a third segment 538, a fourth segment 540 laterally offset from the third segment, and a linking segment 542 which interconnects the third and fourth segments 538 and 540 to one another. The linking segment 542 may be arranged to connect an end of the third segment 538 and an end of the fourth segment 540. The third segment 538 may be elongated from one end of the linking segment 542. The fourth segment 540 may be elongated oppositely against the third segment 538 from another end of the linking segment 542. In some embodiments, the linking segments 524 and 530 within the first wiring level M3 may be referred to as first linking segments, and the linking segments 536 and 542 within the second wiring level M2 may be referred to as second linking segments so that linking segments within the different wiring levels may be distinguished from one another.

An axis system is provided adjacent the top view of FIG. 2. The axis system shows a first axis 503 and a second axis 505 which extends orthogonally relative to the first axis. The first and second segments 520, 522, 526 and 528 extend primarily along a first direction corresponding to the axis 503, and the linking segments 524 and 530 extend primarily along a second direction corresponding to the axis 505. The segments are indicated to extend "primarily" along the indicated directions to indicate that the overall course of the segments is along the indicated directions even if the segments are wavy or otherwise not straight. In some embodiments the segments may be substantially
straight, with the term "substantially straight" meaning that the segments are straight to
within reasonable tolerances of fabrication and measurement.

The third and fourth segments 532, 534, 538 and 540 also extend primarily along
the first direction corresponding to the axis 503, and the linking segments 536 and 542
extend primarily along the second axis 505 in the illustrated embodiment.

In the shown embodiment the linking segment 524 extends substantially
orthogonally to the first and second segments 520 and 522 of shield line 512, the linking
segment 530 extends substantially orthogonally to the first and second segments 526 and
528 of signal line 514, the linking segment 536 extends substantially orthogonally to the
third and fourth segments 532 and 534 of the second shield line 516, and the linking
segment 542 extends substantially orthogonally to the segments 538 and 540 of the
second signal line 518. The term "substantially orthogonally" means that the linking
segments extend orthogonally to the other indicated segments to within reasonable
tolerances of fabrication and measurement. In other embodiments one or both of the
linking segments may extend at an angle other than orthogonal relative to the primary
direction of the segments interconnected by such linking segment.

An advantage of the architecture of FIG. 2 is that the offsets (i.e. bends) provided
in the signal lines and shield lines enable a region of a shield line from the upper wiring
level M3 to vertically overlap a region of a shield line from the lower wiring level M2.
Specifically, the shield line 512 of the upper wiring level vertically overlaps a region of
the shield line 516 of the lower wiring level within an illustrated overlap region 544;
with the illustrated fourth segment 534 of the second shield line 516 extending to under
the first segment 520 of the first shield line 512.

Vertical interconnects 546 are provided within the overlap region 544 to
electrically couple the shield lines 516 and 512 to one another. The vertical interconnects
546 are illustrated in dashed-line (phantom) in the top view of FIG. 2 to indicate that the
interconnects are beneath line 512. The vertical interconnects may extend substantially
vertically, with the term "substantially vertically" meaning that the interconnects are
vertical to within reasonable tolerances of fabrication and measurement.

The illustrated embodiment shows two vertical interconnects within the overlap
region 544. In other embodiments there may be only a single interconnect provided
within the overlap region, or there may be more than two interconnects provided within
the overlap region. Also, although the interconnects 546 are square along the top view of
FIG. 2, in other embodiments the interconnects may have other shapes, including, for example, rectangular, circular, elliptical, etc.

An alternative description of the assembly 510 of FIGS. 2-2C is as follows. The first shield line 512 within the upper wiring level may be considered to have a first portion 548 extending in the first direction of axis 503, a second portion 550 which extends in a second direction (e.g., the direction of axis 505), and a third portion 552 which extends in the first direction. The second portion 550 interconnects the first portion 548 with the third portion 552. The first signal line 514 within the upper wiring layer is immediately adjacent the first shield line, and has a fourth portion 554, a fifth portion 556, and a sixth portion 558. The fourth, fifth and sixth portions (554, 556 and 558) are substantially parallel to the third, second and first portions (552, 550 and 548), respectively. The term "substantially parallel" means parallel to within reasonable tolerances of fabrication and measurement.

Continuing the alternative description of assembly 510, the second shield line 516 within the lower wiring level comprises a seventh portion 560 and an eighth portion 562; with the seventh portion 560 being substantially vertically aligned with the third portion 552 of first shield line 512, and the eighth portion 562 being substantially vertically aligned with the fourth portion 554 of the first signal line 514. The second shield line 516 also comprises a ninth portion 564 which interconnects the seventh portion 560 with the eighth portion 562. The seventh portion 560 extends continuously from under the third portion 552 of first shield line 512 to under the sixth portion 558 of first signal line 514; with the seventh portion 560 being substantially vertically aligned with the third portion 552 of first shield line 512.

Further continuing the alternative description of assembly 510, the overlap region 544 extends across the third portion 552 of first shield line 512 and the seventh portion 560 of second shield line 516, and the vertical interconnects 546 electrically connect the third portion 552 with the seventh portion 560.

FIG. 3 shows an enlarged view of a region "3" of the assembly 510 of FIG. 2, and will be used to describe some of the dimensional relationships within such assembly.

The shield line 512 may be considered an individual first shield line representative of a plurality of shield lines within the upper wiring level, and the signal line 514 may be considered an individual first signal line representative of a plurality of signal lines within the upper wiring level. Similarly, the second shield line 516 may be considered an individual second shield line representative of a plurality of second shield
lines within the lower wiring level, and the second signal line 518 may be considered an individual second signal line representative of a plurality of second signal lines within the lower wiring level.

The first signal line 514 is immediately adjacent the first shield line 512, with the term "immediately adjacent" indicating that there are no other signal lines between signal line 514 and shield line 512 within the upper wiring level (i.e., that signal line 514 is the signal line closest to shield line 512 within the upper wiring level).

The first shield line 512 has the first shield line first segment 520, the first shield line second segment 522, and the linking segment 524 between the first and second segments 520 and 522. The linking segment 524 may be referred to as a first shield line linking segment.

The signal line 514 includes the first signal line first segment 526, the first signal line second segment 528, and the linking segment 530 between the first and second segments 526 and 528. The linking segment 530 may be referred to as a first signal line linking segment.

The first shield line linking segment 524 is offset from the first signal line linking segment 530 along the first direction of axis 503 by a first distance Di.

The second shield line 516 comprises a third segment 532 that is under a region of the first signal line first segment 526. The second shield line 516 also has a fourth segment 534 that extends to under a region of the signal line second segment 528, and that also extends to under a region of the first shield line first segment 520. A second shield line linking segment 536 connects the third segment 532 with the fourth segment 534.

The vertical interconnects 546 extend between the first shield line first segment 520 and the second shield line fourth segment 534 to electrically couple the first and second shield lines 512 and 516 to one another (i.e., to electrically couple the shield line 512 from the upper wiring layer with the shield line 516 from the lower wiring layer).

The second shield line linking segment 536 is offset from the first signal line linking segment 530 along the first direction of axis 503 by a second distance D2.

The second distance D2 is larger than the first distance Di, and in some embodiments may be at least double the first distance.

FIG. 3 also shows that the first shield line 512 and first signal line 514 are spaced from one another by a third distance D3 corresponding to a pitch, and shows that adjacent corners of shield line 512 and signal line 514 are spaced by a fourth distance D4 which
extends along a direction corresponding to an axis 507. The direction of axis 507 is
intermediate the directions of axes 503 and 505, and in some embodiments may be about
45° (i.e., halfway between axes 503 and 505).

In some embodiments the D₄ shift may be considered equivalent to a D₃ shift in
combination with a D₄i shift.

In some embodiments, the illustrated linking segments (e.g., 524, 530 and 536)
may be considered to define steps or bridge paths along the various shield lines and
signal lines.

The wiring level M2 of FIGS. 2 and 3 may be over another wiring level
analogous to the level M1 of FIG. 1. FIGS. 4 and 4A show a region of assembly 510
beneath the region illustrated in FIGS. 2 and 3, and specifically show a third wiring level
M1 under the second wiring level M2 (the level M3 is not shown in FIGS. 4 and 4A in
order to simplify the drawings). The illustrated region of the wiring level M2 of FIG. 4
has the second shield line 516 between a pair of second signal lines 518.

The wiring level M1 includes a signal line 566 between a pair of shield lines 568.
The signal lines and shield lines within the third wiring level M1 may be referred to as
third signal lines and third shield lines in order to distinguish them from the second
shield lines and second signal lines within the second wiring level M2, and to distinguish
them from the first shield lines and first signal lines within the first wiring level M3
(FIG. 2). In the illustrated embodiment, the shield lines and signal lines within the wiring
level M1 extend primarily along the direction of axis 505, or in other words extend
substantially orthogonally to the third and fourth segments 532 and 534 of the second
shield line 516.

The third shield lines 568 are electrically coupled to the third and fourth segments
532 and 534 of the second shield line 516 through vertical interconnects 570 (or
alternatively considered, are electrically coupled to the seventh and eighth portions 560
and 562 of the second shield line through the vertical interconnects 570). In some
embodiments, the vertical interconnects 546 (i.e., the interconnects utilized to connect
shield lines within the first wiring level M3 to shield lines within the second wiring level
M2) may be referred to as a first set of interconnects, and the interconnects 570 may be
referred to as a second set of interconnects in order to distinguish the interconnects 570
from the interconnects 546. The interconnects 546 and 570 are shown to be square and
circular in the top view of FIG. 4 in order to provide clear visual distinction between
interconnects 546 and 570. In actual practice the interconnects 46 and 70 may be the
same shape as one another or may be different shapes; and may be of any suitable shapes, including, for example, square, rectangular, circular, elliptical, etc. The vertical interconnects 570 are illustrated in dashed-line (phantom) in the top view of FIG. 4 to indicate that the interconnects 570 are beneath line 516, and the interconnects 546 are illustrated in dashed-line view to indicate that it is locations of interconnects 546 illustrated in such view (the interconnects 546 may or may not be visible in the view of FIG. 4 depending on the particular architecture of the interconnects 546 and on whether the location chosen for the view of FIG. 4 is a cross-section through the interconnects 546).

FIGS. 5-8 further illustrate an assembly 510 comprising the wiring levels M1, M2 and M3. FIG. 5 is an exploded view showing the wiring levels stacked one atop another; while FIGS. 6-8 show each of the individual wiring levels M1, M2 and M3 in isolation. The wiring within level M3 is shown to be slightly thicker than the wiring within levels M2 and M1. In practice the wiring within levels M1-M3 may all be the same thickness or some wiring may be of different thickness relative to other wiring, depending on the application.

The assembly 510 of FIGS. 5-8 may be considered to comprise a connecting region 572 which encompasses the interconnects 546, and more specifically encompasses locations where portions of the shield lines 512 of level M3 vertically overlap portions of the shield lines 516 of level M2. The linking regions of the shield lines and signal lines within the levels M2 and M3 are within the connecting region 572 (such linking regions are described above with reference to FIG. 2, and may be alternatively referred to as bending regions, bridge regions, etc.).

The connecting region may be considered to comprise a first boundary 571 and a second boundary 573. A first shield region 574 extends outwardly from the connecting region 572 along the direction of axis 505, and a second shield region 576 extends outwardly from the connecting region 572 along the direction of axis 503. The signal lines 514 of level M3 vertically overlap the shield lines 516 of level M2 within the first and second shield regions 574 and 576; and the shield lines 512 of level M3 vertically overlap the signal lines 518 of level M2 within the first and second shield regions.

In the embodiment of FIGS. 5-8, all of the shield lines within the wiring levels M3, M2 and M1 are electrically connected with Vss (the voltage Vss may be any suitable voltage, and in some embodiments may be ground or a negative supply voltage). The various shield lines from the wiring levels M3, M2 and M1 together may form a
three-dimensional mesh 578 of the type shown in FIG. 9, with such mesh having consistent voltage throughout. Specifically, the mesh of FIG. 9 comprises the first shield lines 512 from the upper wiring level M3, the second shield lines 516 from the intermediate wiring level M2, and the third shield lines 568 from the lower wiring level M1. The shield lines 512, 516 and 568 are illustrated with different thicknesses of lines so they may be distinguished from one another in the diagram of FIG. 9. In actual practice, the shield lines may all have substantially the same thickness as one another (or in some embodiments, some of the shield lines may have different thicknesses than others if such is suitable for particular applications). Regions where shield lines from level M3 connect with shield lines from level M2 are shown as overlap regions 544, and such would comprise the vertical interconnects 546 (shown in FIGS. 5-8, but not shown in FIG. 9).

One aspect of the embodiment of FIG. 9 is that each of the first shield lines 512 from the top wiring level M3 is directly connected to a pair of the second shield lines 516 from the intermediate wiring level M2; and conversely, each of the second shield lines 516 from the intermediate wiring level is directly connected to a pair of the first shield lines 512 from the top wiring level. The shield lines 512 and 516 comprise the bridging regions (i.e. linking regions) 524 and 536 described previously.

FIG. 9 shows two of the first shield lines 512 labeled as 512a and 512b to distinguish them from others of the first shield lines, and shows two of the second shield lines 516 labeled as 516a and 516b to distinguish them from others of the second shield lines. The first shield line 512a extends primarily along a first direction corresponding to the axis 503, and extends along two first paths 580 and 582 which are laterally offset relative to one another. Similarly, the second shield line 516b extends primarily along the first direction of axis 503, and extends along two second paths 590 and 592 which are laterally offset relative to one another. The first shield line 512a is primarily laterally offset from the second shield lines 516 except that the first paths 580 and 582 have overlap regions 544 where portions of the first shield line 512a overlap portions of the second shield lines 516a and 516b. Specific overlap regions where portions of the first shield line 512a overlap portions of second shield lines 516a and 516b are labeled as 584 and 586.

Notably, the path 580 of shield line 512a overlaps a second shield line 516a, while the path 582 of the same first shield line 512a overlaps a different second shield line 516b. In a similar manner, the second shield line 516b connects with two different
first shield lines 512a and 512b. Vertical interconnects 546 (not shown in FIG. 9) are
provided within the overlap regions 544 to connect the first shield lines 512 with the
second shield lines 516.

The shield lines 568 of the bottom wiring level M1 may be connected to the
shield lines 516 of the intermediate wiring level M2 through vertical contacts 570 (not
shown in FIG. 9) of the type described above with reference to FIG. 4.

The interwoven interconnections between the first, second and third wiring levels
within mesh 578 enable consistent voltage to be maintained throughout all of the shield
lines that are intertwined within such mesh. Such may alleviate or prevent the problems
described above in the "Background" section of this disclosure.

FIGS. 5-9 illustrate an embodiment in which all of the shield lines are maintained
at a common voltage (illustrated as being Vss, but in other embodiments it may be a
common voltage other than Vss). In some embodiments the shield lines maybe
subdivided amongst groups maintained at different voltages relative to one another. For
instance, in some embodiments some of the shield lines may be maintained at Vss while
others are maintained at Vdd. An example embodiment in which some shield lines are
electrically connected with Vss while others are electrically connected with Vdd is
described with reference to FIGS. 10-14.

The wiring levels M1, M2 and M3 of assembly 10 are illustrated in FIGS. 10-13.
FIG. 10 is an exploded view showing the wiring levels stacked one atop another; while
FIGS. 11-13 show each of the individual wiring levels M1, M2 and M3 in isolation.

The general architecture of FIGS. 10-13 is similar to that described above with
service to FIGS. 5-8, except that additional complexity is introduced so that the shield
lines within the various levels M1-M3 may comprise some shield lines electrically
connected with Vdd and others are electrically connected with Vss.

The various shield lines from the wiring levels M3, M2 and M1 together may
form a pair of three-dimensional meshes similar to the mesh shown in FIG. 9. One of
such meshes is electrically connected with Vss and the other is electrically connected
with Vdd. FIG. 14 shows a three-dimensional mesh 88 which is electrically connected
with Vss, and a similar mesh (not shown) would be electrically connected with Vdd.

The assemblies discussed above may be incorporated into integrated circuitry
supported by an underlying semiconductor substrate (not shown). The substrate may, for
example, comprise, consist essentially of, or consist of monocryalline silicon. The term
"semiconductor substrate" means any construction comprising semiconductive material,
including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductor substrates described above.

In some embodiments, the invention includes architectures which reduce distances between interconnects coupling the shield lines of an upper wiring layer (e.g., M3) to the shield lines of a lower wiring layer (e.g., M2), which enables decreased via-bypass pitch. The signal lines within a given via-bypass pitch may be coupled with a common bus. Accordingly, decreasing the via-bypass pitch may lead to a reduction of the number of signal lines associated with each bus, and thus may lead to reduced resistance across the signal lines and associated buses.

FIGS. 15A and 15B show the assembly 510 comprising the arrangement of FIG. 5, but illustrated in an alternative manner relative to FIG. 5. The assembly 510 is shown in top view in FIG. 15A, with the lines of the wiring layers being heavily compressed. An expanded region of the top wiring layer M3 is shown in cross-sectional side view in FIG. 15B to assist the reader in understanding the top view of FIG. 15A. An approximate location of the illustrated portion of FIG. 5 is diagrammatically illustrated in FIG. 15A as corresponding to region labeled "FIG. 5". The connecting region 572 is diagrammatically illustrated with a line traversing the top view of FIG. 15A.

A continuing goal of semiconductor fabrication is to increase circuit density (i.e., to increase the level of integration). A problem with the architecture of FIGS. 5, 15A and 15B is that there may be a large distance along individual shield lines of a given wiring layer (e.g., shield lines 512 of wiring layer M3 shown in FIGS. 5 and 6) between the interconnects (546 of FIG. 5) utilized to couple the shield lines to shield lines of other wiring layers (e.g., shield lines 516 of wiring layer M2, shown in FIGS. 5 and 7). Such problem is illustrated in the top view of FIG. 15A with an arrow 320 indicating a pitch between interconnects (i.e., a via-bypass pitch). The arrow 320 is open-ended to indicate that the full via-bypass pitch is not visible in the top view of FIG. 15A.

The signal lines (e.g., signal lines 514 of wiring layer M3 (shown in FIG. 6), signal lines 518 of wiring layer M2 (shown in FIG. 7), etc.) are coupled with associated buses (i.e., electrical pathways), and the number of signal lines coupled with an individual bus may be correlated with the via-bypass pitch.
As circuit density increases, there may be an increasing demand on the shield lines (e.g., increased voltage along the shield lines and/or increased current along the shield lines). Also, increased density of signal lines may lead to increased resistance along the signal lines and the associated buses. Accordingly, it would be desired to develop new architectures which reduce distances between interconnects coupling shield lines of one wiring layer to the shield lines of another wiring layer, and which reduce resistances along the signal lines and associated buses.

In some embodiments, one or more redundant (dummy) lanes are provided within the shield line/signal line circuitry of wiring layers (e.g., M2 and M3) in order to enable a reduction of the via-bypass pitch. In such embodiments, bus lines may be considered to be arranged amongst subgroups by providing one or more redundant (dummy) lanes within the signal line/shield line circuitry. For instance, the number of bus lines may be represented as "n", and the bus lines may be arranged into "m" subgroups; with each of the "m" subgroups having "k" signal lines. In some embodiments, the via-bypass pitch on the shield lines may be 1/m as compared to architectures in which the bus lines are not consolidated into the subgroups.

As indicated above, the term "dummy" may be utilized to describe the redundant lanes, with such term indicating that the redundant lanes are different than the other lanes comprising shield/signal lines. In some contexts, the label "dummy" is utilized to identify structures which have no function other than to serve as spacers (i.e., which are not utilized as wiring or components of integrated circuitry). Such is generally not the case in the present context. Instead, the "dummy" structures may include circuitry (for instance, shield lines), and the label "dummy" may be utilized to indicate that a structure (for instance, a shield line) within a wiring layer has a different configuration and/or use than other similar structures across the wiring layer having more traditional configurations.

The dummy (i.e., redundant) structures may be configured as "lanes", or may correspond to other suitable structures and regions.

Example calculations relative to a configuration having 288 signal lines indicate that a single group (i.e., only one sub-group) leads to a worst resistance value of 40.95 ohms, two subgroups leads to the worst resistance value being 21.85 ohms, eight subgroups leads to the worst resistance value being 12.23 ohms, and 16 subgroups leads to the worst resistance value being 6.73 ohms. Accordingly, arrangement of the signal lines amongst subgroups may lead to substantial improvement (specifically, reduction in...
resistance). The calculated resistance values are provided to assist the reader in understanding the invention, and are not to be utilized for limiting the claims that follow; except to the extent, if any, that such values are expressly recited in the claims.

FIGS. 16A and 16B show an assembly 10 analogous to the assembly 510 of FIGS. 15A and 15B. Such assembly may comprise the wiring layers M1, M2 and M3 (analogous to those of FIG. 5) stacked one atop another. FIG. 16A shows a top view with the lines of the upper wiring layer M3 being heavily compressed (analogous to the top view of FIG. 15A), and FIG. 16B shows an expanded region of the top wiring layer M3 in cross-sectional side view. The wiring layer M3 of FIG. 16B comprises shield lines 12 and signal lines 14 analogous to the shield lines 512 and signal lines 514 of FIG. 15B. Additionally, the wiring layer M3 of FIGS. 16A and 16B comprises a redundant (dummy) lane 15 which segregates the shield lines/signal lines of the wiring layer M3 into subgroups 16a and 16b.

A connecting region 18a is associated with subgroup 16a, and a connecting region 18b is associated with subgroup 16b; and such connecting regions 18a/18b are diagrammatically illustrated with lines traversing the top view of FIG. 16A. The connecting regions 18a/18b are analogous to the connecting region 372 of FIG. 15A. However, the connecting regions 18a/18b are on a reduced pitch relative to the connecting region 372 of FIG. 15A, which reduces the via-bypass pitch. Specifically, an arrow 21 is provided in FIG. 16A to diagrammatically illustrate a via-bypass pitch. Such via-bypass pitch 21 is substantially reduced (and in some embodiments may be reduced by about half) as compared to the via-bypass pitch 320 of the assembly 510 of FIG. 15A. The reduction of the via-bypass pitch may substantially reduce resistance along the signal lines and associated buses of assembly 10 of FIG. 16A as compared to the assembly 510 of FIG. 15A.

FIGS. 17 and 18 illustrate an alternative view of the assembly 10 of FIG. 16; with the view of FIG. 18 being an expanded region of FIG. 17.

FIGS. 17 and 18 show wiring layer M3 overlaid on wiring layer M2; and show interconnects 20 and 22 analogous to the interconnects 546 and 570, respectively, which were described above with reference to FIG. 5. Specifically, the interconnects 20 vertically connect shield lines of wiring layer M2 with shield lines of wiring layer M3, and the interconnects 22 vertically connect shield lines of wiring layer M2 with shield lines of wiring layer M1 (not shown in FIGS. 17 and 18). The interconnects 20 and 22 are shown as square features and circular features, respectively, to enable the
interconnects 20 to be readily distinguished from interconnects 22 in the illustrations, but in other applications the interconnects 20 and 22 may have other shapes; and may be the same shape as one another, or different shapes relative to one another.

The wiring layers M2 and M3 are shown in dashed-line view and solid-line view, respectively, in FIGS. 17 and 18 so that they may be distinguished from one another.

FIG. 18 shows a pair of lines (Linel and Line2) provided across the assembly 10, with the status (configuration) of materials in the M2 and M3 wiring layers at locations of each line being described in a table beneath the diagram of assembly 10. The signal lines are represented as "Sig", and the shield lines are represented as "Vss". The term Vss is chosen in that it is common for the shield lines of the wiring layers M3, M2 and M1 to be electrically connected with Vss (with it being understood that the voltage Vss may be any suitable voltage, and in some embodiments may be ground or a negative supply voltage). The shield lines may be coupled with voltage other than Vss in some embodiments.

The table of FIG. 18 shows that the redundant lane 15 differs from other locations of the wiring layers M2/M3 along the position of Linel. Specifically, the redundant lane 15 comprises a space below a signal line of wiring layer M3, and comprises a space above the shield line of wiring layer M2. In contrast, the redundant lane 15 has a same configuration as other locations of the wiring layers M2/M3 at the position of Line2 and simply comprises a Vss line of M3 over a signal line of M2, and a signal line of M3 over a Vss line of M2. Although the term "space" is utilized to describe locations along Linel, it is to be understood that the locations indicated as "space" may comprise insulative materials (e.g., silicon nitride, silicon dioxide, etc.).

FIG. 19 compares the assembly 510 (described above with reference to FIG. 15A) with example assemblies 10, 10a and 10b of other embodiments. The assembly 10 is similar to that described above with reference to FIG. 16A. The assemblies 10a and 10b incorporate additional redundant lanes 15 to thereby form additional subgroups. Specifically, assembly 10 has two subgroups 16a and 16b; assembly 10a has four subgroups 16a, 16b, 16c and 16d; and assembly 10b has eight subgroups 16a, 16b, 16c, 16d, 16e, 16f, 16g and 16h. Example resistances across signal lines and associated buses within the subgroups are estimated to be about 40.95 ohms for assembly 300; 21.85 ohms for assembly 10; 12.23 ohms for assembly 10a; and 6.73 ohms for assembly 10b. Accordingly, arrangement of the signal lines into subgroups within the assemblies 10,
10a and 10b may lead to substantial improvement (specifically, reduction in resistance across signal lines and associated buses).

FIG. 20 shows top views of a pair of example assemblies 10c and 10d which may be utilized in some embodiments. The assembly 10c has connecting regions 18a and 18b which are mirrored about a first plane 5 through a middle of the assembly, and which are also mirrored about a second plane 7 through the middle of the assembly and orthogonal to the first plane 5. The connecting region 18b is shown with a heavier line than the connecting region 18a so that the connecting regions 18a and 18b can be distinguished from one another. A region A is identified in assembly 10c, and such region is discussed in more detail below with reference to FIGS. 21-27.

The assembly 10d has connecting regions 18a and 18b which are mirrored about the plane 5 through the middle of the assembly. Regions B and B’ are identified in assembly 10d, and such regions are discussed in more detail below with reference to FIGS. 28-36.

FIGS. 21-24 illustrate assembly 10c, and show the wiring layers M1, M2 and M3. FIG. 21 is an exploded view showing the wiring layers stacked one atop another; while FIGS. 22-24 show each of the individual wiring layers M1, M2 and M3 in isolation.

Referring to FIG. 22, the wiring layer M1 includes signal lines 30 alternating with shield lines 32. The signal lines and shield lines are spaced from one another by insulative material 34. The shield lines 32 are shown supplied with (i.e., coupled with) a fixed voltage identified as Vss, but may be supplied with any suitable voltage.

The signal lines 30 and shield lines 32 may comprise any suitable electrically conductive composition(s), such as, for example, one or more of various metals (e.g., titanium, tungsten, cobalt, nickel, platinum, etc.), metal-containing compositions (e.g., metal silicide, metal nitride, metal carbide, etc.), and/or conductively-doped semiconductor materials (e.g., conductively-doped silicon, conductively-doped germanium, etc.). The conductive materials of the signal lines 30 and shield lines 32 may be homogenous, or may comprise two or more discrete compositions. The conductive material of the shield lines 32 may be the same as the conductive material of the signal lines 30, or may be different from the conductive material of the signal lines.

The insulative material 34 may comprise any suitable composition, and in some embodiments may comprise, consist essentially of, or consist of one or both of silicon dioxide and silicon nitride. The insulative material 34 may be homogenous, or may comprise two or more discrete compositions.
The interconnects 22 (only some of which are labeled) are shown along the shield lines 32, with such interconnects 22 being utilized to vertically connect shield lines 32 of wiring layer M1 with shield lines 42 of wiring layer M2 (shown in FIG. 23).

Referring to FIG. 23, the wiring layer M2 includes signal lines 40 alternating with shield lines 42. The signal lines and shield lines are spaced from one another by the insulative material 34. The shield lines 42 are shown coupled with a fixed voltage identified as Vss, but may be coupled with any suitable voltage.

The signal lines 40 and shield lines 42 may comprise any suitable electrically conductive composition(s), such as, for example, one or more of various metals (e.g., titanium, tungsten, cobalt, nickel, platinum, etc.), metal-containing compositions (e.g., metal silicide, metal nitride, metal carbide, etc.), and/or conductively-doped semiconductor materials (e.g., conductively-doped silicon, conductively-doped germanium, etc.). The conductive materials of the signal lines 40 and shield lines 42 may be homogenous, or may comprise two or more discrete compositions. The conductive material of the shield lines 42 may be the same as the conductive material of the signal lines 40, or may be different from the conductive material of the signal lines. Further, the lines 40/42 of layer M2 may be the same composition as one or both of the lines 30/32 of layer M1, or may be different compositions from one or both of the lines 30/32 of layer M1.

The interconnects 22 (only some of which are labeled) are shown along the shield lines 42, with such interconnects 22 being utilized to vertically connect shield lines 42 of wiring layer M2 with shield lines 32 of wiring layer M1 (shown in FIG. 22). The interconnects 20 (only some of which are labeled) are also shown along the shield lines 42, with such interconnects 20 being utilized to vertically connect shield lines 42 of wiring layer M2 with shield lines 12 of wiring layer M3 (shown in FIG. 24). The interconnects 20 are shown in paired arrangements (i.e., two interconnects 20 are in each location where shield lines 42 of wiring layer M2 connect with shield lines 12 of wiring layer M3). In other embodiments, only a single interconnect 20 may be in at least some of such locations; and in some embodiments, more than two interconnects 20 may be in at least some of such locations.

Referring to FIG. 24, the wiring layer M3 includes signal lines 14 alternating with shield lines 12. The signal lines and shield lines are spaced from one another by the insulative material 34. The shield lines 12 are shown coupled with a fixed voltage identified as Vss, but may be coupled with any suitable voltage.
The signal lines 14 and shield lines 12 may comprise any suitable electrically conductive composition(s), such as, for example, one or more of various metals (e.g., titanium, tungsten, cobalt, nickel, platinum, etc.), metal-containing compositions (e.g., metal silicide, metal nitride, metal carbide, etc.), and/or conductively-doped semiconductor materials (e.g., conductively-doped silicon, conductively-doped germanium, etc.). The conductive materials of the signal lines 14 and shield lines 12 may be homogenous, or may comprise two or more discrete compositions. The conductive material of the shield lines 12 may be the same as the conductive material of the signal lines 14, or may be different from the conductive material of the signal lines. Further, the lines 12/14 of wiring layer M3 may be the same composition as one or more of the lines 30/32 and 40/42 of wiring layers M1 and M2, or may be different compositions from one or more of the lines 30/32 and 40/42 of wiring layers M1 and M2.

The interconnects 20 (only some of which are labeled) are shown along the shield lines 12, with such interconnects 20 being utilized to vertically connect shield lines 12 of wiring layer M3 with shield lines 42 of wiring layer M2 (shown in FIG. 23). The overlap regions 18a and 18b are diagrammatically indicated in FIGS. 23 and 24, and such correspond to regions where the interconnects 20 vertically connect shield lines 12 of wiring layer M3 with the shield lines 42 of wiring layer M2.

Region A is diagrammatically illustrated relative to the wiring layers M2 and M3 of FIGS. 23 and 24, and such region comprises a redundant (dummy) region (e.g., lane). One of the shield lines 42 of FIG. 23 is identified with a label 42a to distinguish such shield line from the others, and the redundant region of wiring layer M2 includes a widened structure 45 along the shield line 42a. One of the shield lines 12 of FIG. 24 is identified with a label 12a to distinguish such shield line from the others, and the redundant region of wiring layer M3 includes a widened structure 17 along the shield line 12a.

In some embodiments, the wiring layers M2 and M3 of FIGS. 23 and 24 may be referred to as a lower-level wiring layer and an upper-level wiring layer, respectively; and may be considered to comprise the shown first wiring tracks, second wiring tracks, third wiring tracks and fourth wiring tracks (labeled as first, second, third and fourth tracks in FIGS. 23 and 24). The first, second, third and fourth wiring tracks of the upper wiring layer M3 directly overlay the first, second, third and fourth wiring tracks of the lower wiring layer M2, and are within the redundant regions (i.e., redundant lanes).
The first, second, third and fourth wiring tracks extend in a first direction along an x-axis (with the x-axis being shown adjacent the portions of assembly 10c along FIGS. 23 and 24), and extend parallel to one another (or at least substantially parallel to one another, with the term "substantially parallel" meaning parallel to within reasonable tolerances of fabrication and measurement). The first and third wiring tracks sandwich the second wiring track therebetween; and the second and fourth wiring tracks sandwich the third wiring track therebetween.

In some embodiments, the lower-level wiring layer M2 may be considered to comprise a first wiring corresponding to the wiring of shield line 42a. The first wiring may be considered to have a first portion 50 extending along the second wiring track, a second portion 52 extending along the first wiring track, and a third portion 54 extending along the third wiring track. The first portion 50 may be considered to comprise a first side 51 and a second side 53 in opposing relation to the first side. The second portion 52 may be considered to be offset from the first side 51 of the first portion 50 by a first offset region 56, and the third portion 54 may be considered to be offset from the second side 53 by a second offset region 58. In the shown embodiment, the first, second and third portions 50, 52 and 54 extend along the direction of the x-axis. The second portion 52 is offset from the second wiring track by projections 55 and 57 which extend along a y-axis. The third portion 54 is offset from the second wiring track by projections 59 and 61 which extend along the y-axis. The first, second and third portions 50, 52 and 54 may be considered to extend along a first direction (the direction of the x-axis); and the projections 55, 57, 59 and 61 may be considered to extend along a second direction (the direction of the y-axis). In the shown embodiment, the second direction is orthogonal to the first direction. In other embodiments, the first and second directions may intersect one another without being orthogonal to one another.

The upper-level wiring layer M3 may be considered to comprise a second wiring (i.e., the wiring of shield line 12a). The second wiring 12a is connected to the first wiring 42a through the interconnects 20a and 20b (with interconnects 20a and 20b being identical to the other interconnects 20, but being labeled 20a and 20b so that they may be separately identified from the other interconnects). In some embodiments, the second wiring 12a may be considered to comprise a fourth portion 60 which extends along the third wiring track, and to comprise a fifth portion 62 which extends along the second wiring track. The third portion 54 of the first wiring 42a (FIG. 23) is electrically coupled to the fourth portion 60 of the second wiring 12a (FIG. 24) through the interconnects
20a, and the first portion 50 of the first wiring 42a (FIG. 23) is electrically coupled with the fifth portion 62 of the second wiring 12a (FIG. 24) through the interconnects 20b. FIG. 26 shows an overlay of an expanded region of FIGS. 23 and 24; and shows the overlap of the third portion 54 with the fourth portion 60, and the overlap of the first portion 50 and fifth portion 62.

FIG. 25 shows a cross-section along the line 25-25 of FIGS. 23 and 24, and shows the interconnects 20a/20b extending through insulative material 34 to electrically couple shield line 12a of the upper-level wiring layer M3 with the shield line 42a of the lower-level wiring layer M2. Although the illustrated embodiment shows two contact plugs corresponding to interconnects 20a/20b, in other embodiments there may be only a single contact plug, and in yet other embodiments there may be more than two contact plugs.

In some embodiments, the first wiring 42a of lower-level wiring layer M2 may be considered to comprise the first portion 50, second portion 52 and third portion 54 described above; and may be further considered to comprise a fourth portion corresponding to projection 57 (with such fourth portion coupling the first portion 50 with the second portion 52), and a fifth portion corresponding to projection 59 (with such fifth portion coupling the first portion 50 with the third portion 54). In such embodiments, the second wiring 12a of the upper-level wiring layer M3 may be considered to comprise portion 60 as a sixth portion extending along the third wiring track, and portion 62 as a seventh portion extending along the second wiring track. The second wiring 12a also comprises an eighth portion 64 extending along the fourth wiring track, a ninth portion 66 extending along the y-axis and coupling the sixth portion 60 with the seventh portion 62, and a tenth portion 68 extending along the y-axis and coupling the sixth portion 60 with the eighth portion 64. The contact plugs 20a of FIGS. 23 and 24 may be considered to penetrate an insulative layer corresponding to insulative material 34, and couple the third portion 54 of the first wiring 42a with the sixth portion 60 of the second wiring 12a; and similarly the contact plugs 20b may be considered to penetrate the insulative layer corresponding to insulative material 34 and couple the first portion 50 of the first wiring 42a with the seventh portion 62 of the second wiring 12a.

In some embodiments, the lower-level wiring layer M2 may be considered to further comprise a third wiring 40a (i.e., one of the signal lines) which is electrically disconnected from the first wiring 42a; and which has an eleventh portion 70 along the third wiring track, a twelfth portion 72 along the fourth wiring track, and a thirteenth
portion 71 which extends along the y-axis and couples the eleventh portion 70 with the twelfth portion 72.

In some embodiments, the upper-level wiring layer M3 may be considered to further comprise a fourth wiring 14a (i.e., one of the signal lines) which is electrically disconnected from the first wiring 12a, and which has a fourteenth portion 80 along the second wiring track, a fifteenth portion 82 along the first wiring track, and a sixteenth portion 83 which extends along the y-axis and couples the fourteenth portion 80 with the fifteenth portion 82.

In some embodiments, the shield line 12a of the upper-level wiring layer M3 may be referred to as a first shield line, and another shield line 12b may be referred to as a second shield line. The second shield line 12b has a portion 90 extending along the first wiring track and vertically overlapping the second portion 52 of the shield line 42a of the lower-level wiring layer M2. The portion 90 of shield line 12b is coupled with the portion 52 of shield line 42a through interconnects labeled as 20c (shown in FIGS. 23 and 24, and also shown in FIG. 26).

In some embodiments, the first, second and third portions 50, 52 and 54 of the shield line 42a within wiring layer M2, together with the projections 55, 57, 59 and 61 of the shield line 42a, may be considered to comprise the widened structure 45 along the shield line 42a (shown in FIG. 23). FIGS. 27A-C illustrate some example embodiments of such widened structure 45. FIG. 27A shows the widened structure 45 of FIG. 23. Such has the projection 59 (which may be referred to as a fourth portion of shield line 42a in some embodiments) extending in a same direction as the projection 55 (which may be referred to as a fifth portion in some embodiments), but entirely out of alignment (i.e., displaced along the x-axis) relative to the projection 55. Such also has the projection 61 extending in a same direction as the projection 57, but entirely out of alignment (i.e. offset) relative to the projection 57. In contrast, FIG. 27B shows a widened structure 45a having a configuration in which a region of projection 55 is aligned with a region of projection 59, and a region of projection 57 is aligned with a region of projection 61.

The embodiments of FIGS. 27A and 27B retain insulative regions 102 between the second and third portions 52 and 54 of the shield line 42a. In some embodiments, each insulative region 102 may be considered to comprise a first void region 104 corresponding to a first offset region 101 between the first portion 50 of shield line 42a and the second portion 52 of the shield line 42a, and to comprise a second void region 106 corresponding to a second offset region 103 between the first portion 50 and the
third portion 54. The regions 104 and 106 are referred to as "void" regions to indicate that the regions do not comprise conductive material. It is to be understood that such regions may or may not be empty; and, for example, in some embodiments the void regions 104 and 106 may comprise insulative material, such as, for example, one or both of silicon dioxide and silicon nitride.

The insulative region 102 within the widened structures (45/45a) is optional, and may be replaced with conductive material. For instance, FIG. 27C shows a widened structure 45b having a configuration in which conductive material of shield line 42a fills the first and second offset regions 101 and 103 (i.e., a configuration in which the first and second offset regions 101 and 103 are entirely comprised by conductive material).

In some embodiments, the sixth, seventh, eighth, ninth and tenth portions 60, 62, 64, 66 and 68 of the shield line 12a within wiring layer M3 may be considered to comprise the widened structure 17 of FIG. 24. The ninth and tenth portions 66 and 68 include respective parts that are aligned along the y-axis, and include parts that are not aligned along the y-axis. In some embodiments, an entirety of the ninth portion 66 may be aligned with an entirety of the tenth portion 68 along the y-axis; and in some embodiments, an entirety of the ninth portion 66 may be out of alignment with an entirety of the tenth portion 68 along the y-axis (i.e., may be displaced along the x-axis relative to the tenth portion).

In the shown embodiment of FIG. 24, conductive material of shield line 12a extends entirely across the widened structure 17. In other embodiments, an insulative region analogous to the region 102 of FIGS. 27A and 27B may be provided within the widened structure 17.

FIGS. 28-31 illustrate assembly 10d (previously described in FIG. 20), and show the wiring layers M1, M2 and M3. FIG. 28 is an exploded view showing the wiring layers stacked one atop another; while FIGS. 29-31 show each of the individual wiring layers M1, M2 and M3 in isolation.

Referring to FIG. 29, the wiring layer M1 includes signal lines 30 alternating with shield lines 32. The signal lines and shield lines are spaced from one another by insulative material 34. The shield lines 32 are shown coupled with a fixed voltage identified as Vss, but may be coupled with any suitable voltage.

The interconnects 22 (only some of which are labeled) are shown along the shield lines 32, with such interconnects 22 being utilized to vertically connect shield lines 32 of wiring layer M1 with shield lines 42 of wiring layer M2 (shown in FIG. 30).
Referring to FIG. 30, the wiring layer M2 includes signal lines 40 alternating with shield lines 42. The signal lines and shield lines are spaced from one another by the insulative material 34. The shield lines 42 are shown coupled with a fixed voltage identified as Vss, but may be coupled with any suitable voltage.

The interconnects 22 (only some of which are labeled) are shown along the shield lines 42, with such interconnects 22 being utilized to vertically connect shield lines 42 of wiring layer M2 with shield lines 32 of wiring layer M1 (shown in FIG. 29). The interconnects 20 (only some of which are labeled) are also shown along the shield lines 42, with such interconnects 20 being utilized to vertically connect shield lines 42 of wiring layer M2 with shield lines 12 of wiring layer M3 (shown in FIG. 31). The interconnects 20 are shown in paired arrangements (i.e., two interconnects 20 are in each location where shield lines 42 of wiring layer M2 are to connect with shield lines 12 of wiring layer M3). In other embodiments, only a single interconnect 20 may be in at least some of such locations; and in some embodiments, more than two interconnects 20 may be in at least some of such locations.

Referring to FIG. 31, the wiring layer M3 includes signal lines 14 alternating with shield lines 12. The signal lines and shield lines are spaced from one another by the insulative material 34. The shield lines 12 are shown coupled with a fixed voltage identified as Vss, but may be coupled with any suitable voltage.

The interconnects 20 (only some of which are labeled) are also shown along the shield lines 12, with such interconnects 20 being utilized to vertically connect shield lines 12 of wiring layer M3 with shield lines 42 of wiring layer M2 (shown in FIG. 30). The overlay regions 18a and 18b are diagrammatically indicated in FIGS. 30 and 31, and such correspond to regions where the interconnects 20 vertically connect shield lines 12 of wiring layer M3 with the shield lines 42 of wiring layer M2.

Regions B and B' are diagrammatically illustrated relative to the wiring layers M2 and M3 of FIGS. 30 and 31, and such regions comprise redundant (dummy) regions (e.g., lanes). Specifically, one of the shield lines 42 of FIG. 30 is identified with a label 42a to distinguish such shield line from the others. The redundant region of wiring layer M2 includes a widened structure 125 along the shield line 42a in region B, and includes a widened structure 127 along the shield line 42a in region B'. One of the shield lines 12 of FIG. 31 is identified with a label 12a to distinguish such shield line from the others, and the redundant region of wiring layer M3 includes widened structures 131 and 133 along the shield line 12a in regions B and B', respectively.
In some embodiments, the wiring layers M2 and M3 of FIGS. 30 and 31 may be referred to as a lower-level wiring layer and an upper-level wiring layer, respectively; and may be considered to comprise the shown first wiring tracks, second wiring tracks, third wiring tracks and fourth wiring tracks (labeled as first, second, third and fourth tracks in FIGS. 30 and 31). The first, second, third and fourth wiring tracks of the upper wiring layer M3 directly overlay the first, second, third and fourth wiring tracks of the lower wiring layer M2.

The first, second, third and fourth wiring tracks extend in a first direction along an x-axis, and extend parallel to one another (or at least substantially parallel to one another). The first and third wiring tracks sandwich the second wiring track therebetween; and the second and fourth wiring tracks sandwich the third wiring track therebetween.

In some embodiments, the lower-level wiring layer M2 may be considered to comprise first wiring corresponding to the wiring of shield line 42a. The first wiring may be considered to have portions 50, 52 and 54 analogous to those described above relative to the embodiment of FIGS. 21-24. Specifically, the first wiring 42a has the first portion 50 extending along the second wiring track (and extending across both of regions B and B'), the second portion 52 extending along the first wiring track (and within the region B'), and the third portion 54 extending along the third wiring track (and within the region B). The first portion 50 may be considered to comprise the first side 51 and the second side 53 in opposing relation to the first side. The second portion 52 may be considered to be offset from the first side 51 of the first portion 50 by the first offset region 56, and the third portion 54 may be considered to be offset from the second side 53 by the second offset region 58. In the shown embodiment, the first, second and third portions 50, 52 and 54 extend along the direction of the x-axis. The second portion 52 is offset from the second wiring track by the projections 55 and 57 which extend along a y-axis. The third portion 54 is offset from the second wiring track by the projections 59 and 61 which extend along the y-axis.

The upper-level wiring layer M3 may be considered to comprise second wiring corresponding to the wiring of shield line 12a. The second wiring 12a is connected to the first wiring 42a, and may be considered to have a fourth portion 60 analogous to that described above relative to the embodiment of FIGS. 21-24. The fourth portion 60 extends along the third wiring track, and is electrically coupled to the third portion 54 of the first wiring 42a (FIG. 18) through the interconnects 20a.
FIG. 32A shows a cross-section along the line 32A-32A of FIGS. 30 and 31, and shows an interconnect 20a extending through insulative material 34 to electrically couple shield line 12a of the upper-level wiring layer M3 with the shield line 42a of the lower-level wiring layer M2.

The upper-level wiring layer M3 (FIG. 31) comprises a third wiring 12b having a fifth portion 62 analogous to the portion 62 of the embodiment of FIGS. 21-24. The fifth portion 62 of third wiring 12b extends along the first wiring track, and is electrically coupled with the second portion 52 of the lower-level wiring layer M2 (FIG. 30) through the interconnects 20b. A cross-section along the line 32B-32B is shown in FIG. 32B, and such shows the coupling of the fifth portion 62 and the second portion 52 through an interconnect 20b.

In some embodiments, the first wiring 42a of lower-level wiring layer M2 may be considered to comprise the first portion 50, second portion 52 and third portion 54. The upper-level wiring layer M3 may be considered to comprise the wiring 12b as the second wiring, and to comprise the wiring 12a as the third wiring. The second wiring 12b comprises a fourth portion 62 along the first wiring track, and the third wiring 12a comprises a fifth portion 60 extending along the third wiring track. At least one contact plug 20b penetrates insulative layer of material 34 to couple the second portion 52 of the first wiring 42a with the fourth portion 62 of the second wiring 12b; and at least one contact plug 20a penetrates insulative layer of material 34 to couple the third portion 54 of the first wiring 42a with the fifth portion 60 of the third wiring 12a. In the shown embodiment, the third wiring 12a has a sixth portion 64 which extends along the second wiring track, and which is electrically coupled with the first portion 50 of the lower-level wiring 42a (FIG. 30) through the interconnects 20c. A cross-section along the line 32C-32C is shown in FIG. 32C, and such shows the coupling of the sixth portion 64 and the first portion 50 through an interconnect 20c.

In some embodiments, the third wiring 12a of the upper-level wiring layer M3 may be considered to further comprise a seventh portion 66 extending along the fourth wiring track. The fifth and sixth portions (60 and 64) are offset from one another by a first offset region 200, and the fifth and seventh portions (60 and 66) are offset from one another by a second offset region 202. The first and second offset regions 200 and 202 may comprise void regions, as shown in FIG. 31. Alternatively, the first and second offset regions 200 and 202 may be filled with conductive material of shield line 12a (i.e., may entirely comprise such conductive material), as shown in FIGS. 33 and 34. In some
embodiments, regions 64 and 66 of FIG. 31 may be referred to as seventh and eighth regions, respectively; that extend along the second wiring track and the fourth wiring track, respectively.

In some embodiments, the first wiring 42a of the lower-level wiring layer M2 may be considered to further comprise a ninth portion (corresponding to projection 55 or 57) extending along the y-axis to couple the first and second portions 50 and 52 to one another, and tenth portion (corresponding to projection 59 or 61) extending along the y-axis to couple the first and third portions 50 and 54 to one another.

In some embodiments, the first and second portions (50 and 52) of first wiring 42a may be considered to be offset from one another by a third offset region 204, and the first and third portions (50 and 44) of first wiring 42a may be considered to be offset from one another by a fourth offset region 206. The third and fourth offset regions 204 and 206 may comprise void regions, as shown in FIG. 30. Alternatively, the third and fourth offset regions 204 and 206 may be filled with conductive material of shield line 42a (i.e., may entirely comprise such conductive material), as shown in FIGS. 35 and 36.

The assemblies discussed above may be utilized in electronic systems. Such electronic systems may be used in, for example, memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. The electronic systems may be any of a broad range of systems, such as, for example, cameras, wireless devices, displays, chip sets, set top boxes, games, lighting, vehicles, clocks, televisions, cell phones, personal computers, automobiles, industrial control systems, aircraft, etc.

The particular orientation of the various embodiments in the drawings is for illustrative purposes only, and the embodiments may be rotated relative to the shown orientations in some applications. The description provided herein, and the claims that follow, pertain to any structures that have the described relationships between various features, regardless of whether the structures are in the particular orientation of the drawings, or are rotated relative to such orientation.

The cross-sectional views of the accompanying illustrations only show features within the planes of the cross-sections, and do not show materials behind the planes of the cross-sections, unless indicated otherwise, in order to simplify the drawings.

When a structure is referred to above as being "on" or "against" another structure, it can be directly on the other structure or intervening structures may also be present. In contrast, when a structure is referred to as being "directly on" or "directly against"
another structure, there are no intervening structures present. When a structure is referred to as being "connected" or "coupled" to another structure, it can be directly connected or coupled to the other structure, or intervening structures may be present. In contrast, when a structure is referred to as being "directly connected" or "directly coupled" to another structure, there are no intervening structures present.

Some embodiments include an assembly (e.g., 510) having a first wiring level (e.g., M3) with a plurality of first shield lines (e.g., 512) and first signal lines (e.g., 514) in alternating arrangement. The first shield lines and first signal lines have first segments (e.g., 520, 526) extending along a first direction (e.g., the direction of axis 503), second segments (e.g., 522, 528) extending along the first direction and laterally offset from the first segments, and first linking segments (e.g., 524, 530) interconnecting the first and second segments to one another. The assembly includes a second wiring level (e.g., M2) below the first wiring level and having a plurality of second shield lines (e.g., 516) and second signal lines (e.g., 518) in alternating arrangement. The second shield lines and second signal lines have third segments (e.g., 532, 538) extending along the first direction, fourth segments (e.g., 534, 540) extending along the first direction and laterally offset from the third segments, and second linking segments (e.g., 536, 542) interconnecting the third and fourth segments to one another. The fourth segments of the second shield lines extend to under the first segments of the first shield lines and are electrically coupled to the first segments of the first shield lines through vertical interconnects (546).

Some embodiments include an assembly (e.g., 510) having a first wiring level (e.g., M3) which includes a plurality of first shield lines (e.g., 512) and first signal lines (e.g., 514) in alternating arrangement. The assembly has a second wiring level (e.g., M2) below the first wiring level and which includes a plurality of second shield lines (e.g., 516) and second signal lines (e.g., 518) in alternating arrangement. One of the first shield lines has a first portion (e.g., 548) extending in a first direction (e.g., the direction of axis 503), a second portion (e.g., 550) extending in a second direction (e.g., the direction of axis 505), and a third portion (e.g., 552) extending in the first direction. The second portion interconnects the first and third portions with each other. One of the first signal lines is immediately adjacent said one of the first shield lines. Said one of the first signal lines has fourth, fifth and sixth portions (e.g., 554, 556, 558) that are substantially parallel to the third, second and first portions, respectively, of said one of the first shield lines. One of the second shield lines includes seventh and eighth portions (e.g., 560, 562)
that are under and substantially vertically aligned with the third portion of the first shield line and the fourth portion of the first signal line, respectively. A vertical interconnect (e.g., 546) electrically connects the third portion of said one of the first shield lines to the seventh portion of said one of the second shield lines.

Some embodiments include an assembly (e.g., 510) which has a first wiring level (e.g., M3) comprising a plurality of first shield lines (e.g., 512) and first signal lines (e.g., 514) in alternating arrangement. The assembly has second wiring level (e.g., M2) below the first wiring level and which includes a plurality of second shield lines (e.g., 516) and second signal lines (e.g., 518) in alternating arrangement. A mesh structure (e.g., 578) comprises the first shield lines electrically coupled with the second shield lines. Each of the first shield lines of the mesh structure extends primarily along a first direction (e.g., the direction of axis 503), and extends along two first paths (e.g., 580, 582) which are laterally offset relative to one another. Each of the second shield lines of the mesh structure extends primarily along the first direction and extends along two second paths (e.g., 590, 592) which are laterally offset relative to one another. The first shield lines of the mesh structure are primarily laterally offset from the second shield lines of the mesh structure except that each of the first paths of each of the first shield lines have overlap regions (e.g., 544) where portions of the first shield lines vertically overlap portions the second shield lines. Vertical interconnects (e.g., 546) are within said overlap regions to connect the first shield lines with the second shield lines. One of the first paths of an individual first shield line has an overlap region which is over a different second shield line than is the other of the first paths of the individual first shield line.

Some embodiments include an assembly having first, second, third and fourth wiring tracks over a substrate. The first, second, third and fourth wiring tracks extend in a first direction. The first and third wiring tracks sandwich the second wiring track therebetween, and the second and fourth wiring tracks sandwich the third wiring track therebetween. A lower-level wiring layer includes a first wiring which has a first portion extending along the second wiring track, a second portion extending along the first wiring track, and a third portion extending along the third wiring track. The second portion is offset along a first side of the first portion by a first offset region, and the third portion is offset along a second side of the first portion by a second offset region. The first side is in opposing relation to the second side. An upper-level wiring layer includes a second wiring electrically connected to the first wiring and having a fourth portion
extending along the third wiring track. The third portion of the first wiring is electrically coupled with the fourth portion of the second wiring.

Some embodiments include an assembly having first, second, third and fourth wiring tracks over a substrate. The first, second, third and fourth wiring tracks extend in a first direction and are substantially parallel to one another. The first and third wiring tracks sandwich the second wiring track therebetween, and the second and fourth wiring tracks sandwich the third wiring track therebetween. A lower-level wiring layer comprises a first wiring. The first wiring comprises a first portion extending along the second wiring track, a second portion extending along the first wiring track, a third portion extending along the third wiring track, a fourth portion extending in a second direction crossing the first direction to couple the first portion and the second portion, and a fifth portion extending in the second direction to couple the first portion and the third portion. An upper-level wiring layer comprises a second wiring electrically connected to the first wiring. The second wiring comprises a sixth portion extending along the third wiring track, a seventh portion extending along the second wiring track, an eighth portion extending along the fourth wiring track, a ninth portion extending in the second direction to couple the sixth portion and the seventh portion, and a tenth portion extending in the second direction to couple the sixth portion and the eighth portion.

Some embodiments include an assembly having first, second, third and fourth wiring tracks over a substrate. The first, second, third and fourth wiring tracks extend in a first direction and are substantially parallel to one another. The first and third wiring tracks sandwich the second wiring track therebetween, and the second and fourth wiring tracks sandwich the third wiring track therebetween. A lower-level wiring layer comprises a first wiring. The first wiring comprises a first portion extending along the second wiring track, a second portion extending along the first wiring track, and a third portion extending along the third wiring track. An upper-level wiring layer comprises second and third wirings electrically connected to the first wiring. The second wiring comprises a fourth portion extending along the first wiring track, and the third wiring comprises a fifth portion extending along the third wiring track. An insulating layer is between the lower-level wiring layer and the upper-level wiring layer. At least one contact plug penetrates the insulating layer to couple the second portion of the first wiring and the fourth portion of the second wiring. At least one contact plug penetrates
the insulating layer to couple the third portion of the first wiring and the fifth portion of the third wiring.
CLAIMS

I/we claim,

1. An assembly, comprising:
   a first wiring level comprising a plurality of first shield lines and first
   signal lines in alternating arrangement; each of the first shield lines and first signal lines
   having first segments extending along a first direction, second segments extending along
   the first direction and laterally offset from the first segments, and first linking segments
   interconnecting the first and second segments to one another;
   a second wiring level below the first wiring level and comprising a
   plurality of second shield lines and second signal lines in alternating arrangement; each
   of the second shield lines and second signal lines having third segments extending along
   the first direction, fourth segments extending along the first direction and laterally offset
   from the third segments, and second linking segments interconnecting the third and
   fourth segments to one another; and
   the fourth segments of the second shield lines extending to under the first
   segments of the first shield lines and being electrically coupled to the first segments of
   the first shield lines through vertical interconnects.

2. The assembly of claim 1 wherein the first linking segments extend
   substantially orthogonally to the first and second segments.

3. The assembly of claim 2 wherein the first linking segments extend along a
   second direction, and wherein second linking segments also extend along the second
   direction.
4. The assembly of claim 1 wherein:
   an individual first shield line has an individual first shield line first
   segment and an individual first shield line second segment;
   an individual first signal line immediately adjacent the individual first
   shield line has an individual first signal line first segment and an individual first signal
   line second segment;
   the first linking segments include an individual first shield line linking
   segment interconnecting the individual first shield line first segment with the individual
   first shield line second segment, and include an individual first signal line linking
   segment interconnecting the individual first signal line first segment with the individual
   first signal line second segment;
   the first linking segments include an individual first shield line linking
   segment interconnecting the individual first shield line first segment with the individual
   first shield line second segment, and include an individual first signal line linking
   segment interconnecting the individual first signal line first segment with the individual
   first signal line second segment;
   the first linking segments include an individual first shield line linking
   segment is offset from the 
   individual first signal line linking segment along the first direction by a first distance;
   an individual second shield line has an individual second shield line third
   segment under a region of the individual first signal line first segment, and an individual
   second shield line fourth segment under a region of the first shield line first segment and
   extending to under a region of the individual first signal line second segment, and has an
   individual second linking segment between the individual second shield line third
   segment and the individual second shield line fourth segment;
   the individual second shield line fourth segment is electrically coupled to
   the individual first shield line first segment through an individual of the vertical
   interconnects;
   the individual second linking segment is offset from the individual first
   signal line linking segment along the first direction by a second distance; and
   the second distance is greater than the first distance.

5. The assembly of claim 4 wherein the second distance is at least double the
   first distance.

6. The assembly of claim 1 wherein:
   the first shield lines are all electrically connected with Vss; and
   the second shield lines are all electrically connected with Vss.
7. The assembly of claim 1 wherein:
the first shield lines include some lines electrically connected with Vdd and some lines electrically connected with Vss; and
the second shield lines include some lines electrically connected with Vdd and some lines electrically connected with Vss.

8. The assembly of claim 1 wherein the vertical interconnects are a first set of vertical interconnects, and comprising:
a third wiring level below the second wiring level and comprising a plurality of third shield lines and third signal lines in alternating arrangement; the third shield lines and third signal lines extending substantially orthogonally to the third and fourth segments; and
the third shield lines being electrically coupled to the third and fourth segments of the second shield lines through a second set of vertical interconnects.

9. An assembly, comprising:
a first wiring level comprising a plurality of first shield lines and first signal lines in alternating arrangement;
a second wiring level below the first wiring level and comprising a plurality of second shield lines and second signal lines in alternating arrangement;
a mesh structure comprising the first shield lines electrically coupled with the second shield lines; each of the first shield lines of the mesh structure extending primarily along a first direction, and extending along two first paths which are laterally offset relative to one another; each of the second shield lines of the mesh structure extending primarily along the first direction and extending along two second paths which are laterally offset relative to one another;
the first shield lines of the mesh structure being primarily laterally offset from the second shield lines of the mesh structure except that each of the first paths of each of the first shield lines have overlap regions where portions of the first shield lines vertically overlap portions the second shield lines; vertical interconnects being within said overlap regions to connect the first shield lines with the second shield lines; and
one of the first paths of an individual first shield line having an overlap region which is over a different second shield line than is the other of the first paths of the individual first shield line.
10. The assembly of claim 9 wherein each of the first shield lines comprises a first bridging region connecting the two first paths to one another.

11. The assembly of claim 10 wherein said first bridging region extends along a second direction substantially orthogonal to the first direction.

12. The assembly of claim 10 wherein each of the second shield lines comprises a second bridging region connecting the two second paths to one another.

13. The assembly of claim 12 wherein said first and second bridging regions extend along a second direction substantially orthogonal to the first direction.

14. The assembly of claim 9 comprising a third wiring level below the second wiring level and comprising a plurality of third shield lines; the third shield lines extending primarily along a second direction substantially orthogonally to the first direction; and wherein the vertical interconnects correspond to a first set of vertical interconnects and the third shield lines are electrically coupled to the second shield lines through a second set of vertical interconnects.
15. An assembly comprising:
   first, second, third and fourth wiring tracks over a substrate, wherein the
   first, second, third and fourth wiring tracks extend in a first direction and are
   substantially parallel to one another, wherein the first and third wiring tracks sandwich
   the second wiring track therebetween, and wherein the second and fourth wiring tracks
   sandwich the third wiring track therebetween;
   a lower-level wiring layer comprising a first wiring, wherein the first
   wiring comprises a first portion extending along the second wiring track, a second
   portion extending along the first wiring track, a third portion extending along the third
   wiring track, a fourth portion extending in a second direction crossing the first direction
   to couple the first portion and the second portion, and a fifth portion extending in the
   second direction to couple the first portion and the third portion; and
   an upper-level wiring layer comprising a second wiring electrically
   connected to the first wiring, wherein the second wiring comprises a sixth portion
   extending along the third wiring track, a seventh portion extending along the second
   wiring track, an eighth portion extending along the fourth wiring track, a ninth portion
   extending in the second direction to couple the sixth portion and the seventh portion, and
   a tenth portion extending in the second direction to couple the sixth portion and the
   eighth portion.

16. The assembly of claim 15, further comprising an insulating layer between
   the lower-level wiring layer and the upper-level wiring layer, and at least one contact
   plug penetrating the insulating layer to couple the first portion of the first wiring and the
   seventh portion of the second wiring.

17. The assembly of claim 15, further comprising an insulating layer between
   the lower-level wiring layer and the upper-level wiring layer, and at least one contact
   plug penetrating the insulating layer to couple the third portion of the first wiring and the
   sixth portion of the second wiring.

18. The assembly of claim 15, wherein the fourth portion and the fifth portion
   include respective parts that are aligned in line in the second direction and the ninth
   portion and the tenth portion include respective parts that are aligned in line in the
   second direction.
19. The assembly of claim 15, wherein the fourth portion is out of alignment with the fifth portion in the second direction and the ninth portion is out of alignment with the tenth portion in the second direction.

20. The assembly of claim 15, wherein each of the first wiring and the second wiring is supplied with a fixed voltage.

21. The assembly of claim 15, wherein the lower-level wiring layer further comprises a third wiring electrically disconnected from the first wiring, wherein the third wiring comprises an eleventh portion extending along the third wiring track, a twelfth portion extending along the fourth wiring track, and a thirteenth portion extending in the second direction to couple the eleventh portion and the twelfth portion.

22. The assembly of claim 15, wherein the upper-level wiring layer further comprises a fourth wiring electrically disconnected from the second wiring, wherein the fourth wiring comprises a fourteenth portion extending along the second wiring track, a fifteenth portion extending along the first wiring track, and a sixteenth portion extending in the second direction to couple the fourteenth portion and the fifteenth portion.
FIG. 6

(1) M3 : Signal
(2) M3 : VSS
(1) M2 : VSS
(2) M2 : Signal

FIG. 7
(1) M3 : Signal
(2) M3 : VSS
(3) M3 : VDD
(4) M3 : Signal

FIG. 11
FIG. 12

(1) M2 : VSS
(2) M2 : Signal
(3) M2 : Signal
(4) M2 : VDD
### A. CLASSIFICATION OF SUBJECT MATTER

HOIL 23/522(2006.01)i, HOIL 27/06(2006.01)i, HOIL 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

### B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

HOIL 23/522; HOIL 23/52; G06F 17/50; HOIL 21/82; HOIL 23/495; HOIL 27/06; HOIL 21/768

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: shield line, signal line, stack wiring, segment, mesh

### C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:
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Date of the actual completion of the international search: 11 July 2017 (11.07.2017)

Date of mailing of the international search report: 11 July 2017 (11.07.2017)

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