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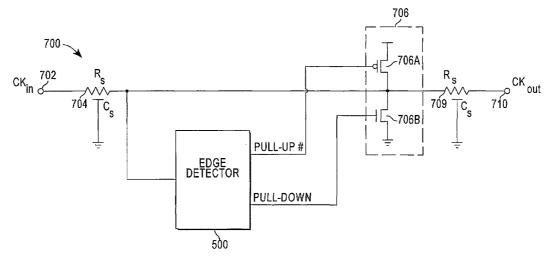
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(54) Title: REGENERATIVE CLOCK REPEATER



(57) Abstract: A regenerative clock repeater (Fig. 5; 700) comprises an edge detector (Fig. 6; 500) and an output driver means (706) to produce the clock signal (CK) by recovering its high logical level and low logical level. The output driver means further comprises a pull-up (706A) and a pull-down (706B) circuitry adapted to receive a pair of control signals (PULL-UP#, PULL-DOWN#). These control signals are generated by the edge detector to sense the rising edge and falling edge of the clock signal. Inside the edge detector, a pair of threshold level detectors (540, 550) detect a high and a low logical level of the clock signal and inputs the results to a combination of logic gates (562, 564, 568, 570) and a latch (566) to keep the locations of the signal markers fixed. These fixed-location of control signals trigger the output driver means to recover the high logical level and the low logical level of said clock signal.



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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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International application No.

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched			
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) Please See Continuation Sheet			
C. DOCUMENTS CONSIDERED TO BE RELEVANT			
Category * Citation of document, with indication, where a	ppropriate, of the relevant passages Re	levant to claim No.	
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A US 5,414,312 A (Wong) 9 May 1995 (09.05.1995), Figure 1		1-9	
A US 6,094,086 A (Chow) 25 July 2000 (25.07.2000), Figure 5		1-9	
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Continuation of B. FIELDS SEARCHED Item 3:	•
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search terms: clock repeater, edge detector, pull-up, pull-down, transistor, NA	ND, NOR, logic, gate, driver
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