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(54) Method for verification of combinational circuits using a filtering oriented approach

(57) A set of filters are arranged in sequence for verification and analysis of digital circuit designs. The filters are either active filters, which are directly involved in verification of circuit designs (e.g., a Binary Decision Diagram (BDD)-based verifier or an automatic test pattern generation (ATPG)-based verifier), or passive filters, which gather information about the circuit or transform the circuit structure in order to simplify the verification problem (e.g., random pattern simulation or circuit partitioning). Given a pair of circuits to be verified, the filter approach first subjects the circuits to very simple, fast techniques having very low memory usage requirements. These steps are followed by a series of increasingly powerful methods that are more time consuming and often require more computer memory for their operation. In between the simpler active filters and the more sophisticated active filters, information about potential equivalent nodes in the circuits is collected and a decision is made as to whether to partition the circuits. The verification methodology is structured such that circuit designs that are easier to verify are never unnecessarily subjected to more expensive techniques. The method provides for a gradual increase in the sophistication of verification techniques applied, according to the difficulty of the verification problem.

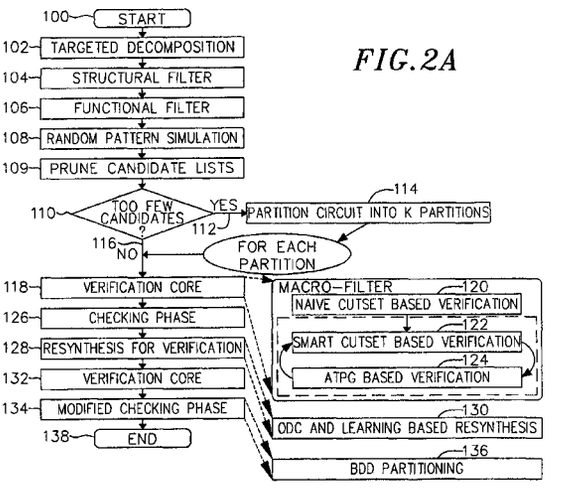

FIG. 2A

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EUROPEAN SEARCH REPORT

Application Number
EP 98 30 3748

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	18 April 2000	Amann, R

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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