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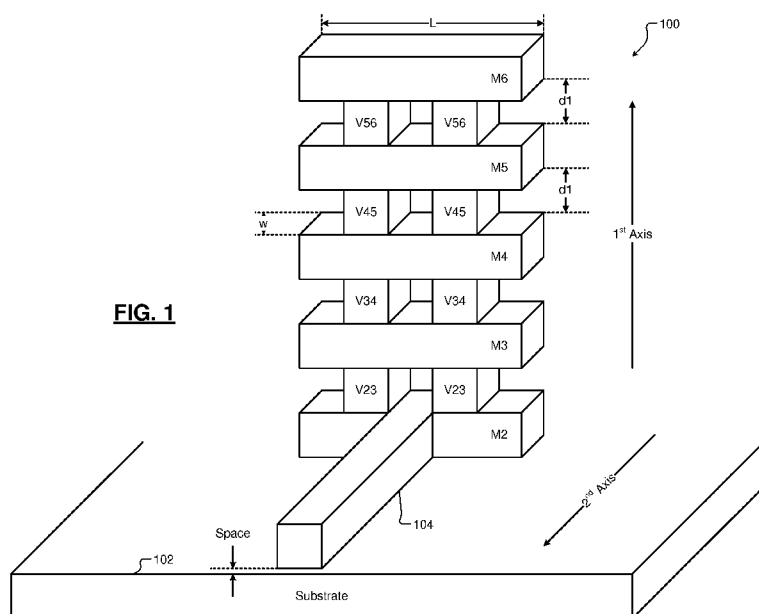
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[Continued on next page]

(54) Title: STACKABLE HIGH-DENSITY METAL-OXIDE-METAL CAPACITOR WITH MINIMUM TOP PLATE PARASITIC CAPACITANCE

FIG. 1



(57) Abstract: Disclosed is a system including first and second plurality of conductors (M2...M6) stacked along a first axis on a substrate. The first axis is perpendicular to a plane on which the substrate lies. In the first and second plurality of conductors, each conductor is connected to an adjacent conductor by one or more first vias (V23...V56) arranged along the first axis. The first and second plurality of conductors are arranged in parallel along a second axis perpendicular to the first axis and parallel to the plane on which the substrate lies. The first plurality of conductors respectively lie on a plurality of planes perpendicular to the first axis and parallel to the plane on which the substrate lies. The second plurality of conductors respectively lie on the plurality of planes. Capacitances are formed along the plurality of planes between the first plurality of conductors and the second plurality of conductors.

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- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
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STACKABLE HIGH-DENSITY METAL-OXIDE-METAL CAPACITOR WITH MINIMUM TOP
PLATE PARASITIC CAPACITANCE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Utility Application No. 14/086,154, filed
5 on November 21, 2013, and the benefit of U.S. Provisional Application No. 61/730,716,
filed on November 28, 2012. The entire disclosures of the applications referenced
above are incorporated herein by reference.

FIELD

[0002] The present disclosure relates generally to integrated circuits and more
10 particularly to stackable high-density metal-oxide-metal (MOM) capacitor with
minimum parasitic capacitance to top plate.

BACKGROUND

[0003] Many circuits include a capacitor array with multiple capacitors. The
capacitors in the capacitor array usually have large geometries to keep the percentage
15 of parasitic capacitance below design specifications (usually well below inherent
capacitance values) or to increase matching performance. To build the capacitor array
with many capacitors, large capacitance values and array area are required, which
increases cost.

SUMMARY

[0004] A system comprises a first plurality of conductors and a second plurality of
20 conductors. The first plurality of conductors is stacked along a first axis on a substrate
of an integrated circuit. The first axis is perpendicular to a plane on which the substrate
lies. Each conductor in the first plurality of conductors is connected to an adjacent
conductor in the first plurality of conductors by one or more first vias arranged along
25 the first axis. The second plurality of conductors is stacked along the first axis on the
substrate of the integrated circuit. Each conductor in the second plurality of conductors
is connected to an adjacent conductor in the second plurality of conductors by one or

more second vias arranged along the first axis. The first plurality of conductors and the second plurality of conductors are arranged in parallel along a second axis (i) perpendicular to the first axis and (ii) parallel to the plane on which the substrate lies. The first plurality of conductors respectively lie on a plurality of planes (i) perpendicular
5 to the first axis and (ii) parallel to the plane on which the substrate lies. The second plurality of conductors respectively lie on the plurality of planes. Capacitances are formed along the plurality of planes between the first plurality of conductors and the second plurality of conductors.

[0005] In another feature, capacitances are formed along the plurality of planes
10 between the first vias and the second vias.

[0006] In another feature, a number of conductors in the first plurality of conductors is equal to a number of conductors in the second plurality of conductors.

[0007] In another feature, a number of conductors in the second plurality of conductors is greater than a number of conductors in the first plurality of conductors.

[0008] In other features, conductors in the first plurality of conductors and the second plurality of conductors have predetermined dimensions. Conductors in the first plurality of conductors and the second plurality of conductors are separated by a first predetermined distance. The first plurality of conductors and the second plurality of conductors are separated by a second predetermined distance. Values of the
15 capacitances between the first plurality of conductors and the second plurality of conductors depend on one or more of (i) the predetermined dimensions, (ii) the first predetermined distance, and (iii) the second predetermined distance.
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[0009] In another feature, the system further comprises a third plurality of conductors stacked along the first axis on the substrate of the integrated circuit. The second
25 plurality of conductors is arranged in parallel to and between the first plurality of conductors and the third plurality of conductors along the second axis. Each conductor in the third plurality of conductors is connected to an adjacent conductor in the third plurality of conductors by one or more third vias arranged along the first axis. The third plurality of conductors respectively lie on the plurality of planes. Capacitances are
30 formed along the plurality of planes between the second plurality of conductors and the third plurality of conductors.

[0010] In other features, a number of conductors in the first plurality of conductors is equal to a number of conductors in the third plurality of conductors. A number of conductors in the second plurality of conductors is greater than a number of conductors in the first plurality of conductors.

5 **[0011]** In other features, conductors in the first plurality of conductors, the second plurality of conductors, and the third plurality of conductors have predetermined dimensions. Conductors in the first plurality of conductors, the second plurality of conductors, and the third plurality of conductors are separated by a first predetermined distance. The first, the second, and the third pluralities of conductors are separated by
10 a second predetermined distance. Values of the capacitances between the first plurality of conductors and the second plurality of conductors and between the second plurality of conductors and the third plurality of conductors depend on one or more of (i) the predetermined dimensions, (ii) the first predetermined distance, and (iii) the second predetermined distance.

15 **[0012]** In another feature, capacitances are formed along the plurality of planes between the second vias and the third vias.

[0013] In still other features, a system comprises a first set of conductors, a second set of conductors, and a third set of conductors. Conductors in each of the first, second, and third sets are stacked along a first axis on a substrate of an integrated
20 circuit. The first axis is perpendicular to a plane on which the substrate lies. In each of the first, second, and third sets, each conductor is connected to an adjacent conductor by one or more vias along the first axis. The first, second, and third sets of conductors are arranged in parallel along a second axis (i) perpendicular to the first axis and (ii) parallel to the plane on which the substrate lies. The second set of conductors is
25 arranged between the first set of conductors and the third set of conductors. The first set of conductors respectively lie on a plurality of planes (i) perpendicular to the first axis, and (ii) parallel to the plane on which the substrate lies. The second set of conductors respectively lie on the plurality of planes. The third set of conductors respectively lie on the plurality of planes.

30 **[0014]** In other features, capacitances are formed along the plurality of planes between the first set of conductors and the second set of conductors. Capacitances are

formed along the plurality of planes between the second set of conductors and the third set of conductors.

[0015] In other features, a number of conductors in the first set of conductors is equal to a number of conductors in the third set of conductors. A number of conductors in the second set of conductors is less than a number of conductors in the first set of conductors.

[0016] In another feature, a first conductor in the first set of conductors is connected to a first conductor in the third set of conductors by a connection along the second axis.

[0017] In other features, the system further comprises a fourth set of conductors and a fifth set of conductors. Conductors in each of the fourth and fifth sets are stacked along the first axis on the substrate of the integrated circuit. In each of the fourth and fifth sets, each conductor is connected to an adjacent conductor by one or more vias along the first axis. The fourth and fifth sets of conductors are arranged in parallel along the second axis. The fourth set of conductors respectively lie on the plurality of planes. The fifth set of conductors respectively lie on the plurality of planes. The fourth set of conductors is arranged between the third set of conductors and the fifth set of conductors.

[0018] In other features, capacitances are formed along the plurality of planes between the first set of conductors and the second set of conductors. Capacitances are formed along the plurality of planes between the second set of conductors and the third set of conductors. Capacitances are formed along the plurality of planes between the third set of conductors and the fourth set of conductors. Capacitances are formed along the plurality of planes between the fourth set of conductors and the fifth set of conductors.

[0019] In other features, a number of conductors in the first set of conductors is equal to a number of conductors in the third set of conductors and is equal to a number of conductors in the fifth set of conductors. A number of conductors in the second set of conductors is equal to a number of conductors in the fourth set of conductors and is less than a number of conductors in the first set of conductors.

[0020] In another feature, a first conductor in the first set of conductors is connected to a first conductor in the third set of conductors and to a first conductor in the fifth set of conductors by a connection along the second axis.

[0021] In other features, the system further comprises a sixth set of conductors, a seventh set of conductors, and an eighth set of conductors. Conductors in each of the sixth, seventh, and eighth sets are stacked along the first axis on the substrate of the integrated circuit. In each of the sixth, seventh, and eighth sets, each conductor is connected to an adjacent conductor by one or more vias along the first axis. The sixth, seventh, and eighth sets of conductors are arranged in parallel along the second axis. The sixth set of conductors lie adjacent to the first set of conductors along a third axis perpendicular to the first and second axes. The seventh set of conductors lie adjacent to the second set of conductors along the third axis. The eighth set of conductors lie adjacent to the third set of conductors along the third axis. The seventh set of conductors is arranged between the sixth set of conductors and the eighth set of conductors. the sixth, seventh, and eighth sets of conductors respectively lie on the plurality of planes.

[0022] In other features, capacitances are formed along the plurality of planes between the first set of conductors and the second set of conductors. Capacitances are formed along the plurality of planes between the second set of conductors and the third set of conductors. Capacitances are formed along the plurality of planes between the third set of conductors and the fourth set of conductors. Capacitances are formed along the plurality of planes between the fourth set of conductors and the fifth set of conductors. Capacitances are formed along the plurality of planes between the sixth set of conductors and the seventh set of conductors. Capacitances are formed along the plurality of planes between the seventh set of conductors and the eighth set of conductors.

[0023] In another feature, a first conductor in the sixth set of conductors is connected to a first conductor in the eighth set of conductors by a connection along the second axis.

[0024] In another feature, a conductor other than first and last conductors in the seventh set of conductors is connected to a conductor other than first and last conductors in the second set of conductors along the third axis.

[0025] In still other features, a method comprises arranging a first plurality of
5 conductors on a substrate of an integrated circuit. The first plurality of conductors is stacked along a first axis on the substrate. The first axis is perpendicular to a plane on which the substrate lies. The method further comprises connecting each conductor in the first plurality of conductors to an adjacent conductor in the first plurality of conductors by one or more first vias arranged along the first axis. The method further
10 comprises arranging a second plurality of conductors on the substrate of the integrated circuit. The second plurality of conductors is stacked along the first axis on the substrate. The method further comprises connecting each conductor in the second plurality of conductors to an adjacent conductor in the second plurality of conductors by one or more second vias arranged along the first axis. The method further comprises
15 arranging the first plurality of conductors and the second plurality of conductors in parallel along a second axis (i) perpendicular to the first axis and (ii) parallel to the plane on which the substrate lies. The method further comprises arranging the first plurality of conductors respectively along a plurality of planes (i) perpendicular to the first axis and (ii) parallel to the plane on which the substrate lies. The method further comprises
20 arranging the second plurality of conductors respectively along the plurality of planes. Capacitances are formed along the plurality of planes between the first plurality of conductors and the second plurality of conductors.

[0026] In another feature, capacitances are formed along the plurality of planes between the first vias and the second vias.

[0027] In another feature, a number of conductors in the first plurality of conductors
25 is equal to a number of conductors in the second plurality of conductors.

[0028] In another feature, a number of conductors in the second plurality of conductors is greater than a number of conductors in the first plurality of conductors.

[0029] In other features, conductors in the first plurality of conductors and the second
30 plurality of conductors have predetermined dimensions. Conductors in the first plurality of conductors and the second plurality of conductors are separated by a first

predetermined distance. The first plurality of conductors and the second plurality of conductors are separated by a second predetermined distance. Values of the capacitances between the first plurality of conductors and the second plurality of conductors depend on one or more of (i) the predetermined dimensions, (ii) the first predetermined distance, and (iii) the second predetermined distance.

[0030] In other features, the method further comprises arranging a third plurality of conductors on the substrate of the integrated circuit. The third plurality of conductors is stacked along the first axis on the substrate. The method further comprises arranging the second plurality of conductors in parallel to and between the first plurality of conductors and the third plurality of conductors along the second axis. The method further comprises connecting each conductor in the third plurality of conductors to an adjacent conductor in the third plurality of conductors by one or more third vias arranged along the first axis. The method further comprises arranging the third plurality of conductors respectively along the plurality of planes. Capacitances are formed along the plurality of planes between the second plurality of conductors and the third plurality of conductors.

[0031] In other features, a number of conductors in the first plurality of conductors is equal to a number of conductors in the third plurality of conductors. A number of conductors in the second plurality of conductors is greater than a number of conductors in the first plurality of conductors.

[0032] In other features, conductors in the first plurality of conductors, the second plurality of conductors, and the third plurality of conductors have predetermined dimensions. Conductors in the first plurality of conductors, the second plurality of conductors, and the third plurality of conductors are separated by a first predetermined distance. The first, the second, and the third pluralities of conductors are separated by a second predetermined distance. Values of the capacitances between the first plurality of conductors and the second plurality of conductors and between the second plurality of conductors and the third plurality of conductors depend on one or more of (i) the predetermined dimensions, (ii) the first predetermined distance, and (iii) the second predetermined distance.

[0033] In another feature, capacitances are formed along the plurality of planes between the second vias and the third vias.

[0034] In still other features, a method comprises arranging a first set of conductors, a second set of conductors, and a third set of conductors on a substrate of an integrated circuit. Conductors in each of the first, second, and third sets are stacked along a first axis on the substrate. The first axis is perpendicular to a plane on which the substrate lies. The method further comprises, in each of the first, second, and third sets, connecting each conductor to an adjacent conductor by one or more vias along the first axis. The method further comprises arranging the first, second, and third sets of conductors in parallel along a second axis (i) perpendicular to the first axis and (ii) parallel to the plane on which the substrate lies. The method further comprises arranging the second set of conductors between the first set of conductors and the third set of conductors. The method further comprises arranging the first set of conductors respectively along a plurality of planes (i) perpendicular to the first axis, and (ii) parallel to the plane on which the substrate lies. The method further comprises arranging the second set of conductors respectively along the plurality of planes. The method further comprises arranging the third set of conductors respectively along the plurality of planes.

[0035] In other features, capacitances are formed along the plurality of planes between the first set of conductors and the second set of conductors. Capacitances are formed along the plurality of planes between the second set of conductors and the third set of conductors.

[0036] In other features, a number of conductors in the first set of conductors is equal to a number of conductors in the third set of conductors. A number of conductors in the second set of conductors is less than a number of conductors in the first set of conductors.

[0037] In another feature, the method further comprises connecting a first conductor in the first set of conductors to a first conductor in the third set of conductors by a connection along the second axis.

[0038] In another feature, the method further comprises arranging a fourth set of conductors and a fifth set of conductors on the substrate of the integrated circuit.

Conductors in each of the fourth and fifth sets are stacked along the first axis on the substrate. The method further comprises, in each of the fourth and fifth sets, connecting each conductor to an adjacent conductor by one or more vias along the first axis. The method further comprises arranging the fourth and fifth sets of conductors in parallel along the second axis. The method further comprises arranging the fourth set of conductors respectively along the plurality of planes. The method further comprises arranging the fifth set of conductors respectively along the plurality of planes. The method further comprises arranging the fourth set of conductors between the third set of conductors and the fifth set of conductors.

5 [0039] In other features, capacitances are formed along the plurality of planes between the first set of conductors and the second set of conductors. Capacitances are formed along the plurality of planes between the second set of conductors and the third set of conductors. Capacitances are formed along the plurality of planes between the third set of conductors and the fourth set of conductors. Capacitances are formed along the plurality of planes between the fourth set of conductors and the fifth set of conductors.

15 [0040] In other features, a number of conductors in the first set of conductors is equal to a number of conductors in the third set of conductors and is equal to a number of conductors in the fifth set of conductors. A number of conductors in the second set of conductors is equal to a number of conductors in the fourth set of conductors and is less than a number of conductors in the first set of conductors.

20 [0041] In another feature, the method further comprises connecting a first conductor in the first set of conductors is connected to a first conductor in the third set of conductors and to a first conductor in the fifth set of conductors by a connection along the second axis.

25 [0042] In other features, the method further comprises arranging a sixth set of conductors, a seventh set of conductors, and an eighth set of conductors on the substrate of the integrated circuit. Conductors in each of the sixth, seventh, and eighth sets are stacked along the first axis on the substrate. The method further comprises, in each of the sixth, seventh, and eighth sets, connecting each conductor to an adjacent conductor by one or more vias along the first axis. The method further comprises

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arranging the sixth, seventh, and eighth sets of conductors in parallel along the second axis. The method further comprises arranging the sixth set of conductors adjacent to the first set of conductors along a third axis perpendicular to the first and second axes. The method further comprises arranging the seventh set of conductors adjacent to the second set of conductors along the third axis. The method further comprises arranging the eighth set of conductors adjacent to the third set of conductors along the third axis. The method further comprises arranging the seventh set of conductors between the sixth set of conductors and the eighth set of conductors. The method further comprises arranging the sixth, seventh, and eighth sets of conductors respectively along the plurality of planes.

[0043] In other features, capacitances are formed along the plurality of planes between the first set of conductors and the second set of conductors. Capacitances are formed along the plurality of planes between the second set of conductors and the third set of conductors. Capacitances are formed along the plurality of planes between the third set of conductors and the fourth set of conductors. Capacitances are formed along the plurality of planes between the fourth set of conductors and the fifth set of conductors. Capacitances are formed along the plurality of planes between the sixth set of conductors and the seventh set of conductors. Capacitances are formed along the plurality of planes between the seventh set of conductors and the eighth set of conductors.

[0044] In another feature, the method further comprises connecting a first conductor in the sixth set of conductors to a first conductor in the eighth set of conductors by a connection along the second axis.

[0045] In another feature, the method further comprises connecting a conductor other than first and last conductors in the seventh set of conductors to a conductor other than first and last conductors in the second set of conductors along the third axis.

[0046] Further areas of applicability of the present disclosure will become apparent from the detailed description, the claims and the drawings. The detailed description and specific examples are intended for purposes of illustration only and are not intended to limit the scope of the disclosure.

BRIEF DESCRIPTION OF DRAWINGS

[0047] FIG. 1 shows an example of a bottom plate of a capacitor unit used in a capacitor array according to the present disclosure.

[0048] FIG. 2A shows an example of a top plate of a capacitor unit used in a capacitor array according to the present disclosure.

[0049] FIG. 2B shows an example of a plurality of top plates used in a capacitor array according to the present disclosure.

[0050] FIG. 3 shows an example of a top view of a capacitor array including a plurality of bottom plates and a plurality of top plates according to the present disclosure.

[0051] FIG. 4 shows an example of a side view of a capacitor array including a plurality of bottom plates and a plurality of top plates according to the present disclosure.

[0052] In the drawings, reference numbers may be reused to identify similar and/or identical elements.

DESCRIPTION

[0053] The present disclosure relates to a metal-oxide-metal (MOM) capacitor array structure. As explained below with reference to FIGs. 1-4, the capacitor array has a unit structure including a center wall of vertically stacked metal wires (conductors). The vertically stacked metal wires are interconnected by vias. The center wall (top plate) is arranged between two walls made of similar stacked structure (bottom plate). A bottom plate is shared between two adjacent unit structures. This structure minimizes parasitic capacitance to the top plate. The bottom plates are connected at the top or bottom of the capacitor array. The bottom plate connection serves as a shield layer to reduce fringing capacitance between the top plate and external connections of the capacitor array. The top plates are connected in a direction perpendicular to the direction in which the bottom plates are connected. The top plate connections run parallel to each other and are eventually connected at one or both ends of the capacitor array to external circuit elements.

[0054] As further explained below with reference to FIGs. 1-4, a dummy cell with the same unit structure is arranged next to the outermost array boundary. The dummy cells are connected to a predetermined potential to improve uniformity of the array

without adding parasitic capacitance to the top plate. Dummy connections are arranged at the sides of the top plate connections. The dummy connections are used to connect the top plates of the dummy cells to a predetermined potential.

[0055] As further explained below with reference to FIGs. 1-4, the unit structure can be replicated or stacked along horizontal and vertical axes. The size (i.e., the value of the capacitance) of the resulting capacitor can be adjusted by reconfiguring bottom or top plate connections. Segment lengths of the top and bottom plates can be adjusted to match pitch of adjacent logic in the integrated circuit. The density of the capacitor array can be adjusted by varying spacing, segment width, and metal-to-VIA overlay. The top and bottom plates can have different number of stacked metal layers depending on capacitor density and parasitic capacitance requirement.

[0056] FIG. 1 shows an example of a bottom plate 100. The bottom plate 100 includes a plurality of conductors arranged on a substrate 102 as shown. For example only, the plurality of conductors is denoted as M2, M3, M4, M5, and M6. The number of conductors in the bottom plate 100 may be more or less than the number shown. The plurality of conductors is stacked along a first axis. The first axis is perpendicular to a plane on which the substrate 102 lies. Each conductor in the bottom plate 100 is separated from an adjacent conductor by a predetermined distance d1.

[0057] Each conductor in the bottom plate 100 is of a predetermined length L (segment length) and a predetermined width W (segment width). Each conductor in the bottom plate 100 is connected to an adjacent conductor by one or more vias. For example only, the vias are denoted as V23, V34, V45, and V56. In the notation V_{pq} , p and q denote the numbers of the conductors connected by the via V_{pq} . The number of vias used to connect adjacent conductors may differ depending on the predetermined length L of the conductors. For example, the number of vias may be less or more than the two vias shown if the predetermined length L of the conductors M_x is shorter or longer than shown.

[0058] A connection 104 connects the bottommost conductor (e.g., M2) of the bottom plate 100 to a bottommost conductor of another bottom plate (not shown here, but see FIG. 3). Alternatively, a connection similar to the connection 104 connects the topmost conductor (e.g., M6) of the bottom plate 100 to a topmost conductor of

another bottom plate (not shown here, but see FIG. 3). The other bottom plate is arranged similar to the bottom plate 100 and is arranged in parallel to the bottom plate 100 on the substrate 102 along a second axis. The second axis is parallel to the plane on which the substrate 102 lies. The connection 104 extends parallel to the second axis. The conductor M2 of the bottom plate 100 and a conductor M2 of another bottom plate lie on a plane parallel to the plane on which the substrate 102 lies. Similarly, the conductor M3 of the bottom plate 100 and a conductor M3 of the other bottom plate lie on a plane parallel to the plane on which the substrate 102 lies, and so on.

5 [0059] A space is shown between the conductor M2 and the substrate 102. A metal layer M1 between the conductor M2 and the substrate 102, a contact between the metal layer M1 and the substrate 102, and at least one via (e.g., V12) connecting the metal layer M1 to the conductor M2 and other suitable layers can be formed in the space. Thus, in the example shown, the order of stacking is substrate 102, contact, metal layer M1, via V12, conductor M2, via V23, conductor M3, via V34, conductor M4, via V45, conductor M5, via V56, and conductor M6. The conductors M2-M6 can be of different width and length although having the same dimensions yields maximum capacitor density.

15 [0060] FIG. 2A shows an example of a top plate 200. The top plate 200 includes a plurality of conductors arranged as shown. For example only, the plurality of conductors is denoted as M3, M4, and M5. A number of conductors in the top plate 200 may be more or less than the number shown. The number of conductors in the bottom plate 100 may be greater than or equal to the number of conductors in the top plate 200. For example, when the number of conductors in the bottom plate 100 is greater than the number of conductors in the top plate 200, the number of conductors in the bottom plate 100 may be at least 3, and the number of conductors in the top plate 200 may be at least 2. Alternatively, the number of conductors in the bottom plate 100 may be at least 5, and the number of conductors in the top plate 200 may be at least 3. In general, the number of the number of conductors in the bottom plate 100 may be at least one greater than the number of conductors in the top plate 200. For example only, the bottom plate 100 shown in FIG. 1 includes five conductors, and the

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top plate 200 shown in FIG. 2A includes three conductors. The plurality of conductors in the top plate 200 is stacked along the first axis. A conductor in the top plate 200 is separated from an adjacent conductor by the predetermined distance $d1$.

[0061] Each conductor in the top plate 200 is of the predetermined length L (segment length) and the predetermined width W (segment width). Each conductor in the top plate 200 is connected to an adjacent conductor by one or more vias. For example only, the vias are denoted as $V34$ and $V45$. In the notation V_{pq} , p and q denote the numbers of the conductors connected by the via V_{pq} . The number of vias used to connect adjacent conductors may differ depending on the predetermined length L of the conductors. For example, the number of vias may be less or more than the two vias shown if the predetermined length L of the conductors M_x is shorter or longer than shown.

[0062] One of the conductors of the top plate 200 (e.g., $M4$) can be extended along a third axis to connect the top plate 200 to another top plate (not shown here, but see FIGs. 2B and 3). The other top plate is arranged similar to the top plate 200 along the third axis. The third axis is perpendicular to the connection 104 of the bottom plate 100. The third axis is perpendicular to the second axis and is parallel to the plane on which the substrate 102 lies. The conductor $M2$ of the top plate 200 and a conductor $M2$ of another top plate lie on a plane parallel to the plane on which the substrate 102 lies. Similarly, the conductor $M3$ of the top plate 200 and a conductor $M3$ of another top plate lie on a plane parallel to the plane on which the substrate 102 lies, and so on.

[0063] FIG. 2B shows an example of a plurality of top plates. For example only, three top plates 200-1, 200-2, and 200-3 are shown. For example only, the three top plates 200-1, 200-2, and 200-3 are connected by the conductor $M4$. Alternatively, a conductor other than $M4$ of each of the three top plates 200-1, 200-2, and 200-3 (e.g., the conductor $M3$ or the conductor $M5$) may be used connect the three top plates 200-1, 200-2, and 200-3.

[0064] FIG. 3 shows a top view of a capacitor array 300, where interconnections between a plurality of bottom plates and a plurality of top plates are shown. The capacitor array 300 includes a plurality of bottom plates (denoted as B) and a plurality of top plates (denoted as T) arranged as shown. Each of the bottom plates B may be

similar to the bottom plate 100. Each of the top plates T may be similar to the top plate 200. The bottom plates and the top plates are arranged in an alternating manner along the second axis as shown. A connection similar to the connection 104 connects the bottom plates along the second axis. Along the second axis, each top plate lies
5 between a pair of bottom plates. A capacitor unit includes a top plate and two bottom plates. Adjacent capacitor units share a bottom plate. For example, a capacitor unit 302-1 and a capacitor unit 302-2 share a bottom plate. Each top plate is separated from an adjacent bottom plate by a predetermined distance d2. The predetermined distance d1 may be greater than the predetermined distance d2.

10 **[0065]** The capacitor array 300 can be extended (and shrunk) along the second axis as well as along the third axis. FIG. 3 shows only an example. Additional top and bottom plates than those shown can be added (or removed) along the second axis and/or the third axis. After the capacitor array 300 is manufactured, the outermost capacitor units (i.e., the capacitor units along the edges or boundaries) of the capacitor array 300 are
15 designated as dummy capacitor units. The dummy capacitor units are similar to other capacitor units within the capacitor array 300. However, the dummy capacitor units are not included in the capacitance formed by the capacitor array 300. Instead, the dummy capacitor units are utilized as follows. The top plates of the dummy capacitor units are connected to connections 306. Specifically, one of the conductors of the top plates
20 (e.g., the conductor M4) of the dummy capacitor units is connected to a connection 306. The connections 306 are connected to a predetermined potential (e.g., ground) to improve uniformity of the capacitor array 300 without adding parasitic capacitance to the top plate of the capacitance formed by the capacitor array 300.

[0066] One of the conductors of the top plates (e.g., the conductor M4) of the
25 capacitor units along the third axis is connected to a connection 308. The connections 308 can be used to connect the capacitor array 300 to other circuits in an integrated circuit comprising the capacitor array 300. The capacitor units along the third axis may be interconnected by one of the conductors (e.g., the conductor M4) of the top plates of the respective capacitor units. The size (i.e., value) of the capacitance of the
30 capacitor array 300 can be varied by varying the interconnections between the capacitor units. For example, one capacitor unit 304-1 can be connected to two

capacitor units 304-2, which in turn can be connected to four capacitor units 304-3 by one or more connections 308 as shown. Accordingly, in the example shown, the size (i.e., value) of the capacitance of the capacitor array 300 is equal to a sum of the one capacitor unit 304-1, the two capacitor units 304-2, and the four capacitor units 304-3.

5 **[0067]** FIG. 4 shows a side view of a portion of the capacitor array 300, where capacitances formed between the top and bottom plates of the capacitor array 300 are shown. In FIG. 4, D1-D2 denote examples of bottom plates of dummy capacitor units in a portion of the capacitor array 300. T1-T4 denote examples of top plates of capacitor units in the portion of the capacitor array 300. B1-B3 denote examples of bottom
10 plates of capacitor units in the portion of the capacitor array 300.

[0068] As shown, the conductors M2 of the bottom plates B1-B3 and D1-D2 lie on a plane perpendicular to the first axis and parallel to the plane on which the substrate 102 lies. The conductors M6 of the bottom plates B1-B3 and D1-D2 lie on a plane perpendicular to the first axis and parallel to the plane on which the substrate 102 lies.
15 The conductors M3 of top plates T1-T4 and the conductors M3 of the bottom plates B1-B3 and D1-D2 lie on a plane perpendicular to the first axis and parallel to the plane on which the substrate 102 lies. The conductors M4 of the top plates T1-T4 and the conductors M4 of the bottom plates B1-B3 and D1-D2 lie on a plane perpendicular to the first axis and parallel to the plane on which the substrate 102 lies. The conductors
20 M5 of the top plates T1-T4 and the conductors M5 of the bottom plates B1-B3 and D1-D2 lie on a plane perpendicular to the first axis and parallel to the plane on which the substrate 102 lies. The bottom plates B1-B3 may or may not be interconnected along the second axis.

[0069] Capacitances formed between the conductor M3 of the bottom plate B1 and
25 the conductors M3 of each of the top plates T1 and T2 contribute to the value of the capacitance of the capacitor array 300. Capacitances formed between the conductor M4 of the bottom plate B1 and the conductors M4 of each of the top plates T1 and T2 contribute to the value of the capacitance of the capacitor array 300. Capacitances formed between the conductor M5 of the bottom plate B1 and the conductors M5 of
30 each of the top plates T1 and T2 contribute to the value of the capacitance of the capacitor array 300.

[0070] Additionally, capacitances formed between the conductor M3 of the top plate T1 and each of the conductors M2 and M3 of the bottom plate B1 also contribute to the value of the capacitance of the capacitor array 300. Further, as shown, capacitances formed between vias interconnecting adjacent conductors of the top plate T1 and vias interconnecting adjacent conductors of the bottom plate B1, where the interconnected conductors of the top and bottom plates are coplanar, also contribute to the value of the capacitance of the capacitor array 300. The capacitance of the capacitor array 300 is inversely proportional to the predetermined distance d2 between the top and bottom plates.

[0071] Capacitances similar to those shown are also formed between the bottom plate B2 and the top plates T2 and T3, and between the bottom plate B3 and the top plates T3 and T4. These capacitances are not shown for simplicity of illustration. Further, only dominant capacitances (i.e., capacitances that contribute to the value of the capacitance of the capacitor array 300) formed between a bottom plate and a top plate are shown. Parasitic capacitances (e.g., capacitances between the conductor M3 of the top plate T1 and each of the conductors M4, M5, and M6 of the bottom plate B1; capacitances between the conductor M4 of the top plate T1 and each of the conductors M2, M3, M5, and M6 of the bottom plate B1; and so on) are omitted for simplicity of illustration.

[0072] For example only, the conductors are shown to be of the shape of a rectangle or a square. Alternatively, the conductors can be of other shapes including but not limited to a hexagon, an octagon, a circle, an oval, and so on.

[0073] The foregoing description is merely illustrative in nature and is in no way intended to limit the disclosure, its application, or uses. The broad teachings of the disclosure can be implemented in a variety of forms. Therefore, while this disclosure includes particular examples, the true scope of the disclosure should not be so limited since other modifications will become apparent upon a study of the drawings, the specification, and the following claims. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A or B or C), using a non-exclusive logical OR. It should be understood that one or more steps within a method may be executed

in different order (or concurrently) without altering the principles of the present disclosure.

CLAIMS

What is claimed is:

1. A system comprising:

a first plurality of conductors stacked along a first axis on a substrate of an integrated circuit, wherein the first axis is perpendicular to a plane on which the substrate lies, wherein each conductor in the first plurality of conductors is connected to an adjacent conductor in the first plurality of conductors by one or more first vias arranged along the first axis; and

a second plurality of conductors stacked along the first axis on the substrate of the integrated circuit, wherein each conductor in the second plurality of conductors is connected to an adjacent conductor in the second plurality of conductors by one or more second vias arranged along the first axis;

wherein the first plurality of conductors and the second plurality of conductors are arranged in parallel along a second axis (i) perpendicular to the first axis and (ii) parallel to the plane on which the substrate lies;

wherein the first plurality of conductors respectively lie on a plurality of planes (i) perpendicular to the first axis and (ii) parallel to the plane on which the substrate lies;

wherein the second plurality of conductors respectively lie on the plurality of planes; and

wherein capacitances are formed along the plurality of planes between the first plurality of conductors and the second plurality of conductors.

2. The system of claim 1, wherein capacitances are formed along the plurality of planes between the first vias and the second vias.

3. The system of claim 1, wherein a number of conductors in the second plurality of conductors is greater than a number of conductors in the first plurality of conductors.

4. The system of claim 1, wherein:

conductors in the first plurality of conductors and the second plurality of conductors have predetermined dimensions;

conductors in the first plurality of conductors and the second plurality of conductors are separated by a first predetermined distance;

the first plurality of conductors and the second plurality of conductors are separated by a second predetermined distance; and

values of the capacitances between the first plurality of conductors and the second plurality of conductors depend on one or more of (i) the predetermined dimensions, (ii) the first predetermined distance, and (iii) the second predetermined distance.

5. The system of claim 1, further comprising:

a third plurality of conductors stacked along the first axis on the substrate of the integrated circuit, wherein the second plurality of conductors is arranged in parallel to and between the first plurality of conductors and the third plurality of conductors along the second axis, wherein each conductor in the third plurality of conductors is connected to an adjacent conductor in the third plurality of conductors by one or more third vias arranged along the first axis;

wherein the third plurality of conductors respectively lie on the plurality of planes;

wherein capacitances are formed along the plurality of planes between the second plurality of conductors and the third plurality of conductors; and

wherein capacitances are formed along the plurality of planes between the second vias and the third vias.

6. A system comprising:

a first set of conductors;

a second set of conductors; and

a third set of conductors;

wherein conductors in each of the first, second, and third sets are stacked along a first axis on a substrate of an integrated circuit, wherein the first axis is perpendicular to a plane on which the substrate lies;

wherein, in each of the first, second, and third sets, each conductor is connected to an adjacent conductor by one or more vias along the first axis;

wherein the first, second, and third sets of conductors are arranged in parallel along a second axis (i) perpendicular to the first axis and (ii) parallel to the plane on which the substrate lies;

wherein the second set of conductors is arranged between the first set of conductors and the third set of conductors;

wherein the first set of conductors respectively lie on a plurality of planes (i) perpendicular to the first axis, and (ii) parallel to the plane on which the substrate lies;

wherein the second set of conductors respectively lie on the plurality of planes;
and

wherein the third set of conductors respectively lie on the plurality of planes.

7. The system of claim 6, wherein:

capacitances are formed along the plurality of planes between the first set of conductors and the second set of conductors, and

capacitances are formed along the plurality of planes between the second set of conductors and the third set of conductors.

8. The system of claim 6, wherein:

a number of conductors in the first set of conductors is equal to a number of conductors in the third set of conductors, and

a number of conductors in the second set of conductors is less than a number of conductors in the first set of conductors.

9. The system of claim 6, wherein a first conductor in the first set of conductors is connected to a first conductor in the third set of conductors by a connection along the second axis.

10. The system of claim 6, further comprising:
a fourth set of conductors; and
a fifth set of conductors;
wherein conductors in each of the fourth and fifth sets are stacked along the first axis on the substrate of the integrated circuit;
wherein, in each of the fourth and fifth sets, each conductor is connected to an adjacent conductor by one or more vias along the first axis;
wherein the fourth and fifth sets of conductors are arranged in parallel along the second axis;
wherein the fourth set of conductors respectively lie on the plurality of planes;
wherein the fifth set of conductors respectively lie on the plurality of planes;
wherein the fourth set of conductors is arranged between the third set of conductors and the fifth set of conductors;
a number of conductors in the first set of conductors is equal to a number of conductors in the third set of conductors and is equal to a number of conductors in the fifth set of conductors;
a number of conductors in the second set of conductors is equal to a number of conductors in the fourth set of conductors and is less than a number of conductors in the first set of conductors; and
wherein a first conductor in the first set of conductors is connected to a first conductor in the third set of conductors and to a first conductor in the fifth set of conductors by a connection along the second axis.
11. The system of claim 10, wherein:
capacitances are formed along the plurality of planes between the first set of conductors and the second set of conductors,
capacitances are formed along the plurality of planes between the second set of conductors and the third set of conductors,
capacitances are formed along the plurality of planes between the third set of conductors and the fourth set of conductors, and

capacitances are formed along the plurality of planes between the fourth set of conductors and the fifth set of conductors.

12. The system of claim 10, further comprising:

a sixth set of conductors;

a seventh set of conductors; and

an eighth set of conductors;

wherein conductors in each of the sixth, seventh, and eighth sets are stacked along the first axis on the substrate of the integrated circuit;

wherein, in each of the sixth, seventh, and eighth sets, each conductor is connected to an adjacent conductor by one or more vias along the first axis;

wherein the sixth, seventh, and eighth sets of conductors are arranged in parallel along the second axis;

wherein the sixth set of conductors lie adjacent to the first set of conductors along a third axis perpendicular to the first and second axes;

wherein the seventh set of conductors lie adjacent to the second set of conductors along the third axis;

wherein the eighth set of conductors lie adjacent to the third set of conductors along the third axis;

wherein the seventh set of conductors is arranged between the sixth set of conductors and the eighth set of conductors;

wherein the sixth, seventh, and eighth sets of conductors respectively lie on the plurality of planes;

wherein a first conductor in the sixth set of conductors is connected to a first conductor in the eighth set of conductors by a connection along the second axis; and

wherein a conductor other than first and last conductors in the seventh set of conductors is connected to a conductor other than first and last conductors in the second set of conductors along the third axis.

13. The system of claim 12, wherein:

capacitances are formed along the plurality of planes between the first set of conductors and the second set of conductors,

capacitances are formed along the plurality of planes between the second set of conductors and the third set of conductors,

capacitances are formed along the plurality of planes between the third set of conductors and the fourth set of conductors,

capacitances are formed along the plurality of planes between the fourth set of conductors and the fifth set of conductors,

capacitances are formed along the plurality of planes between the sixth set of conductors and the seventh set of conductors,

capacitances are formed along the plurality of planes between the seventh set of conductors and the eighth set of conductors.

14. A method comprising:

arranging a first plurality of conductors on a substrate of an integrated circuit, wherein the first plurality of conductors is stacked along a first axis on the substrate, and wherein the first axis is perpendicular to a plane on which the substrate lies;

connecting each conductor in the first plurality of conductors to an adjacent conductor in the first plurality of conductors by one or more first vias arranged along the first axis;

arranging a second plurality of conductors on the substrate of the integrated circuit, wherein the second plurality of conductors is stacked along the first axis on the substrate;

connecting each conductor in the second plurality of conductors to an adjacent conductor in the second plurality of conductors by one or more second vias arranged along the first axis;

arranging the first plurality of conductors and the second plurality of conductors in parallel along a second axis (i) perpendicular to the first axis and (ii) parallel to the plane on which the substrate lies;

arranging the first plurality of conductors respectively along a plurality of planes (i) perpendicular to the first axis and (ii) parallel to the plane on which the substrate lies; and

arranging the second plurality of conductors respectively along the plurality of planes,

wherein capacitances are formed along the plurality of planes between the first plurality of conductors and the second plurality of conductors.

15. The method of claim 14, wherein capacitances are formed along the plurality of planes between the first vias and the second vias.

16. The method of claim 14, wherein a number of conductors in the second plurality of conductors is greater than a number of conductors in the first plurality of conductors.

17. The method of claim 14, wherein:

conductors in the first plurality of conductors and the second plurality of conductors have predetermined dimensions;

conductors in the first plurality of conductors and the second plurality of conductors are separated by a first predetermined distance;

the first plurality of conductors and the second plurality of conductors are separated by a second predetermined distance; and

values of the capacitances between the first plurality of conductors and the second plurality of conductors depend on one or more of (i) the predetermined dimensions, (ii) the first predetermined distance, and (iii) the second predetermined distance.

18. The method of claim 14, further comprising:

arranging a third plurality of conductors on the substrate of the integrated circuit, wherein the third plurality of conductors is stacked along the first axis on the substrate;

arranging the second plurality of conductors in parallel to and between the first plurality of conductors and the third plurality of conductors along the second axis;

connecting each conductor in the third plurality of conductors to an adjacent conductor in the third plurality of conductors by one or more third vias arranged along the first axis; and

arranging the third plurality of conductors respectively along the plurality of planes,

wherein capacitances are formed along the plurality of planes between the second plurality of conductors and the third plurality of conductors, and

wherein capacitances are formed along the plurality of planes between the second vias and the third vias.

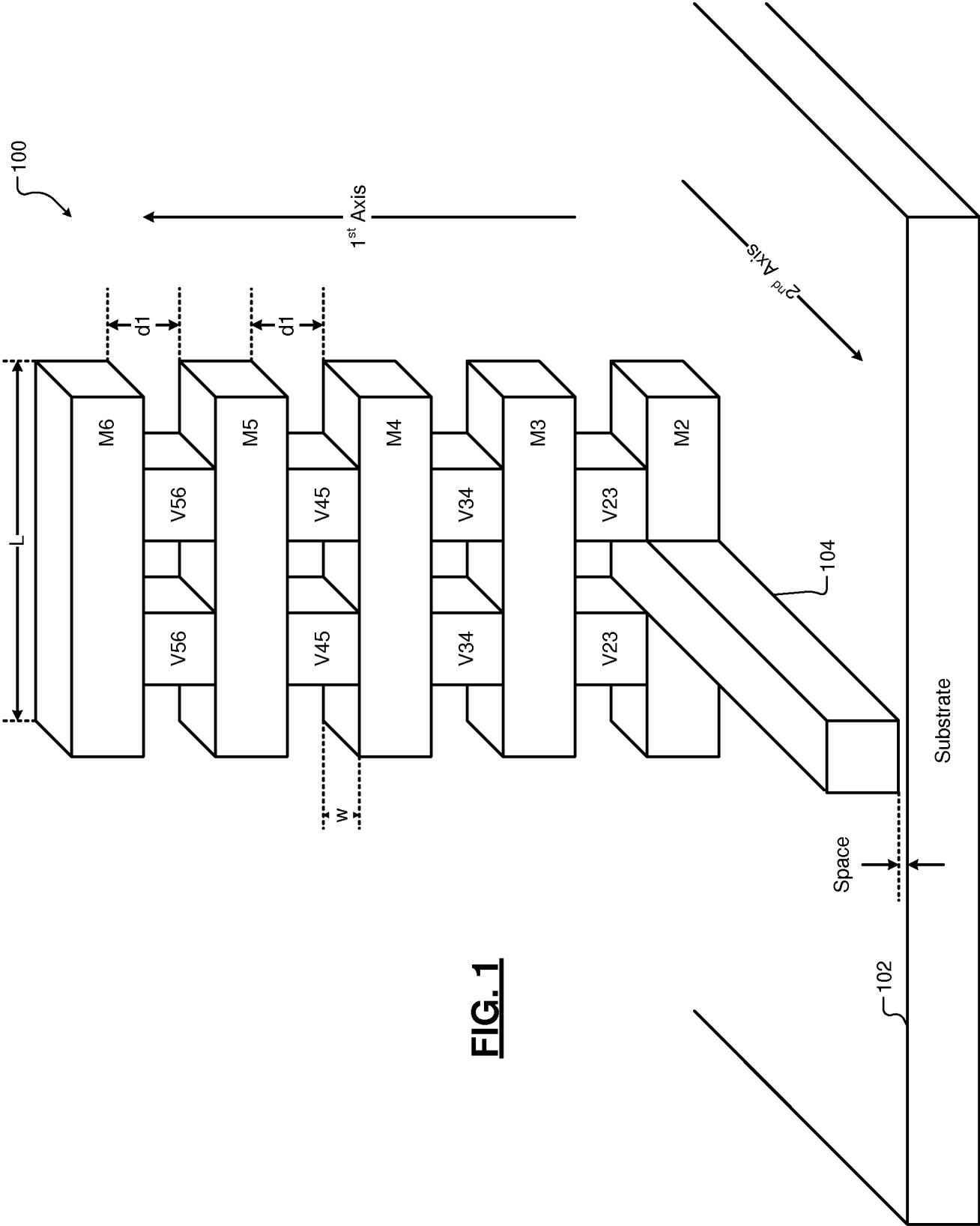


FIG. 1

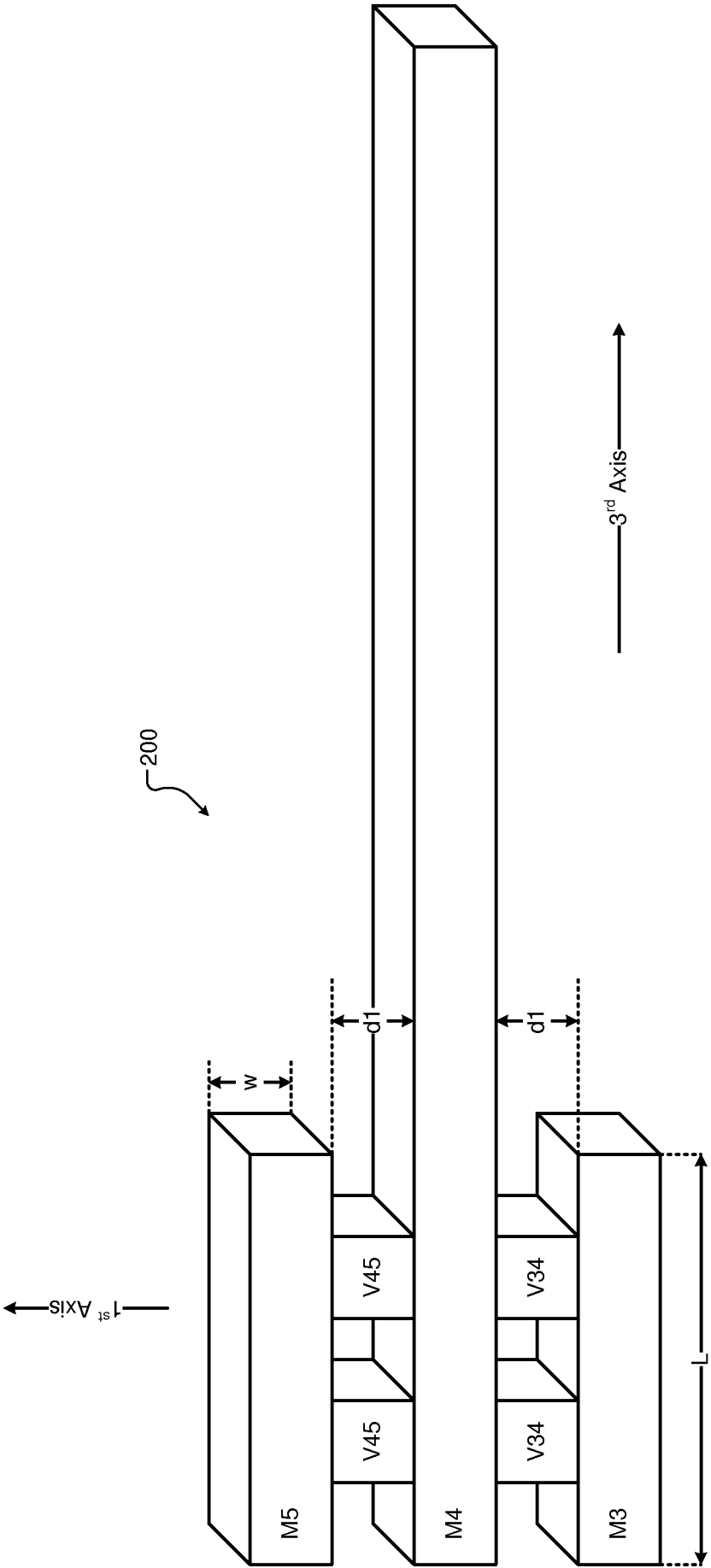


FIG. 2A

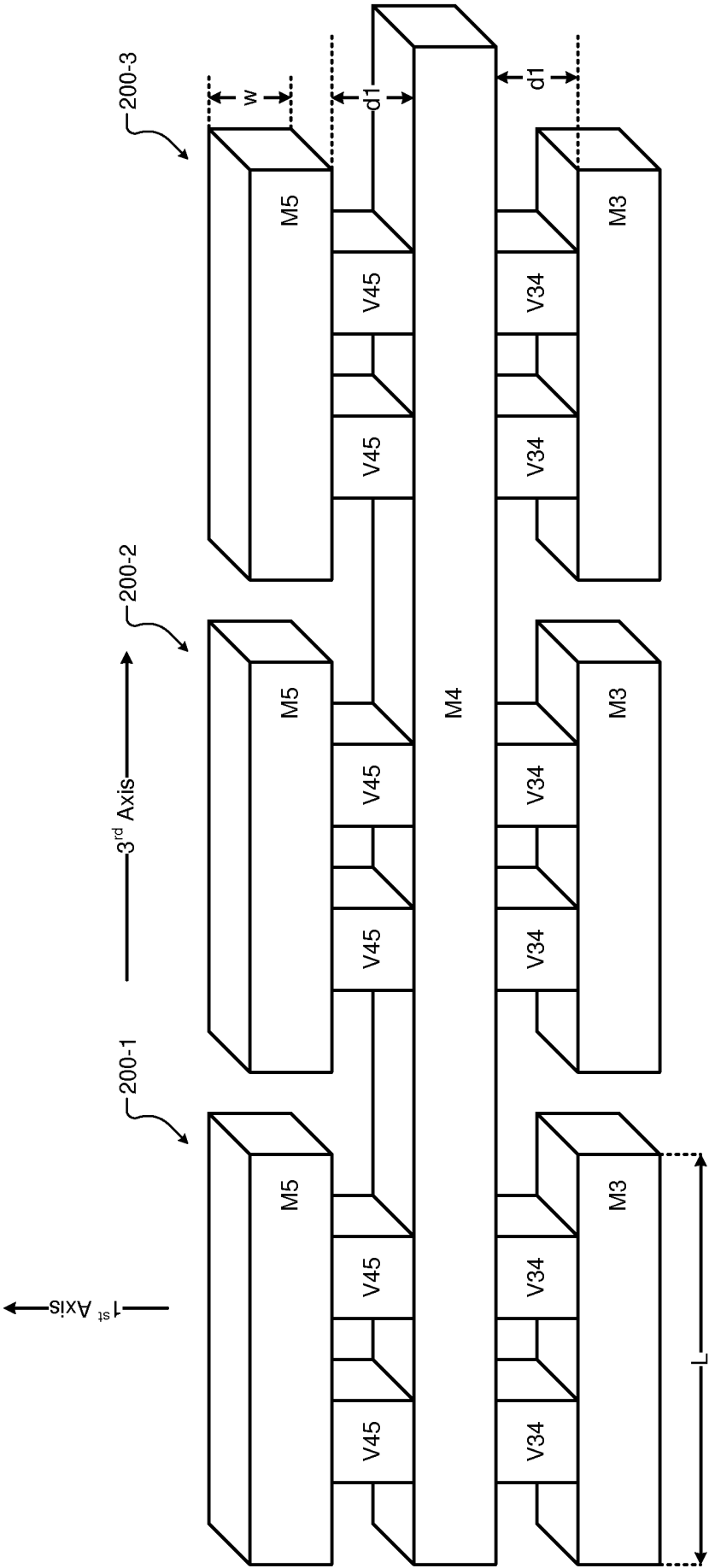
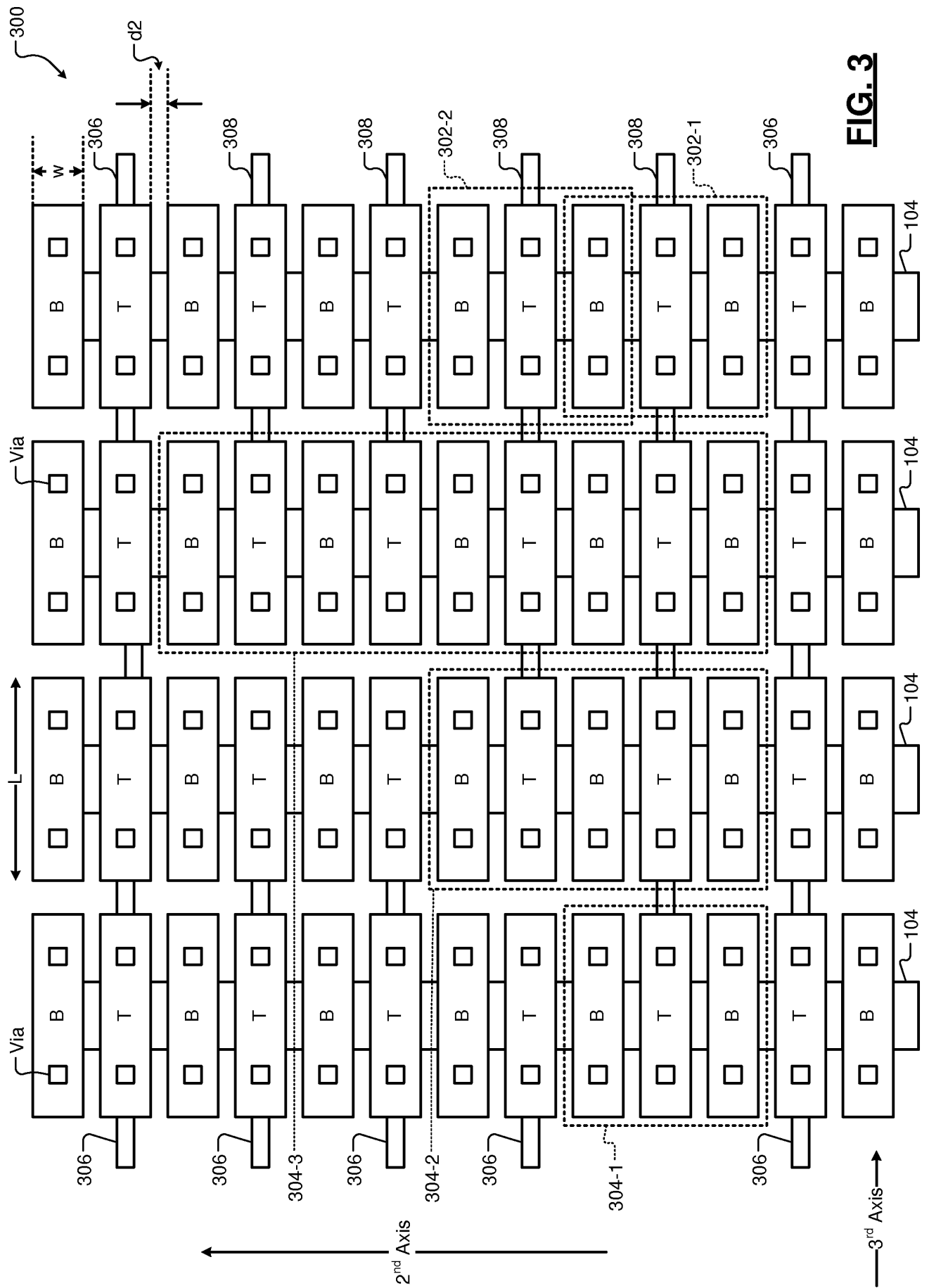


FIG. 2B



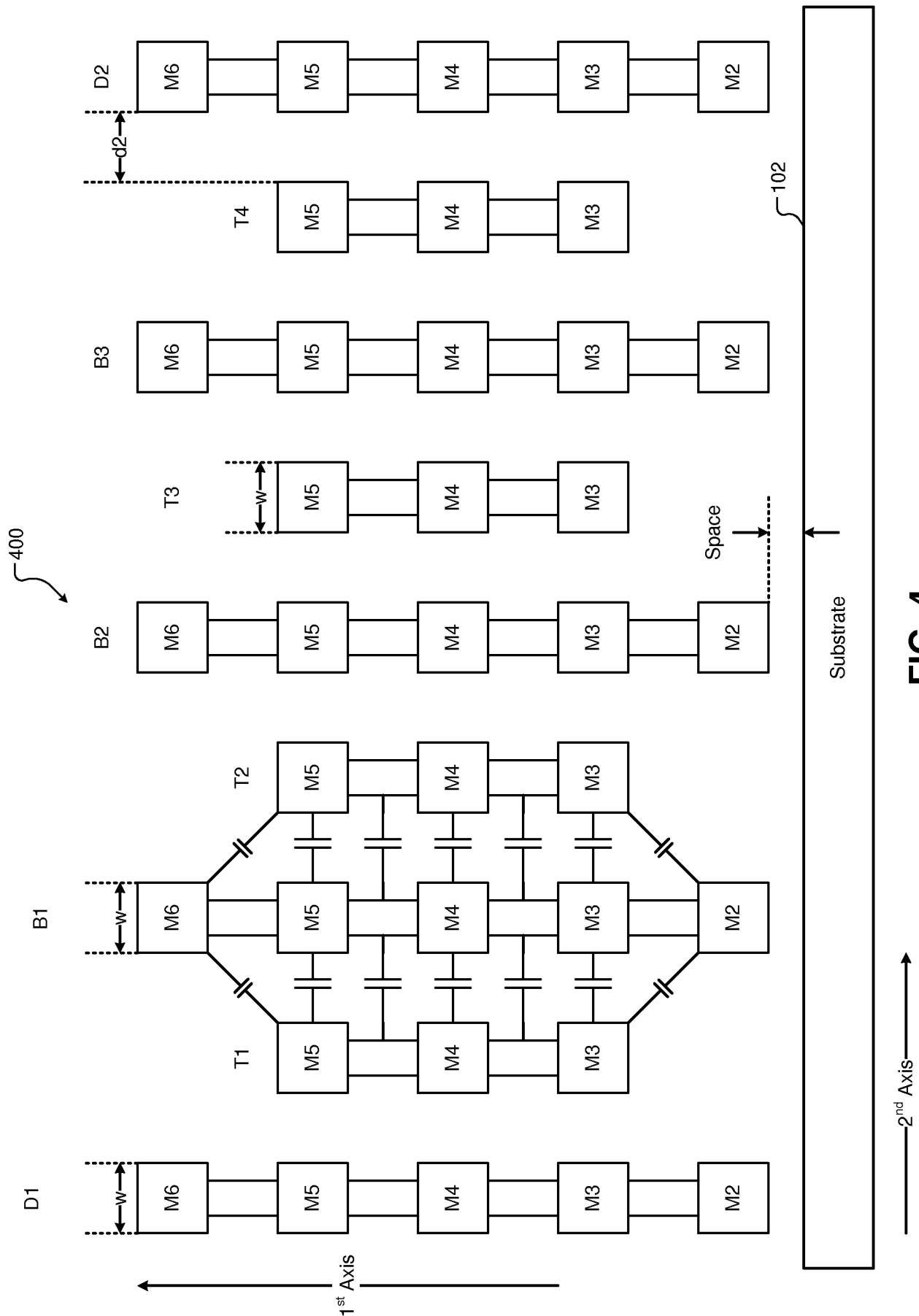


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/071367

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L49/02 H01L23/522 H01G4/005 H01G4/10 H01G4/228 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L H01G Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, WPI Data		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7 456 462 B1 (HESHAMI MEHRDAD [US] ET AL) 25 November 2008 (2008-11-25) column 4, line 13 - column 6, line 11; figures 3-7 -----	1-18
X	US 2012/286394 A1 (SUTARDJA SEHAT [US]) 15 November 2012 (2012-11-15) paragraphs [0037] - [0044]; figures 5-7 -----	1-18
X	US 2003/206389 A1 (HAJIMIRI SEYED-ALI [US] ET AL) 6 November 2003 (2003-11-06) paragraphs [0040] - [0048]; figures 4,7,8 -----	1-18
X	US 2007/267673 A1 (KIM JONGHAE [US] ET AL) 22 November 2007 (2007-11-22) paragraphs [0031] - [0037]; figures 2a,2b,3,4 ----- -/-	1-18
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 4 March 2014		Date of mailing of the international search report 13/03/2014
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Mosig, Karsten

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2013/071367

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ROBERTO APARICIO ET AL: "Capacity Limits and Matching Properties of Integrated Capacitors", IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, USA, vol. 37, no. 3, March 2002 (2002-03), XP011061701, ISSN: 0018-9200 page 387, left-hand column - page 388, left-hand column; figures 5,7,8,11 -----	1-18
A	US 2007/215928 A1 (MCLEOD SCOTT C [US]) 20 September 2007 (2007-09-20) paragraphs [0025] - [0027]; figures 1-6 -----	1-18

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